IRU3055

5-BIT PROGRAMMABLE 3-PHASE SYNCHRONOUS BUCK CONTROLLER IC

PRELIMINARY DATA SHEET TEST SPEC

FEATURES

- Meets VRM 9.0 Specification
- 3-Phase Controller with On-Board MOSFET Driver
- On-Board DAC programs the output voltage from 1.075V to 1.850V
- Loss-less Short Circuit Protection
- Programmable Frequency
- Synchronous operation allows maximum efficiency
- Minimum Part Count
- Soft-Start
- Power Good Function
- Hiccup Mode Current Limit

APPLICATIONS

- Intel Pentium 4 and AMD K7

DESCRIPTION

The IRU3055 is a 3-phase synchronous Buck controller which provides high performance DC to DC converter for high current applications.

The IRU3055 controller IC is specifically designed to meet Intel and AMD specifications for the new microprocessor requiring low voltage and high current.

The IRU3055 features under-voltage lockout for both 5V and 12V supplies, an external and programmable soft-start function as well as programming the oscillator frequency by using an external resistor.

TYPICAL APPLICATION

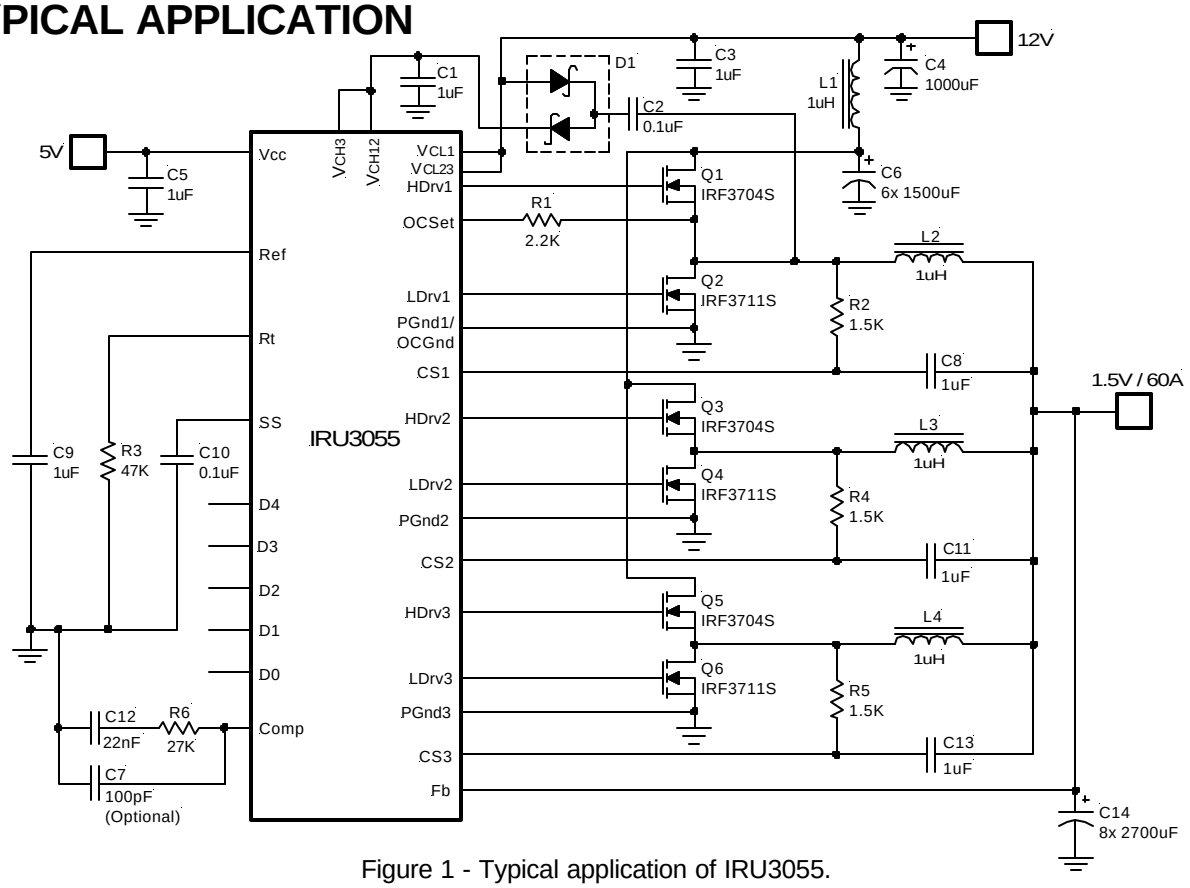


Figure 1 - Typical application of IRU3055.

PACKAGE ORDER INFORMATION

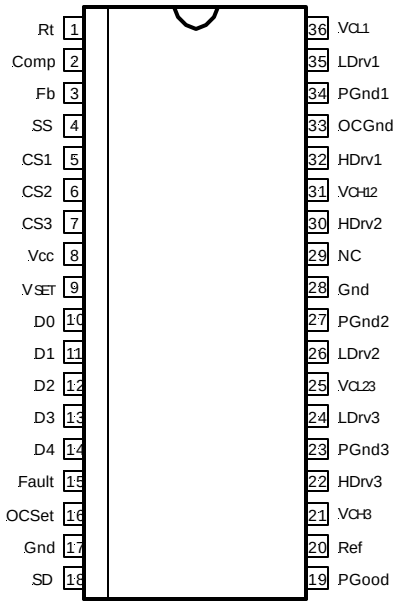
T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3055CQ	36-Pin Plastic QSOP WB (Q)

ABSOLUTE MAXIMUM RATINGS

V_{CH12} and V_{CH3} Supply Voltage ..... 30V (not rated for inductor load)
V_{CL1} and V_{CL23} Supply Voltage 20V
V_{CC} Supply Voltage 7V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

36-PIN WIDE BODY PLASTIC QSOP (Q)



θ_{JA} =60°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V_{CL1}=V_{CL23}=V_{CH12}=V_{CH3}=12V, Vcc=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Current Section						
Operating Supply Current		C_L High Side=3000pF C_L Low Side=6000pF				
	I_{CC}	V5	17	19	21	
	I_{CLH}	V12 (150KHz frequency)	30	50	70	mA
VID Section						
DAC Output Voltage (Note 1)	V_{DAC}		-1.5	Vs	+1.5	%
DAC Output Line Regulation	L_{REG}	4.5 < Vcc < 5.5V	-0.7	-0.06	+0.7	%
DAC Output Temp Variation	T_{REG}	0°C < temp < 70°C		1.4	2	%
VID Input LO					0.4	V
VID Input HI			2			V
VID Input Internal Pull-Up Resistor to 3.3V	VID_R		12.4	16.4	20.4	KΩ

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Power Good Section						
Under-Voltage Lower Trip Point	PG_{UVL}	V_{OUT} Ramping Down	0.88Vs	0.90Vs	0.92Vs	V
Under-Voltage Upper Trip Point	PG_{UVH}	V_{OUT} Ramping Up	0.89Vs	0.91Vs	0.93Vs	V
UV Hysteresis	PG_{HYST}		0.001Vs	0.01Vs	0.02Vs	V
Over-Voltage Upper Trip Point	OV_L	V_{OUT} Ramping Up	1.10Vs	1.11Vs	1.12Vs	V
Over-Voltage Lower Trip Point	OV_H	V_{OUT} Ramping Down	1.09Vs	1.10Vs	1.11Vs	V
OV Hysteresis	OV_{HYST}		0.001Vs	0.01Vs	0.02Vs	V
Power Good Output LO	PG_L	R_L=3mA	0	0.04	0.4	V
Power Good Output HI	PG_H	R_L=5K Pull-Up to 5V	4.8	4.9	5	V
UVLO Threshold - 5V	$UVLO_{5UP}$	Supply Ramping Up	4.2	4.34	4.5	V
UVLO Hysteresis - 5V	$UVLO_{5HYST}$	Supply Ramping Down	0.22	0.32	0.42	V
UVLO Threshold - 12V	$UVLO_{12UP}$	Supply Ramping Up	10.2	10.5	10.8	V
UVLO Hysteresis - 12V	$UVLO_{12HYST}$	Supply Ramping Down	0.5	0.7	0.9	V
Over-Voltage Section						
OVP Threshold	OVP_{TH}	Fault Pin	1.1Vs	1.15Vs	1.2Vs	V
Error Amp Section						
Transconductance	g_m			720		µmho
Input Bias Current	IB_{ERR}	CS1, CS2, CS3	0.5	2.5	5	µA
Input Offset Voltage	VOS_{ERR}	Fb to V_{SET}		3	6	mV
Current Sense Section						
Input Bias Current	IB_{CS}	CS1, CS2, CS3		0.9		µA
Input Offset Voltage	VOS_{CS}	CS1 to CS2, CS1 to CS3		2	4	mV
CS Matching	CS_{MATCH}	Difference between any CS		2	4	mV
Current Limit Section						
OC Threshold Set Current	IB_{OC}	OCSet @ 0V	120	160	200	µA
OC Comp Offset Voltage	VOS_{OC}	OCSet @ OC Threshold	-8	-3	+2	mV
Hiccup Duty Cycle	H_{IC}	Css=0.1uF	1	2.4		%
Soft-Start Section						
Charge Current	I_{SS}	Soft-Start @ 0V	7	10	13	µA
Output Drivers Section						
Rise Time	TR_L TR_H	C_L High Side=3000pF, C_L Low Side=6000pF	25	50	75	ns
Fall Time	TF_L TF_H	C_L High Side=3000pF, C_L Low Side=6000pF	25	50	75	ns
Dead Band	DB_{LH} DB_{HL}	C_L High Side=3000pF, C_L Low Side=6000pF, (Both Measured @ 10%)		130		ns
Oscillator Section						
Osc Frequency per Phase	f_{OSC}	Rt = 50KΩ	100	150	200	KHz
PWM Ramping Voltage	V_{OSC}	Peak to Peak	1.98	2.02	2.06	V
Duty cycle Matching	OSC_{MATCH}	LDrv or HDrv		0.03		%

Note 1: Vs refers to the set point voltage given in Table 1

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	1.075
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.475
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

Table 1 - Set point voltage (Vs) vs. VID codes.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Rt	This pin programs the oscillator frequency in the range of 50KHz to 500KHz with an external resistor connected from this pin to the ground.
2	Comp	Compensation for error amplifier.
3	Fb	This pin is connected directly to the output of the Core supply to provide feedback to the Error amplifier.
4	SS	This pin provides the soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to the ground which ramps up the outputs of the switching regulator, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft-Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
5 6 7	CS1 CS2 CS3	Current sense feedback for channel 1, 2, 3.
8	Vcc	5V supply voltage.
9	V_{SET}	Output of the DAC.
10	D0	LSB input to the DAC that programs the output voltage. This pin is internally connected to 3.3V by a 16K resistor. This pin can be pulled up externally by a 10K resistor to 5V supply. This pin programs the output voltage in 25mV steps based on the VID table.
11	D1	Input to the DAC that programs the output voltage. This pin is internally connected to 3.3V by a 16K resistor. This pin can be pulled up externally by a 10K resistor to 5V supply.
12	D2	Input to the DAC that programs the output voltage. This pin is internally connected to 3.3V by a 16K resistor. This pin can be pulled up externally by a 10K resistor to 5V supply.
13	D3	Input to the DAC that programs the output voltage. This pin is internally connected to 3.3V by a 16K resistor. This pin can be pulled up externally by a 10K resistor to 5V supply.
14	D4	MSB input to the DAC that programs the output voltage. This pin is internally connected to 3.3V by a 16K resistor. This pin can be pulled up externally by a 10K resistor to 5V supply.

PIN#	PIN SYMBOL	PIN DESCRIPTION
15	Fault	Fault detector. When the output exceeds the OVP trip point, the fault pin switches to 2.8V and pulls down the soft-start.
16	OCSet	This pin is connected to the drain of the synchronous MOSFET in channel 1 of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the over current threshold depending on the $R_{DS(ON)}$ of the power MOSFET.
17 28	Gnd	Analog ground for internal reference and control circuitry. Connect to PGnd with a short trace.
18	SD	Shut down pin. Pulling-up this pin disables the outputs.
19	PGood	Power good pin. This pin is a collector output that switches Low when the output of the converter is not within ±10%(typ) of the nominal output voltage.
20	Ref	2V reference output.
21 31	V_{CH3} V_{CH12}	These pins power the high side MOSFET driver. A minmum 1µF ceramic cap must be connected from these pins to ground to provide peak drive current capability.
22 30 32	HDrv3 HDrv2 HDrv1	Output drivers for the high side power MOSFET.
23 27 34	PGnd3 PGnd2 PGnd1	These pins serve as the ground pins and must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1µF) must be connected from pins V_{CL1}, V_{CL23} and V_{CH3}, V_{CH12} to PGnd1, 2 and 3 for noise free operation.
24 26 35	LDrv3 LDrv2 LDrv1	Output driver for the synchronous power MOSFET.
25 36	V_{CL23} V_{CL1}	These pins are connected to the 12V supply and serves as the power Vcc pin for the low side output drivers. A high frequency capacitor (0.1 to 1µF) must be connected directly from these pins to PGnd1, PGnd2 and PGnd3 pins in order to supply the peak current to the power MOSFET during the transitions.
29	NC	No connection.
33	OCGnd	This pin is connected from the source of the synchronous MOSFET in channal 1 of the Core supply and it provides the reference point for the internal current sensing circuitry.

BLOCK DIAGRAM

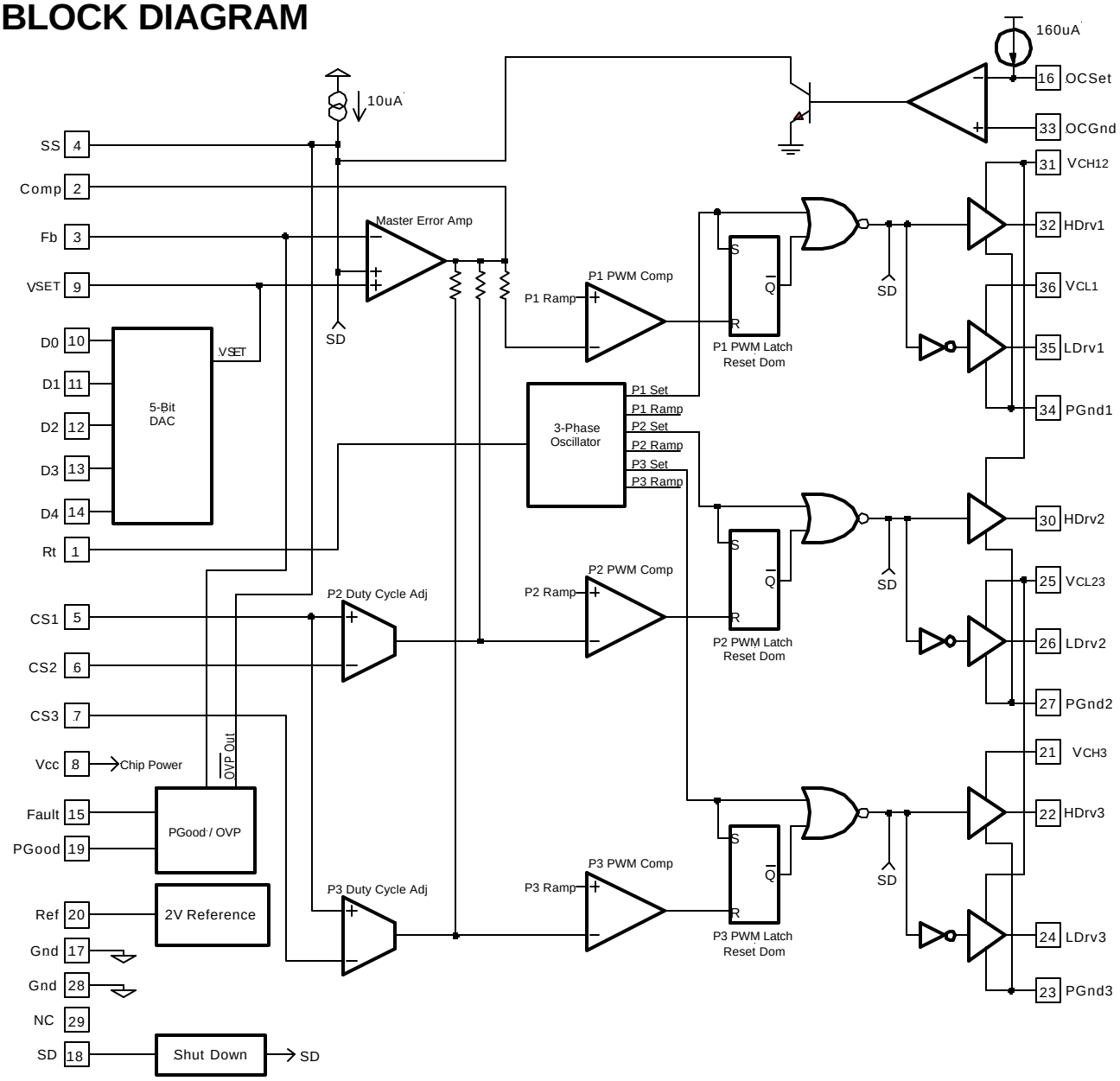


Figure 2 - Simplified block diagram of the IRU3055.

TYPICAL APPLICATION (1)

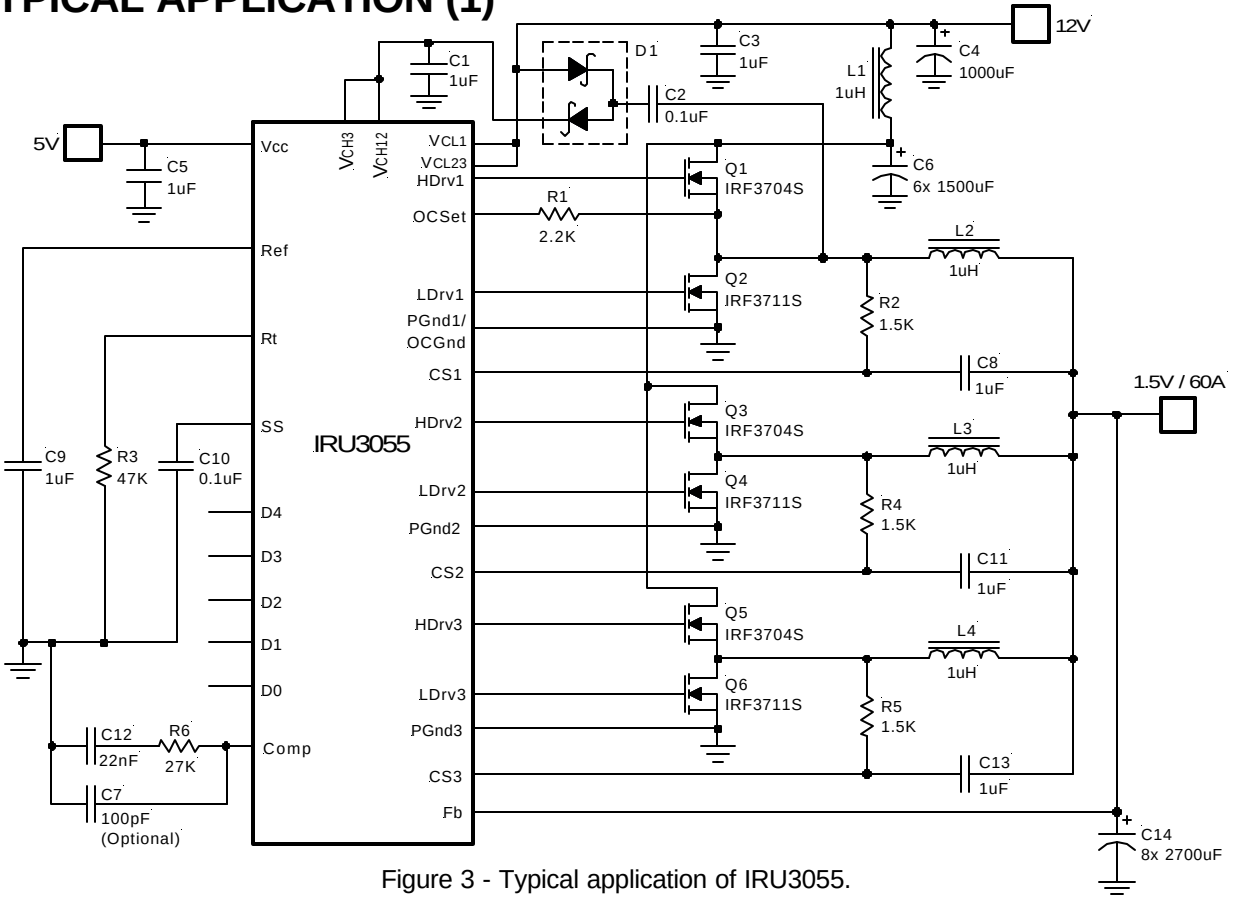


Figure 3 - Typical application of IRU3055.

Parts List

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1,Q3,Q5	MOSFET	20V, 9mΩ	3	IRF3704S	IR	irf.com
Q2,Q4,Q6	MOSFET	20V, 6mΩ	3	IRF3711S	IR	
U1	Controller	Synchronous PWM	1	IRU3055	IR	
D1	Schottky Diode	In Series	1	BAT54S	IR	
L1	Inductor	1µH	1	Z9479-A	Coilcraft	coilcraft.com
L2,L3,L4	Inductor	1µH	3	T60-18 Core, 6-turns #14 AWG wire		
C1	Cap, Ceramic	1µF, X7R, 25V	1	ECJ-3YB1E105K	Panosonic	maco.panasonic.co.jp
C2,C10	Cap, Ceramic	0.1µF, Y5V, 25V	2	ECJ-2VF1E104Z	Panosonic	
C3,C5,C9, C8,C11,C13	Cap, Ceramic	1µF, Y5V, 16V	6	ECJ-3VF1C105Z	Panosonic	
C4	Cap,Electrolytic	1000µF, 16V	1		Any	
C6	Cap,Electrolytic	1500µF, 16V	6	EEU-FJ1C152U	Panosonic	maco.panasonic.co.jp
C7	Cap (Optional)	100pF, X7R, 50V	1	ECU-V1H101KBN	Panosonic	
C12	Cap, Ceramic	22nF, X7R, 50V	1	ECU-V1H223KBG	Panosonic	
C14	Cap,Electrolytic	2700µF,6.3V,13mΩ	8	EEU-FJ0J272U	Panosonic	
R1	Resistor	2.2K, 1%	1		Any	
R2,R4,R5	Resistor	1.5K, 1%	3		Any	
R3	Resistor	47K, 1%	1		Any	
R6	Resistor	27K, 1%	1		Any	

APPLICATION INFORMATION

Constant Switching Frequency 3-Phase Controller

IRU3055 is a 3-phase buck converter controller. For high current applications, multiple converters are usually connected in parallel to reduce the power capability for each individual converter as well as alleviate the thermal stress on each of the power devices. These individual converters share a common output, but may have different input sources. Each individual converter operates at the same switching frequency but at a different phase. As a result, the effective input current and output current ripple are much smaller compared with a single-phase converter. Another benefit will be faster dynamic load responses.

The block diagram of IRU3055 is shown in Figure 2. The 3-phase oscillator provides a constant frequency and the three PWMs ramp signals with 120 degree phase shift. The three comparators and three PWM latches will generate three PWM outputs to the drivers which are built inside the IC. A typical 3-phase PWM signal is shown in Figure 4.

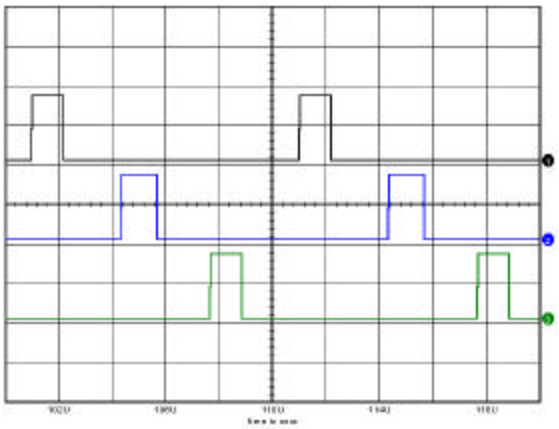


Figure 4 - The 3-phase PWM signal.

Voltage and Current Loop

IRU3055 has three transconductance error amplifiers. The master Error amplifier is used to regulate the output voltage. The output voltage can connect directly, or through a resistor divider, to the Fb pin of the error amplifier. The compensation network at the output of the amplifier (Comp Pin) helps to stabilize the voltage loop. The non-inverting pin of the master amplifier is connected to the output of the DAC which interfaces with the micro processor core and determines the desired output voltage. Two additional transconductance amplifiers are used to balance the output inductor current among 3-phases.

Output Current Ripple Reduction

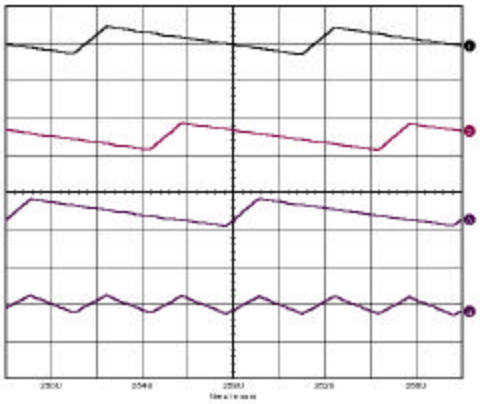


Figure 5 - Output inductor currents and output capacitor ripple current.

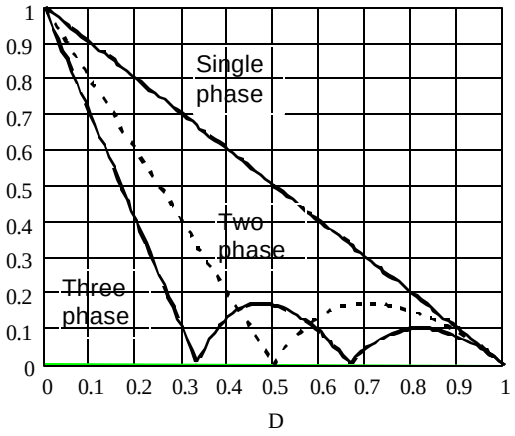


Figure 6 - Normalized output current across output capacitor.
(Peak to peak current normalized to the Vo/(L × Fs)).

One of advantages of the multi-phase converter is that the output current ripple is significantly reduced. The current from multiple converters tend to cancel each other so that the total output current flowing into the output capacitor is reduced. In this case, the output inductor in each individual buck converter can be selected smaller to improve the load transient response without sacrificing the output current ripple. Figure 5 shows a 3-phase inductor current and current ripple in the capacitor for 12V input 1.5V, 50A, 3-phase buck converter. The effective output ripple has three times frequency and a smaller amplitude compared with each individual converter. Figure 6 indicates the total ripple current, as a function of duty cycle, normalized to the parameter Vo/(L × Fs) at zero duty cycle.

It is shown that the output current ripple is greatly reduced by multi-phase operation. At the certain duty cycle D=1/m, where m is the phase number, the output ripple will be near zero due to complete cancelation of inductor current ripple. The optimum number of phases exists for different applications.

Output Inductor Current Sensing

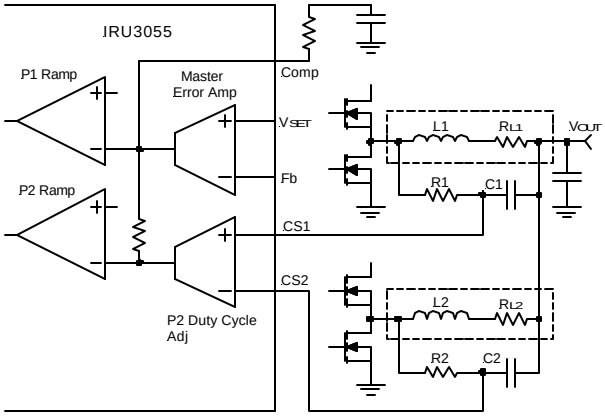


Figure 7 - Loss-less inductive current sensing and current sharing.

The loss-less sensing current is achieved by sensing the voltage across the inductor. In Figure 7, L1 and L2 are inductors. R_{L1} and R_{L2} are inherent inductor resistance. The resistor R1 and capacitor C1 are used to sense the average inductor current. The voltage across the capacitors C1 and C2 represent the average current flowing into resistance R_{L1} and R_{L2}. The time constant of the RC network should be equal or at most three times larger than the time constant L/R_L.

$$R1 \times C1 = (1\sim3) \times \frac{L}{R_L} \qquad \text{---(1)}$$

In order to minimize the effect of the bias current in IRU3055, the sensing resistor should be as small as possible. However, a small resistor will result in high power dissipation and a high value capacitor, a trade off has to be chosen. Typically, a 1µF ceramic capacitor is a good start. In the Application Circuit (1), L=1µH and R_L=1.6mΩ. The sensing resistor and capacitor is chosen as:

R1= 1.5K and C1= 1µF

The voltage across the sensing capacitors are sent to the pins CS1 and CS2. Suppose the inductor current in the inductor L2 is smaller than in inductor L1 and the voltage across capacitor C1 will be greater than that across C2. The transconductance amplifier in IRU3055 will generate a positive current flowing into node Comp. Through an internal resistor, there will be an additional voltage drop above the node Comp and then the voltage sent to the PWM comparator will be higher and the generated duty cycle for phase-2 will be larger. As a result, the inductor (L2) current will go up until the current balance is achieved. For accurate current sharing, the current sense from each inductor should be as symmetrical as possible. The layout is critical and the layout of the RC network should be as follows:

Connect the node from Resistor R1 (or R2) directly to the pad of inductor. Connect the other node of capacitor C1 and C2 together and connect to the output voltage terminal. In this case, the voltage at node C1 and C2 will have a common reference voltage that is output voltage. If the inductor inherent resistance as well as PCB trace are almost identical or symmetrical, almost perfect current sharing can be obtained. The PCB connection from three inductors to the output capacitor should have the same length and width. The feedback point from the output should be located such that the effect impedances from the three inductors to the output feedback sensing point are almost symmetrical or identical so that the noise will cancel each other. The current sharing accuracy is dependent upon the mismatch among the values of current sensing components and the current amplifier offset. It is recommended that all the inductors be from the same manufacturer and also be the same model so that mismatch will be minimized and the cost reduced. In most cases, with a good layout, the difference between 3-channel currents can be limited to be below 2A.

Operation of IRU3055

Over Current Protection

The IRU3055 senses the MOSFET switching current to achieve the over current protection. The diagram is shown in Figure 8. A resistor (R_{SET}) is connected between pin OCSet and the drain of the low side MOSFET for phase1. Inside the IC, there is an internal 160µA current source connected to OCSet pin. When the upper switch is turned off, the inductor current flows through the low side switch. The voltage at OCSet pin is given as:

$$V_{OCSet} = 160\mu A \times R_{SET} - R_{DS(ON)} \times i_{L1} \qquad \text{---(2)}$$

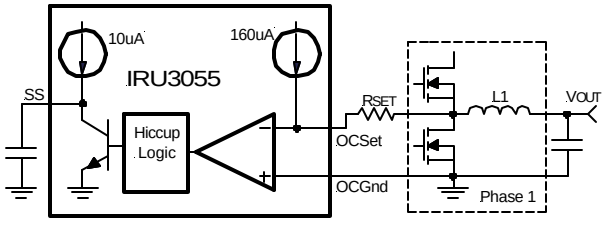


Figure 8 - Diagram of the over current sensing.

When the inductor current is large enough, the voltage across the low side switch is low enough so that the voltage at OCSet node is below zero and the comparator will flip and trigger a switch to discharge the soft-start capacitor at a certain slope rate. The system enters into a hiccup mode. The over current threshold can be set by resistor R_{SET}. Suppose the current sharing is perfect, then the current flowing into phase 1 will be one third of the total output current. The maximum allowed output current can be represented as:

$$I_{MAX} = 160\mu A \times R_{SET} / (R_{DS(ON)}/3)$$

$$R_{SET} = I_{MAX} \times R_{DS(ON)}/3/160\mu A \quad ---(3)$$

Where $R_{DS(ON)}$ is the ON resistance of low side MOSFET. In practice, the $R_{DS(ON)}$ of MOSFET is temperature dependent. The overhead has to be considered. For practice, over current threshold has to be at least 50% higher than the nominal current plus ripple. In the demo-board, the maximum output current is set to be:

$$I_{MAX} = (1+50\%) \times I_{OUT} = 1.5 \times 60A = 90A$$

Consider ripple current, select I_{MAX}=100A

For each phase, the maximum current is one third (33A), assuming good current sharing. The low side of MOSFET is IRF3711S. The On resistor at 150 degrees is given from the data sheet:

$$R_{DS(ON)} = 1.5 \times 6m\Omega = 9m\Omega$$

The over current setting resistor can be set as

$$R_{SET} = 33A \times 0.009/160\mu A = 1.86K$$

Select R_{SET} = 2.2K

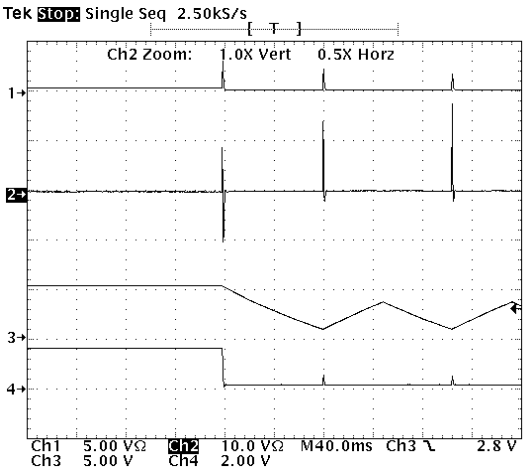


Figure 9 - Operation waveforms at short circuit. (Hiccup mode)

Ch1: Input current, 5A/div.
Ch2: Phase 1 inductor current, 10A/div.
Ch3: Soft-start capacitor voltage, 5V/div.
Ch4: Output voltage, 2V/div.

Over Voltage Protection

The Fb pin is connected to the output voltage. An overvoltage condition is detected when the voltage at Fb pin is 15% higher than the programmed voltage by DAC. When the overvoltage occurs, the soft-start capacitor is discharged. The high side MOSFETs are turned off and the low side MOSFETs are turned on. As a result, the low side MOSFET of synchronous rectifier conduct and shunt the output voltage to ground and protect the load. In the meantime, the PGood pin is held to low.

Soft-Start

The IRU3055 has a soft-start function to limit the current surge at the start-up. An external capacitor which is charged by a 10μA internal current source is used to program the soft-start timing. The voltage of the external capacitor linearly increases, which forces the output voltage to go up linearly until the voltage at soft-start reaches the desired voltage. The following equation can be used to calculate the start up time.

$$10\mu A \times t_{START}/Css = V_{SET}+0.7V$$

$$t_{START} = (V_{SET}+0.7V) \times Css/10\mu A \quad ---(4)$$

Where:

Css is the soft-start capacitor (μF).

V_{SET} is the voltage from DAC and equal to the desired output voltage.

For a 7.5ms start-up time and 1.5V output, the required capacitor will be 33nF.

Operation Frequency Selection

The operation switching frequency is determined by an external resistor (Rt). The switching frequency is approximately inversely proportioned to resistance (see Fig.10). The switching frequency can also be estimated by:

$$Fs \cong 7500/Rt \quad ---(5)$$

Where Rt is in KΩ and Fs is in KHz.

For example, if the 150KHz switching frequency is selected, the required Rt is calculated as:

$$Rt \cong 7500/150 = 50K\Omega$$

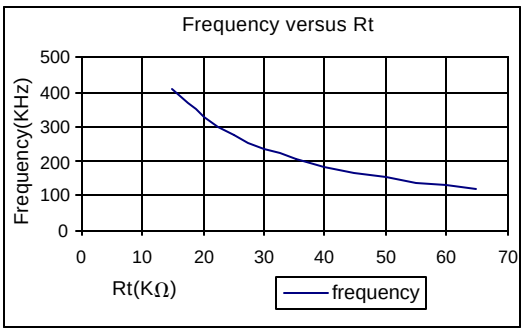


Figure 10 - The operation frequency vs. Rt.

Synchronous-Rectifier Driver

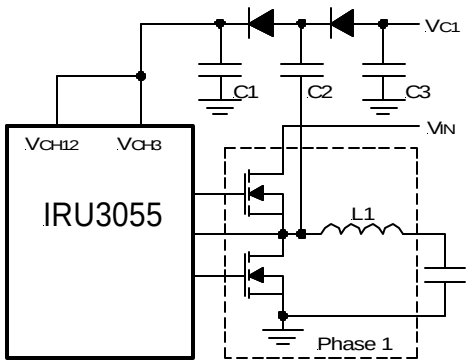


Figure 11 - Supply V_{CH12}, V_{CH3} with charge bump configuration.

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky diode or MOSFET body diode with a low on-resistance MOSFET switch. The synchronous rectification also ensures good transient dynamic. For IRU3055, the 3-phase synchronous rectifier MOSFET drivers are built inside. To drive the high-side MOSFET, it is necessary to supply a gate voltage at least 4V greater than the bus voltage. In IRU3055, the driver supply voltage for high side MOSFET driver is supplied through the V_{CH12} and V_{CH3} pins. If the input voltage for DC-DC converter is 5V, the V_{CH12} and V_{CH3} pins can be connected to 12V or supplied by using charge pump configuration as shown in Figure 11.

If the voltage Vc1 and V_{IN} in Figure 11 is connected to input voltage 12V, the voltage at V_{CH12} and V_{CH3} pins are charged up to almost twice the input voltage. The high side driver can be enabled. A capacitor in the range of 0.1µF to 1µF is generally adequate for capacitor C2. For high current applications, a large ceramic capacitor such as 2.2µF is recommended. The diode can be a Schottky diode such as BAT54S.

With the charge bump configuration, shown in Figure 11, the voltage at pins V_{CH12} and V_{CH3} can be boosted up. When the low side MOSFET is on, the capacitor C2 is charged to voltage Vc1. When the high side MOSFET is ON, the energy in the capacitor C2 is discharged to the bypass capacitor C1 next to pins V_{CH12} and V_{CH3}. The voltage at V_{CH12} and V_{CH3} pins is approximately the sum of the voltage Vc1 and V_{IN}. The high side driver signal should be at least 4V higher than the input voltage (V_{IN}). The voltage Vc1 has to be 5V or higher. For the demo-board, Vc1 is equal to input voltage (V_{IN}=12V). If the low power dissipation of IC is preferred, especially at higher frequency, Vc1 can be connected to 5V instead.

Component Selection Guide

Output Inductor Selection

The inductor is selected based on the inductor current ripple, operation frequency and efficiency consideration. In general, a large inductor results in small output ripple and higher efficiency but big size. A small value inductor causes large current ripple and poor efficiency but small size. Generally, the inductor is selected based on the output current ripple. The optimum point is usually found between 20% and 50% ripple of output inductor current. For each phase synchronous buck converter, the output peak-to-peak current ripple is given by:

$$\Delta i_{(PEAK - PEAK)} = (V_{IN}-V_{OUT}) \times V_{OUT}/(L \times Fs \times V_{IN}) \quad ---(6)$$

Assuming the output current is evenly distributed in each phase, we can define the ratio of the ripple current and nominal output current as:

$$LIR = \Delta i_{(PEAK - PEAK)} / I_{OUT} / m$$

Where LIR is typically between 20% to 50% and m is the phase number. In this case m=3. Then the inductor can be selected by:

$$L > V_{OUT} \times (V_{IN}-V_{OUT})/(Fs \times V_{IN} \times LIR \times I_{OUT}/m) \quad ---(7)$$

For example, in the application circuit, the ripple is selected as LIR=40%, the inductor is selected as:

$$L > 1.5 \times (12-1.5)/(150K \times 12 \times 40\% \times 60A/3) = 1.1\mu H$$

Select L=1µH

The RMS current of the inductor will be approximately equal to average current:

$$I_{OUT}/m = 60/3 = 20A.$$

The peak inductor current is about:

$$I_{L(PEAK)} = (1+LIR/2) \times I_{OUT}/m = 1.2 \times 20 = 24A$$

Output capacitor selection

The voltage rating of the output capacitor is the same as output voltage. Typical available capacitors on the market are electrolytic, tantalum and ceramic. If electrolytic or tantalum capacitors are employed, the criteria is normally based on the value of Effective Series Resistance (ESR) of total output capacitor. In most cases, the ESR of the output capacitor is calculated based on the following relationship:

$$ESR < \Delta V/\Delta i \quad ---(8)$$

Where ΔV is the maximum allowed output voltage drop during the transient and Δi is the maximum output current variation. In the worst case, Δi is the maximum output current minus zero.

Power MOSFET Selection

The IRU3055 is a controller for 3-phase synchronous buck converter. For each phase, the average inductor current will be one third of the total output current in an ideal case, which will greatly alleviate the thermal management for power switch. In general, the MOSFET selection criteria depends on the maximum drain-source voltage, RMS current and ON resistance ($R_{DS(ON)}$). For both high side and low side MOSFET, a drain-source voltage rating higher than maximum input voltage is necessary. In the demo-board, 20V rating should be satisfied. The gate drive requirement for each MOSFET is almost the same. If logic-level MOSFET is used, some caution should be taken with devices at very low VGS to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through circuit.

If output inductor current ripple is neglected, the RMS current of high side switch is given by:

$$I_{RMS(HI)} = \sqrt{D} \times I_{OUT}/m$$

$$I_{RMS(HI)} = \sqrt{(V_{OUT}/V_{IN})} \times I_{OUT}/m \quad \text{---(9)}$$

The RMS current of low side switch is given as:

$$I_{RMS(LO)} = \sqrt{(1 - D)} \times I_{OUT}/m$$

$$I_{RMS(LO)} = \sqrt{(1 - V_{OUT}/V_{IN})} \times I_{OUT}/m$$

In the demo board, RMS current of high side switch is:

$$I_{RMS(HI)} = \sqrt{(1.5/12)} \times 60/3 = 7.1A$$

RMS current of low side switch is:

$$I_{RMS(LO)} = \sqrt{(1 - 1.5/12)} \times 60/3 = 18.7A$$

For $R_{DS(ON)}$ of MOSFET, it should be as small as possible in order to get highest efficiency. The MOSFET from International rectifier IRF3704S with a $R_{DS(ON)}$=9mΩ, 20V drain source voltage rating and 77A I_D is selected for high side MOSFET.

For a high input and low output case, the low side switch conducts most of output current and handles most of the thermal management. Two MOSFETs can be put in parallel to further reduce the effect $R_{DS(ON)}$ and conduction losses. In the demo-board, MOSFET from International Rectifier IRF3711S with $R_{DS(ON)}$=6mΩ, 20V V_{DS} and 110A I_D is selected as synchronous MOSFET. The power dissipation includes conduction loss and switching loss.

The conduction loss for high side switch in each phase can be estimated by the following equation:

$$P_{CON(HI)} = R_{DS(ON)} \times q \times (I_{OUT}/m) \times (I_{OUT}/m) \times (V_{OUT}/V_{IN})$$

The low side switch power dissipation is:

$$P_{CON(LO)} = R_{DS(ON)} \times q \times (I_{OUT}/m) \times (I_{OUT}/m) \times (1-V_{OUT}/V_{IN})$$

Where q is the temperature coefficient of ON resistor of MOSFET $R_{DS(ON)}$ and can be found in MOSFET data sheet (typically between 1 and 2).

In this example, the MOSFET IRF3704S is chosen to be the high side switch with:

$R_{DS(ON)}$ = 9mΩ
q = 1.5 @ 150°C

The conduction loss for high side MOSFET is given as:

$$P_{CON(HI)} = 9m\Omega \times 1.5 \times (60/3) \times (60/3) \times 1.5/12 = 0.68W$$

Low side switch is configured with one IRF3711 with 6mΩ $R_{DS(ON)}$. The conduction loss is calculated as:

$$P_{CON(LO)} = 6m\Omega \times 1.5 \times (60/3) \times (60/3) \times (1-1.5/12)$$
$$P_{CON(LO)} = 3.15W$$

The switching loss for MOSFET is more difficult to calculate due to effect of the parasitic components, etc. The switching loss can be estimated by the following equation:

$$P_{SW} = V_{DS(OFF)} \times (tr+tf) \times F_S \times I_{SW}/2$$

Where:
$V_{DS(OFF)}$ is the Drain to Source voltage when switch is turned off.
tr is the rising time.
tf is the fall time.
F_S is the switching frequency.
I_{SW} is the current in MOSFET when MOSFET is turned off. It can be estimated by:

I_{SW} = I_{LOAD}/m + half of the ripple current

In this example, for low side MOSFET, the body diode is turned on before MOSFET is on. Therefore, the switching losses for low side MOSFET is almost zero due to zero voltage switching. For high side MOSFET, from data sheet, we have:

tr = 50ns
tf = 50ns
Select F_S = 150KHz
$V_{DS(OFF)}$ = 12V
I_{SW} = Peak Inductor Current = 24A
$P_{SW(HI)} = 12V \times (50ns+50ns) \times 150KHz \times 24A/2$
$P_{SW(HI)}$ = 2.1W

The total power dissipation is:

$P_{D(HI)} = P_{CON(HI)} + P_{SW(HI)}$
$P_{D(HI)}$ = 0.68W+2.16W = 2.84W
$P_{D(LO)} \cong P_{CON(LO)}$ = 3.15W

Heat Sink Selection

The criteria of selecting heat sink is based on the maximum allowable junction temperature of the MOSFETs. That is:

$$T_A + P_D \times (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) < T_{J(MAX)}$$

Where:

T_A = The Ambient Temperature

P_D = Power Dissipation of each MOSFET

$R_{\theta JC}$ = The Thermal Resistance from junction to case

$R_{\theta CS}$ = the thermal resistance from case to heat sink

$R_{\theta SA}$ = the heat-sink-to-air thermal resistance

$T_{J(MAX)}$ = maximum allowable junction temperature of MOSFET, for example 150°C.

The maximum heat-sink-to-air thermal resistance is calculated as:

$$R_{\theta SA} < (T_{J(MAX)} - T_A)/P_D - R_{\theta JC} + R_{\theta CS}$$

In this example, the MOSFET is mounted in the PCB board with more than 1" square PCB board. Therefore, the junction temperature for MOSFET can be calculated as:

$$T_J = T_A + P_D \times R_{\theta JA}$$

Where $R_{\theta JA}$ is the junction-to-ambient thermal resistance with MOSFET on 1" square PCB board and it is available from MOSFET data sheet.

For MOSFET IRF3704S with D2 package, $R_{\theta JA}$ = 40°C/W. Assume ambient temperature is T_A=35°C. For high side MOSFET, the junction temperature is given as:

$$35°C + 2.84W \times 40°C/W = 149°C$$

For low side MOSFET, IRF3711s, the maximum junction temperature can be calculated as:

$$35°C + 3.15W \times 40°C/W = 161°C$$

This is the worst case. For conservative consideration, two IRF3711 can be put in parallel.

Input Filter Selection

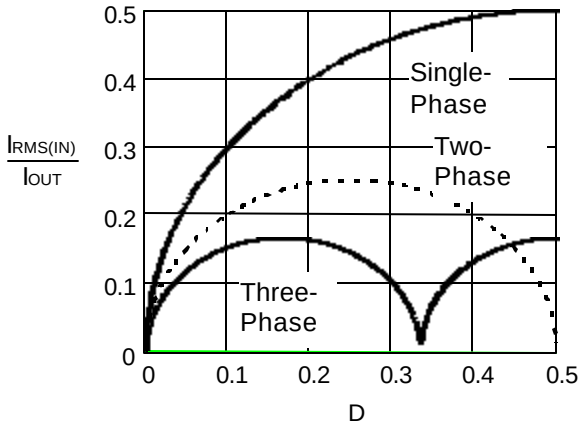


Figure 12 - Normalized input RMS current vs. duty cycle.

The selection criteria of input capacitor are voltage rating and the RMS current rating. For conservative consideration, the capacitor voltage rating should be 1.5 times higher than the maximum input voltage. The RMS current rating of the input capacitor for multi-phase converter can be estimated from the above Figure 12.

First, determine the duty cycle of the converter (V_O/V_{IN}). The ratio of input RMS current over output current can be obtained. Then the total input RMS current can be calculated. From this figure, it is obvious that a multi-phase converter can have a much smaller input RMS current, which results in a lower amount of input capacitors that are required.

For high current applications, multiple bulk input capacitors in parallel may be necessary. Some electrolytic capacitors, such as Panasonic HFQ series, Sanyo MV-WX or equivalent may be put in parallel to provide a large current. In addition, ceramic bypass capacitors for high frequency de-coupling are recommended. Furthermore, some small ceramic capacitors should be put very close to the drain of the high side MOSFET and source of the low side switch to suppress the voltage spike caused by parasitic circuit parameters.

For high current applications, a 1µH input inductor is recommended to slow down the input current transient.

Design Example

In the demo-board, the condition is as follows:

V_{IN}=12V, V_{OUT}=1.5V and I_{OUT}=60A

Output voltage regulation is within 100mV during transient.

(1) Select Switching Frequency

Fs = 150KHz for each phase

According to Figure 10 and equation (5), the oscillator selection resistor is given by:

Rt ≅ 7500/150 = 50K
From Figure 10, select Rt=47K

(2) Soft-Start Capacitor

For 1.5V output, V_{SET}=1.5V. The soft-start time of the converter can be estimated from equation (4):

$t_{START} = (V_{SET}+0.7V) \times Css/10\mu A$

If t_{START}=20ms, then:

Css = 20ms × 10μA/(1.5V+0.7V) = 95nF
Choose Css=0.1μF

(3) Output Inductor and Capacitor

Select the current ripple LIR=40%, by equation (7):

$L>V_{OUT} \times (V_{IN}-V_{OUT})/(Fs \times V_{IN} \times LIR \times I_{OUT}/m)$

$L>1.5 \times (12-1.5)/(150K \times 12 \times 40\% \times 60A/3)=1.1\mu H$

Select core from Micrometal, T60-18 with 6 turns #14 AWG wire, which gives 1μH inductor, 15A RMS and 25A saturation current. The DC resistor of inductor is 1.6mΩ.

L = 1μH and R_L = 1.6mΩ

The output capacitor is based on ESR. Suppose the maximum allowed voltage droop for 60A load is:

ΔV = 100mV
ESR < ΔV/Δi = 100mV/60A = 1.66mΩ

Select 8 Panasonic capacitors. EEUFJ0J272U with 2700μF and 13mΩ ESR each. The total:

C_{OUT} = 8 × 2700μF = 21600μF
ESR = 13mΩ/8 = 1.6mΩ

(4) Senseless Inductor Current Sensing

With equation (1), we select the inductor sensing network which has a time constant:

$R2 \times C8 = 2 \times L/R_L$
Select: C8 = 1μF
R2 = 2 × 1μH/(1.6mΩ × 1uF) = 1.25K

Select R2, R4 and R5 = 1.5K

(5) MOSFET Selection

By equation (9), the RMS current of high side MOSFET is given as:

$I_{RMS(HI)} = \sqrt{D} \times I_{OUT}/m$
$I_{RMS(HI)} = \sqrt{(V_{OUT}/V_{IN})} \times I_{OUT}/m$
D = 1.5/12 = 0.125
$I_{RMS} = \sqrt{0.125} \times 60A/3 = 7.1A$

Select MOSFET from International Rectifier IRF3704S with D-2 pak, which will result to:

$R_{RDS(ON)}$ = 9mΩ and 110A I_{DS} current

For low side MOSFET:

$I_{RMS(LO)} = \sqrt{(1-D)} \times I_{OUT}/m$
$D = V_{OUT}/V_{IN}$ = 1.5/12 = 0.125
$I_{RMS(LO)} = \sqrt{(1-0.125)} \times 60/3 = 19A$

Select MOSFET from International Rectifier IRF3711S with D-2 package, which will result to:

$R_{DS(ON)(LO)}$ = 6mΩ and 110A current

(6) Over Current Setting

By equation (3), over current limit is set by R_{SET}. The current limit should be at least 150% of the nominal output current. Set I_{MAX}=90A and 30A for each phase. For low side MOSFET, $R_{DS(ON)}$=6mΩ and 9mΩ at 150°C. The over current setting resistor is given by:

$R_{SET} = I_{MAX} \times R_{DS(ON)}/3/160\mu A$
R_{SET} = 90A × 9mΩ/3/160μA = 1.7KΩ
Select R_{SET} = 2.2KΩ

(7) Compensation Design

For detailed explanation, please see IRU3037 data sheet. Select bandwidth of the system to be 1/10 of switching frequency that is 15KHz:

Fo = 2 × 3.14 × 15KHz = 94KHz

The compensation resistor can be calculated as:

$Rc = Vosc \times Fo \times L/(V_{IN} \times ESR \times g_m)$

Where Vosc is the ramp peak voltage and g_m is the transconductance of the error amplifier. From the data sheet:

Vosc = 2V
g_m = 720μmho

Rc = 2 × 94KHz × 1μH/(12 × 1.6mΩ × 720μmho)
Rc = 12KΩ. Select R6=Rc=12.7KΩ

The compensator capacitor is given as:

$Cc = \sqrt{(L \times C_{OUT})}$ /0.75/Rc
$Cc = \sqrt{(1\mu H \times 21600\mu F)}$ /0.75/12KΩ = 16.3nF
Select C12=Cc=22nF

In practice, the resistor Rc (R6 in Fig.3) can be tuned for a better dynamic load response. Higher Rc will result in a fast transient response. Cc (C12 in Fig.3) can be kept unchanged. In Fig.3. R6=27KΩ.

(8) Input Capacitor Selection

From the Figure 12, according to the duty ratio, pick up the normalized input RMS current. For this example:

$I_{RMS(IN)}/I_{OUT} = 0.15$

$I_{RMS(IN)} = 0.15 \times 60A = 9A$

Select Panosonic capacitor. Four EEUFJ1C152U with1500μF give results to:

$4 \times 2.5 = 10A$ RMS current.

Layout Considerations

For any switching converter, the current transition from one power device to another usually causes voltage spikes across the power component due to parasitic inductance and capacitance. These voltage spikes will result in reduction of efficiency, increased voltage stress of power components and radiated noise to circuit. A good layout can minimize these effects.

There are several critical loops for IRU3055 controlled multi-phase converter. The loop by synchronous MOSFETs and input capacitor is the most critical loop and it should be minimized as small as possible. Put a small ceramic capacitor next to the drain of high side switch and source of low side switch. Put the input capacitors to the high and low side switch as close as possible. The second loop is the gate of MOSFETs and the drivers from IRU3055. Because the IRU3055 includes the MOSFETs drivers inside, the signal path between driver to the gate of MOSFETs should be minimized. The trace should handle 1A transient current ability.

The following is a guideline of how to place the critical components and the connections between components in order to minimize the switching noises.

Start the layout by first placing the power components:

(1) Place the high side MOSFET Q1 and low side MOSFET Q2 as close to each other as possible so that the source of Q1 and drain of Q2 has the most possible shortest length.

(2) Place a capacitor (Electrolytic or ceramic or both) close to the drain of Q1 and source of Q2.

(3). If needed, place a snubber RC circuit next to Q2.

(4). Place the other 2-phase Q3, Q4 and Q5, Q6 following the same rule.

(5) Place output inductor Lo1, Lo2, Lo3 and output capacitor C_{OUT}. Make sure the output capacitors are evenly distributed among 3-phases and close to the output slot.

(6) Place IC IRU3055 such that the driver pins, HDrv1, HDrv2, Hdrv3 and LDrv1, LDrv2, LDrv3, have a relatively short distance from the corresponding MOSFET gate. In addition, make the 3-phase driving signal path as symmetrical as possible. If the length of the gate signal path is more than 1cm long, a 2 to 10Ω gate resistor is recommended to be in series in the gate signal path.

(7) Place bypass capacitor close to Vcc pin, V_{REF} pin and V_{CH12},V_{CH3} pins and also soft-start capacitor to SS pin.

(8) Place a frequency selection resistor (Rt) close to Rt pin.

(9) Connect output inductor current sensing network such as R2, C8 close to IRU3055. One example of the layout is shown as follows:

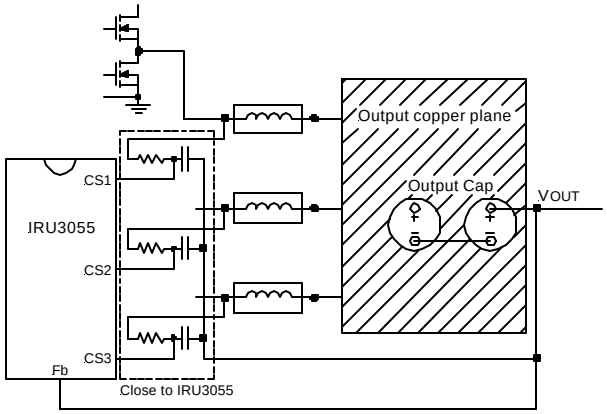


Figure 13 - An example of layout connection for inductor current sensing.

Connect current sensing resistors Rs1,Rs2,Rs3 right to the pads of output inductor Lo1,Lo2,Lo3. Connect the other node of current sensing capacitors Cs1,Cs2,Cs3 together and directly connect to the output voltage terminal, which is also the sensing point for output voltage feedback sensing.

(10) Place feedback resistors (R_{FB1} and R_{FB2}) close to IC and place compensator network close to Comp pin. Note that the resistor R_{FB1} and R_{FB2}, can be used to set the outputs slightly higher to account for the output drop at the load due to the trace resistance.

Component Connection

• No data bus should be passing through the switching regulator especially close to the fast transition nodes such as PWM drivers or the inductor voltage.

• If possible, using four layer board, dedicate one layer to ground, another layer as power layer for the constant power input and output such as 5V, 12V, and 1.5V output. Connect all grounds to the ground plane using direct vias to the ground plane.

• Use large and low impedance/low inductance PCB plane to connect the high current path connections either using component side or the solder side. These connections include:

(a) Input capacitor to the drain of high side MOSFET Q1, Q3 and Q5.

(b) The interconnection between source of high side MOSFET such as Q1 and low side MOSFET such as Q2.

(c) From drain of low side MOSFET to output Inductor .

(d) From output inductor to output capacitor. Make sure the impedance from output inductor to output voltage slot (also the voltage feedback sensing point) are as identical or symmetrical as possible.

(e) From each output capacitor to output slot.

(f) From input inductor to input capacitor.

Connect the rest of the components using the shortest trace possible.

TEST WAVEFORMS FOR TYPICAL APPLICATION (1)

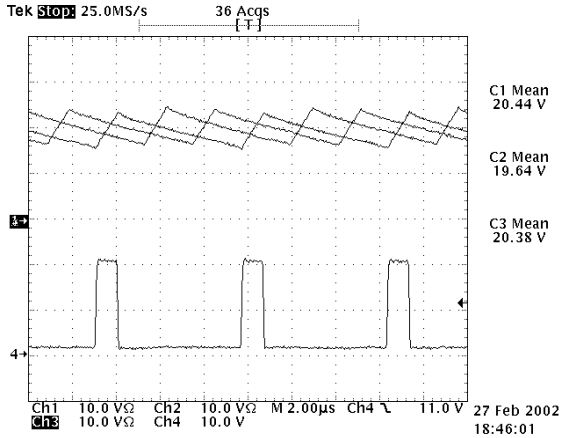


Figure 14 - 3-Phase inductor current at 60A load, Ch1, Ch2 and Ch3: 10A/div. Ch4: gate signal.

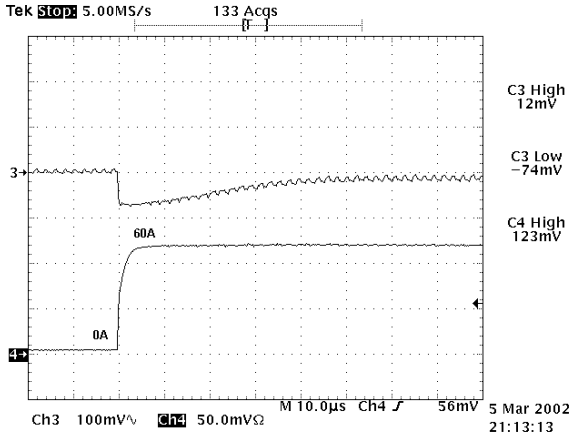


Figure 17 - Zoomed 60A Load dynamic (rising).
Ch3: Output voltage, 100mV/div, AC.
Ch4: Load current, 20A/us, sensed by 2mΩ resistor, 25A/div.

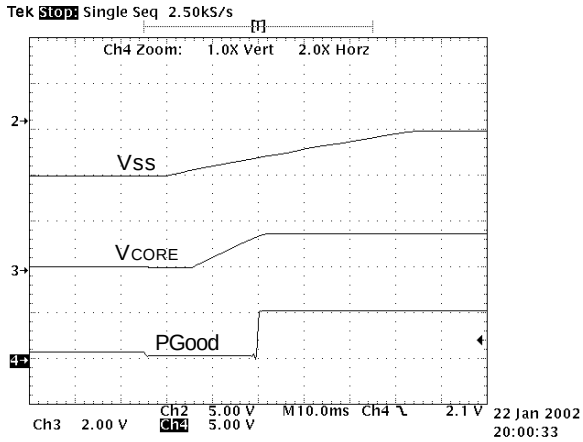


Figure 15 - Soft-start, Vcore and PGood.

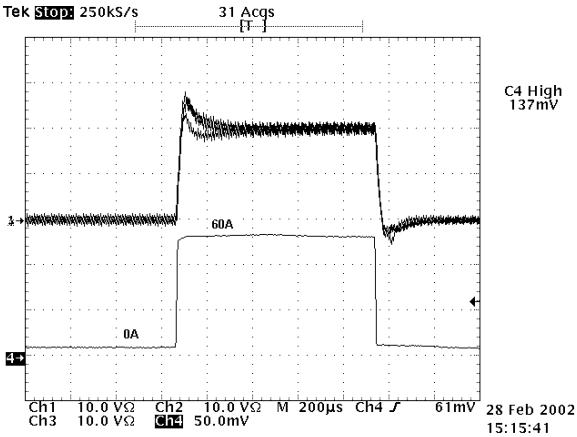


Figure 18 - 60A load dynamic waveforms with three-phase inductor current.
Ch1, Ch2 and Ch3: Inductor current, 10A/div.
Ch4: Load current, 20A/us, sensed by 2mΩ resistor, 25A/div.

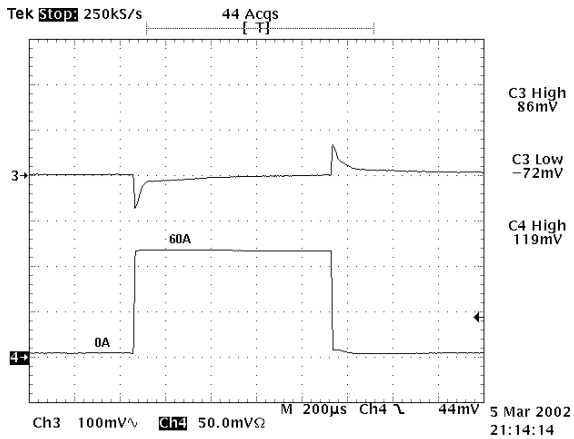


Figure 16 - 60A Dynamic load response with 20A/µs slew rate.
Ch3: Output voltage, 100mV/div, AC.
Ch4: Load current, 20A/us, sensed by 2mΩ resistor, 25A/div.

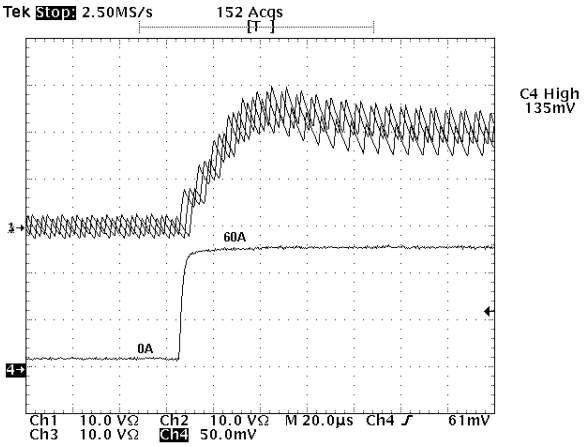


Figure 19 - 60A load dynamic waveforms with three-phase inductor current. (Zoomed)
Ch1, Ch2 and Ch3: Inductor current, 10A/div.
Ch4: Load current, 20A/us, sensed by 2mΩ resistor, 25A/div.

TYPICAL APPLICATION (2)

For Intel Pentium 4 processor with Vcc VID generation and active voltage droop

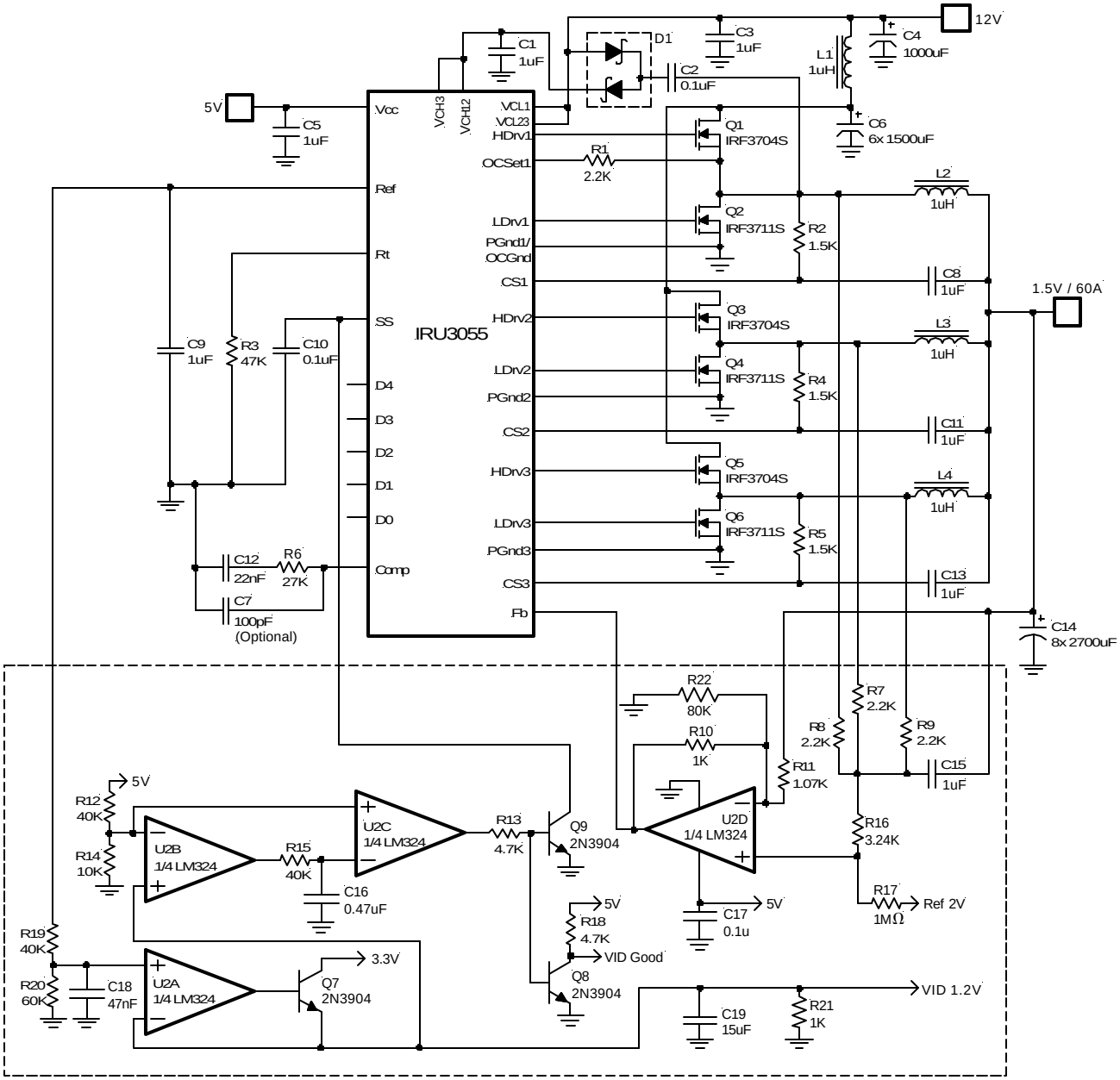


Figure 20 - Application circuit of IRU3055 to implement active voltage droop as well as the 1.2V VID voltage with VccVID Power Good.

PARTS LIST FOR TYPICAL APPLICATION (2)

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1,Q3,Q5	MOSFET	20V, 9mΩ	3	IRF3704S	IR	irf.com
Q2,Q4,Q6	MOSFET	20V, 6mΩ	3	IRF3711S	IR	
U1	Controller	Synchronous PWM	1	IRU3055	IR	
D1	Schottky Diode	In Series	1	BAT54S	IR	
L1	Inductor	1μH	1	Z9479-A	Coilcraft	coilcraft.com
L2,L3,L4	Inductor	1μH	3	T60-18 Core, 6-turns #14 AWG wire		
C1	Cap, Ceramic	1μF, X7R, 25V	1	ECJ-3YB1E105K	Panosonic	maco.panasonic.co.jp
C2,C10	Cap, Ceramic	0.1μF, Y5V, 25V	2	ECJ-2VF1E104Z	Panosonic	
C3,C5,C9, C8,C11,C13	Cap, Ceramic	1μF, Y5V, 16V	6	ECJ-3VF1C105Z	Panosonic	
C4	Cap,Electrolytic	1000μF, 16V	1		Any	
C6	Cap,Electrolytic	1500μF, 16V	6	EEU-FJ1C152U	Panosonic	maco.panasonic.co.jp
C7	Cap (Optional)	100pF, X7R, 50V	1	ECU-V1H101KBN	Panosonic	
C12	Cap, Ceramic	22nF, 50V	1		Panosonic	
C14	Cap,Electrolytic	2700μF,6.3V,13mΩ	8	EEU-FJ0J272U	Panosonic	
R1	Resistor	2.2K, 1%	1		Any	
R2,R4,R5	Resistor	1.5K, 1%	3		Any	
R3	Resistor	47K, 1%	1		Any	
R6	Resistor	27K, 5%	1		Any	
Q7,Q8,Q9	NPN Transistor		3	2N3904	Any	
U2A,B,C,D	OPAMP		1	LM324	Any	
C15	Cap, Ceramic	1μF, X7R, 16V	1	ECJ-2YB1C105K	Panosonic	maco.panasonic.co.jp
C16	Cap, Ceramic	0.47μF, X7R, 16V	1	ECJ-2YB1C474K	Panosonic	
C17	Cap, Ceramic	0.1μF, Y5V, 25V	1	ECJ-2VF1E104Z	Panosonic	
C18	Cap, Ceramic	47nF, X7R, 16V	1	ECJ-2VF1E473K	Panosonic	sanyo.com
C19	Cap, POSCAP	15μF, 6.3V	1		Sanyo	
R7,R8,R9	Resistor	2.2K, 1%	3		Any	
R13,R18	Resistor	4.7K, 5%	2		Any	
R10,R21	Resistor	1K, 1%	2		Any	
R11	Resistor	1.07K, (tuned), 1%	1		Any	
R12,R15, R19	Resistor	40K, 1%	3		Any	
R14	Resistor	10K, 1%	1		Any	
R16	Resistor	3.24K, (tuned), 1%	1		Any	
R17	Resistor	1MΩ, 1%	1		Any	
R20	Resistor	60K, 1%	1		Any	
R22	Resistor	80K, 1%	1		Any	

Introduction to Intel Specification

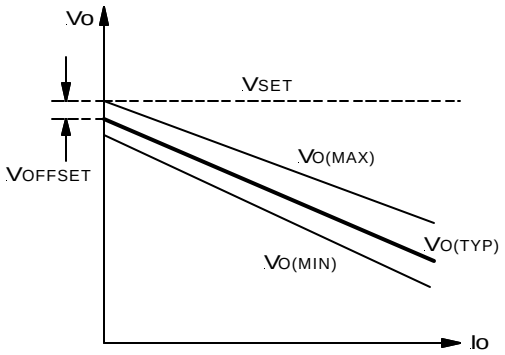


Figure 21 - The Intel specification for the load line.

According to the Intel spec, the output voltage is dependent on the load current. When the current goes up, the voltage goes down. The characteristic can be modeled by the following:

$$Vo = V_{SET} - V_{OFFSET} - K_{LOAD} \times Io \quad ---(10)$$

Where V_{OFFSET} is the offset voltage and K_{LOAD} is the slope of load line.

Rearrangement results in:

$$V_{SET} = Vo + V_{OFFSET} + K_{LOAD} \times Io \quad ---(11)$$

For Intel spec:

V_{OFFSET} = 25mV

K_{LOAD} = 98mV/45A = 2.18mΩ

Implementation of Voltage Droop with IRU3055

With a single single-ended OPAMP, the IRU3055 can achieve voltage droop function as shown in Figure 22. The voltage Vc is a constant voltage such as 2V or 5V. The signal Vo+Rs × Io can be from inductor current sensing. The real application circuit is shown in Figure 20.

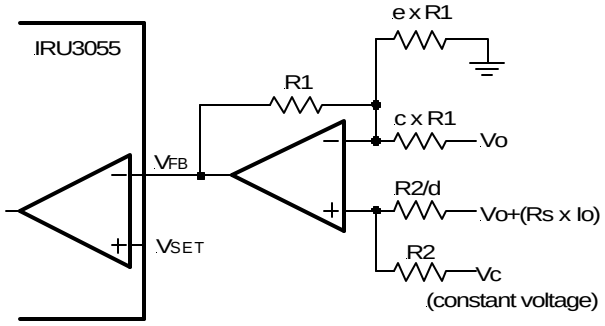


Figure 22 - Implement voltage droop with a single OPAMP.

With this simple circuit, the output voltage will linearly decrease as load current increases. The output voltage will fall in Intel spec. The resistor ratio “c” will determine the slope of the voltage-current load line. The resistor ratios “d” and “e” determine the offset voltage.

In an ideal case, these parameters can be calculated by:

$$c = \frac{Rs}{K_{LOAD} - Rs}$$

$$d = \frac{K_{LOAD}}{Rs} \times \frac{Vc}{V_{OFFSET}}$$

$$e = \frac{Vc}{V_{OFFSET}}$$

Where Rs is equivalent current sensing resistors.

For a 3-phase converter with inductor current sensing:

$$Rs = \frac{R_L}{3}$$

Where R_L is the DC resistance of the inductor.

In practice, the resistor ratios “c” and “d” have to be tuned in order to take some parasitic parameters such as PCB layout trace into account.

Component selection guide

The implementation circuit is shown in Fig.20, Resistor R7, R8, R9 and capacitor C15 configures a inductor current losses sensing network to sense the load current. (Attn: The C15 and R11 must connect directly to the output terminal.) The RC networks that sense the inductor current have to satisfy the following:

$$(R/3) \times C = L/R_L$$

For example, in the application circuit in Figure 20, the inductor is 1μH and the DC resistance is 1.6mΩ. If the filter capacitor C15 is chosen to be 1μF, then the current sensing resistors R7, R8 and R9 are:

$$R = 3 \times L/R_L/C$$

$$R = 3 \times 1\mu H/1.6m\Omega/1\mu F = 1.87K$$

Because the given inductor is larger at zero current (it is 1.3μH at 0 current). A large resistor has to be taken.

In the application circuit in Figure 20, R7,R8 and R9=2.2K. Select R17 (referring to R2 in Figure 22) to be 1MΩ if we consider the input bias of OPAMP LM324. Select R10 (referring to R1 in Figure 22) to be 1KΩ.

R10=1K and R17=1MΩ

Connect the voltage Vc to 2V reference voltage shown in Figure 20.

Vc=2V

Calculating R22 (referring to e × R1 in Figure 22) by the provided equation, we get

$$R22 = R17 \times Vc/V_{OFFSET} = 1K \times 2V/25mV = 80K$$

The resistor R11 and R16 (referring to c × R1 and d × R2 in Figure 22) have to be tuned. From the suggested equation, they are in a few KΩ range. Because resistor R11 and R16 function independent, they can be tuned separately. First, connect the board and make the board work first. Put no load in the output. Then replace R16 with a 5K~20K potentiometer and adjust the potentiometer so as the output voltage is about 25mV lower than the DAC output setting. Because the output current is zero, the resistor R11 will not affect the output voltage. The DC offset is only dependent on R16. Select R16 with the tuned potentiometer value.

After R16 is tuned, replace R11 with a potentiometer. Connect the output voltage to certain current load (for example, half of the nominal load, 30A). Adjust the potentiometer so that the output voltage has the same voltage drops as Intel spec requests (for example, 95mV drop comparing with zero current condition). Then select R11 with tuned potentiometer value.

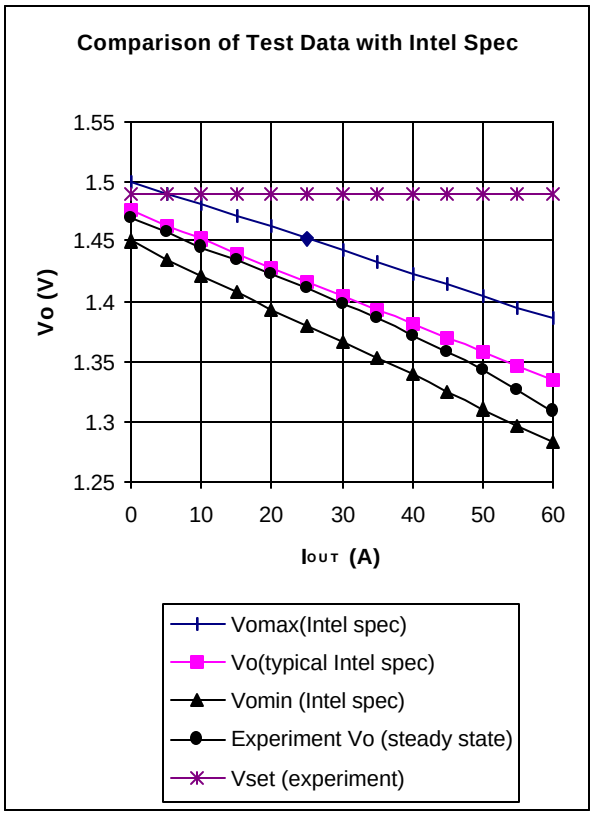


Figure 23 - Test steady state output voltage for the circuit of IRU3055 with active droop.

The test data is displayed in Figure 23. The DAC input is 01110, which refers to output voltage 1.5V. The measured DAC output V_{SET} is 1.490V. The measured output voltage versus load current falls into the Intel specification as shown in Figure 23.

In this figure, at light load, the output voltage almost follows the Intel typical specification. At 40A, 50A and 60A loads, the output voltage is a slight deviation from the typical Intel spec. The reason is because the inductors get hot at high current loads. The resistance increases comparing with low load condition. As a result, there is more voltage droop than the theoretical prediction, because the specification at high current has larger tolerance. The Intel specification can be satisfied easily with the proposed circuit.

Implement the 1.2V VID Regulator

If a Quadra-OPAMP such as LM324 is used, the additional 1.2V VID regulator as well as the power sequence can be implemented. In application circuit Figure 20, one OPAMP and a NPN transistor 2N3904 implement a 1.2V, 30mA VID voltage regulator. The VID voltage is also sent to the minus input of one OPAMP. When the VID voltage reaches 1V, the OPAMP changes to high state and starts to charge up the RC network. The Resistor R15 and the capacitor C16 function as a delay network. 40K and 0.1μF will give about 1ms delay. In the application circuit, C16=0.47μF, which gives about 5ms delay for a better illustration. When the voltage across capacitor C16 reaches 1V, the OPAMP will turn off the two NPN transistors. The soft-start capacitor of IRU3055, C10, starts to be charged up and output voltage, Vo, will smoothly go into steady state.

EXPERIMENT WAVEFORMS FOR TYPICAL APPLICATION (2)

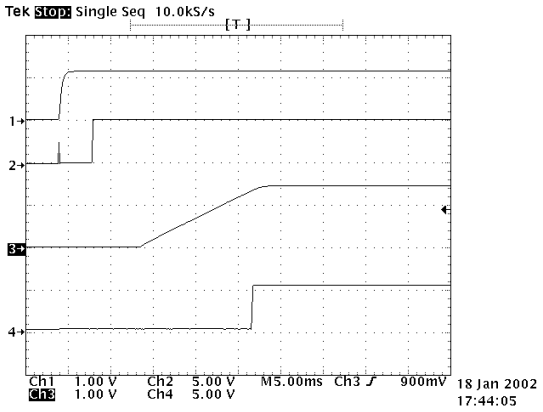


Figure 24 - Soft-start.
Ch1: 1.2V VID. Ch2: VID Good.
Ch3: 1.5V Output. Ch4: PGood.

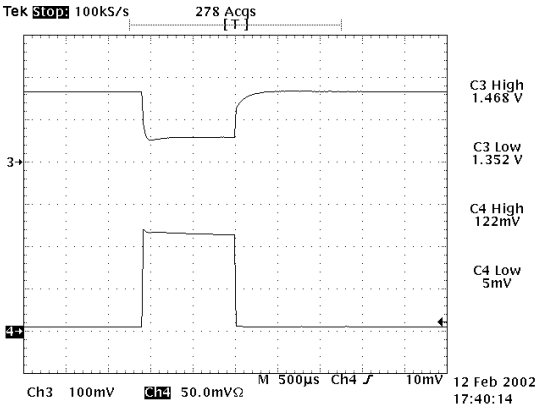


Figure 25 - 60A Load dynamic with 20A/µs slew rate.
Ch4: Output current, sensed through 2mΩ resistor, 25A/div.
Ch3: Ouput voltage, DC offset 1.3V, 100mV/div.

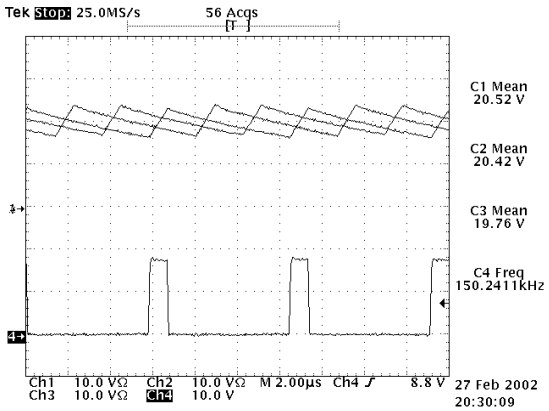


Figure 26 - 3-Phase inductor current at 60A load,
Ch1, Ch2 and Ch3: 10A/div and gate signal.

TYPICAL APPLICATION (3)

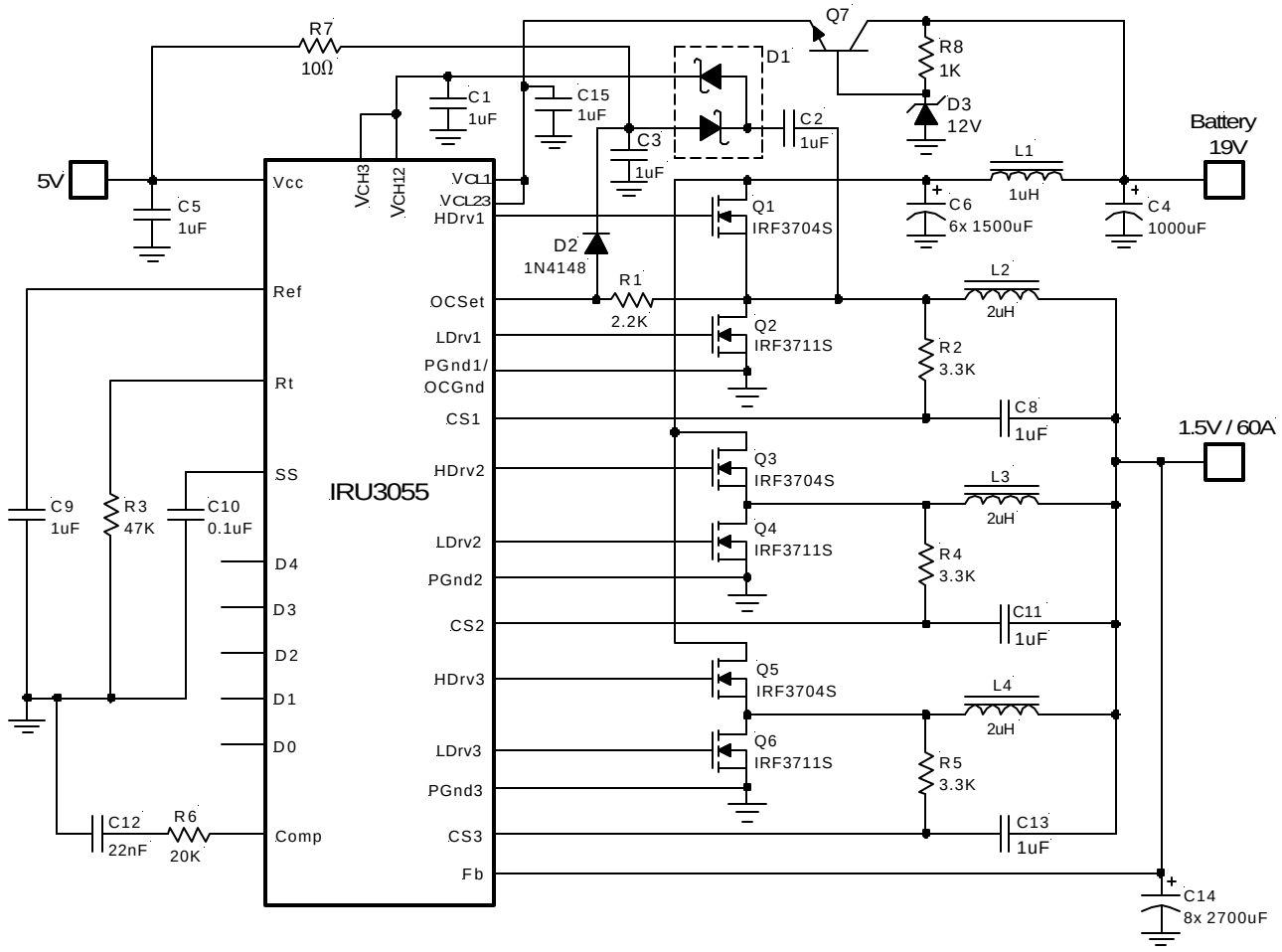


Figure 26 - Typical application of IRU3055 in notebook application.

PARTS LIST FOR TYPICAL APPLICATION (3)

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1, Q3, Q5	MOSFET	20V, 9mΩ	3	IRF3704S	IR	irf.com
Q2, Q4, Q6	MOSFET	20V, 6mΩ	3	IRF3711S	IR	
Q7	NPN Transistor		1	2N3904	Any	
U1	Controller	Synchronous PWM	1	IRU3055	IR	irf.com
D1	Schottky Diode	In Series	1	BAT54S	IR	
D2	Diode		1	1N4148	Any	
D3	Zener Diode		1	1N5242A	Any	
L1	Inductor	1.3μH	1	Z9479-A	Coilcraft	coilcraft.com
L2,L3,L4	Inductor	2μH, 15A	3	T60-18 Core, 6-turns #14 AWG wire		
C1	Cap, Ceramic	1μF, X7R, 25V	1	ECJ-3YB1E105K	Panosonic	maco.panasonic.co.jp
C2, C10	Cap, Ceramic	0.1μF, Y5V, 25V	2	ECJ-2VF1E104Z	Panosonic	
C3,5,8,9, 11,13,15	Cap, Ceramic	1μF, Y5V, 16V	7	ECJ-3VF1C105Z	Panosonic	
C4	Cap,Electrolytic	1000μF, 16V	1		Any	
C6	Cap,Electrolytic	1500μF, 16V	6	EEU-FJ1C152U	Panosonic	maco.panasonic.co.jp
C12	Cap, Ceramic	22nF, X7R, 50V	1	ECU-V1H223KBG	Panosonic	
C14	Cap,Electrolytic	2700μF,6.3V,13mΩ	8	EEU-FJ0J272U	Panosonic	
R1	Resistor	2.2K, 1%	1		Any	
R2,R4,R5	Resistor	3.3K, 1%	3		Any	
R3	Resistor	47K, 1%	1		Any	
R6	Resistor	20K, 1%	1		Any	
R7	Resistor	10Ω, 5%	1		Any	

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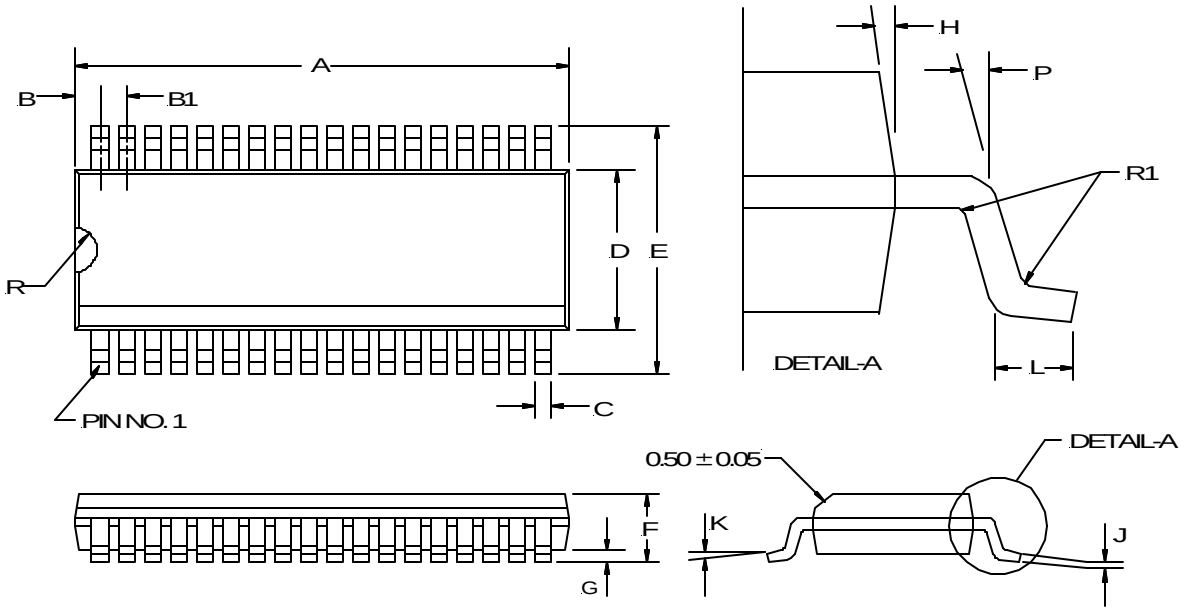
(Q) QSOP Package, Wide Body
36-Pin

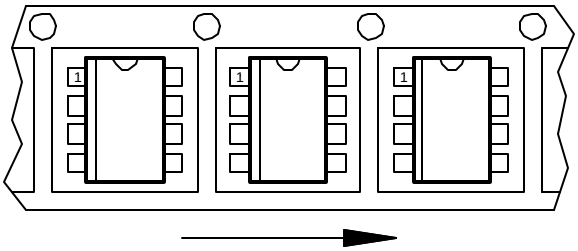


36-PIN		
SYMBOL	**MIN**	**MAX**
A	15.20	15.40
B	0.85	
B1	0.80 REF	
C	0.28	0.51
D	7.40	7.60
E	10.11	10.51
F	2.44	2.64
G	0.10	0.30
H	7° TYP	
J	0.23	0.32
K	0°	8°
L	0.40	1.27
R	0.63	0.89
R1	0.20 ± 0.05	
P	7° ± 3°	

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
Q	QSOP Plastic, Wide Body	36	---	1500	Fig A



Feed Direction
Figure A

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