

Precision Single and Dual Low Noise Operational Amplifiers

ISL28107, ISL28207

The ISL28107 and ISL28207 are single and dual amplifiers featuring low noise, low input bias current, and low offset and temperature drift. This makes them the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of precision, low noise, and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision active filters, medical and analytical instrumentation, precision power supply controls, and industrial controls.

The ISL28107 single is available in an 8 Ld SOIC package. The ISL28207 dual amplifier will be offered in an 8 Ld SOIC package. All devices are offered in standard pin configurations and operate over the extended temperature range to -40°C to $+125^{\circ}\text{C}$.

Applications* (see page 21)

- Precision Instruments
- Medical Instrumentation
- Spectral Analysis Equipment
- Geophysical Analysis Equipment
- Active Filter Blocks
- Microphone Pre-amplifier
- Thermocouples and RTD Reference Buffers
- Data Acquisition
- Power Supply Control

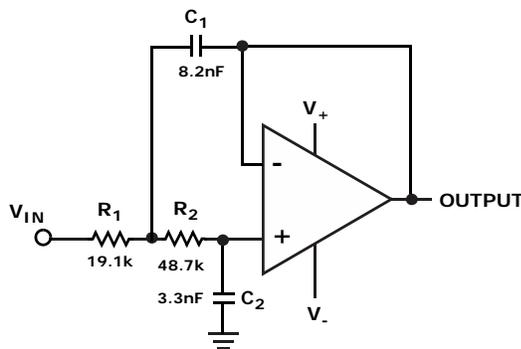
Features

- Low Input Offset $75\mu\text{V}$, Max.
- Input Bias Current 60pA
- Superb Temperature Drift
 - Voltage Offset $0.65\mu\text{V}/^{\circ}\text{C}$, Max.
 - Input Current $0.9\text{pA}/^{\circ}\text{C}$, Max
- Outstanding ESD performance
 - Human Body Model 4.5kV
 - Machine Model 500V
 - Charged Device Model 1.5kV
- Very Low Voltage Noise, 10Hz $14\text{nV}/\sqrt{\text{Hz}}$
- Low Current Consumption (per amp) . 0.29mA , Max.
- Gain-bandwidth Product 1MHz
- Wide Supply Range. 4.5V to 40V
- Operating Temperature Range . . . -40°C to $+125^{\circ}\text{C}$
- No Phase Reversal
- Pb-Free (RoHS Compliant)

Related Literature* (see page 21)

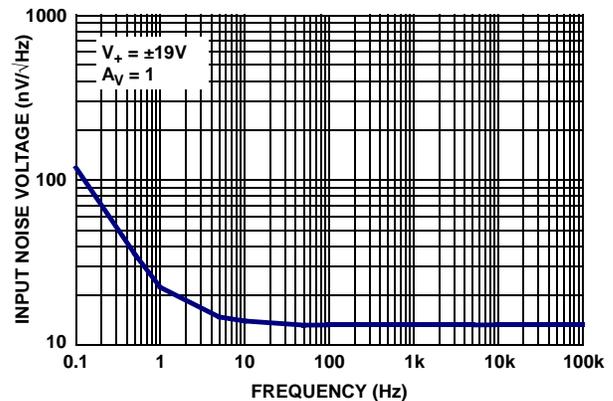
- See [AN1508](#) "ISL281X7SOICEVAL1Z Evaluation Board User's Guide"
- See [AN1509](#) "ISL282X7SOICEVAL2Z Evaluation Board User's Guide"

Typical Application



Sallen-Key Low Pass Filter (1kHz)

Input Noise Voltage Spectral Density



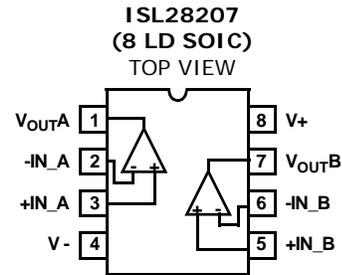
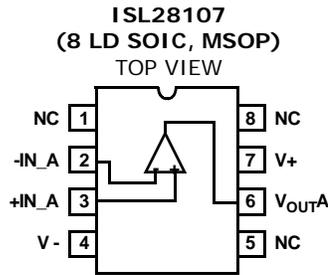
Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28107FBZ	28107 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28107FBZ-T7 (Note 1)	28107 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28107FBZ-T13 (Note 1)	28107 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28107FUZ	8107Z	-40 to +125	8 Ld MSOP	M8.118
ISL28107FUZ-T13 (Note 1)	8107Z	-40 to +125	8 Ld MSOP	M8.118
ISL28207FBZ	28207 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28207FBZ-T7 (Note 1)	28207 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28207FBZ-13 (Note 1)	28207 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28107SOICEVAL1Z	Evaluation Board			
ISL28207SOICEVAL2Z	Evaluation Board			

NOTES:

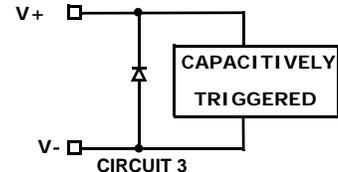
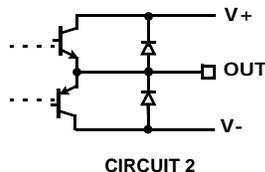
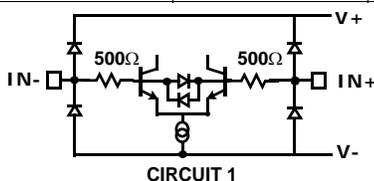
1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL28107](#) and [ISL28207](#). For more information on MSL please see techbrief [TB363](#).

Pin Configurations



Pin Descriptions

ISL28107 (8 LD SOIC, MSOP)	ISL28207 (8 LD SOIC)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	3	+IN_A	Circuit 1	Amplifier A non-inverting input
4	4	V-	Circuit 3	Negative power supply
	5	+IN_B	Circuit 1	Amplifier B non-inverting input
	6	-IN_B	Circuit 1	Amplifier B inverting input
	7	V_OUTB	Circuit 2	Amplifier B output
7	8	V+	Circuit 3	Positive power supply
6	1	V_OUTA	Circuit 2	Amplifier A output
2	2	-IN_A	Circuit 1	Amplifier A inverting input
1, 5, 8		NC	-	No internal connection



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Absolute Maximum Ratings

Maximum Supply Voltage	42V
Maximum Differential Input Current	20mA
Maximum Differential Input Voltage (V-) - 0.5V to (V+) + 0.5V	
Min/Max Input Voltage (V-) - 0.5V to (V+) + 0.5V	
Max/Min Input current for input voltage >V+ or <V- . ±20mA	
Output Short-Circuit Duration (1 output at a time)	Indefinite
ESD Tolerance	
Human Body Model	4.5kV
Machine Model	500V
Charged Device Model	1.5kV

Thermal Information

Thermal Resistance (Typical, Notes 4, 5) θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC (ISL28107)	120
8 Ld SOIC (ISL28207)	105
8 Ld MSOP (ISL28107)	155
Storage Temperature Range	-65°C to +150°C
Pb-Free Reflow Profile	see link below
	http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Operating Temperature Range	-40°C to +125°C
Maximum Operating Junction Temperature	+150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- For θ_{JC} , the "case temp" location is taken at the package top center.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_S \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ\text{C}$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OS}	Offset Voltage Magnitude; SOIC Package	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-75	5	75	μV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-140		140	μV
	Offset Voltage Magnitude; MSOP Package	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-100	5	100	μV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-180		180	μV
TCV_{OS}	Offset Voltage Drift; SOIC Package		-0.65	0.1	0.65	$\mu\text{V}/^\circ\text{C}$
	Offset Voltage Drift; MSOP Package		-0.85	0.1	0.85	$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-300	15	300	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-600		600	pA
TCI_B	Input Bias Current Drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-0.9	0.19	0.9	$\text{pA}/^\circ\text{C}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-3.5	0.26	3.5	$\text{pA}/^\circ\text{C}$
I_{OS}	Input Offset Current	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-300	15	300	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-600		600	pA
TCI_{OS}	Input Offset Current Drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-0.9	0.19	0.9	$\text{pA}/^\circ\text{C}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-3.5	0.26	3.5	$\text{pA}/^\circ\text{C}$
V_{CM}	Input Voltage Range	Guaranteed by CMRR test	-13		13	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -13\text{V}$ to $+13\text{V}$	115	145		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.25\text{V}$ to $\pm 20\text{V}$	115	145		dB
A_{VOL}	Open-Loop Gain	$V_O = -13\text{V}$ to $+13\text{V}$, $R_L = 10\text{k}\Omega$ to ground	3,000	40,000		V/mV

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Electrical Specifications $V_S \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ\text{C}$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to $+125^\circ\text{C}$. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OH}	Output Voltage High	$R_L = 10k\Omega$ to ground	13.5	13.7		V
			13.2			V
		$R_L = 2k\Omega$ to ground	13.3	13.55		V
			13.1			V
V_{OL}	Output Voltage Low	$R_L = 10k\Omega$ to ground		-13.7	-13.5	V
				-	-13.2	V
		$R_L = 2k\Omega$ to ground		-13.55	-13.3	V
				-	-13.1	V
I_S	Supply Current/Amplifier	$R_L = \text{Open}$		0.21	0.29	mA
					0.35	mA
I_{SC}	Output Short-Circuit Current	(Note 7)		± 40		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	± 2.25		± 20	V
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product			1		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz, $V_S = \pm 19V$		340		nV _{P-P}
e_n	Voltage Noise Density	$f = 10\text{Hz}$, $V_S = \pm 19V$		14		nV/ $\sqrt{\text{Hz}}$
e_n	Voltage Noise Density	$f = 100\text{Hz}$, $V_S = \pm 19V$		13		nV/ $\sqrt{\text{Hz}}$
e_n	Voltage Noise Density	$f = 1\text{kHz}$, $V_S = \pm 19V$		13		nV/ $\sqrt{\text{Hz}}$
e_n	Voltage Noise Density	$f = 10\text{kHz}$, $V_S = \pm 19V$		13		nV/ $\sqrt{\text{Hz}}$
i_n	Current Noise Density	$f = 10\text{kHz}$, $V_S = \pm 19V$		53		fA/ $\sqrt{\text{Hz}}$
THD + N	Total Harmonic Distortion + Noise	1kHz, $G = 1$, $V_O = 3.5V_{RMS}$, $R_L = 2k\Omega$		0.0035		%
TRANSIENT RESPONSE						
SR	Slew Rate	$A_V = 10$, $R_L = 10k\Omega$, $V_O = 10V_{P-P}$		± 0.32		V/ μs
t_r , t_f , Small Signal	Rise Time 10% to 90% of V_{OUT}	$A_V = 1$, $V_{OUT} = 100mV_{P-P}$, $R_f = 0\Omega$, $R_L = 2k\Omega$ to V_{CM}		355		ns
	Fall Time 90% to 10% of V_{OUT}	$A_V = 1$, $V_{OUT} = 100mV_{P-P}$, $R_f = 0\Omega$, $R_L = 2k\Omega$ to V_{CM}		365		ns
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 10V_{P-P}$, $R_g = R_f = 10k$, $R_L = 2k\Omega$ to V_{CM}		29		μs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 10V_{P-P}$, $R_g = R_f = 10k$, $R_L = 2k\Omega$ to V_{CM}		31.2		μs
t_{OL}	Output Overload Recovery Time	$A_V = 100$, $V_{IN} = 0.2V$, $R_L = 2k\Omega$ to V_{CM}		6		μs

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Electrical Specifications $V_S \pm 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+125^\circ C$. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OS}	Offset Voltage Magnitude; SOIC Package	$T_A = -40^\circ C$ to $+85^\circ C$	-75	5	75	μV
		$T_A = -40^\circ C$ to $+125^\circ C$	-140		140	μV
	Offset Voltage Magnitude; MSOP Package	$T_A = -40^\circ C$ to $+85^\circ C$	-100	5	100	μV
		$T_A = -40^\circ C$ to $+125^\circ C$	-180		180	μV
TCV_{OS}	Offset Voltage Drift; SOIC Package		-0.65	0.1	0.65	$\mu V/^\circ C$
	Offset Voltage Drift; MSOP Package		-0.85	0.1	0.85	$\mu V/^\circ C$
I_B	Input Bias Current	$T_A = -40^\circ C$ to $+85^\circ C$	-300	15	300	pA
		$T_A = -40^\circ C$ to $+125^\circ C$	-600		600	pA
TCI_B	Input Bias Current Drift	$T_A = -40^\circ C$ to $+85^\circ C$	-0.9	0.19	0.9	pA/°C
		$T_A = -40^\circ C$ to $+125^\circ C$	-3.5	0.26	3.5	pA/°C
I_{OS}	Input Offset Current	$T_A = -40^\circ C$ to $+85^\circ C$	-300	15	300	pA
		$T_A = -40^\circ C$ to $+125^\circ C$	-600		600	pA
TCI_{OS}	Input Offset Current Drift	$T_A = -40^\circ C$ to $+85^\circ C$	-0.9	0.19	0.9	pA/°C
		$T_A = -40^\circ C$ to $+125^\circ C$	-3.5	0.26	3.5	pA/°C
V_{CM}	Common Mode Input Voltage Range	Guaranteed by CMRR test	-3		3	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -3V$ to $+3V$	115	145		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.25V$ to $\pm 5V$	115	145		dB
A_{VOL}	Open-Loop Gain	$V_O = -3V$ to $+3V$, $R_L = 10k\Omega$ to ground	3,000	40,000		V/mV
V_{OH}	Output Voltage High	$R_L = 10k\Omega$ to ground	3.5	3.7		V
			3.2			V
		$R_L = 2k\Omega$ to ground	3.3	3.55		V
			3.1			V
V_{OL}	Output Voltage Low	$R_L = 10k\Omega$ to ground		-3.7	-3.5	V
					-3.2	V
		$R_L = 2k\Omega$ to ground		-3.55	-3.3	V
					-3.1	V
I_S	Supply Current/Amplifier	$R_L = \text{Open}$		0.21	0.29	mA
					0.35	mA
I_{SC}	Output Short-Circuit Current	(Note 7)		± 40		mA
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product			1		MHz
THD + N	Total Harmonic Distortion + Noise	1kHz, $G = 1$, $V_O = 2.5V_{RMS}$, $R_L = 2k\Omega$		0.0053		%
TRANSIENT RESPONSE						
SR	Slew Rate	$A_V = 10$, $R_L = 2k\Omega$		0.32		V/ μs

Electrical Specifications $V_S = \pm 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ C$, unless otherwise noted. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+125^\circ C$. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
t_r , t_f , Small Signal	Rise Time 10% to 90% of V_{OUT}	$A_V = 1$, $V_{OUT} = 100mV_{P-P}$, $R_f = 0\Omega$, $R_L = 2k\Omega$ to V_{CM}		355		ns
	Fall Time 90% to 10% of V_{OUT}	$A_V = 1$, $V_{OUT} = 100mV_{P-P}$, $R_f = 0\Omega$, $R_L = 2k\Omega$ to V_{CM}		370		ns
t_s	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_f = R_g = 2k\Omega$, $R_L = 2k\Omega$ to V_{CM}		12.4		μs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_f = R_g = 2k\Omega$, $R_L = 2k\Omega$ to V_{CM}		22		μs

NOTES:

- Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Output Short Circuit Current is the minimum current (source or sink) when the output is driven into the supply rails with $R_L = 0\Omega$ to ground.

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ C$ unless otherwise specified.

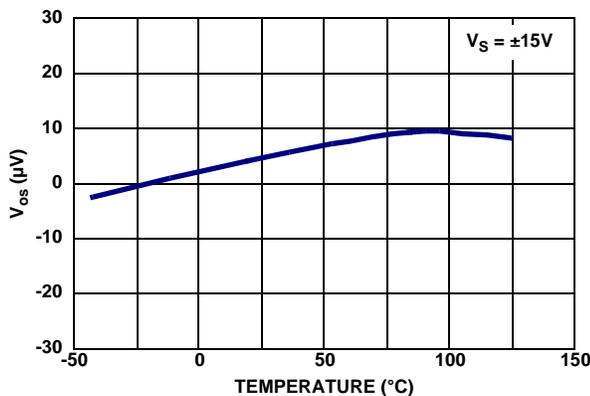


FIGURE 1. INPUT OFFSET VOLTAGE vs TEMPERATURE, $V_S = \pm 15V$

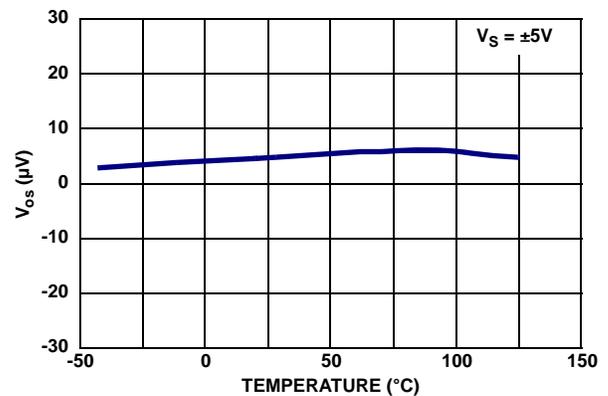


FIGURE 2. INPUT OFFSET VOLTAGE vs TEMPERATURE, $V_S = \pm 5V$

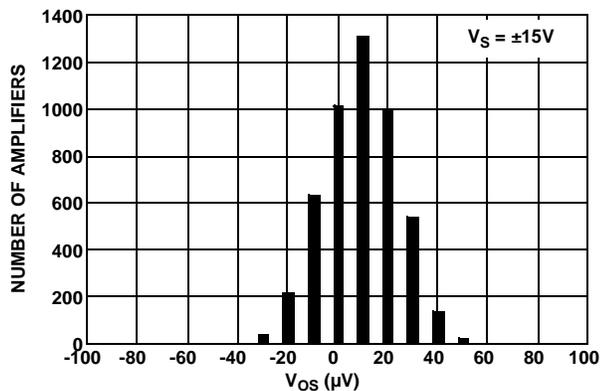


FIGURE 3. INPUT OFFSET VOLTAGE DISTRIBUTION, $V_S = \pm 15V$

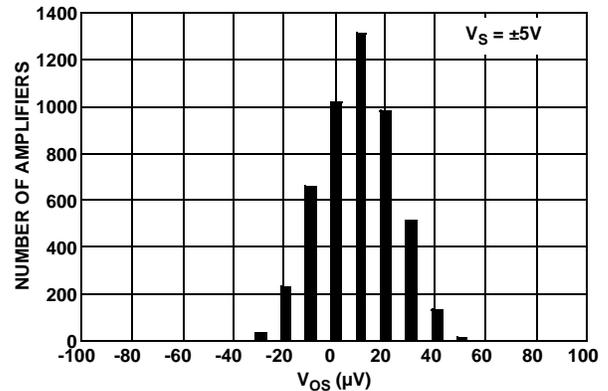


FIGURE 4. INPUT OFFSET VOLTAGE DISTRIBUTION, $V_S = \pm 5V$

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ C$ unless otherwise specified. (Continued)

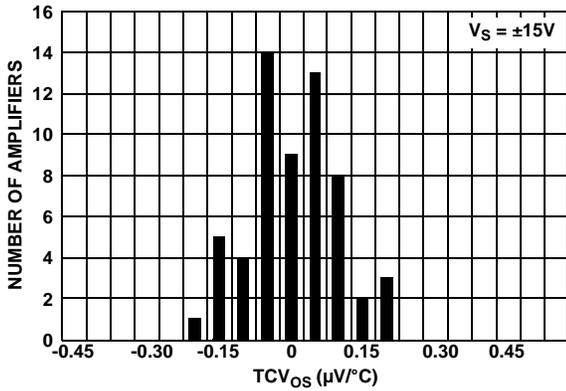


FIGURE 5. TCV_{OS} vs NUMBER OF AMPLIFIERS, $V_S = \pm 15V$

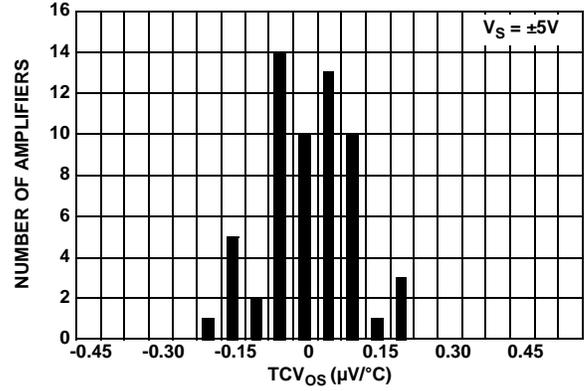


FIGURE 6. TCV_{OS} vs NUMBER OF AMPLIFIERS, $V_S = \pm 5V$

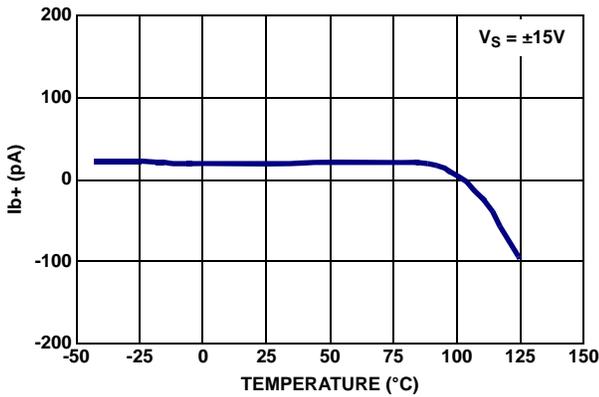


FIGURE 7. POSITIVE BIAS CURRENT vs TEMPERATURE, $V_S = \pm 15V$

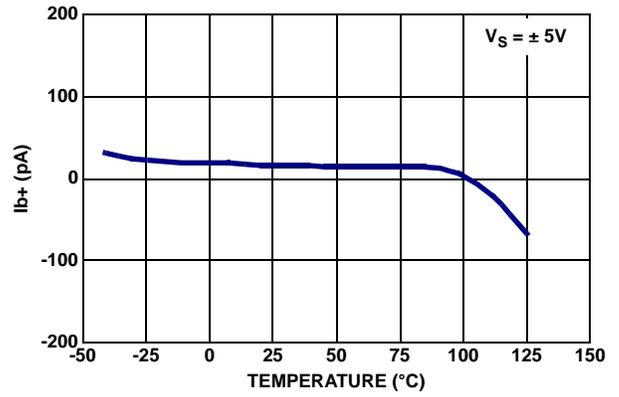


FIGURE 8. POSITIVE BIAS CURRENT vs TEMPERATURE, $V_S = \pm 5V$

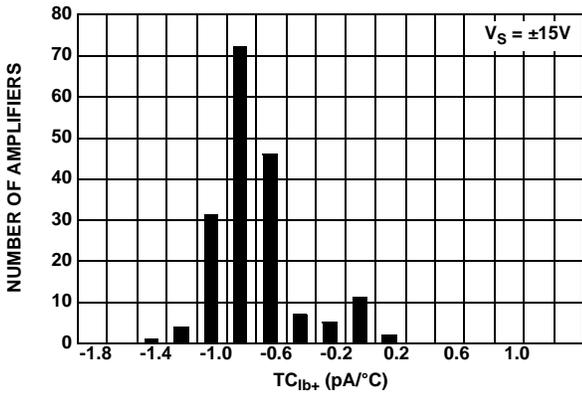


FIGURE 9. TC_{Ib+} vs NUMBER OF AMPLIFIERS, $V_S = \pm 15V$

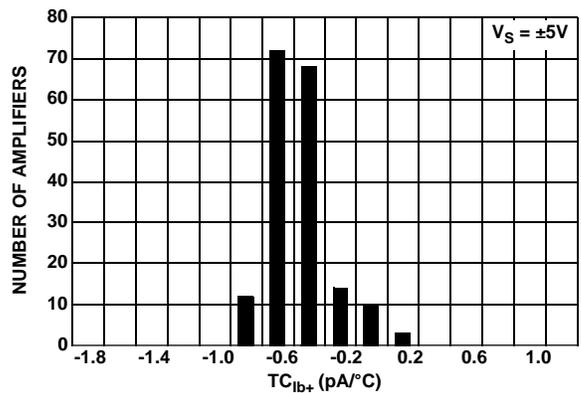


FIGURE 10. TC_{Ib+} vs NUMBER OF AMPLIFIERS, $V_S = \pm 5V$

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ C$ unless otherwise specified. (Continued)

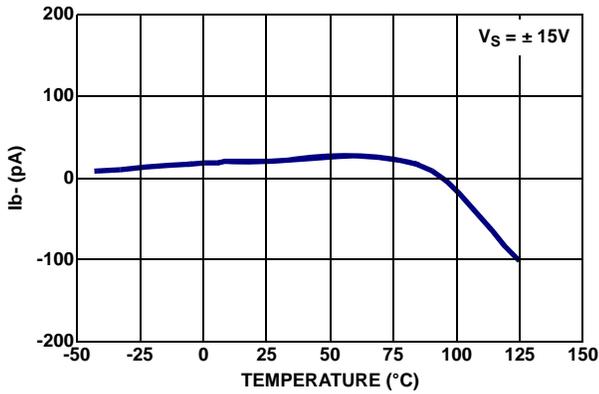


FIGURE 11. NEGATIVE BIAS CURRENT vs TEMPERATURE, $V_S = \pm 15V$

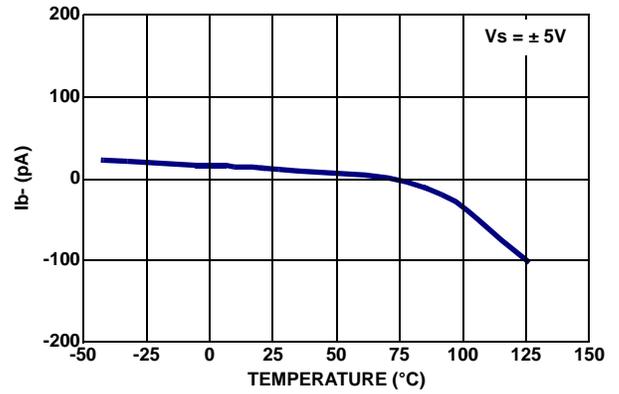


FIGURE 12. NEGATIVE BIAS CURRENT vs TEMPERATURE, $V_S = \pm 5V$

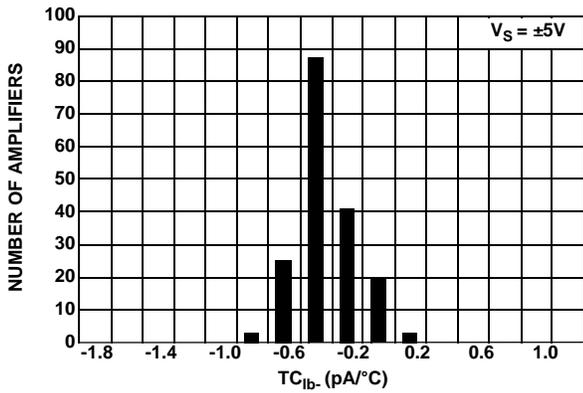


FIGURE 13. TC_{Ib-} vs NUMBER OF AMPLIFIERS, $V_S = \pm 5V$

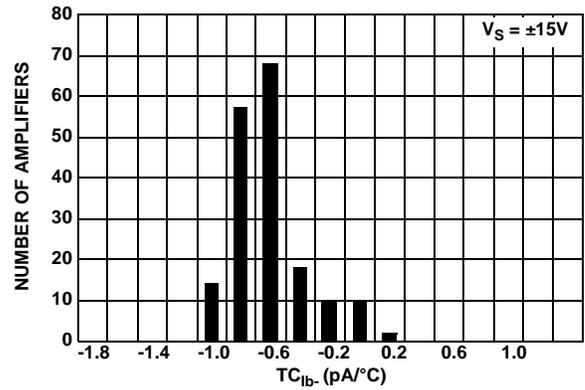


FIGURE 14. TC_{Ib-} vs NUMBER OF AMPLIFIERS, $V_S = \pm 15V$

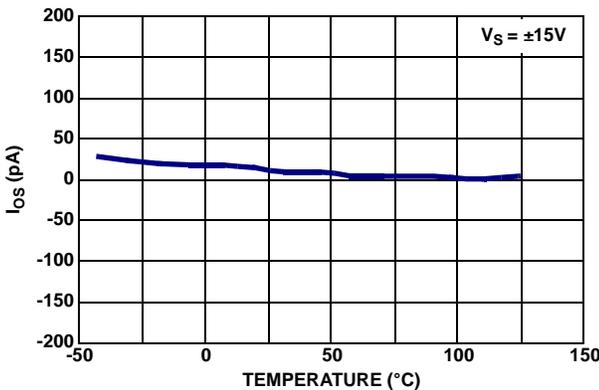


FIGURE 15. OFFSET CURRENT vs TEMPERATURE, $V_S = \pm 15V$

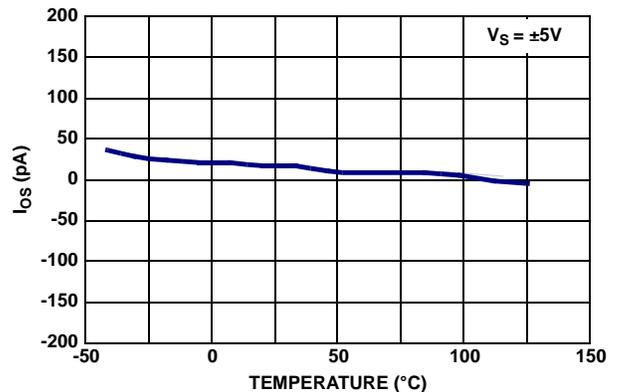


FIGURE 16. OFFSET CURRENT vs TEMPERATURE, $V_S = \pm 5V$

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ C$ unless otherwise specified. (Continued)

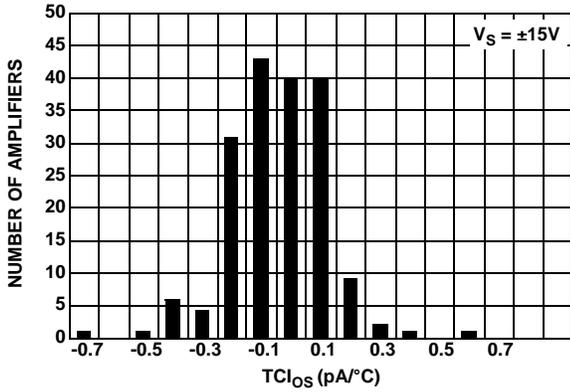


FIGURE 17. TCI_{OS-} vs NUMBER OF AMPLIFIERS, $V_S = \pm 15V$

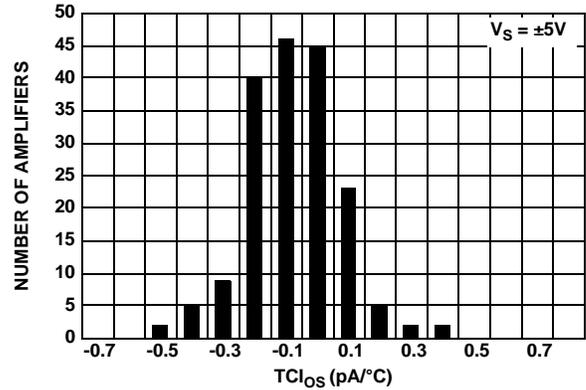


FIGURE 18. TCI_{OS-} vs NUMBER OF AMPLIFIERS, $V_S = \pm 5V$

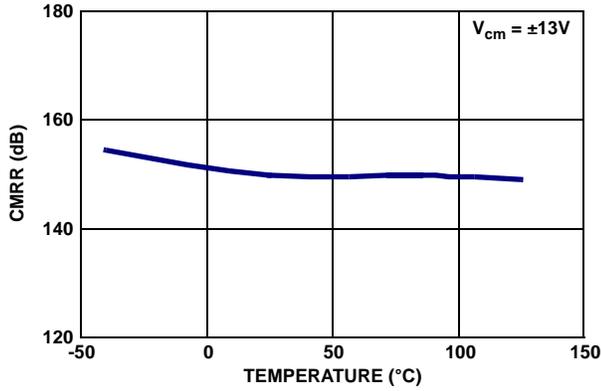


FIGURE 19. CMRR vs TEMPERATURE

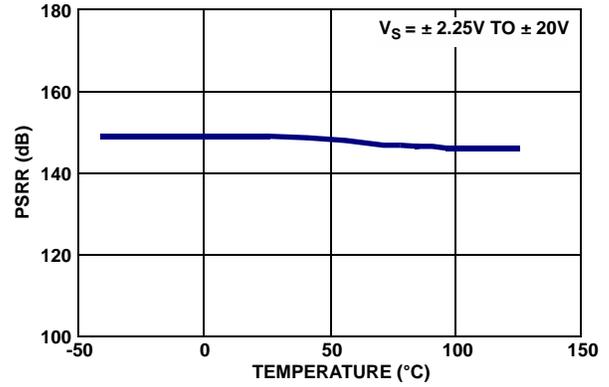


FIGURE 20. PSRR vs TEMPERATURE

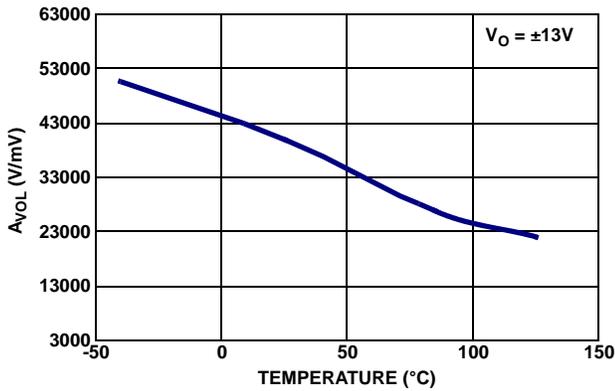


FIGURE 21. A_{VOL} vs TEMPERATURE

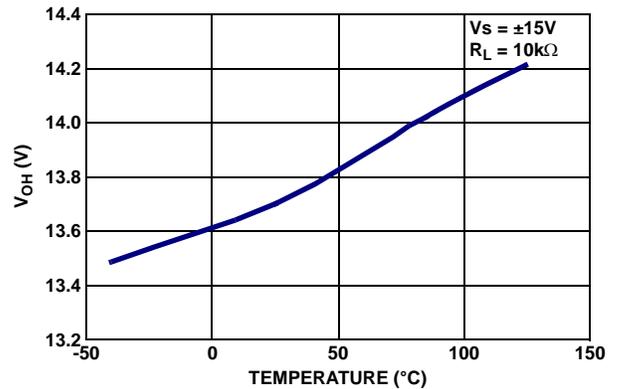


FIGURE 22. V_{OH} vs TEMPERATURE, $V_S = \pm 15V$, $R_L = 10k\Omega$

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ C$ unless otherwise specified. (Continued)

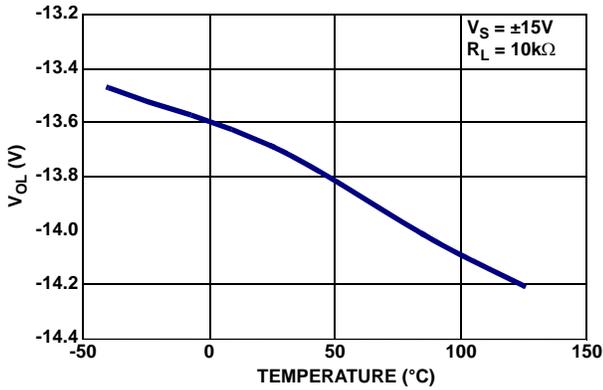


FIGURE 23. V_{OL} vs TEMPERATURE, $V_S = \pm 15V$, $R_L = 10k\Omega$

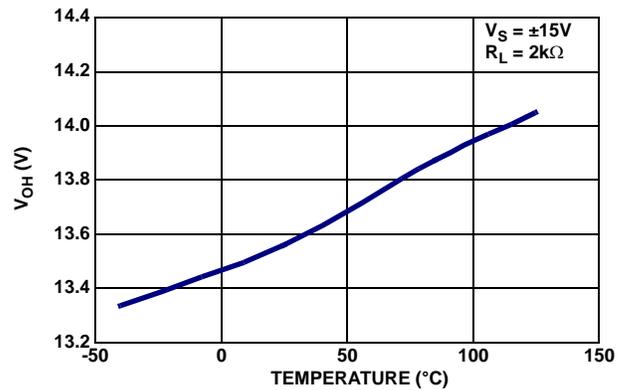


FIGURE 24. V_{OH} vs TEMPERATURE, $V_S = \pm 15V$, $R_L = 2k\Omega$

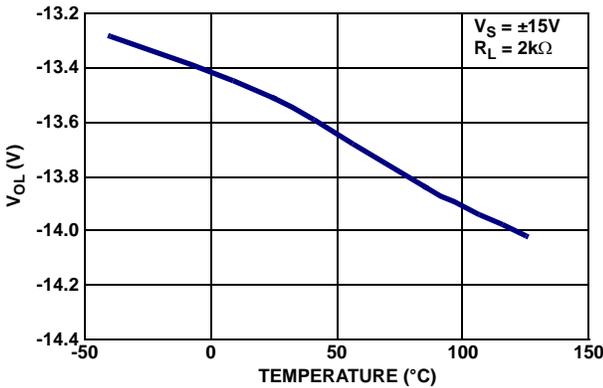


FIGURE 25. V_{OL} vs TEMPERATURE, $V_S = \pm 15V$, $R_L = 2k\Omega$

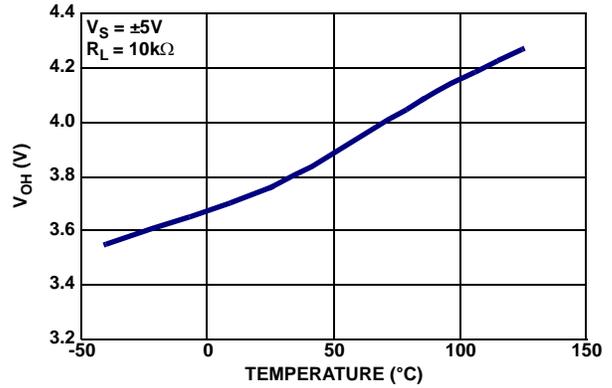


FIGURE 26. V_{OH} vs TEMPERATURE, $V_S = \pm 5V$, $R_L = 10k\Omega$

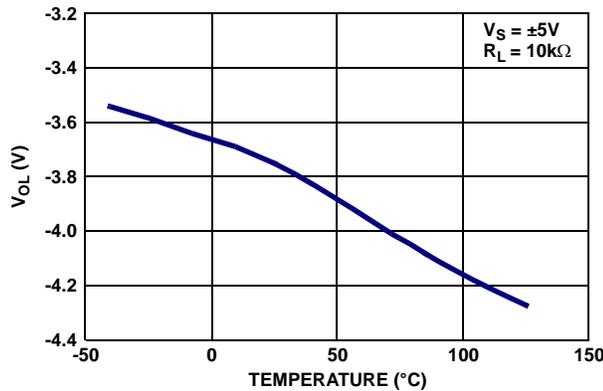


FIGURE 27. V_{OL} vs TEMPERATURE, $V_S = \pm 5V$, $R_L = 10k\Omega$

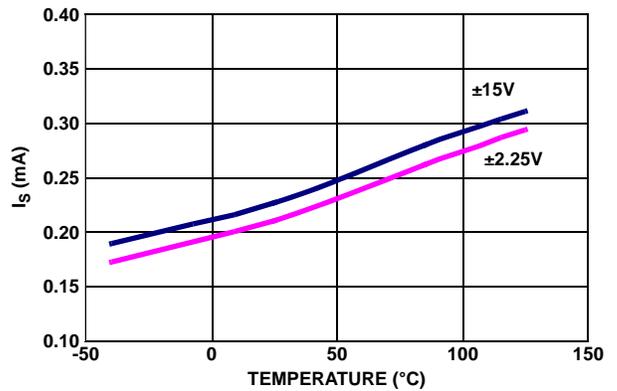


FIGURE 28. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ C$ unless otherwise specified. (Continued)

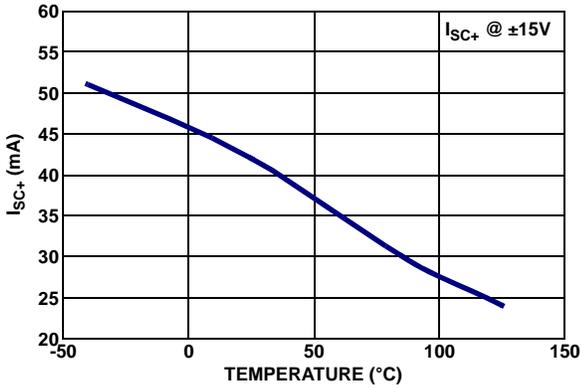


FIGURE 29. POSITIVE SHORT CIRCUIT CURRENT vs TEMPERATURE

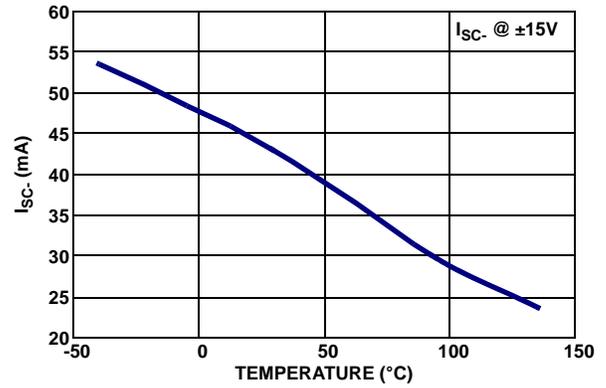


FIGURE 30. NEGATIVE SHORT CIRCUIT CURRENT vs TEMPERATURE

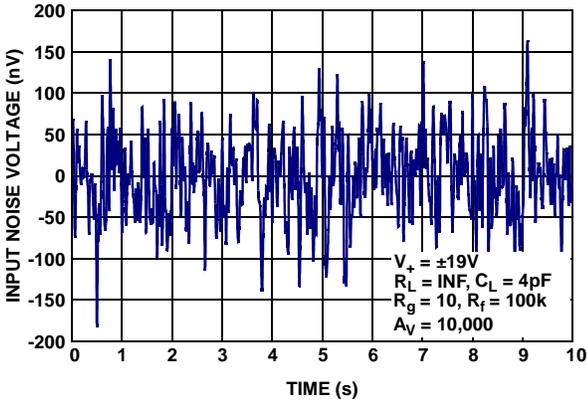


FIGURE 31. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz

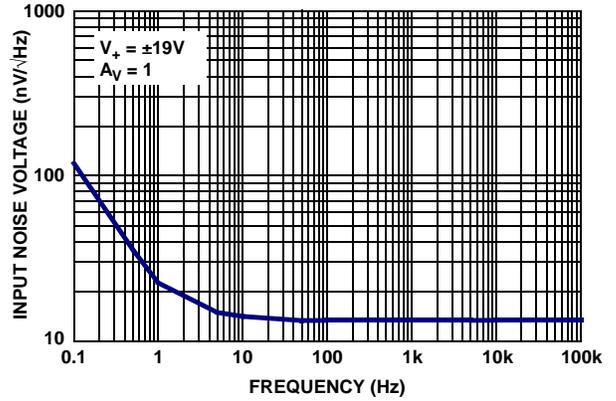


FIGURE 32. INPUT NOISE VOLTAGE SPECTRAL DENSITY

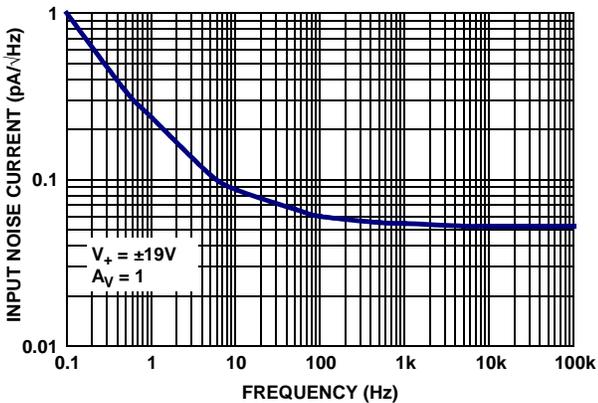


FIGURE 33. INPUT NOISE CURRENT SPECTRAL DENSITY

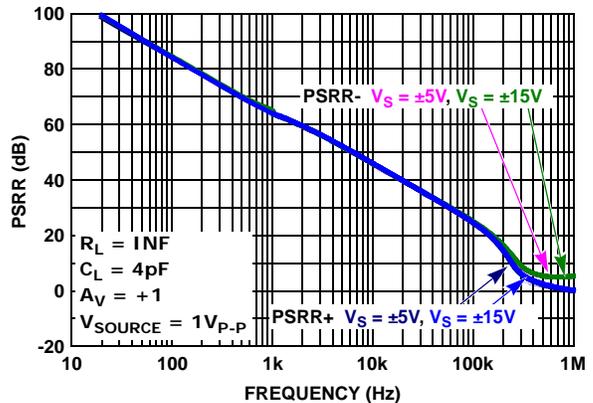


FIGURE 34. PSRR vs FREQUENCY, $V_S = \pm 5V, \pm 15V$

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ C$ unless otherwise specified. (Continued)

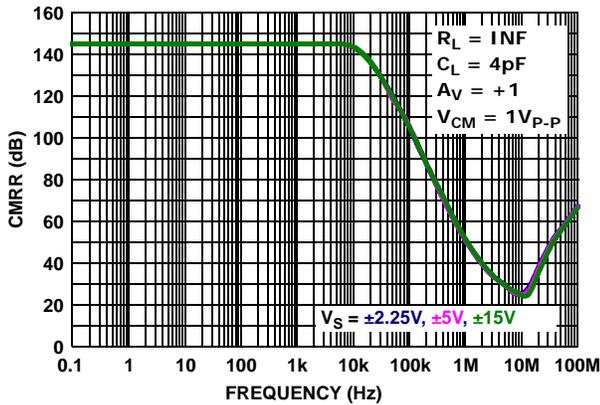


FIGURE 35. CMRR vs FREQUENCY, $V_S = \pm 2.25, \pm 5V, \pm 15V$

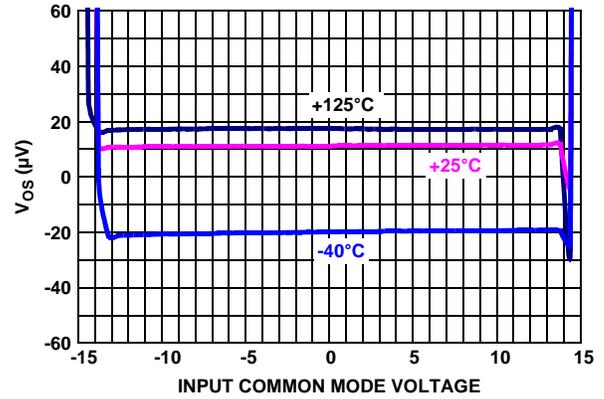


FIGURE 36. INPUT OFFSET VOLTAGE vs INPUT COMMON MODE VOLTAGE, $V_S = \pm 15V$

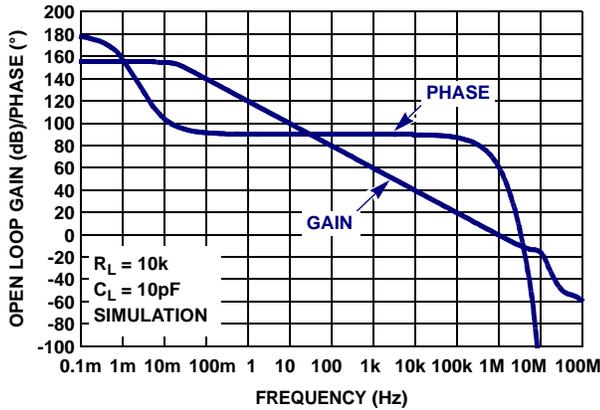


FIGURE 37. OPEN-LOOP GAIN, PHASE vs FREQUENCY, $R_L = 10k\Omega$, $C_L = 10pF$

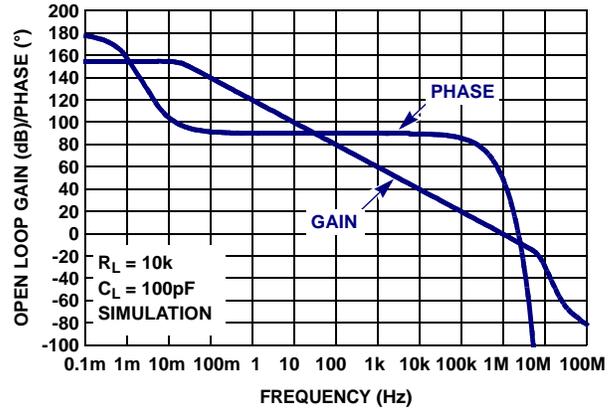


FIGURE 38. OPEN-LOOP GAIN, PHASE vs FREQUENCY, $R_L = 10k\Omega$, $C_L = 100pF$

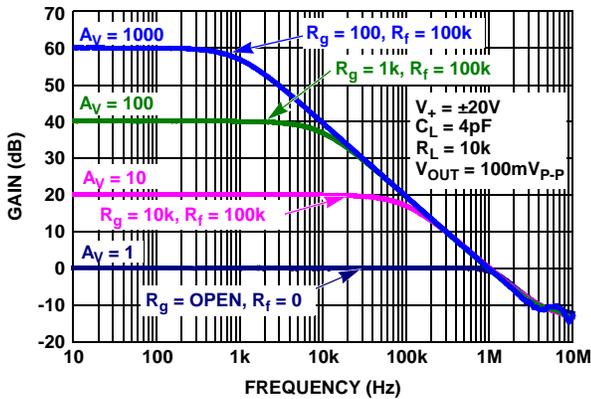


FIGURE 39. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

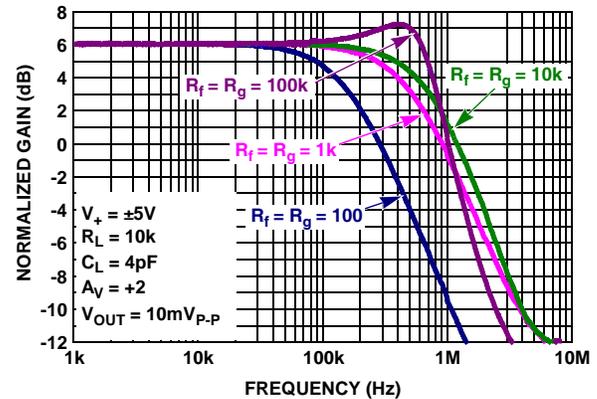


FIGURE 40. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE R_f/R_g

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ C$ unless otherwise specified. (Continued)

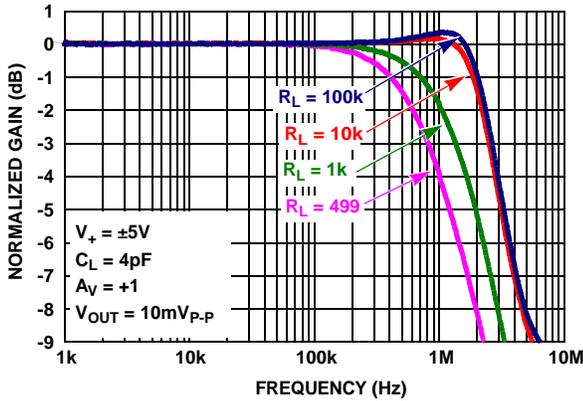


FIGURE 41. GAIN vs FREQUENCY vs R_L

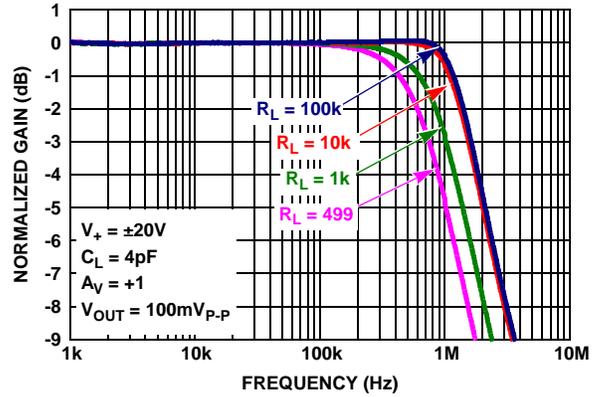


FIGURE 42. GAIN vs FREQUENCY vs R_L

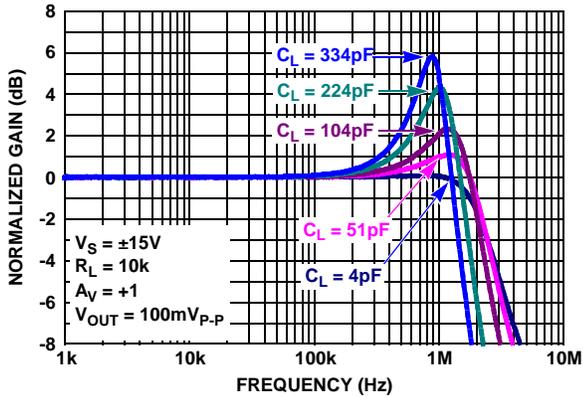


FIGURE 43. GAIN vs FREQUENCY vs C_L

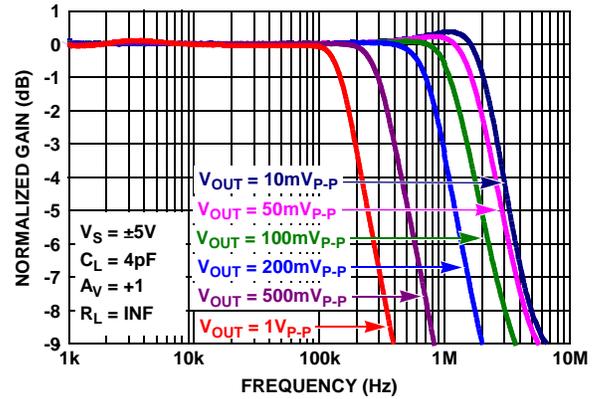


FIGURE 44. GAIN vs FREQUENCY vs OUTPUT VOLTAGE

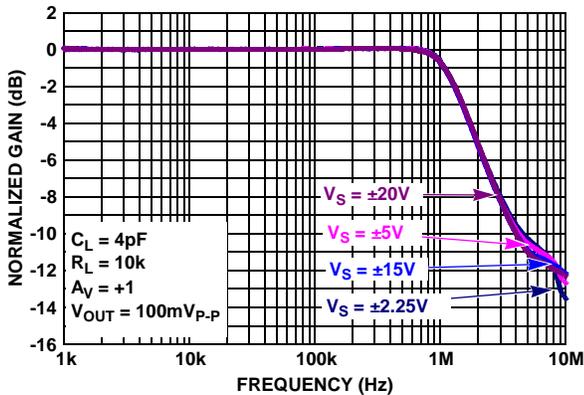


FIGURE 45. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

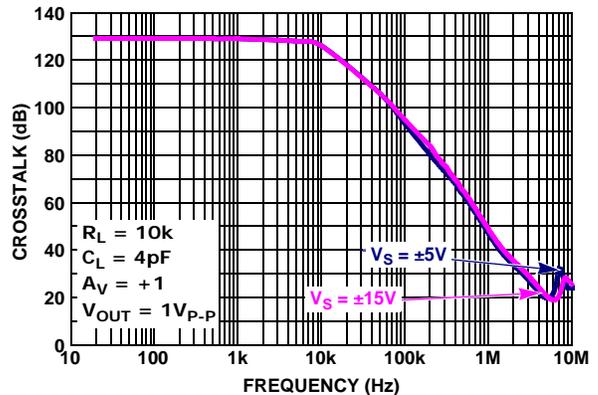


FIGURE 46. CROSSTALK vs FREQUENCY, $V_S = \pm 5V$, $\pm 15V$

Typical Performance Curves

$V_S = \pm 15V$, $V_{CM} = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ C$ unless otherwise specified. (Continued)

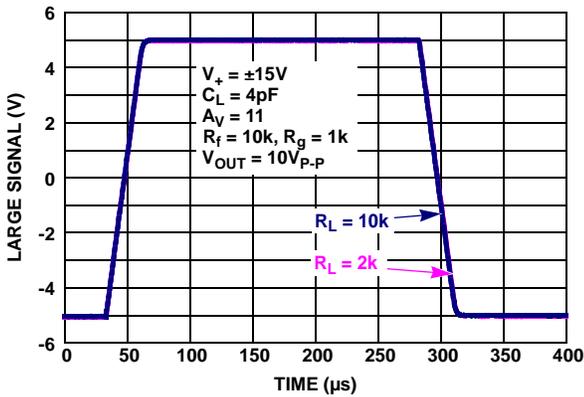


FIGURE 47. LARGE SIGNAL 10V STEP RESPONSE, $V_S = \pm 15V$

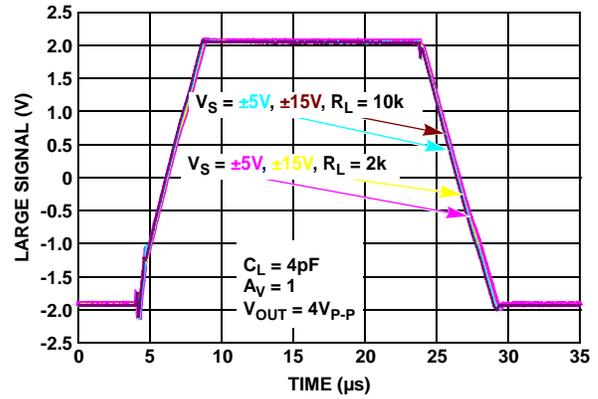


FIGURE 48. LARGE SIGNAL TRANSIENT RESPONSE vs R_L $V_S = \pm 5V, \pm 15V$

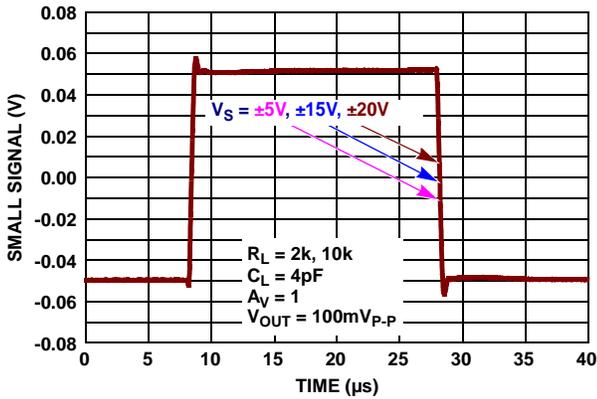


FIGURE 49. SMALL SIGNAL TRANSIENT RESPONSE $V_S = \pm 5V, \pm 15V, \pm 20V$

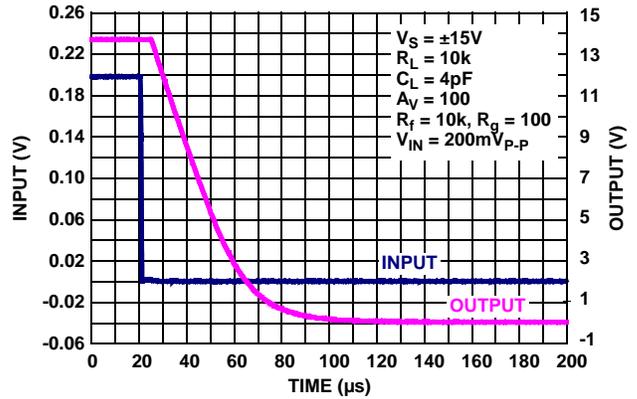


FIGURE 50. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S = \pm 15V$

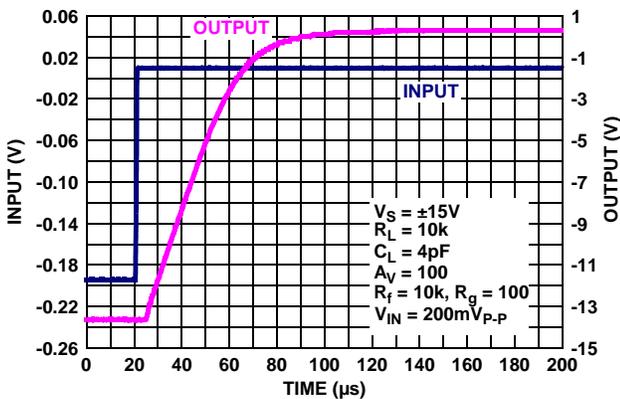


FIGURE 51. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S = \pm 15V$

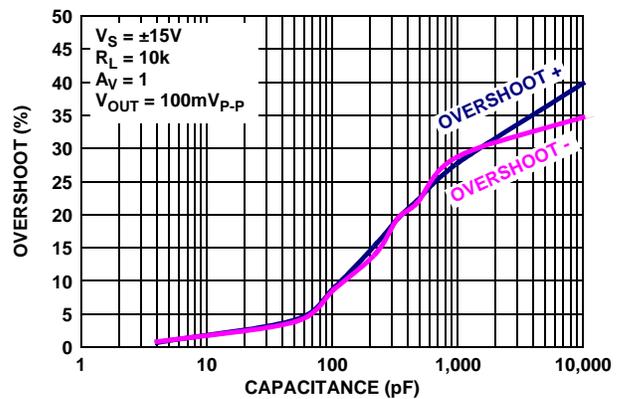


FIGURE 52. % OVERSHOOT vs LOAD CAPACITANCE, $V_S = \pm 15V$

Applications Information

Functional Description

The ISL28107 and ISL28207 are single and dual, very low 1/f noise (14nV/√Hz @ 10Hz) precision op-amps. These amplifiers feature very high open loop gain (50kV/mV) for excellent CMRR (145dB), and gain accuracy. Both devices are fabricated in a new precision 40V complementary bipolar DI process.

The super-beta NPN input stage with bias current cancellation provides bipolar-like levels of AC performance with the low input bias currents approaching JFET levels. The temperature stabilization provided by bias current cancellation removes the high input bias current temperature coefficient commonly found in JFET amplifiers. Figures 7 and 8 show the input bias current variation over temperature.

The input offset voltage (V_{OS}) has an very low, worst case value of 75μV max at +25°C and a maximum T_C of 0.65μV/°C. Figure 36 shows V_{OS} as a function of supply voltage and temperature with the common mode voltage at 0V for split supply operation.

The complimentary bipolar output stage maintains stability driving large capacitive loads (to 10nF) without external compensation. The small signal overshoot vs. load capacitance is shown in Figure 52.

Operating Voltage Range

The devices are designed to operate over the 4.5V (±2.25V) to 40V (±20V) range and are fully characterized at 10V (±5V) and 30V (±15V). Both DC and AC performance remain virtually unchanged over the complete 4.5V to 40V operating voltage range. Parameter variation with operating voltage is shown in the "Typical Performance Curves" beginning on page 6. The input common mode voltage range sensitivity to temperature is shown in Figure 36 (±15V).

Input ESD Diode Protection

The input terminals (IN+ and IN-) each have internal ESD protection diodes to the positive and negative supply rails, a series connected 500Ω current limiting resistor followed by an anti-parallel diode pair across the input NPN transistors (Circuit 1 in "Pin Descriptions" on page 2).

The resistor-ESD diode configuration enables a wide differential input voltage range equal to the lesser of the Maximum Supply Voltage in the "Absolute Maximum Ratings" on page 3 (42V) or, a maximum of 0.5V beyond the V+ and V- supply voltage. The internal protection resistors eliminate the need for external input current limiting resistors in unity gain connections and other circuit applications where large voltages or high slew rate signals are present. Although the amplifier is fully protected, high input slew rates that exceed the amplifier slew rate (±0.32V/μs) may cause output distortion.

Output Current Limiting

The output current is internally limited to approximately ±40mA at +25°C and can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the dual op-amp. Continuous operation under these conditions may degrade long term reliability.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28107 and ISL28207 are immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

Using Only One Channel

The ISL28207 is a dual op-amp. If the application only requires one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the inverting input and ground the positive input (as shown in Figure 53).

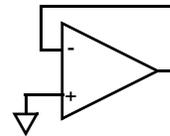


FIGURE 53. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} \times PD_{MAXTOTAL} \quad (EQ. 1)$$

where:

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad (EQ. 2)$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

ISL28107, ISL28207 SPICE Model

Figure 54 shows the SPICE model schematic and Figure 55 shows the net list for the ISL28107, ISL28207 SPICE model. The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: 1/f and flatband noise, Slew Rate, CMRR, Gain and Phase. The DC parameters are VOS, IOS, total supply current and output voltage swing. The model uses typical parameters given in the "Electrical Specifications" Table beginning on page 3. The AVOL is adjusted for 155dB with the dominate pole at 0.01Hz. The CMRR is set (145dB, $f_{cm} = 100\text{Hz}$). The input stage models the actual device to present an accurate AC representation. The model is configured for ambient temperature of +25°C.

Figures 56 through 66 show the characterization vs simulation results for the Noise Voltage, Closed Loop Gain vs Frequency, Closed Loop Gain vs R_L , Large Signal Step Response, Open Loop Gain Phase and Simulated CMRR vs Frequency.

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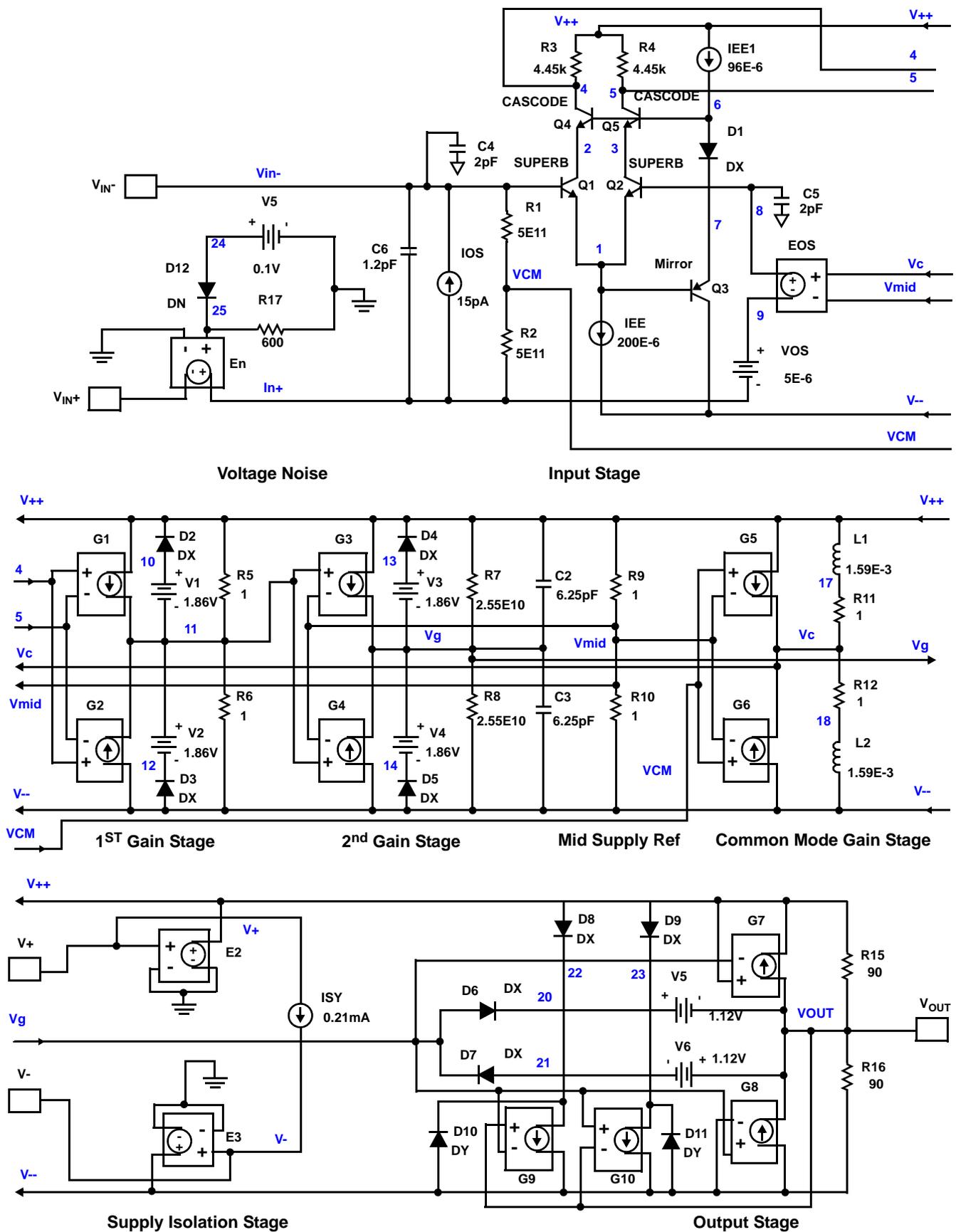


FIGURE 54. SPICE SCHEMATIC

ISL28107, ISL28207

```

* source ISL28107_SPICEmodel
* Revision A, October 28th 2009 LaFontaine
* Model for Noise, supply currents, 145dB f=100Hz
CMRR, *155dB f=0.01Hz AOL
*Copyright 2009 by Intersil Corporation
*Refer to data sheet "LICENSE STATEMENT" Use of
*this model indicates your acceptance with the
*terms and provisions in the License Statement.
* Connections: +input
*               |           -input
*               |           |           +Vsupply
*               |           |           -Vsupply
*               |           |           |           output
*               |           |           |           |
.subckt ISL28107subckt Vin+ Vin-V+ V- VOUT
* source ISL28127_SPICEMODEL_0_0
*
*Voltage Noise
E_En      IN+ VIN+ 25 0 1
R_R17     25 0 600
D_D12     24 25 DN
V_V7      24 0 0.1
*
*Input Stage
I_IOS     IN+ VIN- DC 15e-12
C_C6      IN+ VIN- 1.2E-12
R_R1      VCM VIN- 5e11
R_R2      IN+ VCM 5e11
Q_Q1      2 VIN- 1 SuperB
Q_Q2      3 8 1 SuperB
Q_Q3      V-- 1 7 Mirror
Q_Q4      4 6 2 Cascode
Q_Q5      5 6 3 Cascode
R_R3      4 V++ 4.45e3
R_R4      5 V++ 4.45e3
C_C4 VIN- 0 2e-12
C_C5 8 0 2e-12
D_D1      6 7 DX
I_IEE     1 V-- DC 200e-6
I_IEE1    V++ 6 DC 96e-6
V_VOS     9 IN+ 5e-6
E_EOS     8 9 VC VMID 1
*
*1st Gain Stage
G_G1      V++ 11 4 5 101.6828e-3
G_G2      V-- 11 4 5 101.6828e-3
R_R5      11 V++ 1
R_R6      V-- 11 1
D_D2      10 V++ DX
D_D3      V-- 12 DX
V_V1      10 11 1.86
V_V2      11 12 1.86
*
*2nd Gain Stage
G_G3      V++ VG 11 VMID 2.21e-3
G_G4      V-- VG 11 VMID 2.21e-3
R_R7      VG V++ 2.55e10
R_R8      V-- VG 2.55e10
C_C2      VG V++ 6.25e-10
C_C3      V-- VG 6.25e-10
D_D4      13 V++ DX
D_D5      V-- 14 DX
V_V3      13 VG 1.86
V_V4      VG 14 1.86
*
*Mid supply Ref
R_R9      VMID V++ 1
R_R10     V-- VMID 1
I_ISY     V+ V- DC 0.21E-3
E_E2      V++ 0 V+ 0 1
E_E3      V-- 0 V- 0 1
*
*Common Mode Gain Stage with Zero
G_G5      V++ VC VCM VMID 5.62e-8
G_G6      V-- VC VCM VMID 5.62e-8
R_R11     VC 17 1
R_R12     18 VC 1
L_L1      17 V++ 1.59e-3
L_L2      18 V-- 1.59e-3
*
*Output Stage with Correction Current Sources
G_G7      VOUT V++ V++ VG 1.11e-2
G_G8      V-- VOUT VG V-- 1.11e-2
G_G9      22 V-- VOUT VG 1.11e-2
G_G10     23 V-- VG VOUT 1.11e-2
D_D6      VG 20 DX
D_D7      21 VG DX
D_D8      V++ 22 DX
D_D9      V++ 23 DX
D_D10     V-- 22 DY
D_D11     V-- 23 DY
V_V5      20 VOUT 1.12
V_V6      VOUT 21 1.12
R_R15     VOUT V++ 9E1
R_R16     V-- VOUT 9E1
*
.model SuperB npn
+ is=184E-15 bf=30e3 va=15 ik=70E-3 rb=50
+ re=0.065 rc=35 cje=1.5E-12 cjc=2E-12
+ kf=0 af=0
.model Cascode npn
+ is=502E-18 bf=150 va=300 ik=17E-3 rb=140
+ re=0.011 rc=900 cje=0.2E-12 cjc=0.16E-12f
+ kf=0 af=0
.model Mirror pnp
+ is=4E-15 bf=150 va=50 ik=138E-3 rb=185
+ re=0.101 rc=180 cje=1.34E-12 cjc=0.44E-12
+ kf=0 af=0
.model DN D(KF=6.69e-9 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28107subckt

```

FIGURE 55. SPICE NET LIST

Characterization vs Simulation Results

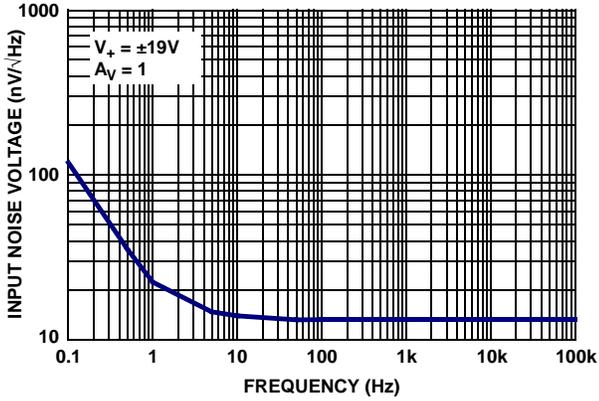


FIGURE 56. CHARACTERIZED INPUT NOISE VOLTAGE

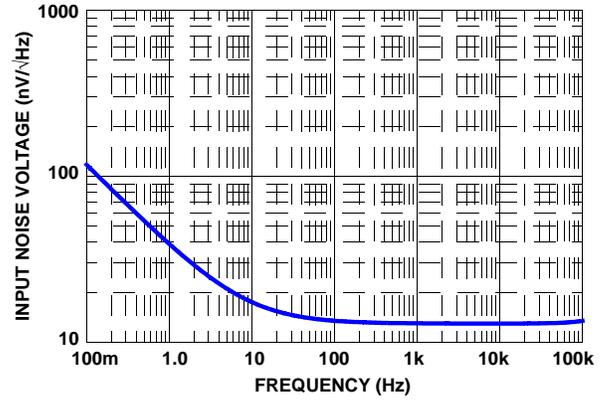


FIGURE 57. SIMULATED INPUT NOISE VOLTAGE

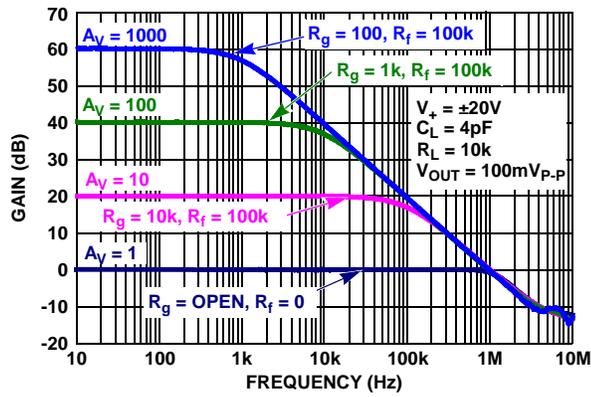


FIGURE 58. CHARACTERIZED CLOSED LOOP GAIN vs FREQUENCY

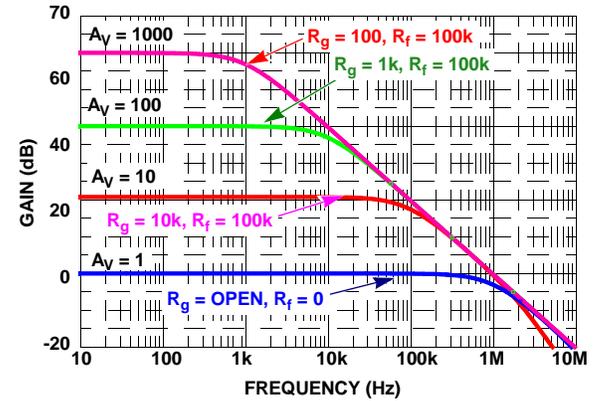


FIGURE 59. SIMULATED CLOSED LOOP GAIN vs FREQUENCY

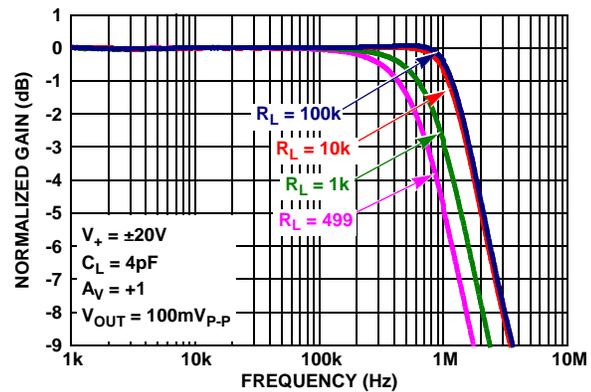


FIGURE 60. CHARACTERIZED CLOSED LOOP GAIN vs R_L

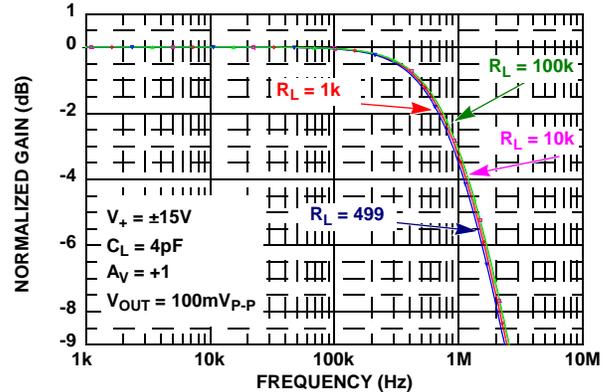


FIGURE 61. SIMULATED CLOSED LOOP GAIN vs R_L

Characterization vs Simulation Results (Continued)

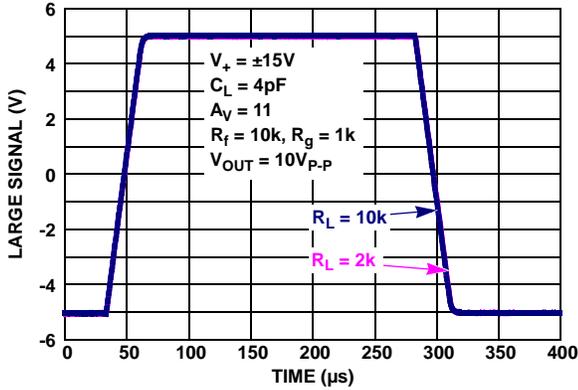


FIGURE 62. CHARACTERIZED LARGE SIGNAL 10V STEP RESPONSE

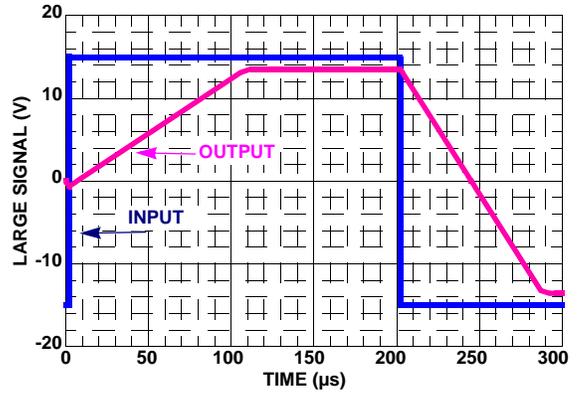


FIGURE 63. SIMULATED LARGE SIGNAL 10V STEP RESPONSE

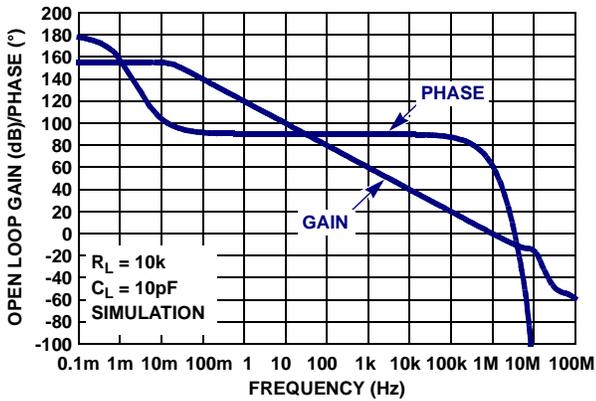


FIGURE 64. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

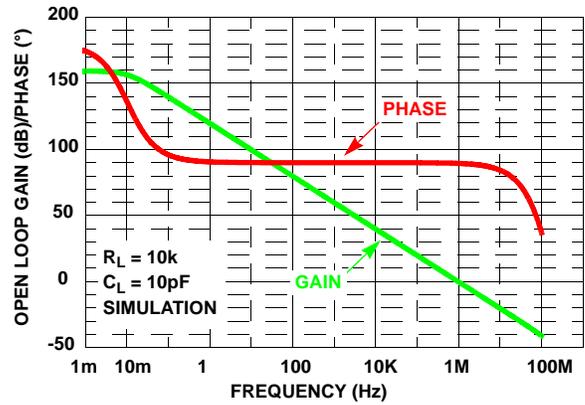


FIGURE 65. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

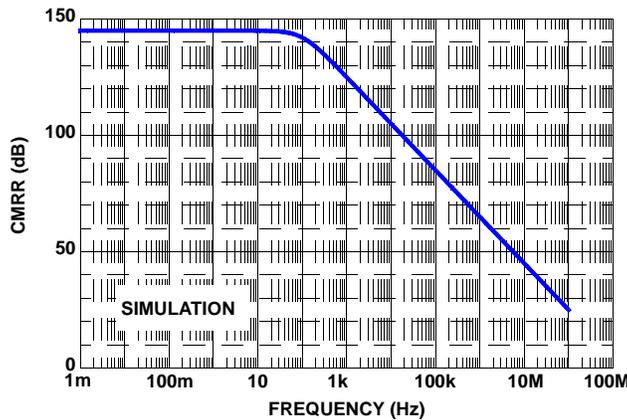


FIGURE 66. SIMULATED CMRR vs FREQUENCY

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to Web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
3/9/10	FN6631.2	<ol style="list-style-type: none"> Added MSOP package to the ordering information and added applicable POD M8.118 to end of datasheet Separated each part number with it's own specific -T7 and -T13 suffix. Removed "Add "-T7" or "-T13" suffix for Tape and Reel." from Note 1. Added MSOP to the Pin Configuartion and Pin Descriptions Updated ± 15 and $\pm 5V$ Electrical Specification table with the following edits: <ol style="list-style-type: none"> Separated VOS specs for SOIC and MSOP packages. Added new VOS specs for MSOP Grade package. Separated TCvos specs for SOIC and MSOP packages. Added new TCvos specs for MSOP package. Added Theta JA and JC for the 8 Ld MSOP package. Added Theta JC values for both SOIC package options. Changed Theta JA for 8 Ld SOIC (ISL28207) from 115 to 105.
2/22/10		<ol style="list-style-type: none"> Added "Related Literature*(see page 21)" on page 1. Added Evaluation Boards to "Ordering Information" on page 2. "Electrical Specifications" Tables, page 3 to page 6. Unbolded MIN/MAX specs with "$T_A = -40^\circ C$ to $+85^\circ C$" conditions (since only MIN/MAX specs with "$T_A = -40^\circ C$ to $+125^\circ C$" conditions should be bolded, per note in common conditions) Corrected Note reference in I_{SC} parameter on page 4 and page 5 from Note 3 to Note 7.
11/10/09	FN6631.1	<ol style="list-style-type: none"> Updated VOS, IB, and IOS electrical specifications. Added Typical performance curves, Figures 1 through 30. Output Short Circuit Current test condition has been clarified with Note 7. Updated POD. Added Spice Model, associated text and Figures 56 through 66. Deleted old figures 6, 7, 8, 10, 11 and 12. Added Licence Statement on page 16 and referenced in spice model.
6/5/09	FN6631.0	Initial Release.

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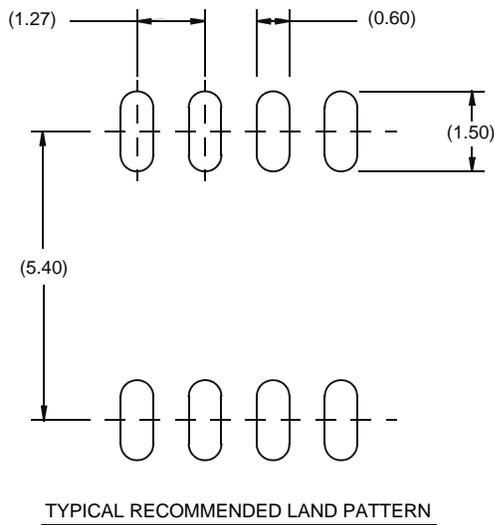
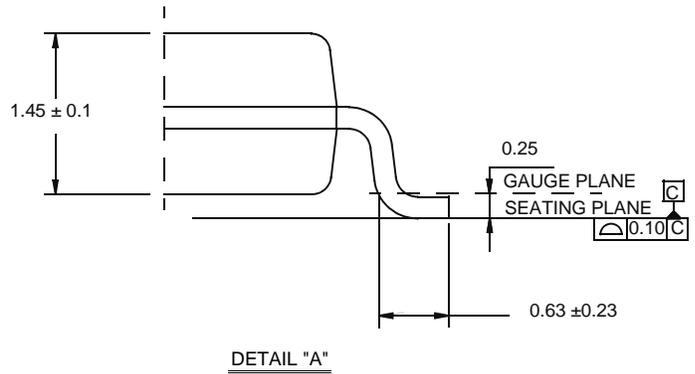
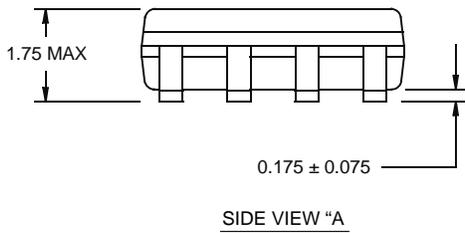
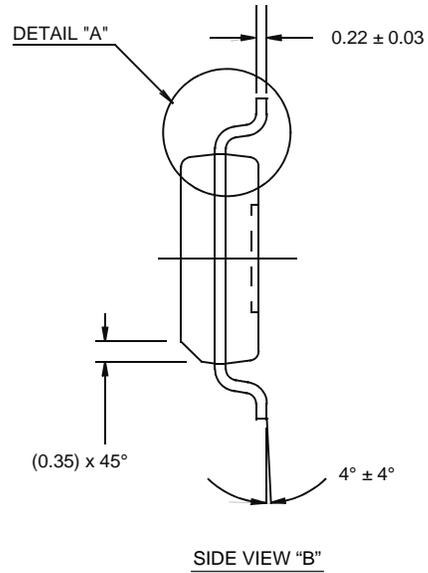
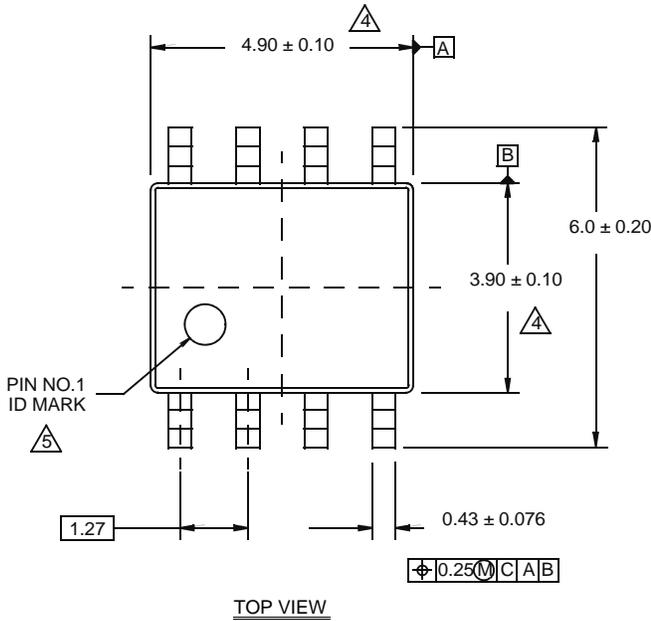
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Package Outline Drawing

M8.15E

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 0, 08/09



NOTES:

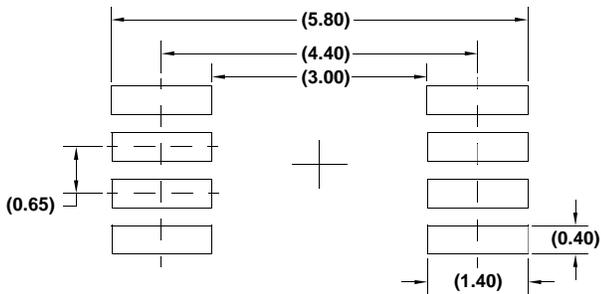
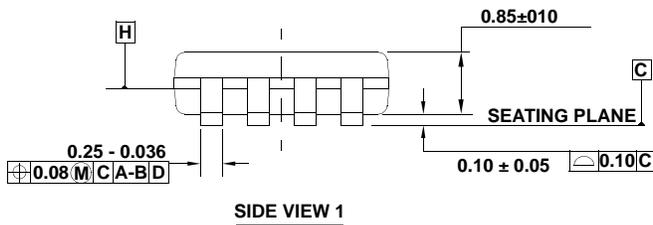
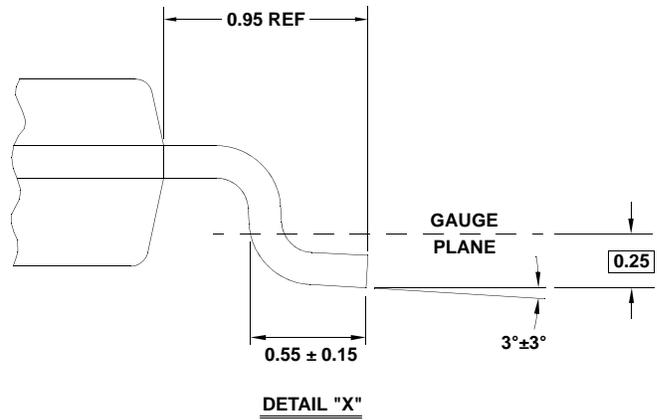
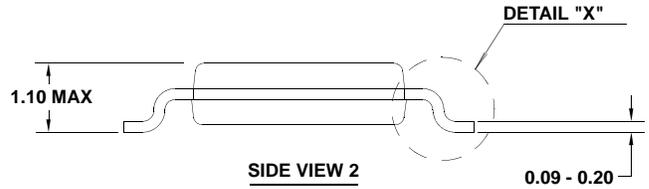
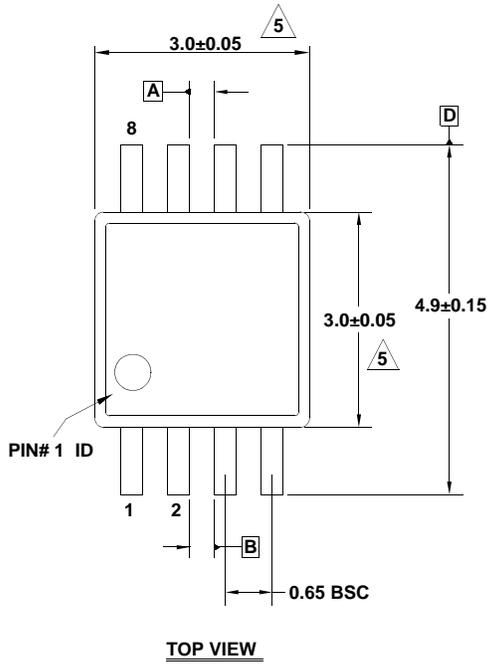
1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

Package Outline Drawing

M8.118

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 3, 3/10



NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in () are for reference only.