Compact Synchronous Buck Regulators

ISL8026, ISL8026A

The ISL8026, ISL8026A are highly efficient, monolithic, synchronous step-down DC/DC converters that can deliver 6A of continuous output current from a 2.5V to 5.5V input supply. The devices use current mode control architecture to deliver a very low duty cycle operation at high frequency with fast transient response and excellent loop stability.

The ISL8026, ISL8026A integrate a very low ON-resistance P-channel (36mΩ) high-side FET and N-channel (13mΩ) low-side FET to maximize efficiency and minimize external component count. The 100% duty-cycle operation allows less than 180mV dropout voltage at 6A output current. The operation frequency of the Pulse-width Modulator (PWM) is adjustable from 500kHz to 4MHz. The default switching frequency, which is set by connecting the FS pin high, is 1MHz for the ISL8026 and 2MHz for the ISL8026A.

The ISL8026, ISL8026A can be configured for discontinuous or forced continuous operation at light load. Forced continuous operation reduces noise and RF interference, while discontinuous mode provides higher efficiency by reducing switching losses at light loads.

Fault protection is provided by internal hiccup mode current limiting during short-circuit and overcurrent conditions. Other protection, such as overvoltage and over-temperature, are also integrated into the device. A power-good output voltage monitor indicates when the output is in regulation.

The ISL8026, ISL8026A offer a 1ms Power-Good (PG) timer at power-up. When in shutdown, the ISL8026, ISL8026A discharge the output capacitor through an internal soft-stop switch. Other features include internal fixed or adjustable soft-start and internal/external compensation.

The ISL8026, ISL8026A are offered in a space saving 16 Ld 3x3 Pb-free TQFN package with an exposed pad for improved thermal performance and 0.8mm maximum height. The complete converter occupies less than 142mm^2.

Features

- 2.5V to 5.5V input voltage range
- Very low ON-resistance FETs - P-channel 36mΩ and N-channel 13mΩ typical values
- High efficiency synchronous buck regulator with up to 95% efficiency
- 1.0% reference accuracy over load/line/temperature (-40°C to +85°C)
- 1.5% reference accuracy over load/line/temperature (-40°C to +125°C)
- Internal soft-start: 1ms or adjustable
- Soft-stop output discharge during disable
- Adjustable frequency from 500kHz to 4MHz - default at 1MHz (ISL8026) or 2MHz (ISL8026A)
- External synchronization up to 4MHz
- Over-temperature, overcurrent, overvoltage and negative overcurrent protection

Applications

- DC/DC POL modules
- µC/µP, FPGA and DSP power
- Video processor/SOC power
- Li-ion battery powered devices
- Routers and switchers
- Portable instruments
- Test and measurement systems
- Industrial PCs

Related Literature

- UG033, “ISL8026xEVAL3Z Evaluation Board User Guide”

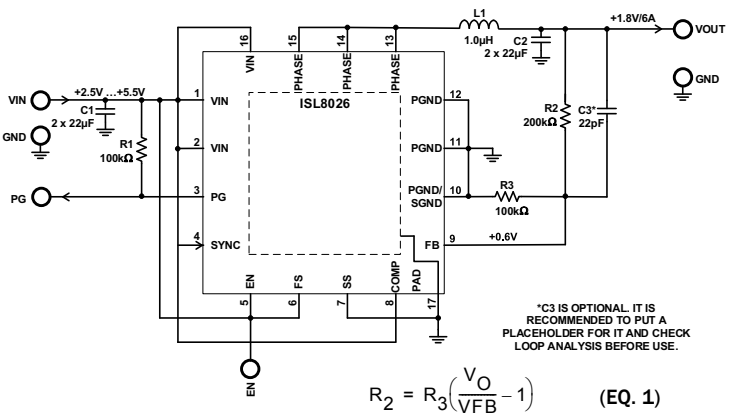

FIGURE 1. TYPICAL APPLICATION CIRCUIT CONFIGURATION (INTERNAL COMPENSATION OPTION)

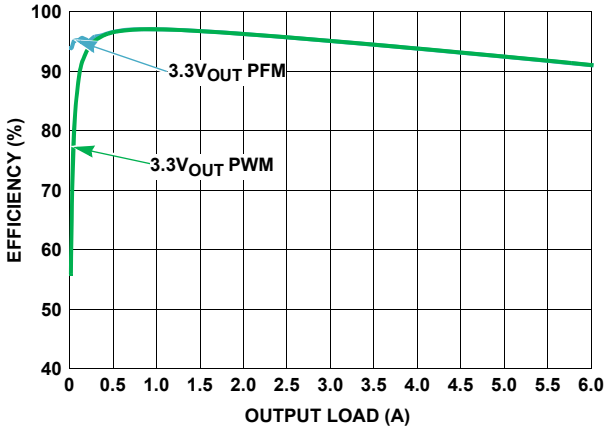

FIGURE 2. EFFICIENCY vs LOAD 1MHz 5V_{IN}

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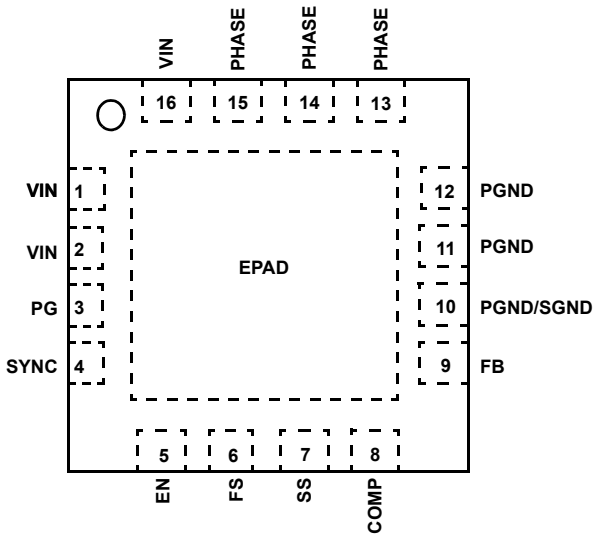
Pin Configuration

ISL8026, ISL8026A
(16 LD TQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 2, 16	VIN	Input supply voltage. Place a minimum of two 22µF ceramic capacitors from VIN to PGND as close as possible to the IC for decoupling.
3	PG	Power-good is an open-drain output. Use a 10kΩ to 100kΩ pull-up resistor connected between VIN and PG. At power-up or EN HI, PG rising edge is delayed by 1ms once the output voltage reaches regulation.
4	SYNC	Mode Selection pin. Connect to logic high or input voltage VIN for PWM mode. Connect to logic low or ground for PFM mode. Connect to an external function generator for synchronization with the positive edge trigger. There is an internal 1MΩ pull-down resistor to prevent an undefined logic state in case the SYNC pin is floating.
5	EN	Regulator enable pin. Enable the output when driven high. Shut down the chip and discharge output capacitor when driven low.
6	FS	This pin sets the oscillator switching frequency using a resistor, R_{FS}, from the FS pin to GND. The frequency of operation may be programmed between 500kHz to 4MHz. The default frequency is 1MHz (ISL8026), 2MHz (ISL8026A) if FS is connected to VIN.
7	SS	SS is used to adjust the soft-start time. Connect to SGND for internal 1ms rise time. Connect a capacitor from SS to SGND to adjust the soft-start time. Do not use more than 33nF per IC.
8, 9	COMP, FB	The feedback network of the regulator, FB, is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider connected to FB. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. COMP is the output of the amplifier if COMP is not tied to VIN. Otherwise, COMP is disconnected through a MOSFET for internal compensation. Must connect COMP to VIN in internal compensation mode to meet a typical application. Additional external networks across COMP and SGND might be required to improve the loop compensation of the amplifier operation. In addition, the regulator power-good and undervoltage protection circuitry use FB to monitor the regulator output voltage.
10	PGND/SGND	Power/signal ground
11, 12	PGND	Power ground
13, 14, 15	PHASE	Switching node connections. Connect to one terminal of the inductor. This pin is discharged by a 100Ω resistor when the device is disabled. See "Block Diagram" on page 5 for more detail.
Exposed Pad	-	The exposed pad must be connected to the SGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to the SGND plane for optimal thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	OPERATION FREQUENCY (MHz)	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL8026IRTAJZ	026A	1	-40 to +85	16 Ld 3x3 TQFN	L16.3x3D
ISL8026AIRTAJZ	26AA	2	-40 to +85	16 Ld 3x3 TQFN	L16.3x3D
ISL8026FRTAJZ	026F	1	-40 to +125	16 Ld 3x3 TQFN	L16.3x3D
ISL8026AFRTAJZ	026AF	2	-40 to +125	16 Ld 3x3 TQFN	L16.3x3D
ISL8026EVAL3Z	Evaluation board for ISL8026				
ISL8026AEVAL3Z	Evaluation board for ISL8026A				

NOTES:

1. Add “-T” suffix for 6k unit or “-T7A” suffix for 250 unit Tape and Reel options. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL8026, ISL8026A. For more information on MSL please see techbrief TB363.

TABLE 1. SUMMARY OF KEY DIFFERENCES

PART NUMBER	I_{OUT} (MAX) (A)	f_{SW} RANGE (MHz)	V_{IN} RANGE (V)	V_{OUT} RANGE (V)	PART SIZE (mm)
ISL8026	6	Programmable 0.5MHz to 4MHz	2.5 to 5.5	0.6 to 5.5	3x3
ISL8026A		Programmable 1MHz to 4MHz			

TABLE 2. ISL8026 COMPONENT SELECTION

V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	3.6V
C_1	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF
C_2	4 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF
C_3	22pF	22pF	22pF	22pF	22pF	22pF	22pF
L_1	0.47~1µH	0.47~1µH	0.47~1µH	0.68~1.5µH	0.68~1.5µH	1~2.2µH	1~2.2µH
R_2	33kΩ	100kΩ	150kΩ	200kΩ	316kΩ	450kΩ	500kΩ
R_3	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ

TABLE 3. ISL8026A COMPONENT SELECTION

V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	3.6V
C_1	22µF	22µF	22µF	22µF	22µF	22µF	22µF
C_2	3 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF
C_3	22pF	22pF	22pF	22pF	22pF	22pF	22pF
L_1	0.22~0.47µH	0.22~0.47µH	0.22~0.47µH	0.33~0.68µH	0.33~0.68µH	0.47~1µH	0.47~1µH
R_2	33kΩ	100kΩ	150kΩ	200kΩ	316kΩ	450kΩ	500kΩ
R_3	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ

Block Diagram

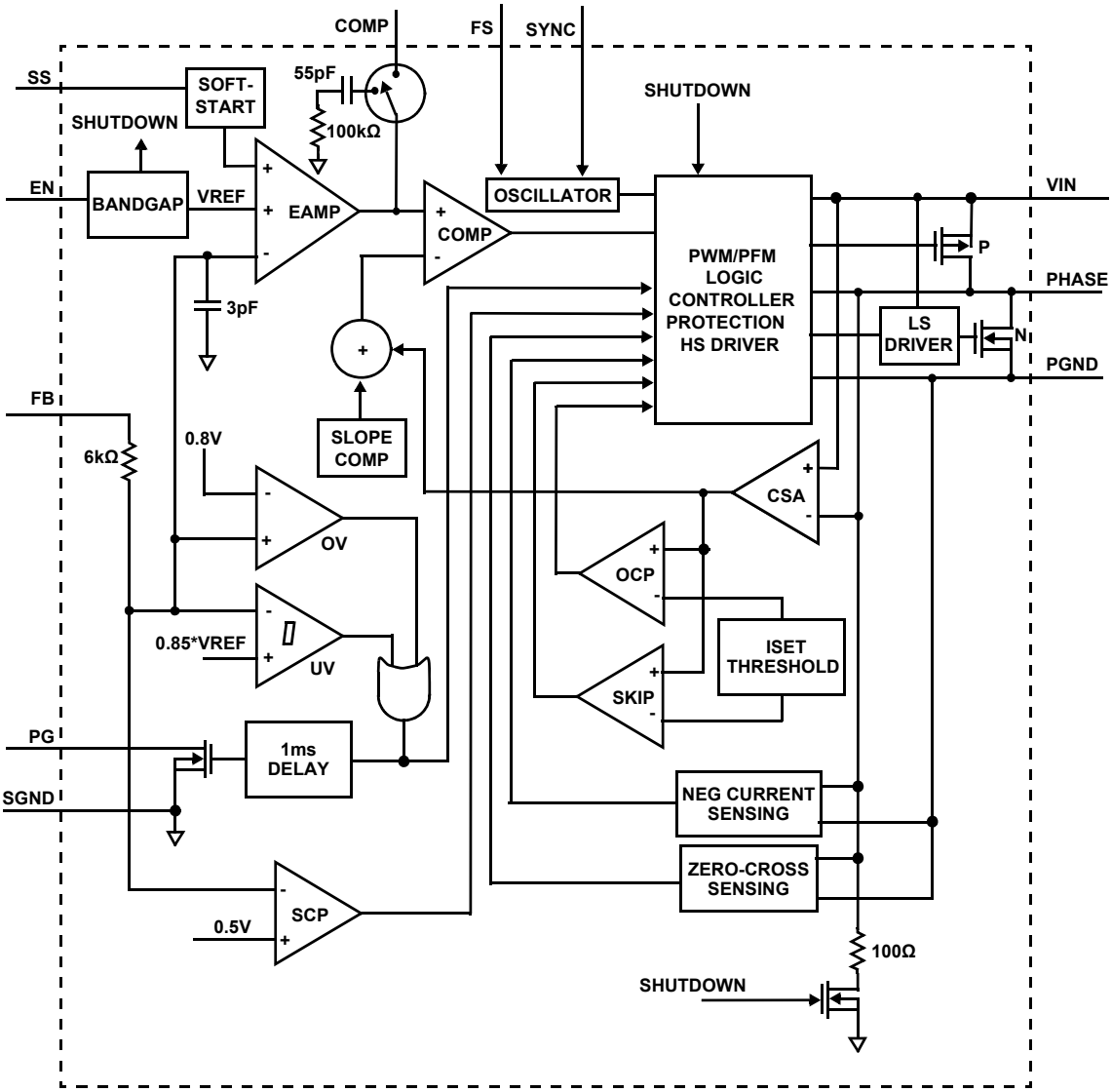


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings (Reference to GND)

VIN . . . . . -0.3V to 5.8V (DC) or 7V (20ms)
EN, FS, PG, SYNC, VFB . . . . . -0.3V to VIN + 0.3V
PHASE . . . . . -1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or 7V (20ms)
COMP, SS . . . . . -0.3V to 2.7V
ESD Ratings
Human Body Model (Tested per JESD22-A114) 3kV
Charged Device Model (Tested per JESD22-C101E) 2kV
Machine Model (Tested per JESD22-A115) 200V
Latch-Up (Tested per JESD-78A; Class 2, Level A) . . . . . 100mA at +85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 LD TQFN Package (Notes 4, 5)	47	6.5

Junction Temperature Range . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

V_{IN} Supply Voltage Range . . . . . 2.5V to 5.5V
Load Current Range . . . . . 0A to 6A
Ambient Temperature Range (Industrial) . . . . . -40°C to +85°C
Ambient Temperature Range (Full-Range Industrial) . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameter limits are established across the recommended operating conditions and are measured at the following conditions: V_{IN} = 3.6V, EN = V_{IN}, unless otherwise noted. Typical values are at T_A = +25°C. Unless otherwise noted, **Boldface limits apply across the operating temperature range, -40°C to +125°C**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
INPUT SUPPLY						
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising, no load		2.3	**2.5**	V
		Falling, no load	**2.10**	2.25		V
Quiescent Supply Current	I_{VIN}	SYNC = GND, no load at the output		50		µA
		SYNC = GND, no load at the output and no switching		50	**62**	µA
		SYNC = V_{IN}, f_{SW} = 1MHz, no load at the output (ISL8026)		9	**16**	mA
		SYNC = V_{IN}, f_{SW} = 2MHz, no load at the output (ISL8026A)		16	**23**	mA
Shutdown Supply Current	I_{SD}	SYNC = GND, V_{IN} = 5.5V, EN = low		5	**8**	µA
OUTPUT REGULATION						
Reference Voltage	V_{REF}	-40°C < T_J < +85°C	**0.594**	0.600	**0.606**	V
		-40°C < T_J < +125°C	**0.591**	0.600	**0.606**	V
VFB Bias Current	I_{VFB}	VFB = 0.75V		0.1		µA
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V (minimal 2.5V)		0.2		%/V
Soft-Start Ramp Time Cycle		SS = SGND		1		ms
Soft-Start Charging Current	ISS	V_{SS} = 0.1V	**1.45**	1.85	**2.25**	µA
OVERCURRENT PROTECTION						
Current Limit Blanking Time	t_{OCON}			17		Clock pulses
Overcurrent and Auto Restart Period	t_{OCOFF}			8		SS cycle
Positive Peak Current Limit	I_{PLIMIT}	6A application	**7.5**	9	**11**	A
Peak Skip Limit	I_{SKIP}	6A application (See "Application Information" on page 19 for more detail)	**1**	1.3	**1.8**	A
Zero Cross Threshold			**-300**		**300**	mA
Negative Current Limit	I_{NLIMIT}		**-4.5**	-3.0	**-1.5**	A

Electrical Specifications Unless otherwise noted, all parameter limits are established across the recommended operating conditions and are measured at the following conditions: V_{IN} = 3.6V, EN = V_{IN}, unless otherwise noted. Typical values are at T_A = +25°C. Unless otherwise noted, **Boldface limits apply across the operating temperature range, -40°C to +125°C (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
COMPENSATION						
Error Amplifier Transconductance		Internal compensation		60		µA/V
		External compensation		120		µA/V
Transresistance	Rt	6A application (test at 3.6V) -40°C < T_J < +85°C	**0.119**	0.140	**0.166**	Ω
		6A application (test at 3.6V) -40°C < T_J < +125°C	**0.110**	0.140	**0.170**	Ω
PHASE						
P-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA		36	**63**	mΩ
		V_{IN} = 2.7V, I_O = 200mA		52	**89**	mΩ
N-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA		13	**30**	mΩ
		V_{IN} = 2.7V, I_O = 200mA		17	**36**	mΩ
PHASE Maximum Duty Cycle				100		%
PHASE Minimum On-Time		SYNC = High			**140**	ns
OSCILLATOR						
Nominal Switching Frequency	f_{SW}	f_{SW} = V_{IN}, ISL8026A. -40°C < T_J < +85°C	**1600**	2000	**2400**	kHz
		f_{SW} = V_{IN}, ISL8026A. -40°C < T_J < +125°C	**1550**	2000	**2450**	kHz
		f_{SW} = V_{IN}, ISL8026	**780**	1000	**1200**	kHz
		f_{SW} with RS = 402kΩ		490		kHz
		f_{SW} with RS = 42.2kΩ		4200		kHz
SYNC Logic LOW to HIGH Transition Range			**0.70**	0.75	**0.80**	V
SYNC Hysteresis				0.15		V
SYNC Logic Input Leakage Current		V_{IN} = 3.6V		3.6	**5**	µA
PG						
Output Low Voltage					**0.3**	V
Delay Time (Rising Edge)		Time from V_{OUT} reached regulation	**0.5**	1	**2**	ms
PG Pin Leakage Current		PG = V_{IN}		0.01	**0.10**	µA
OVP PG Rising Threshold				0.80		V
UVP PG Rising Threshold			**80**	85	**90**	%
UVP PG Hysteresis				30		mV
PGOOD Delay Time (Falling Edge)				7.5		µs
EN						
Logic Input Low					**0.4**	V
Logic Input High			**0.9**			V
EN Logic Input Leakage Current		Pulled up to 3.6V		0.1	**1**	µA
Thermal Shutdown		Temperature Rising		150		°C
Thermal Shutdown Hysteresis		Temperature Falling		25		°C

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 6A. Resistor load is used in the test.

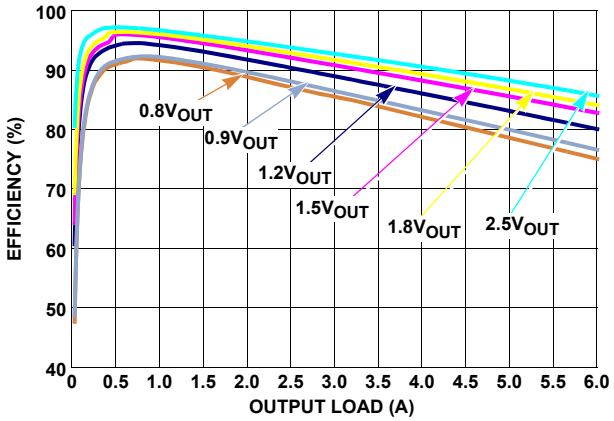


FIGURE 4. EFFICIENCY vs LOAD (1MHz 3.3 V_{IN} PWM)

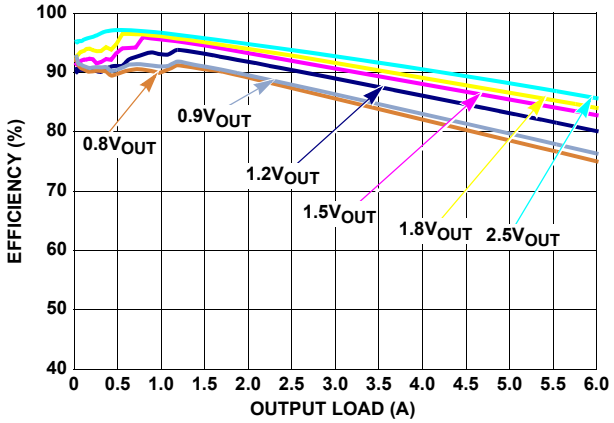


FIGURE 5. EFFICIENCY vs LOAD (1MHz 3.3 V_{IN} PFM)

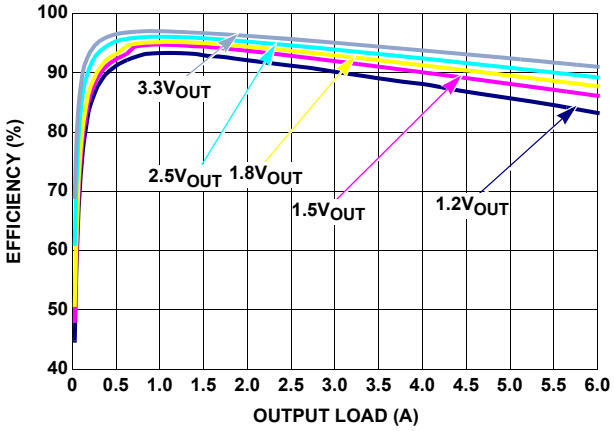


FIGURE 6. EFFICIENCY vs LOAD (1MHz 5V_{IN} PWM)

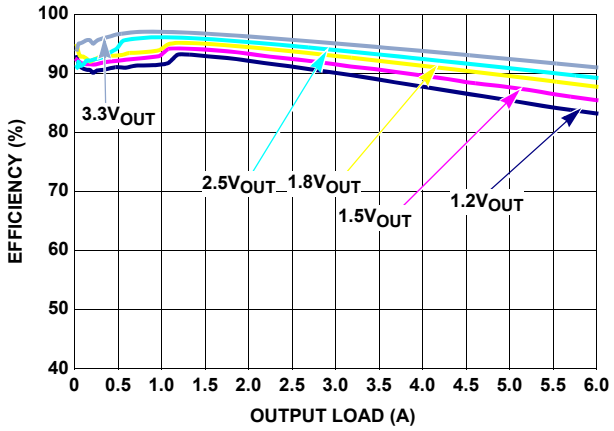


FIGURE 7. EFFICIENCY vs LOAD (1MHz 5V_{IN} PFM)

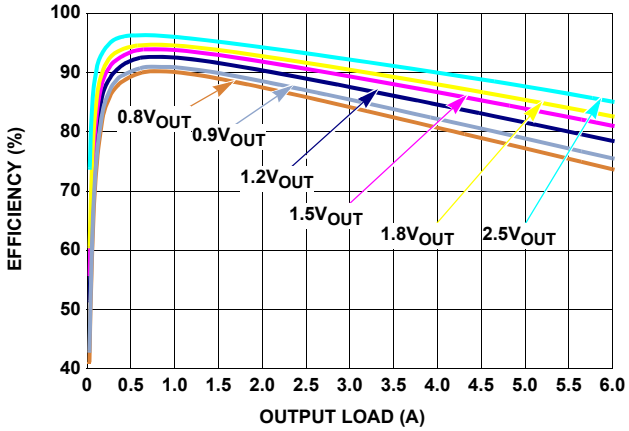


FIGURE 8. EFFICIENCY vs LOAD (2MHz 3.3V_{IN} PWM)

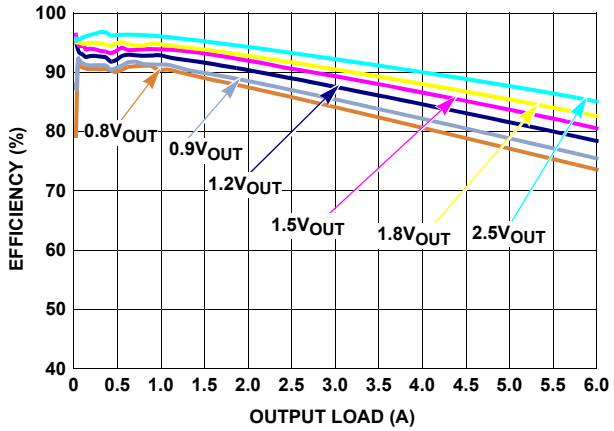


FIGURE 9. EFFICIENCY vs LOAD (2MHz 3.3V_{IN} PFM)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 6A. Resistor load is used in the test. **(Continued)**

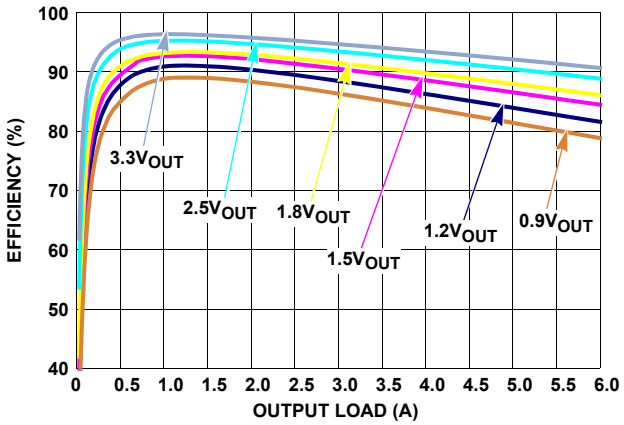


FIGURE 10. EFFICIENCY vs LOAD (2MHz $5V_{IN}$ PWM)

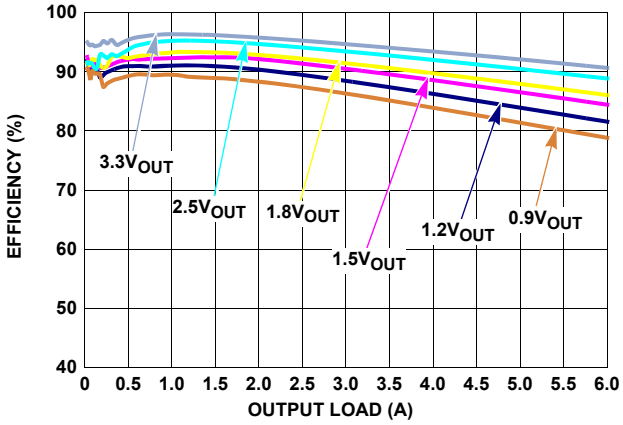


FIGURE 11. EFFICIENCY vs LOAD (2MHz $5V_{IN}$ PFM)

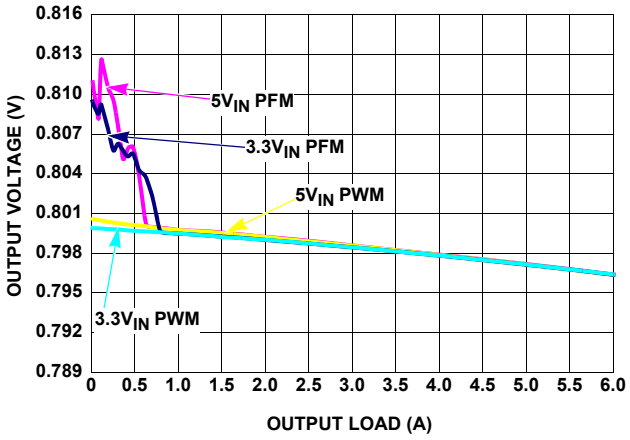


FIGURE 12. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 0.8V)

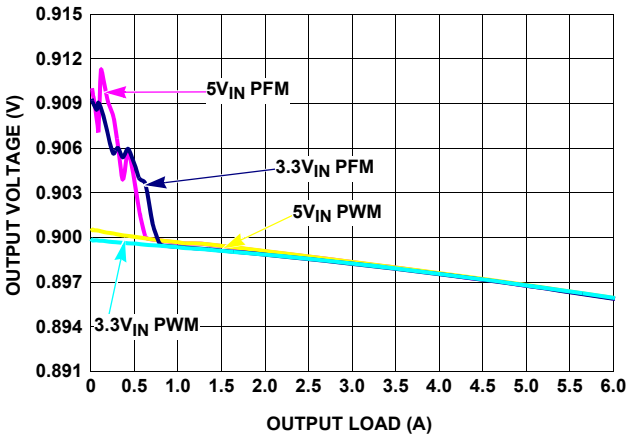


FIGURE 13. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 0.9V)

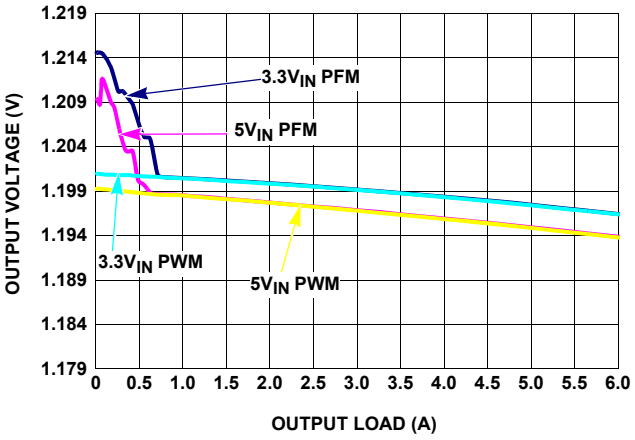


FIGURE 14. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.2V)

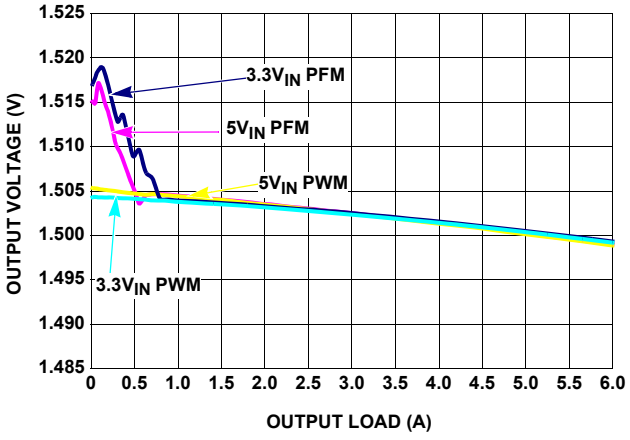


FIGURE 15. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.5V)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 6A. Resistor load is used in the test. **(Continued)**

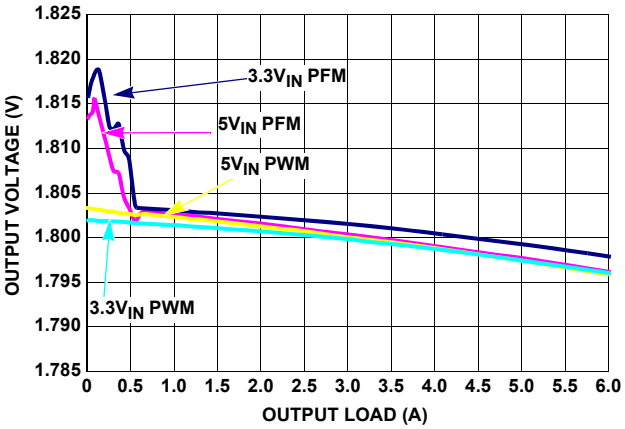


FIGURE 16. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.8V)

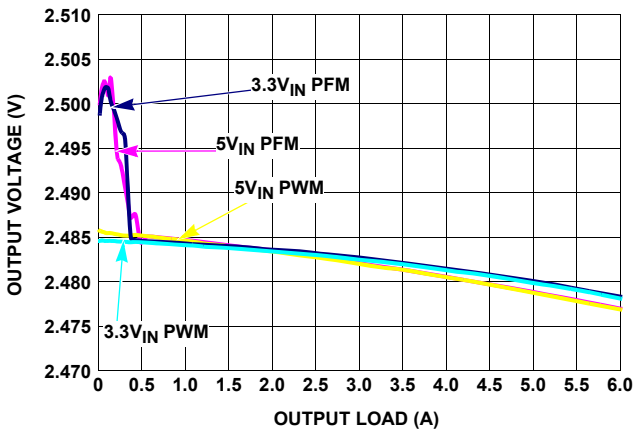


FIGURE 17. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 2.5V)

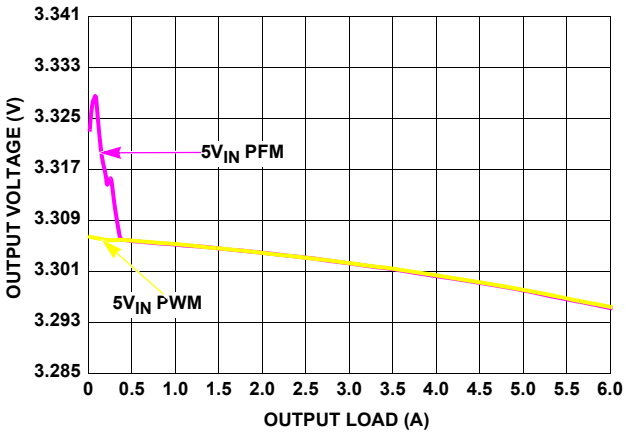


FIGURE 18. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 3.3V)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 6A. Resistor load is used in the test. **(Continued)**

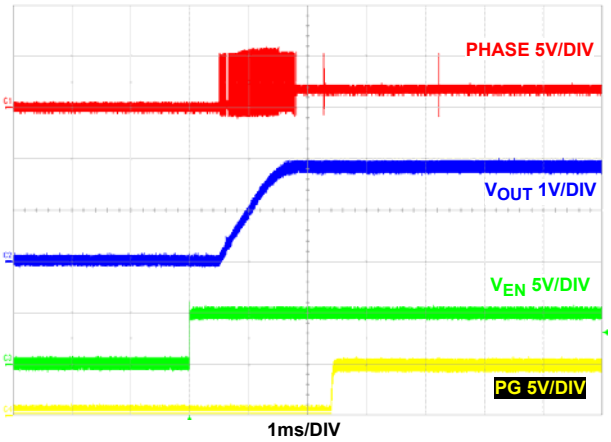


FIGURE 19. START-UP AT NO LOAD (PFM)

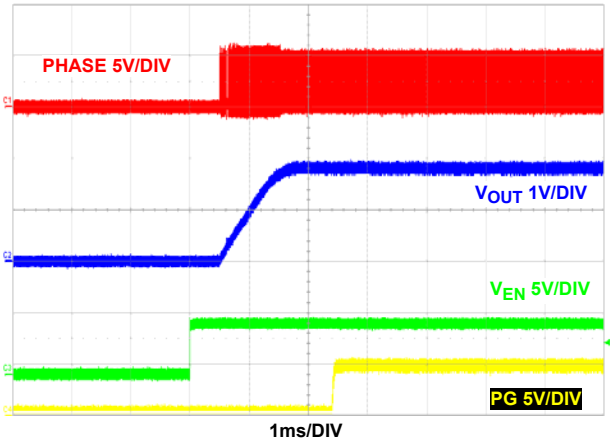


FIGURE 20. START-UP AT NO LOAD (PWM)

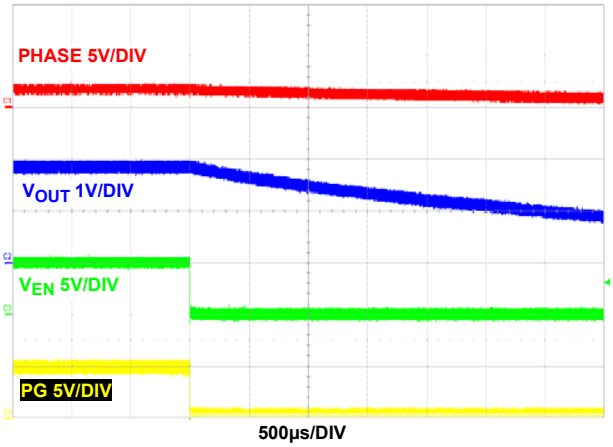


FIGURE 21. SHUTDOWN AT NO LOAD (PFM)

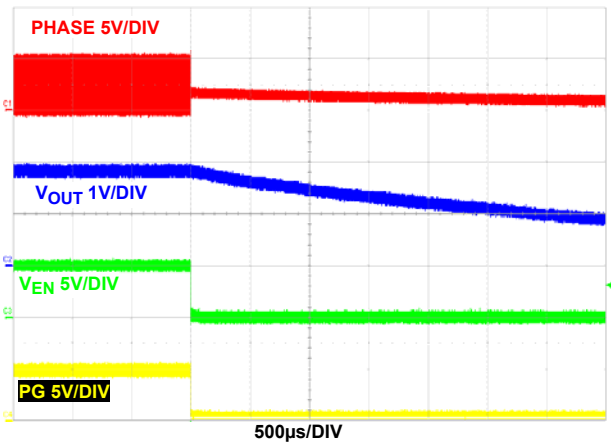


FIGURE 22. SHUTDOWN AT NO LOAD (PWM)

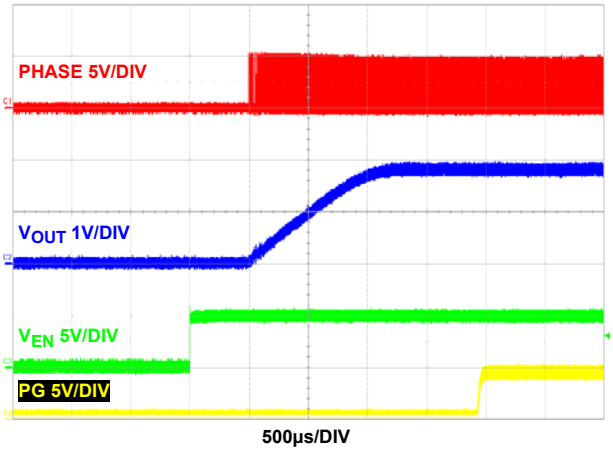


FIGURE 23. START-UP AT 6A LOAD (PWM)

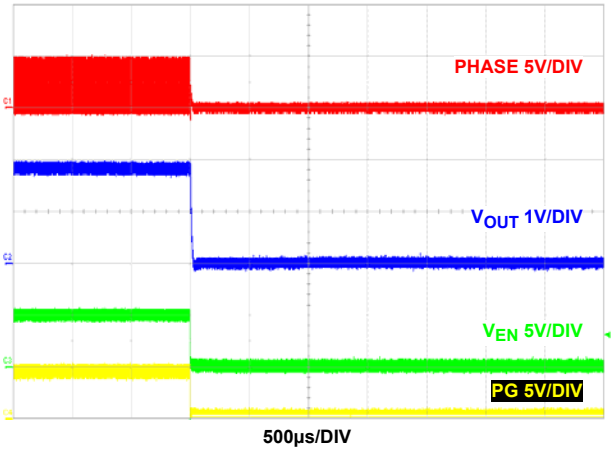


FIGURE 24. SHUTDOWN AT 6A LOAD (PWM)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 6A. Resistor load is used in the test. **(Continued)**

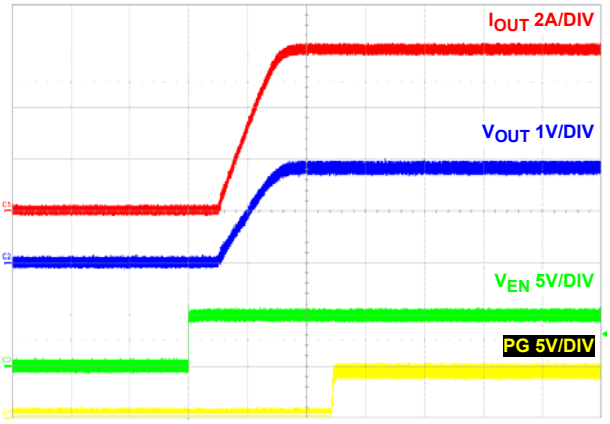


FIGURE 25. START-UP AT 6A LOAD (PFM)

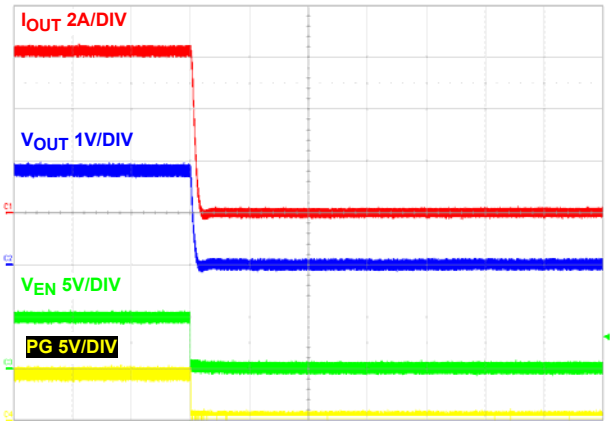


FIGURE 26. SHUTDOWN AT 6A LOAD (PFM)

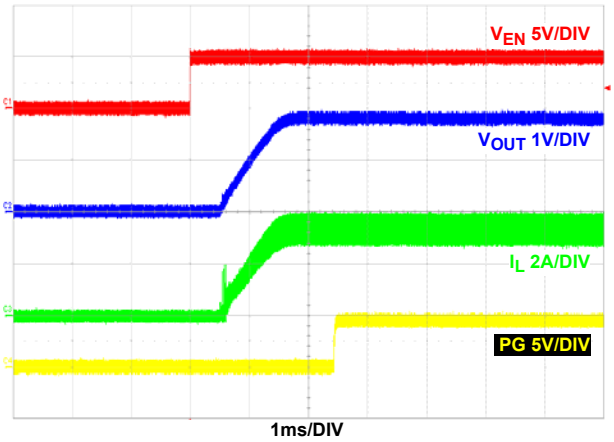


FIGURE 27. START-UP AT 3A LOAD (PWM)

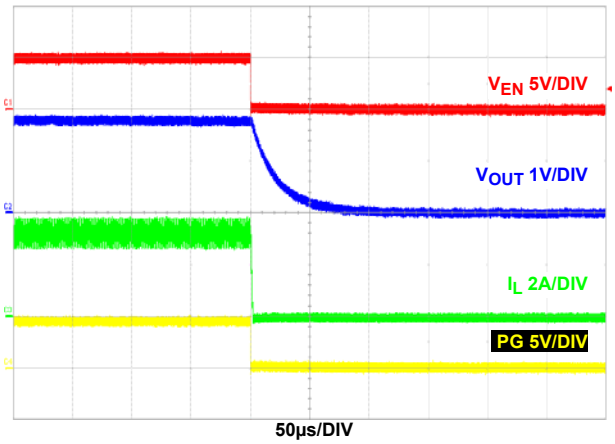


FIGURE 28. SHUTDOWN AT 3A LOAD (PWM)

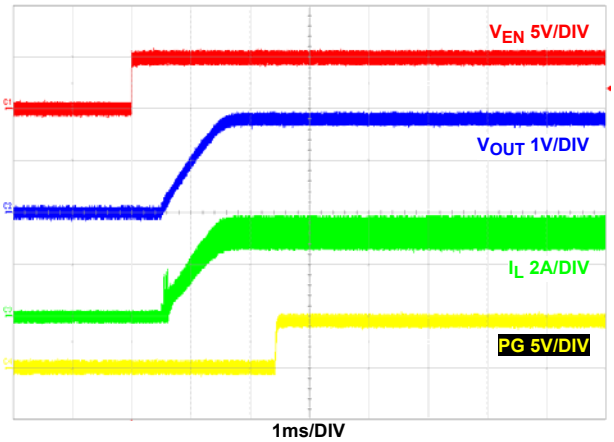


FIGURE 29. START-UP AT 3A LOAD (PFM)

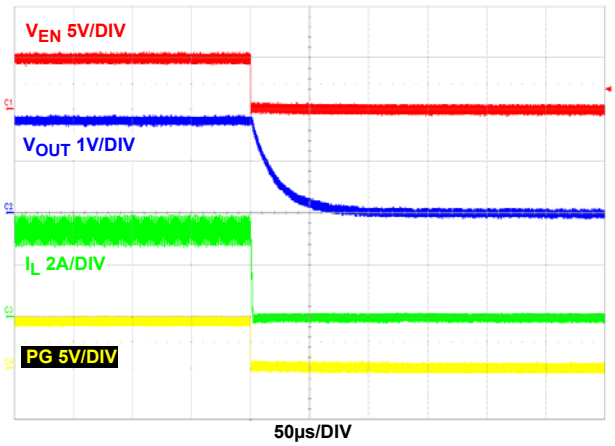


FIGURE 30. SHUTDOWN AT 3A LOAD (PFM)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 6A. Resistor load is used in the test. **(Continued)**

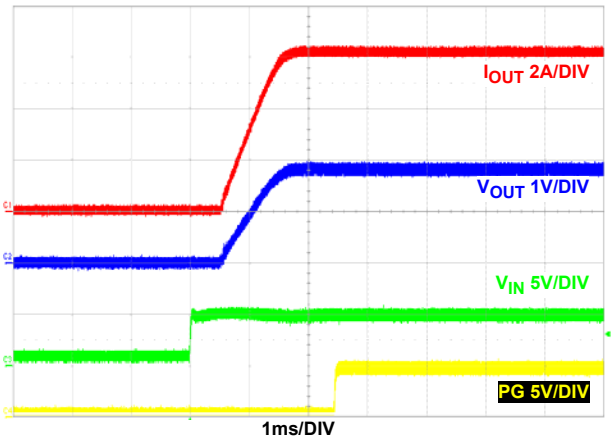


FIGURE 31. START-UP V_{IN} AT 6A LOAD (PFM)

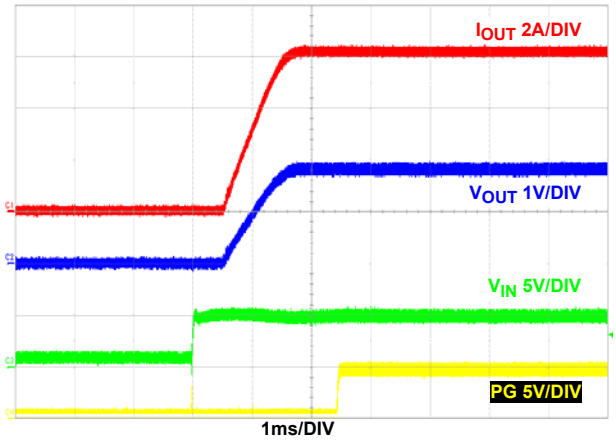


FIGURE 32. START-UP V_{IN} AT 6A LOAD (PWM)

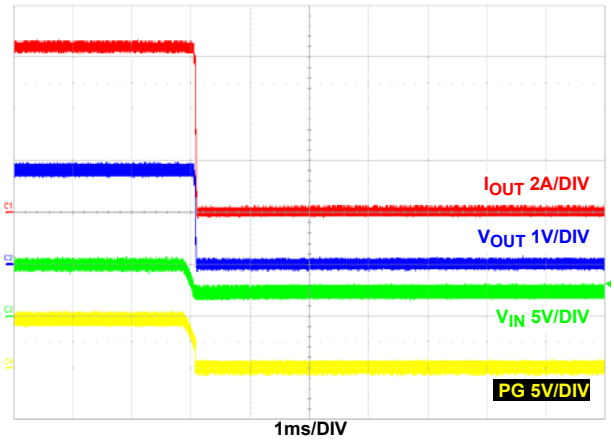


FIGURE 33. SHUTDOWN V_{IN} AT 6A LOAD (PFM)

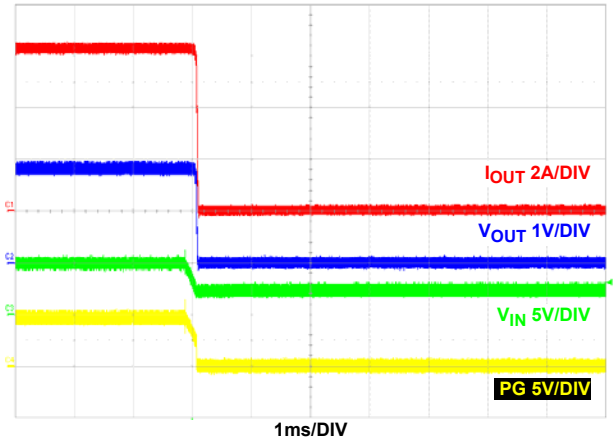


FIGURE 34. SHUTDOWN V_{IN} AT 6A LOAD (PWM)

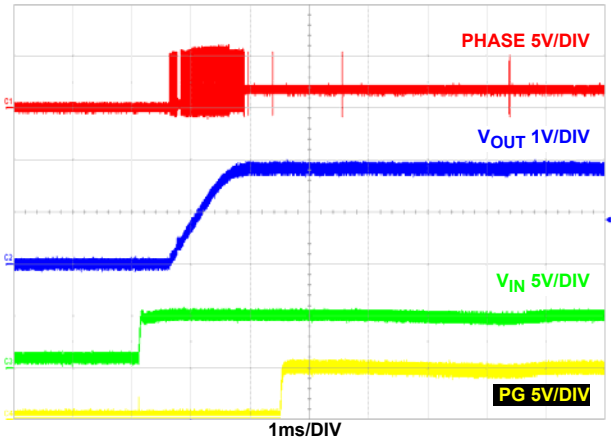


FIGURE 35. START-UP VIN AT NO LOAD (PFM)

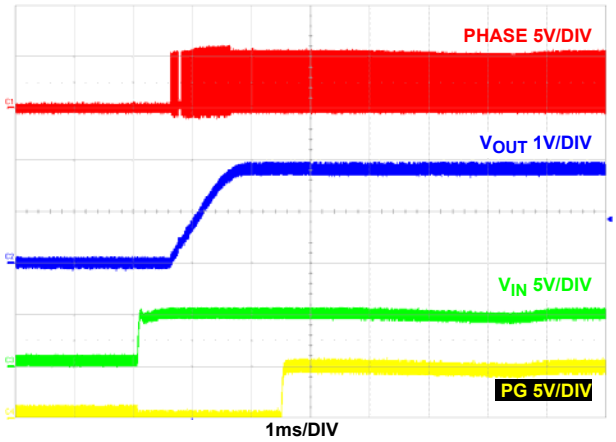


FIGURE 36. START-UP VIN AT NO LOAD (PWM)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 6A. Resistor load is used in the test. **(Continued)**

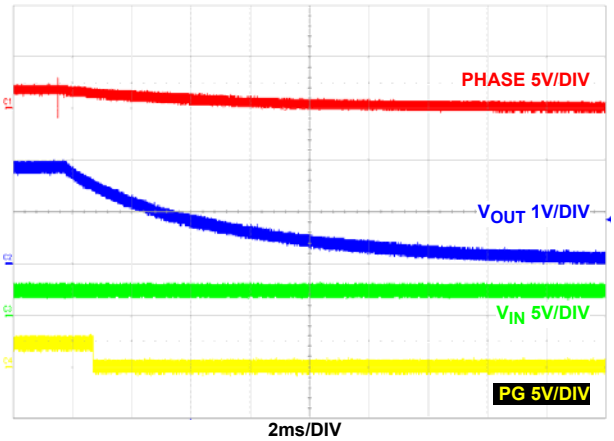


FIGURE 37. SHUTDOWN VIN AT NO LOAD (PFM)

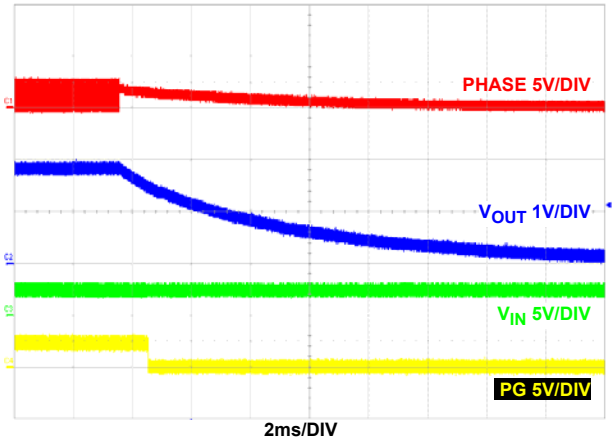


FIGURE 38. SHUTDOWN VIN AT NO LOAD (PWM)

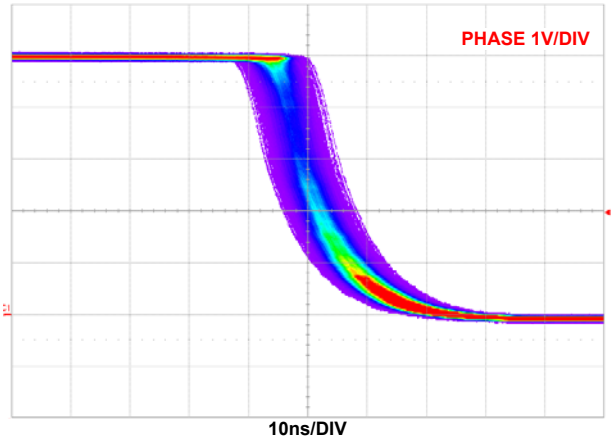


FIGURE 39. JITTER AT NO LOAD PWM

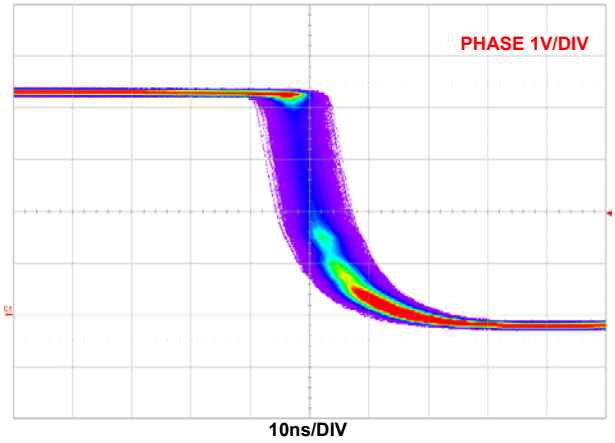


FIGURE 40. JITTER AT FULL LOAD PWM

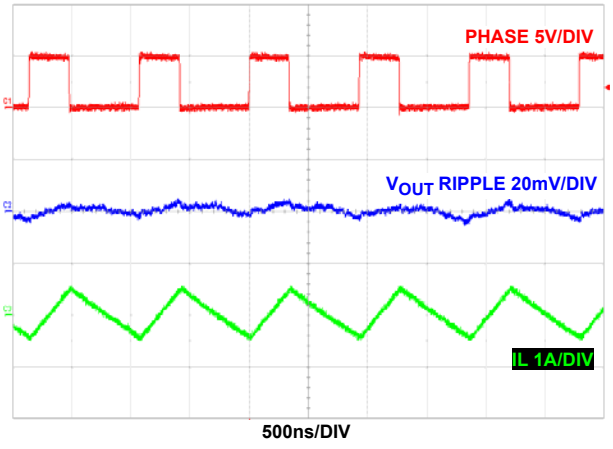


FIGURE 41. STEADY STATE AT NO LOAD PWM

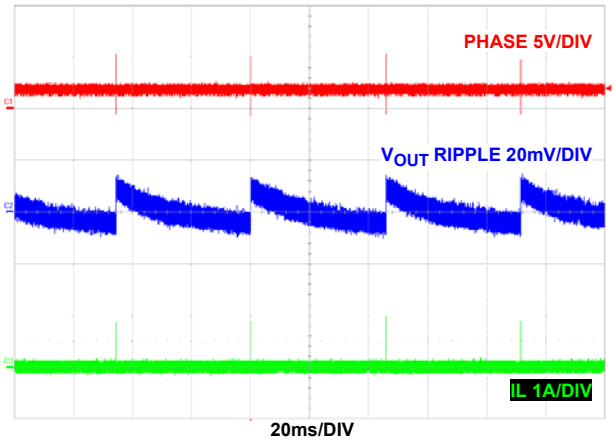


FIGURE 42. STEADY STATE AT NO LOAD PFM

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 6A. Resistor load is used in the test. **(Continued)**

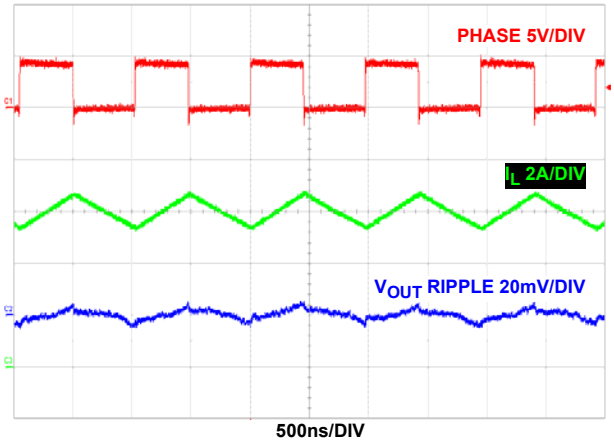


FIGURE 43. STEADY STATE AT 6A PWM

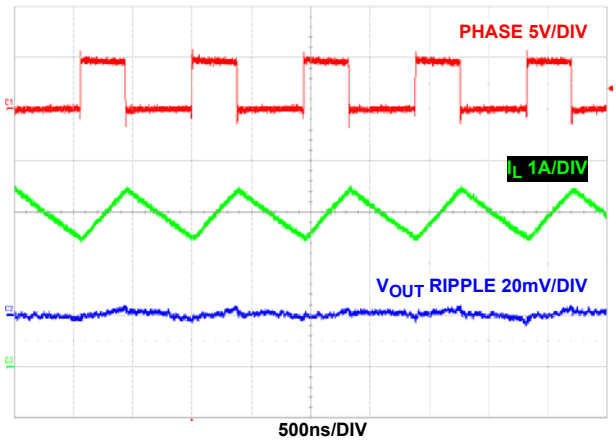


FIGURE 44. STEADY STATE AT 3A PFM

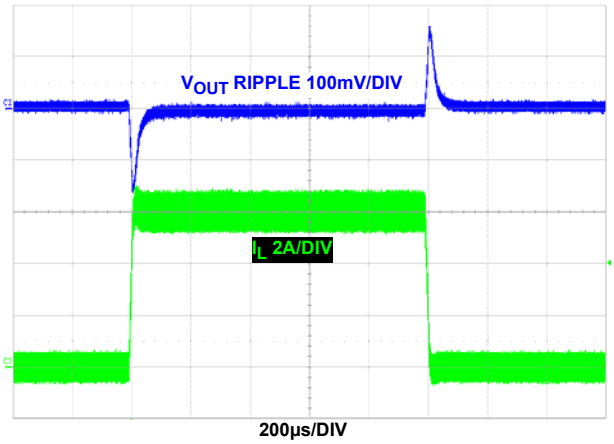


FIGURE 45. LOAD TRANSIENT (PWM)

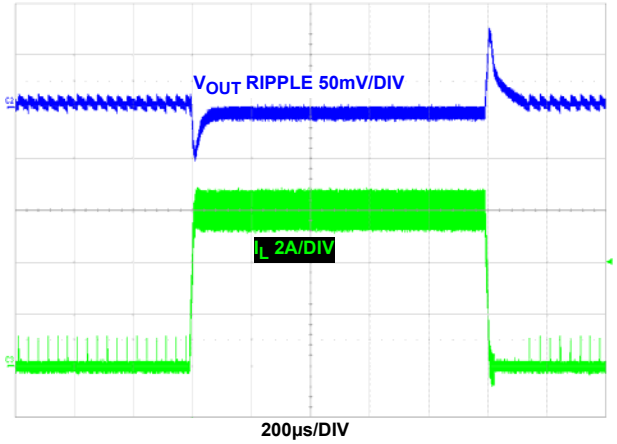


FIGURE 46. LOAD TRANSIENT (PFM)

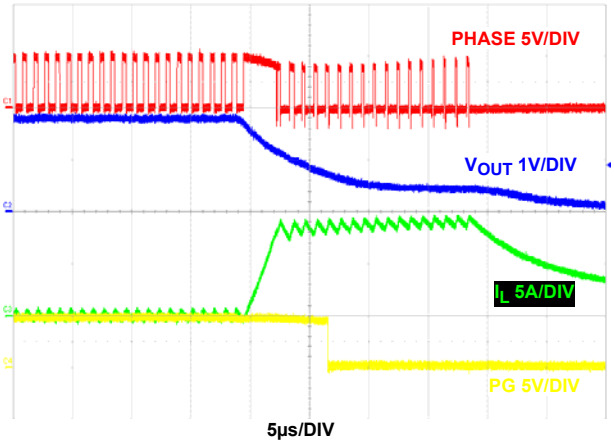


FIGURE 47. OUTPUT SHORT-CIRCUIT

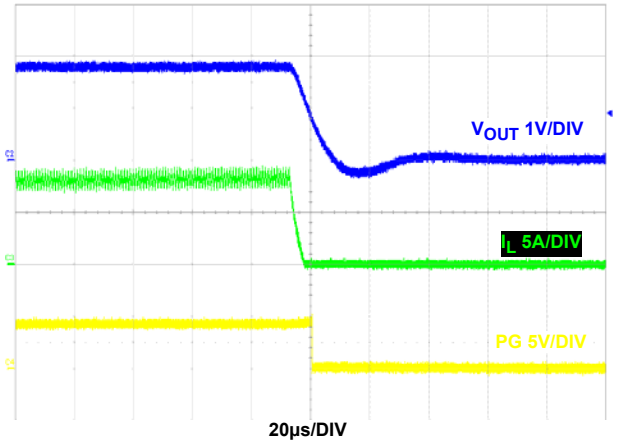


FIGURE 48. OVERCURRENT PROTECTION

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 6A. Resistor load is used in the test. **(Continued)**

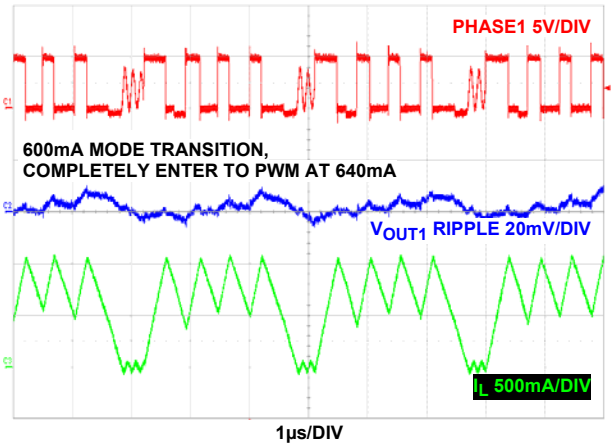


FIGURE 49. PFM TO PWM TRANSITION

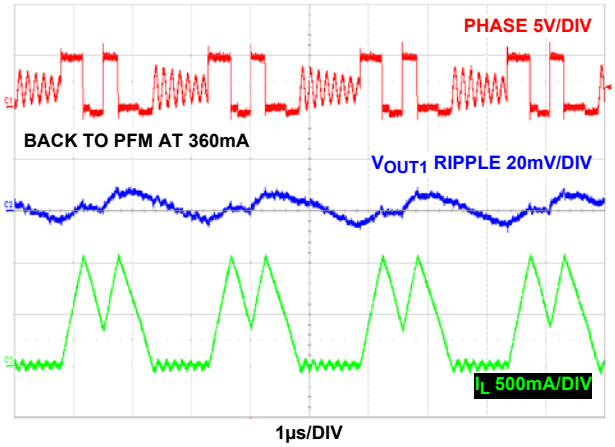


FIGURE 50. PWM TO PFM TRANSITION

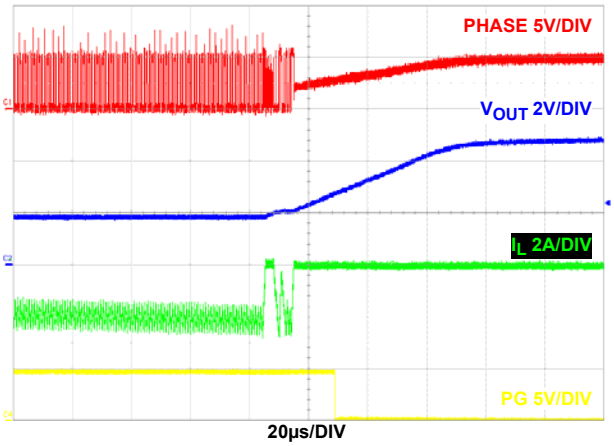


FIGURE 51. OVERVOLTAGE PROTECTION

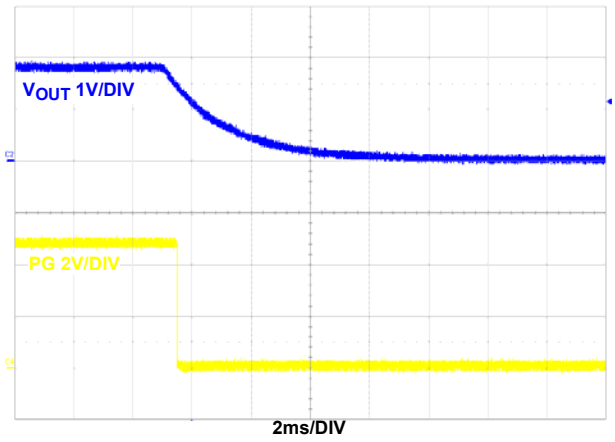


FIGURE 52. OVER-TEMPERATURE PROTECTION

Theory of Operation

The ISL8026, ISL8026A are step-down switching regulators optimized for battery-powered applications. The regulators operate at a 1MHz or 2MHz fixed default switching frequency for high efficiency and allow smaller form factor when FS is connected to VIN. By connecting a resistor from FS to SGND, the operational frequency adjustable range is 500kHz to 4MHz. At light load, the regulator reduces the switching frequency, unless forced to the fixed frequency, to minimize the switching loss and to maximize the battery life. The quiescent current when the output is not loaded is typically only 50µA. The supply current is typically only 5µA when the regulator is shut down.

PWM Control Scheme

Pulling the SYNC pin HI (>0.8V) forces the converter into PWM mode, regardless of output current. The ISL8026, ISL8026A employs the current-mode Pulse-width Modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 3 on page 5 shows the functional block diagram. The current loop consists of the oscillator, the PWM comparator, current sensing circuit and the slope compensation for the current loop stability. The slope compensation is 440mV/Ts, which changes with frequency. The gain for the current sensing circuit is typically 140mV/A. The control reference for the current loops comes from the Error Amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-Channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier, CSA, and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-FET and turn on the N-channel MOSFET. The N-FET stays on until the end of the PWM cycle. Figure 53 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the Current-Sense Amplifier's (CSA) output.

The output voltage is regulated by controlling the V_{EAMP} voltage to the current loop. The bandgap circuit outputs a 0.6V reference voltage to the voltage loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and will be discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 55pF and 100kΩ RC network. The maximum EAMP voltage output is precisely clamped to 1.6V.

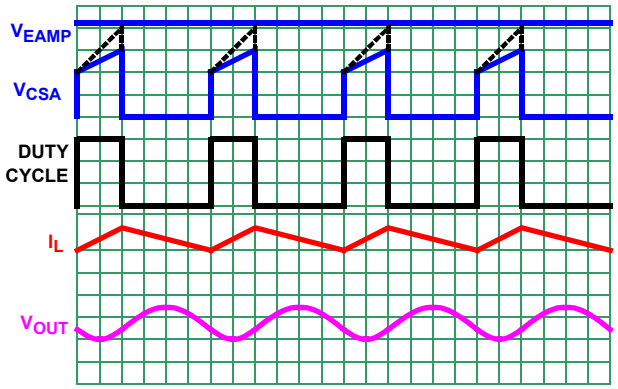


FIGURE 53. PWM OPERATION WAVEFORMS

SKIP Mode

Pulling the SYNC pin LOW (<0.4V) forces the converter into PFM mode. The ISL8026, ISL8026A enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 54 illustrates the skip mode operation. A zero-cross sensing circuit shown in Figure 3 on page 5 monitors the N-FET current for zero crossing. When 16 consecutive cycles are detected, the regulator enters the Skip mode. During the sixteen detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

Once the skip mode is entered, the pulse modulation starts being controlled by the Skip comparator shown in Figure 3 on page 5. Each pulse cycle is still synchronized by the PWM clock. The P-FET is turned on at the clock's rising edge and turned off when the output is higher than 1.2% of the nominal regulation or when its current reaches the peak skip current limit value. Then, the inductor current is discharged to 0A and stays at zero (the internal clock is disabled) and the output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-FET will be turned on again at the rising edge of the internal clock as it repeats the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 2.5% below the nominal voltage.

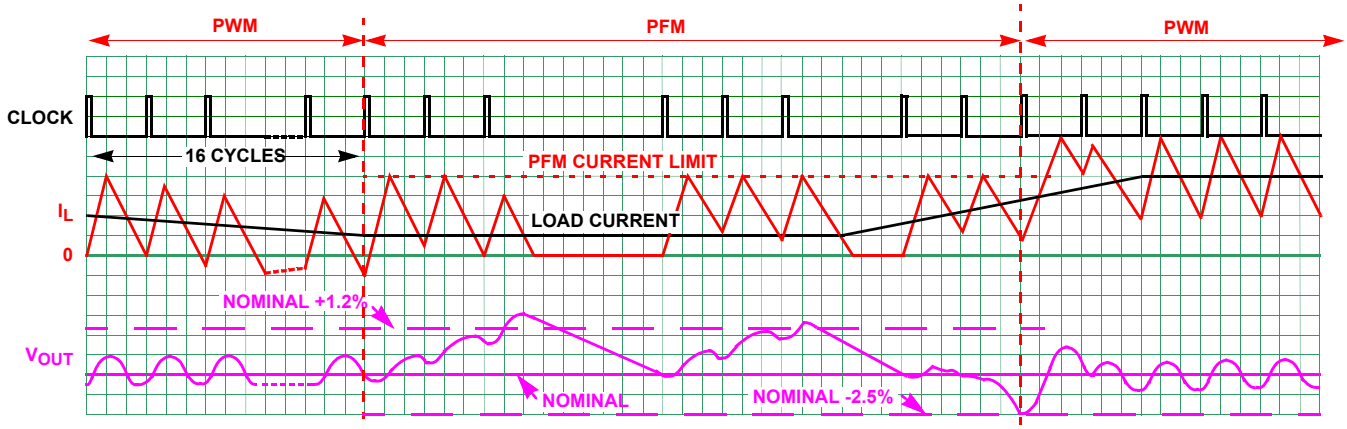


FIGURE 54. SKIP MODE OPERATION WAVEFORMS

Frequency Adjust

The frequency of operation is fixed at 1MHz for ISL8026, 2MHz for ISL8026A when FS is tied to VIN. Adjustable frequency ranges from 500kHz to 4MHz via a simple resistor connecting FS to SGND, according to Equation 2:

$$R_{FS}[k\Omega] = \frac{220 \cdot 10^3}{f_{OSC}[kHz]} - 14 \quad \text{(EQ. 2)}$$

Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 3 on page 5. The current sensing circuit has a gain of 140mV/A, from the P-FET current to the CSA output. When the CSA output reaches the threshold, the OCP comparator is tripled to turn off the P-FET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of an overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the overcurrent fault counter is set to 1. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter will be incremented. If there are 17 sequential OC fault detections, the regulator will be shut down under an overcurrent fault condition. An overcurrent fault condition will result in the regulator attempting to restart in a hiccup mode within the delay of eight soft-start periods. At the end of the 8^{th} soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away during the delay of 8 soft-start periods, the output will resume back into regulation after hiccup mode expires.

Negative Current Protection

Similar to overcurrent, the negative current protection is realized by monitoring the current across the low-side N-FET, as shown in Figure 3 on page 5. When the valley point of the inductor current reaches -3A for 4 consecutive cycles, both P-FET and N-FET are turned off. The 100Ω in parallel to the N-FET will activate discharging the output into regulation. The control will begin to switch when output is within regulation. The regulator will be in PFM for 20µs before switching to PWM, if necessary.

PG

PG is an open-drain output of a window comparator that continuously monitors the buck regulator output voltage. PG is actively held low when EN is low and during the buck regulator soft-start period. After 1ms delay of the soft-start period, PG becomes high impedance as long as the output voltage is within the nominal regulation voltage set by VFB. When VFB drops 15% below or raises 0.8V above the nominal regulation voltage, the ISL8026, ISL8026A pulls PG low. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start. For logic level output voltages, connect an external pull-up resistor, R_1, between PG and VIN. A 100kΩ resistor works well in most applications.

UVLO

When the input voltage is below the Undervoltage Lockout (UVLO) threshold, the regulator is disabled.

Soft Start-Up

The soft start-up reduces the inrush current during the start-up. The soft-start block outputs a ramp reference to the input of the error amplifier. This voltage ramp limits the inductor current as well as the output voltage speed, so that the output voltage rises in a controlled fashion. When VFB is less than 0.1V at the beginning of the soft-start, the switching frequency is reduced to 200kHz, so that the output can start-up smoothly at light load condition. During soft-start, the IC operates in the Skip mode to support prebiased output condition.

Tie SS to SGND for internal soft-start, which is approximately 1ms. Connect a capacitor from SS to SGND to adjust the soft-start time. This capacitor, along with an internal 1.85µA current source sets the soft-start interval of the converter, t_{SS}, as shown by Equation 3.

$$C_{SS}[\mu F] = 3.1 \cdot t_{SS}[s] \quad \text{(EQ. 3)}$$

C_{SS} must be less than 33nF to insure proper soft-start reset after fault condition.

Enable

The Enable (EN) input allows the user to control the turning on or off of the regulator for purposes such as power-up sequencing. When the regulator is enabled, there is typically a 600µs delay for waking up the bandgap reference and then the soft start-up begins.

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs or the VIN UVLO is set, the outputs discharge to GND through an internal 100Ω switch.

Power MOSFETs

The power MOSFETs are optimized for best efficiency. The ON-resistance for the P-FET is typically 36mΩ and the ON-resistance for the N-FET is typically 13mΩ.

100% Duty Cycle

The ISL8026, ISL8026A features a 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL8026, ISL8026A can no longer maintain the regulation at the output, the regulator completely turns on the P-FET. The maximum dropout voltage under the 100% duty cycle operation is the product of the load current and the ON-resistance of the P-FET.

Thermal Shutdown

The ISL8026, ISL8026A has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shut down. As the temperature drops to +125°C, the ISL8026, ISL8026A resumes operation by stepping through the soft-start.

Power Derating Characteristics

To prevent the regulator from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by Equation 4:

$$T_{RISE} = (PD)(\theta_{JA}) \quad \text{(EQ. 4)}$$

Where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by Equation 5:

$$T_J = (T_A + T_{RISE}) \quad \text{(EQ. 5)}$$

Where T_A is the ambient temperature. For the TQFN package, the θ_{JA} is 47 (°C/W).

The actual junction temperature should not exceed the absolute maximum junction temperature of +125°C when considering the thermal design.

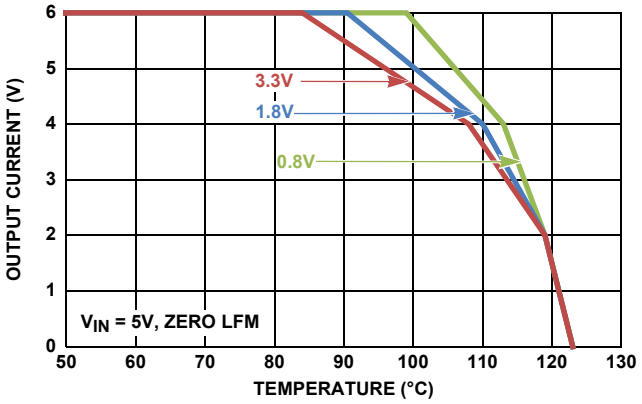


FIGURE 55. DERATING CURVE vs TEMPERATURE

Application Information

Output Inductor and Capacitor Selection

To consider steady state and transient operations, the ISL8026 typically uses a 1.0µH output inductor and the ISL8026A uses a 0.68µH output inductor. The higher or lower inductor value can be used to optimize the total converter system performance. For example, for a higher output voltage 3.3V application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. It is recommended to set the ripple inductor current approximately 30% of the maximum output current for optimized performance. The inductor ripple current can be expressed, as shown in Equation 6:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_S} \quad \text{(EQ. 6)}$$

The inductor's saturation current rating needs to be at least larger than the peak current. The ISL8026, ISL8026A protects the typical peak current 9A. The saturation current needs to be over 10A for maximum output current application.

The ISL8026, ISL8026A uses an internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended X5R or X7R minimum output capacitor values are shown in Table 3 on page 4.

In Table 3, the minimum output capacitor value is given for the different output voltages to ensure that the whole converter system is stable. Additional output capacitance should be added for better performance in applications where high load transient or low output ripple is required. It is recommended to check the system level performance along with the simulation model.

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage, relative to the internal reference voltage, and feed it back to the inverting input of the error amplifier (refer to Figure 1 on page 1).

The output voltage programming resistor, R_2, will depend on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor, R_3, is typically between 10kΩ and 100kΩ, as shown in Equation 7.

$$R_2 = R_3\left(\frac{V_O}{VFB} - 1\right) \quad \text{(EQ. 7)}$$

If the output voltage desired is 0.6V, then R_3 is left unpopulated and R_2 is shorted. There is a leakage current from V_{IN} to PHASE. It is recommended to preload the output with 10µA minimum. For better performance, add 22pF in parallel with R_2 (200kΩ). Check loop analysis before use in application.

Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and provide a filtering function to prevent the switching current flowing back to the battery rail. At least two 22µF X5R or X7R ceramic capacitors are a good starting point for the input capacitor selection.

Loop Compensation Design

When COMP is not connected to VIN, the COMP pin is active for external loop compensation. The ISL8026, ISL8026A uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant and the system becomes a single order system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 56 on page 20 shows the small signal model of the synchronous buck regulator.

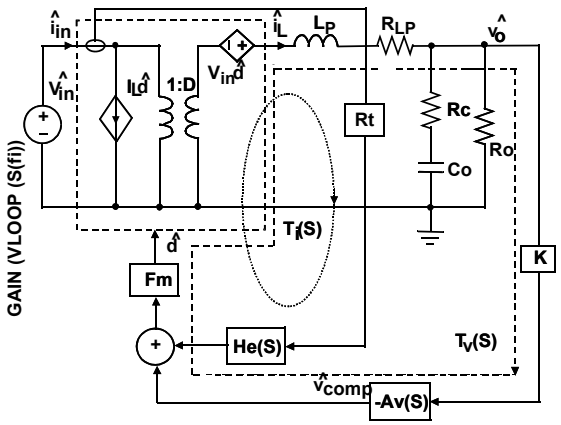


FIGURE 56. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

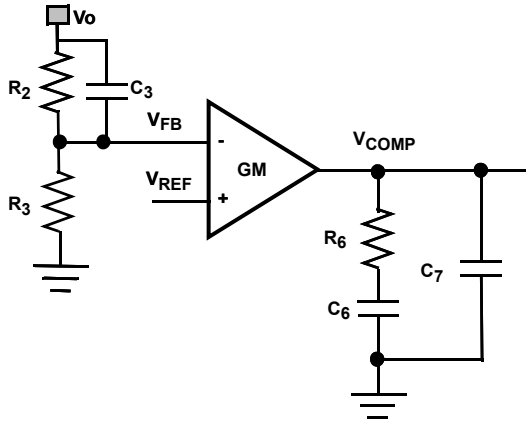


FIGURE 57. TYPE II COMPENSATOR

Figure 57 shows the type II compensator and its transfer function is expressed as shown in Equation 8:

$$A_V(S) = \frac{\hat{v}_{comp}}{\hat{v}_{FB}} = \frac{GM \cdot R_3}{(C_6 + C_7) \cdot (R_2 + R_3)} \frac{\left(1 + \frac{S}{\omega_{cz1}}\right)\left(1 + \frac{S}{\omega_{cz2}}\right)}{S\left(1 + \frac{S}{\omega_{cp1}}\right)\left(1 + \frac{S}{\omega_{cp2}}\right)} \quad \text{(EQ. 8)}$$

Where,

$$\omega_{cz1} = \frac{1}{R_6 C_6}, \quad \omega_{cz2} = \frac{1}{R_2 C_3}, \omega_{cp1} = \frac{C_6 + C_7}{R_6 C_6 C_7}, \omega_{cp2} = \frac{R_2 + R_3}{C_3 R_2 R_3}$$

Compensator design goal:

High DC gain

Choose loop bandwidth f_c less than 100kHz

Gain margin: >10dB

Phase margin: >40°

The compensator design procedure is as follows:

The loop gain at crossover frequency of f_c has a unity gain. Therefore, the compensator resistance R_6 is determined by Equation 9.

$$R_6 = \frac{2\pi f_c V_o C_o R_t}{GM \cdot V_{FB}} = 12.2 \times 10^3 \cdot f_c V_o C_o \quad \text{(EQ. 9)}$$

Where GM is the sum of the transconductance, g_m, of the voltage error amplifier in each phase. Compensator capacitor C_6 is then given by Equation 10.

$$C_6 = \frac{R_o C_o}{R_6} = \frac{V_o C_o}{I_o R_6}, C_7 = \max\left(\frac{R_c C_o}{R_6}, \frac{1}{\pi f_s R_6}\right) \quad \text{(EQ. 10)}$$

Put one compensator pole at zero frequency to achieve high DC gain, and put another compensator pole at either ESR zero frequency or half switching frequency, whichever is lower in Equation 10. An optional zero can boost the phase margin. ω_{CZ2} is a zero due to R_2 and C_3.

Put compensator zero 2 to 5 times f_c.

$$C_3 = \frac{1}{\pi f_c R_2} \quad \text{(EQ. 11)}$$

Example: V_{IN} = 5V, V_O = 1.8V, I_O = 6A, f_{sw} = 1MHz, R_2 = 200kΩ, R_3 = 100kΩ, C_o = 2x22µF/3mΩ, L = 1µH, f_c = 100kHz, then compensator resistance R_6:

$$R_6 = 12.2 \times 10^3 \cdot 100\text{kHz} \cdot 1.8\text{V} \cdot 44\mu\text{F} = 97.6\text{k}\Omega \quad \text{(EQ. 12)}$$

$$C_6 = \frac{1.8\text{V} \cdot 44\mu\text{F}}{6\text{A} \cdot 97.6\text{k}\Omega} = 135\text{pF} \quad \text{(EQ. 13)}$$

$$C_7 = \max\left(\frac{3\text{m}\Omega \cdot 44\mu\text{F}}{97.6\text{k}\Omega}, \frac{1}{\pi \cdot 1\text{MHz}(97.6\text{k}\Omega)}\right) = (1\text{pF}, 3.3\text{pF}) \quad \text{(EQ. 14)}$$

It is also acceptable to use the closest standard values for C_6 and C_7. There is approximately 3pF parasitic capacitance from V_{COMP} to GND. Therefore, C_7 is optional. Use C_6 = 150pF and C_7 = OPEN.

$$C_3 = \frac{1}{\pi 100\text{kHz} \cdot 200\text{k}\Omega} = 16\text{pF} \quad \text{(EQ. 15)}$$

Use C_3 = 15pF. Note that C_3 may increase the loop bandwidth from previous estimated value. Figure 58 on page 21 shows the simulated voltage loop gain. It is shown that it has a 150kHz loop bandwidth with a 42° phase margin and 10dB gain margin. It may be more desirable to achieve an increased phase margin. This can be accomplished by lowering R_6 by 20% to 30%.

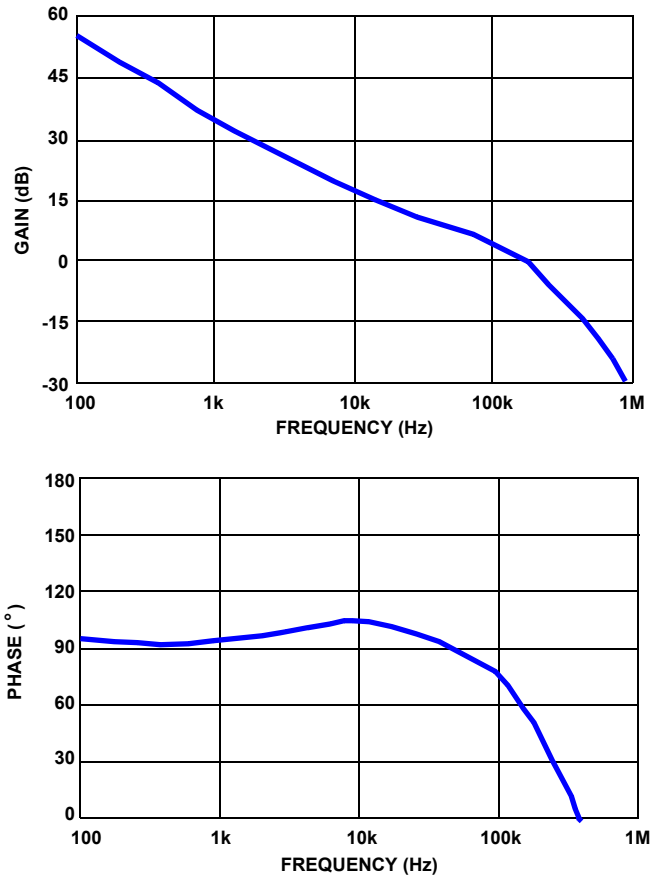


FIGURE 58. SIMULATED LOOP GAIN

PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well. For the ISL8026, ISL8026A, the power loop is composed of the output inductor L's, the output capacitor (C_{OUT}), the PHASE pins and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the PHASE pins and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as close as possible to the VIN pin. The ground of input and output capacitors should be connected as close as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least 5 vias ground connection within the pad for the best thermal relief.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
October 28, 2016	FN8736.2	On page 1, last paragraph - converted - 0.22in^2 to 142mm^2. Added “1.5% reference accuracy over load/line/temperature (-40°C to +125°C)” to Features section on page 1. Updated Ordering Information table on page 4: Added 2 parts - ISL8026FRTAJZ and ISL8026AFRTAJZ Removed “-T” from bulk parts and added Tape and Reel unit options to Note 1. Updated Recommended Operating Conditions: Added full-range industrial temperature range Electrical Spec table updates: Reference Voltage added temp -40°C < T_J < +85°C and added row for -40°C < Tj < +125°C Transresistance - Added temp -40°C < T_J < +85°C and added row for temperature -40°C < T_J < +125°C Nominal Switching Frequency - added temperature -40°C < Tj < +85°C and added row for temperature -40°C < T_J < +125°C
June 26, 2015	FN8736.1	Updated the 4th Features bullet by changing from 1.2% to 1% and adding temperature range. Updated Applications bullets. on page 1. Added Related Literature section. Added evaluation boards to Ordering Information table on page 4. In “Electrical Specifications” on page 6, updated min/max specs for Reference Voltage parameter (min) from”0.593” to “0.594” and (max) from “0.607” to “0.606”. Updated Equation 9 and Equations 12 through 14 on page 20. Updated example I_O information from “5A” to “6A” on page 20.
May 13, 2015	FN8736.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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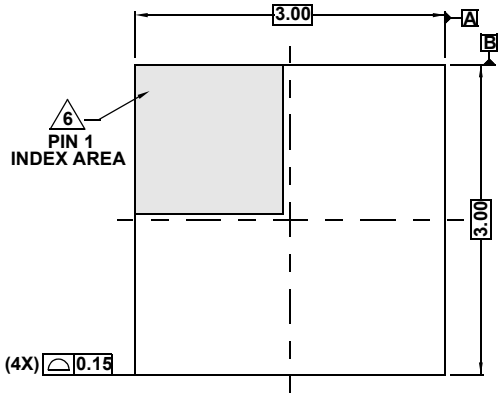
Package Outline Drawing

For the most recent package outline drawing, see L16.3x3D.

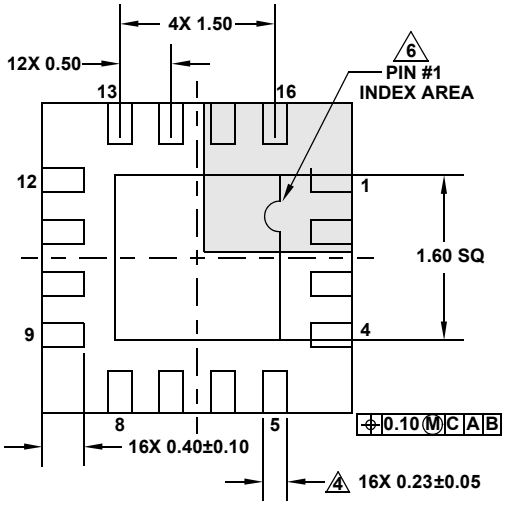
L16.3x3D

16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

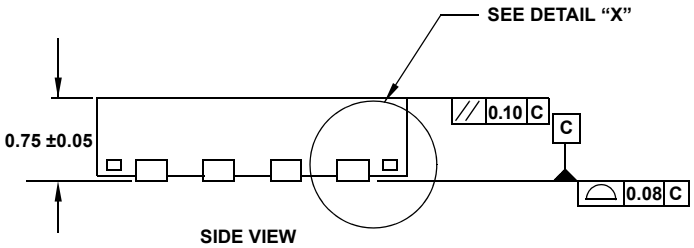
Rev 0, 3/10



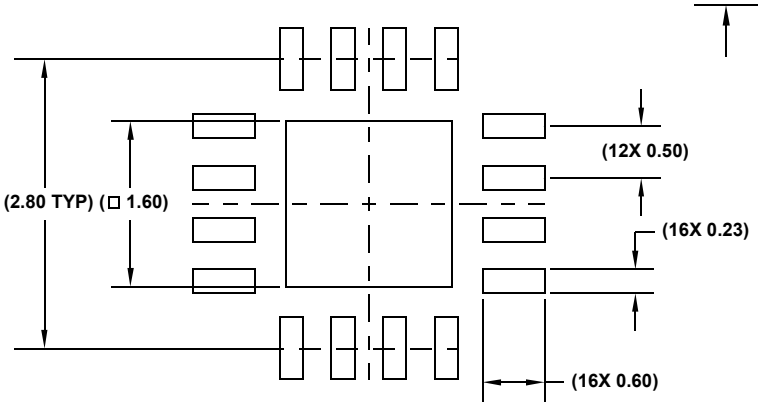
TOP VIEW



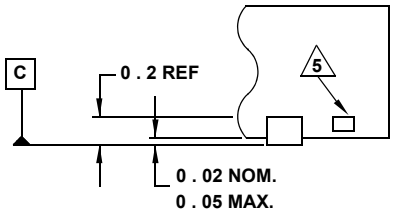
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220 WEED.

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