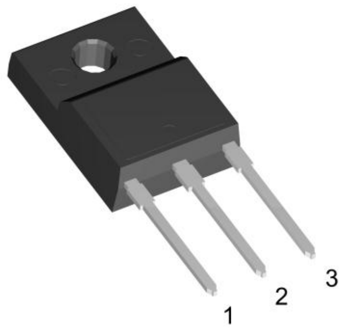
STFH12N150K5

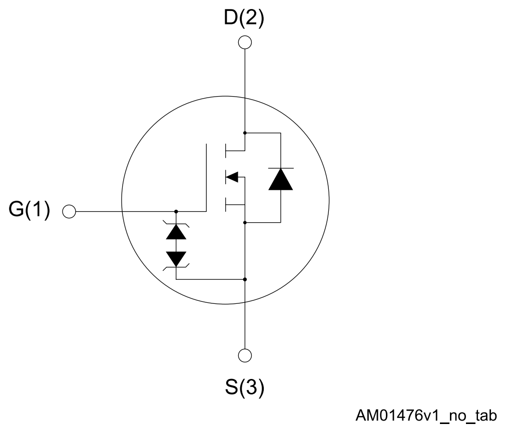
N-channel 1500 V, 1.6 Ω typ.,7 A MDmesh™ K5 Power MOSFET in a TO-220FP wide creepage package

Datasheet - preliminary data



TO-220FP wide creepage

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STFH12N150K5	1500 V	1.9 Ω	7 A	40 W

- Industry's lowest $R_{DS(on)}$ * area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected
- Wide creepage distance of 4.25 mm between the pins

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

The TO-220FP wide creepage package provides increased surface insulation for Power MOSFETs to prevent failure due to arcing, which can occur in polluted environments.

Table 1: Device summary

Order code	Marking	Package	Packing
STFH12N150K5	12N150K5	TO-220FP wide creepage	Tube

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current at T_C = 25 °C	7	A
I_D	Drain current at T_C = 100 °C	4	A
I_{DM}[(1)]	Drain current (pulsed)	28	A
P_{TOT}	Total dissipation at T_C = 25 °C	40	W
dv/dt [(2)]	Peak diode recovery voltage slope	4.5	V/ns
dv/dt [(3)]	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2500	V
T_j	Operating junction temperature range	- 55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

[(1)]Pulse width limited by safe operating area

[(2)]I_{SD} ≤ 7 A, di/dt ≤ 100 A/µs, V_{Peak} ≤ $V_{(BR)DSS}$

[(3)]V_{DS} ≤ 1200 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3.1	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb	62.5	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Max current during repetitive or single pulse avalanche	2	A
E_{AS}	Single pulse avalanche energy	900	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1500			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1500 V			1	µA
		V_{GS} = 0 V, V_{DS} = 1500 V, Tc=125 °C[(1)]			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3.5 A		1.6	1.9	Ω

Notes:

[(1)]Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 100 V,f = 1MHz	-	1360	-	pF
C_{oss}	Output capacitance		-	80	-	pF
C_{rss}	Reverse transfer capacitance		-	0.7	-	pF
$C_{o(tr)}$[(1)]	Equivalent capacitance time related	V_{DS} = 0 V to 1200 V, V_{GS} = 0 V	-	82	-	pF
$C_{o(er)}$[(2)]	Equivalent capacitance energy related		-	32	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	3	-	Ω
Q_g	Total gate charge	V_{DD} = 1200V, I_D = 7 A	-	47	-	nC
Q_{gs}	Gate-source charge	V_{GS} = 10 V	-	8	-	nC
Q_{gd}	Gate-drain charge	(see *Figure 16: "Test circuit for gate charge behavior"*)	-	32	-	nC

Notes:

[(1)]Time related is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% VDSS.

[(2)] Energy related is defined as a constant equivalent capacitance giving the same stored energy as Coss when VDS increases from 0 to 80% VDSS.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 750 V, I_D = 3.5 A, R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 18: "Unclamped inductive load test circuit"*)	-	25	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time		-	90	-	ns
t_f	Fall time		-	37	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7	A
I_{SDM}	Source-drain current (pulsed)		-		28	A
V_{SD}(1)	Forward on voltage	I_{SD} = 7 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 7 A, V_{DD} = 60 V di/dt = 100 A/µs, (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	302		ns
Q_{rr}	Reverse recovery charge		-	3.71		µC
I_{RRM}	Reverse recovery current		-	24.6		A
t_{rr}	Reverse recovery time	I_{SD} = 7 A,V_{DD} = 60 V di/dt = 100 A/µs, Tj = 150 °C (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	432		ns
Q_{rr}	Reverse recovery charge		-	4.71		µC
I_{RRM}	Reverse recovery current		-	21.8		A

Notes:

(1)Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	30	-		V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

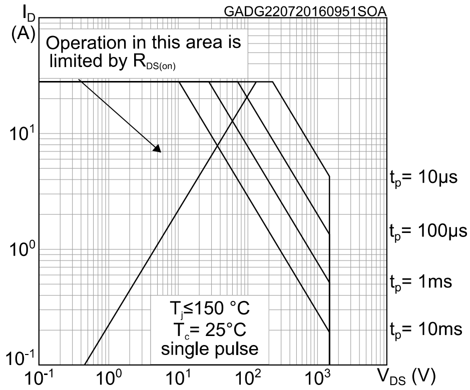


Figure 3: Thermal impedance

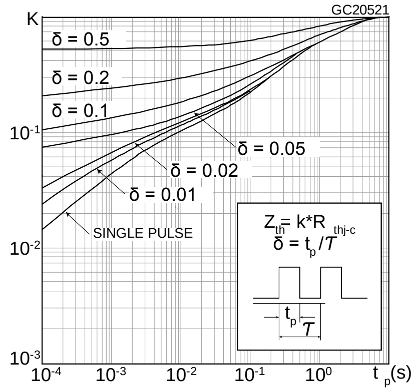


Figure 4: Output characteristics

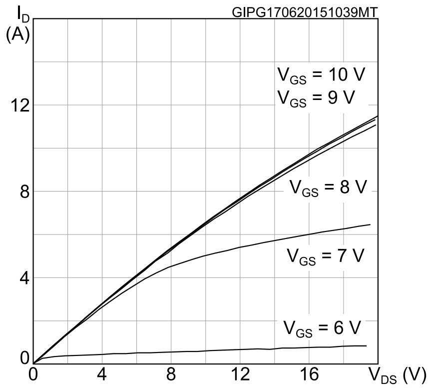


Figure 5: Transfer characteristics

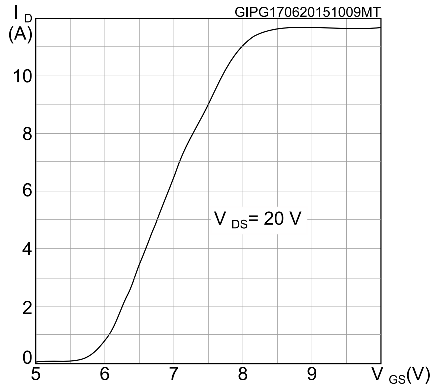


Figure 6: Gate charge vs gate-source voltage

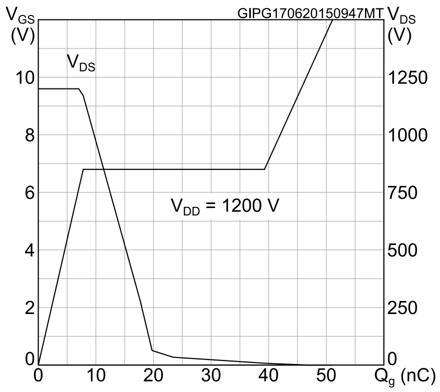


Figure 7: Static drain-source on-resistance

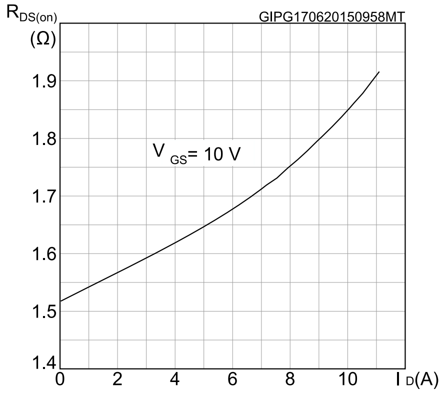


Figure 8: Capacitance variation

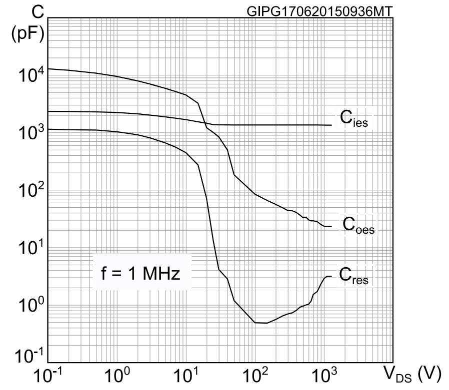


Figure 9: Output capacitance stored energy

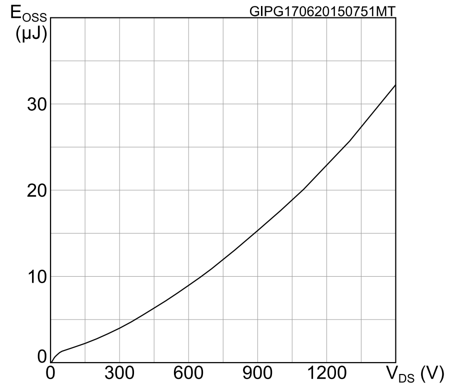


Figure 10: Normalized gate threshold voltage vs temperature

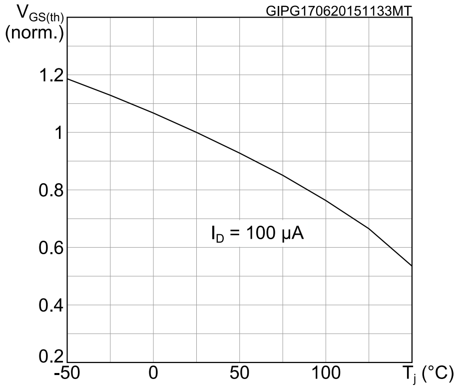


Figure 11: Normalized on-resistance vs temperature

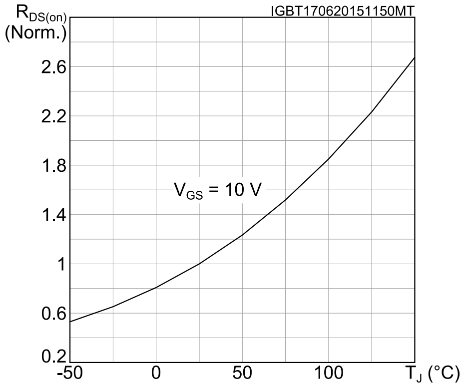


Figure 12: Normalized V(BR)DSS vs temperature

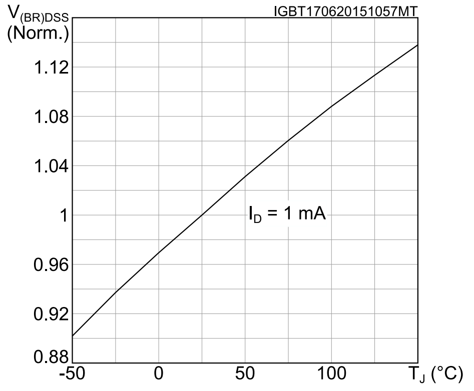


Figure 13: Source-drain diode forward characteristics

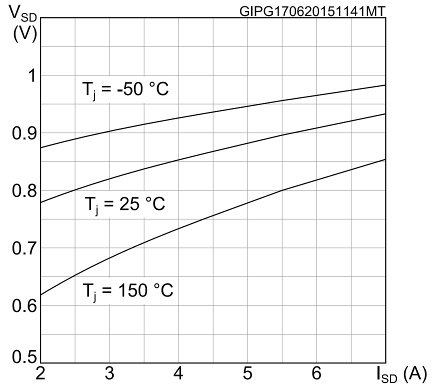
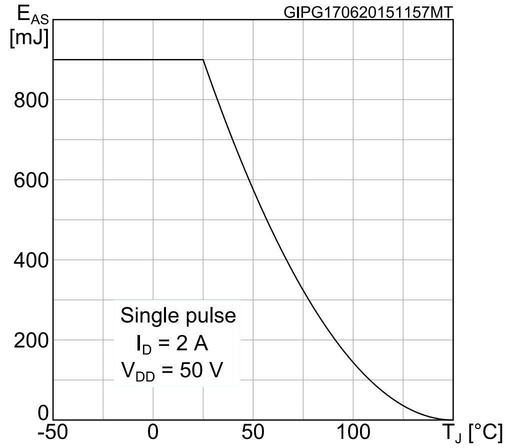


Figure 14: Maximum avalanche energy vs TJ



3 Test circuits

Figure 15: Test circuit for resistive load switching times

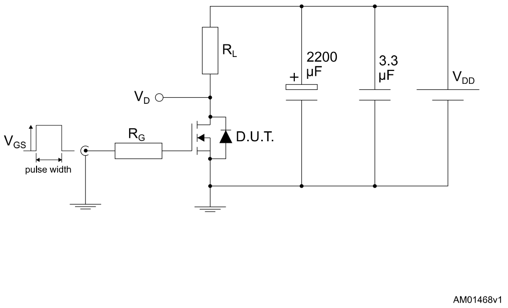


Figure 16: Test circuit for gate charge behavior

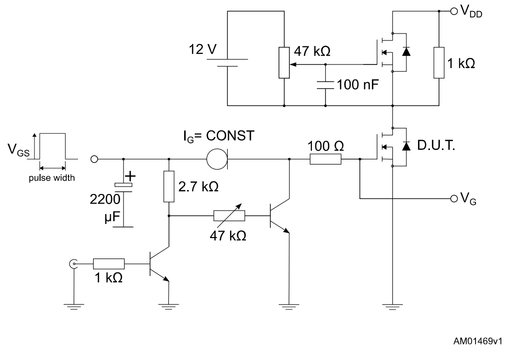


Figure 17: Test circuit for inductive load switching and diode recovery times

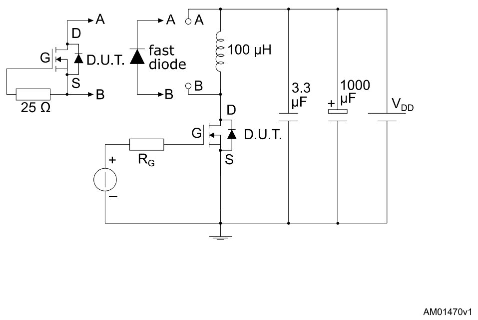


Figure 18: Unclamped inductive load test circuit

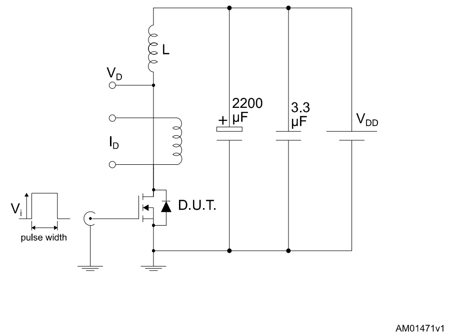


Figure 19: Unclamped inductive waveform

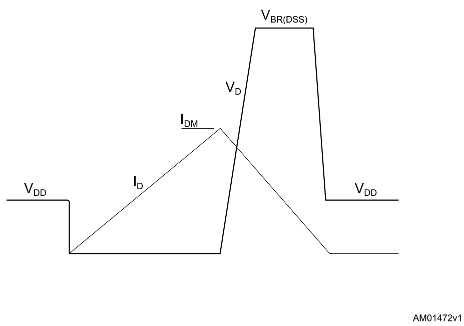
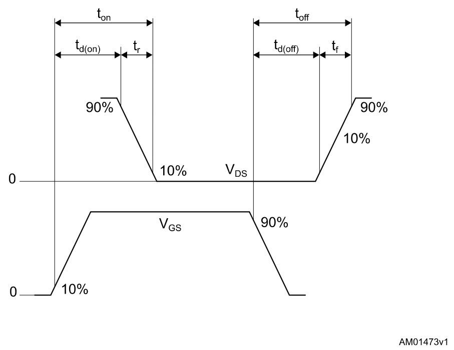


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220 wide creepage package information

Figure 21: TO-220FP wide creepage package outline

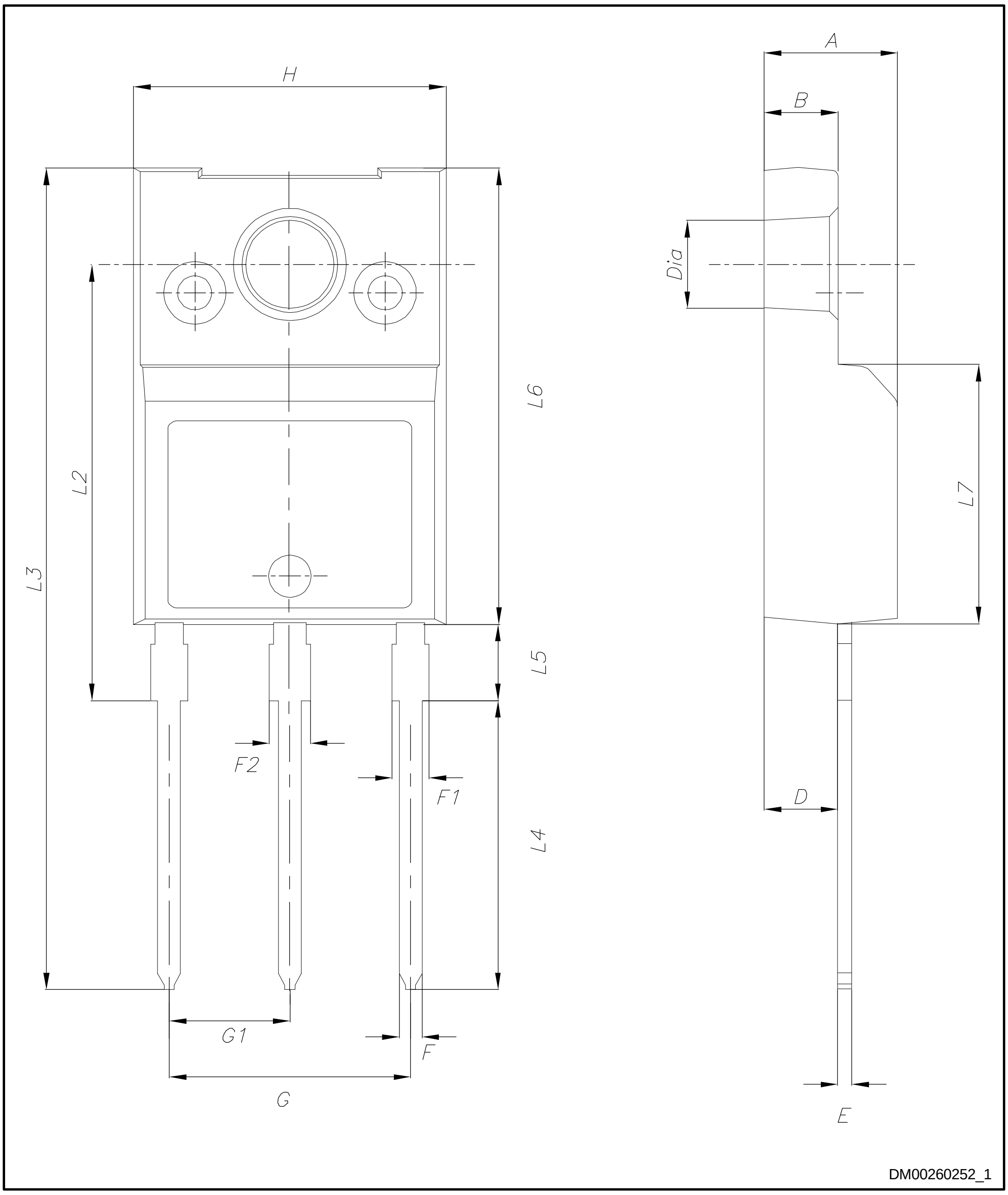


Table 10: TO-220FP wide creepage package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.60	4.70	4.80
B	2.50	2.60	2.70
D	2.49	2.59	2.69
E	0.46		0.59
F	0.76		0.89
F1	0.96		1.25
F2	1.11		1.40
G	8.40	8.50	8.60
G1	4.15	4.25	4.35
H	10.90	11.00	11.10
L2	15.25	15.40	15.55
L3	28.70	29.00	29.30
L4	10.00	10.20	10.40
L5	2.55	2.70	2.85
L6	16.00	16.10	16.20
L7	9.05	9.15	9.25
Dia	3.00	3.10	3.20

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
20-Jul-2016	1	First release.
22-Jul-2016	2	Updated *Figure 2: "Safe operating area"*.

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