

**REPETITIVE AVALANCHE AND dv/dt RATED
 HEXFET[®] TRANSISTORS
 SURFACE MOUNT (LCC-18)**

**IRFE9230
 JANTX2N6851U
 JANTXV2N6851U
 REF:MIL-PRF-19500/564
 200V, P-CHANNEL**

Product Summary

Part Number	BVDSS	RDS(on)	ID
IRFE9230	-200V	0.80Ω	-4.0A



The leadless chip carrier (LCC) package represents the logical next step in the continual evolution of surface mount technology. Designed to be a close replacement for the TO-39 package, the LCC will give designers the extra flexibility they need to increase circuit board density. International Rectifier has engineered the LCC package to meet the specific needs of the power market by increasing the size of the bottom source pad, thereby enhancing the thermal and electrical performance. The lid of the package is grounded to the source to reduce RF interference.

Features:

- Surface Mount
- Small Footprint
- Alternative to TO-39 Package
- Hermetically Sealed
- Dynamic dv/dt Rating
- Avalanche Energy Rating
- Simple Drive Requirements
- Light Weight
- ESD Rating: Class 1C per MIL-STD-750, Method 1020

Absolute Maximum Ratings

	Parameter		Units
I_D @ $V_{GS} = -10V, T_C = 25^\circ C$	Continuous Drain Current	-4.0	A
I_D @ $V_{GS} = -10V, T_C = 100^\circ C$	Continuous Drain Current	-2.4	
I_{DM}	Pulsed Drain Current ①	-16	
P_D @ $T_C = 25^\circ C$	Max. Power Dissipation	25	W
	Linear Derating Factor	0.20	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
EAS	Single Pulse Avalanche Energy ②	171	mJ
IAR	Avalanche Current ①	-4.0	A
EAR	Repetitive Avalanche Energy ①	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-1.1	V/ns
T_J	Operating Junction	-55 to 150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Pckg. Mounting Surface Temp.	300 (for 5 S)	
	Weight	0.42 (typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	V _{GS} = 0V, I _D = -1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.21	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.80	Ω	V _{GS} = -10V, I _D = -2.4A ^④
		—	—	1.68		V _{GS} = -10V, I _D = -4.0A ^④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	2.2	—	—	S	V _{DS} = -15V, I _{DS} = -2.4A ^④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V _{DS} = -160V, V _{GS} = 0V
		—	—	-250		V _{DS} = -160V V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	100	nA	V _{GS} = 20V
Q _g	Total Gate Charge	—	—	35	nC	V _{GS} = -10V, I _D = -4.0A V _{DS} = -100V
Q _{gs}	Gate-to-Source Charge	—	—	6.1		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	21		
t _{d(on)}	Turn-On Delay Time	—	—	50	ns	V _{DD} = -100V, I _D = -4.0A, R _G = 7.5Ω
t _r	Rise Time	—	—	100		
t _{d(off)}	Turn-Off Delay Time	—	—	80		
t _f	Fall Time	—	—	80		
L _S + L _D	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	700	—	pF	V _{GS} = 0V, V _{DS} = -25V f = 1.0MHz
C _{oss}	Output Capacitance	—	200	—		
C _{rss}	Reverse Transfer Capacitance	—	45	—		

Source-Drain Diode Ratings and Characteristics

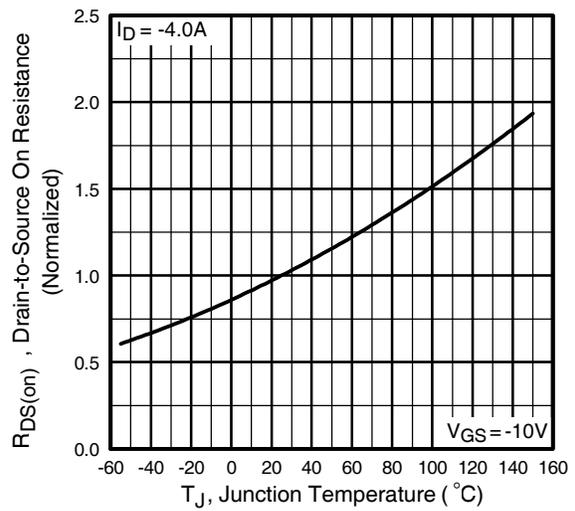
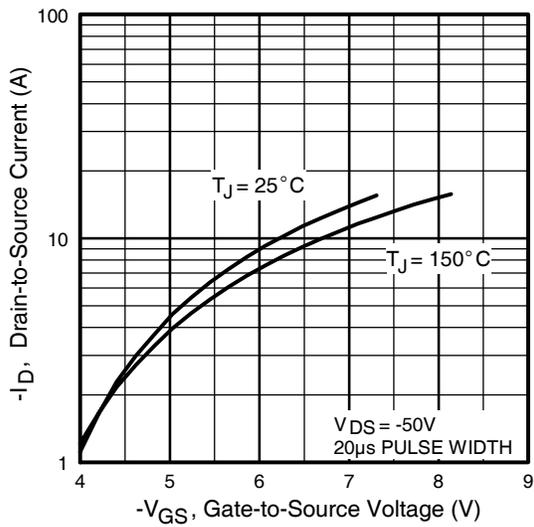
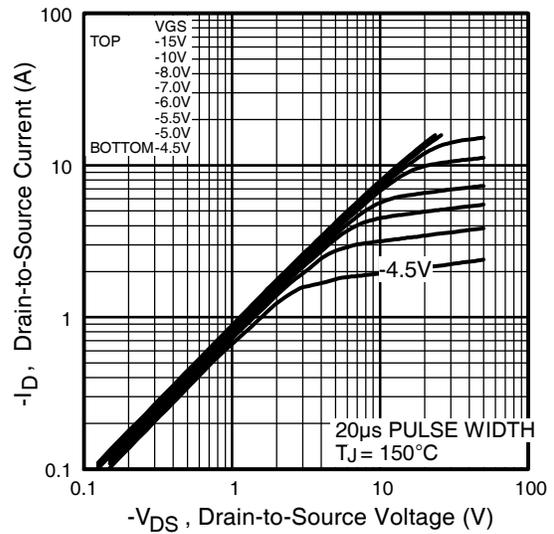
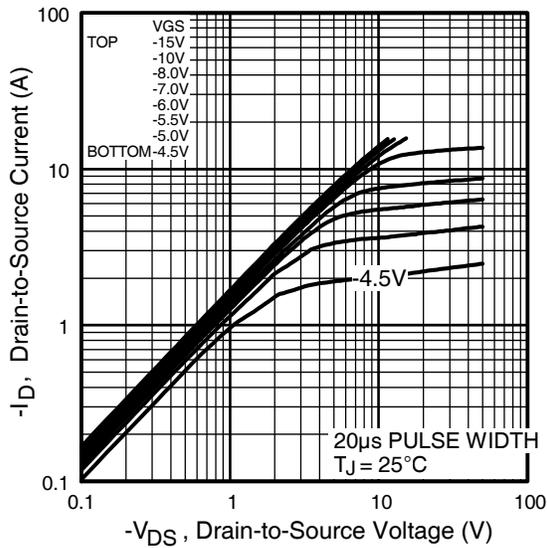
	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-4.0	A	
I _{SM}	Pulse Source Current (Body Diode) ^①	—	—	-16		
V _{SD}	Diode Forward Voltage	—	—	-5.6	V	T _j = 25°C, I _S = -4.0A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	—	400	ns	T _j = 25°C, I _F = -4.0A, di/dt ≤ 100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	4.0	μC	V _{DD} ≤ -50V ^④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction to Case	—	—	5.0	°C/W	Soldered to a copper clad PC board
R _{thJ-PCB}	Junction to PC Board	—	—	19		

Note: Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes refer to the last page



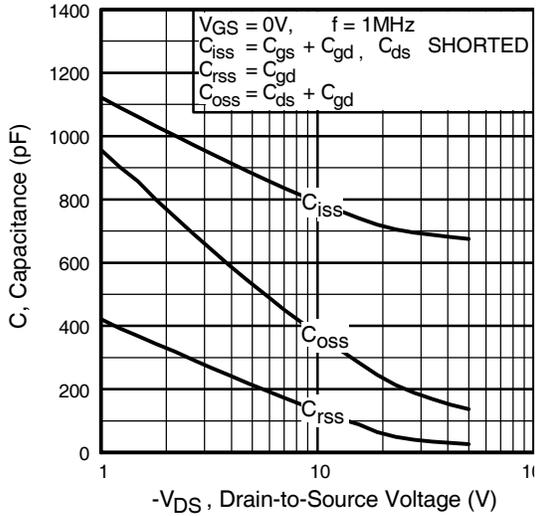


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

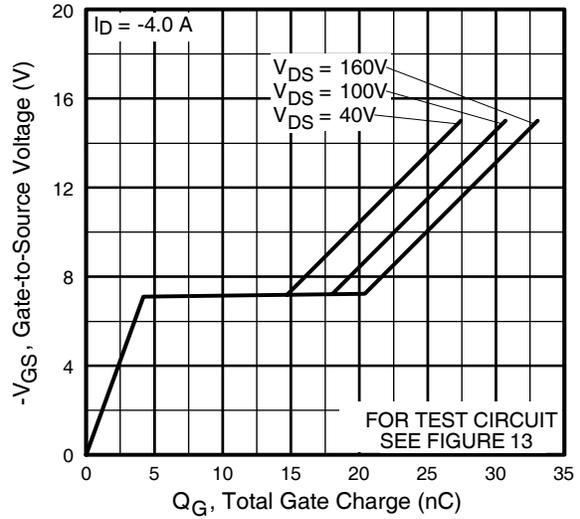


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

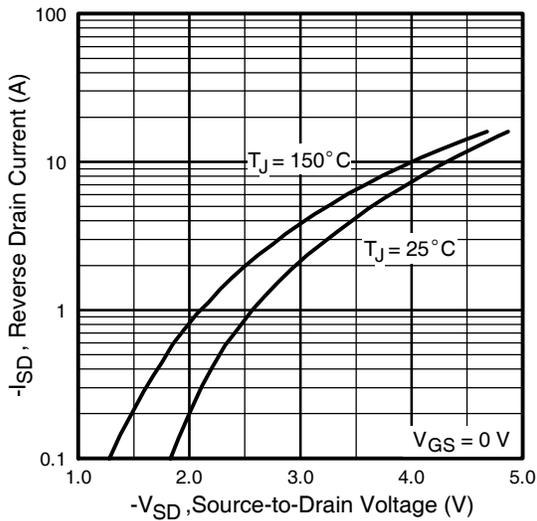


Fig 7. Typical Source-Drain Diode Forward Voltage

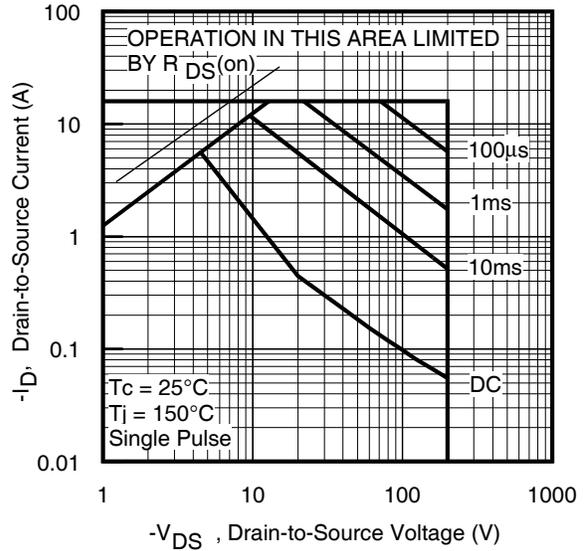


Fig 8. Maximum Safe Operating Area

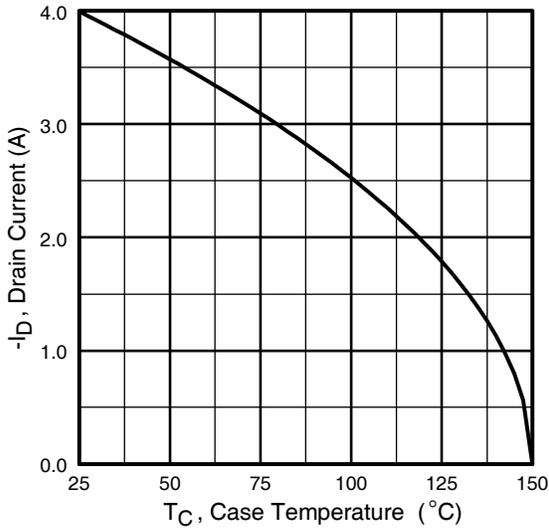


Fig 9. Maximum Drain Current Vs. Case Temperature

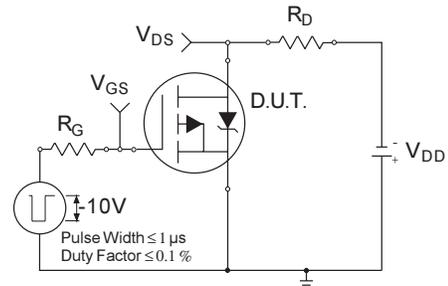


Fig 10a. Switching Time Test Circuit

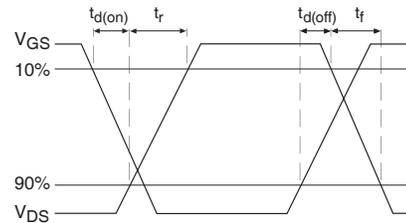


Fig 10b. Switching Time Waveforms

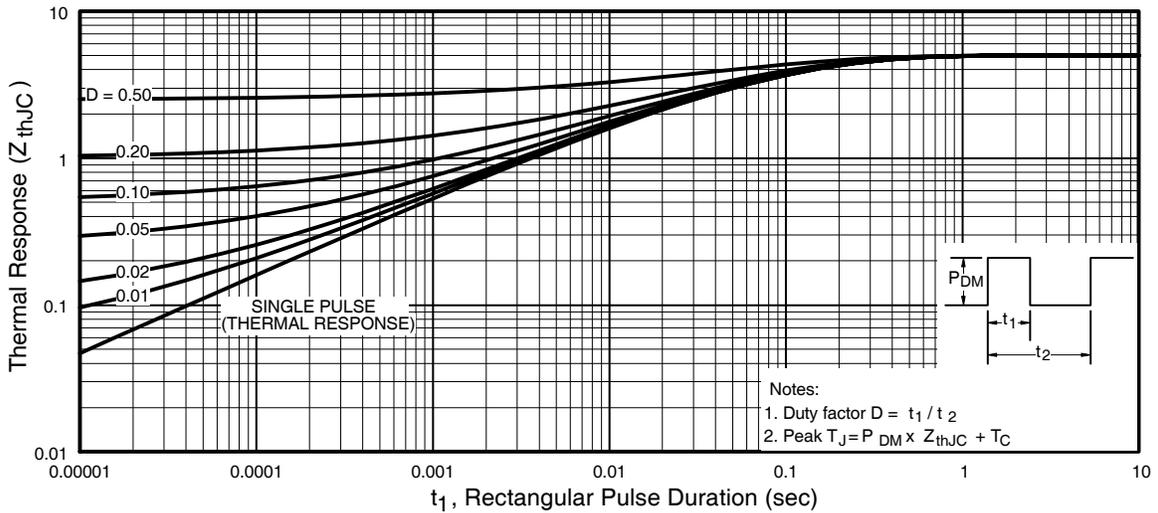


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

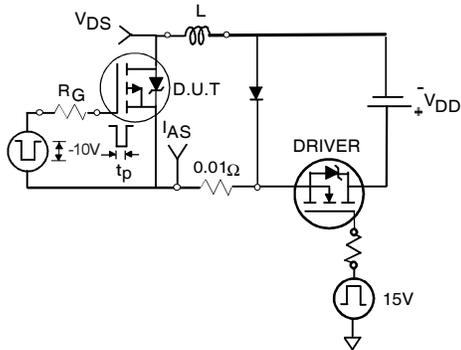


Fig 12a. Unclamped Inductive Test Circuit

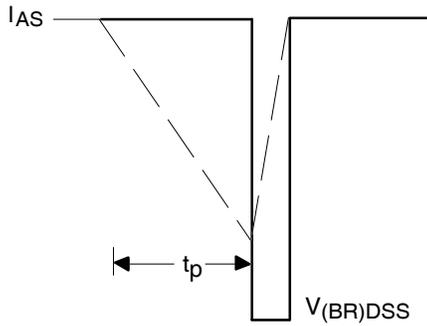


Fig 12b. Unclamped Inductive Waveforms

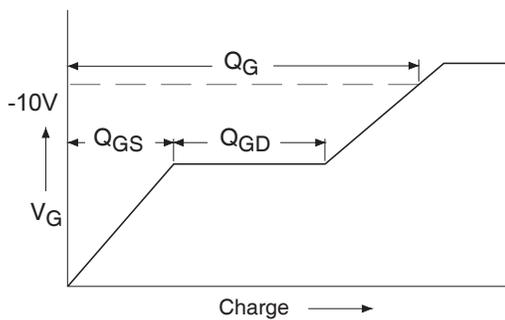


Fig 13a. Basic Gate Charge Waveform

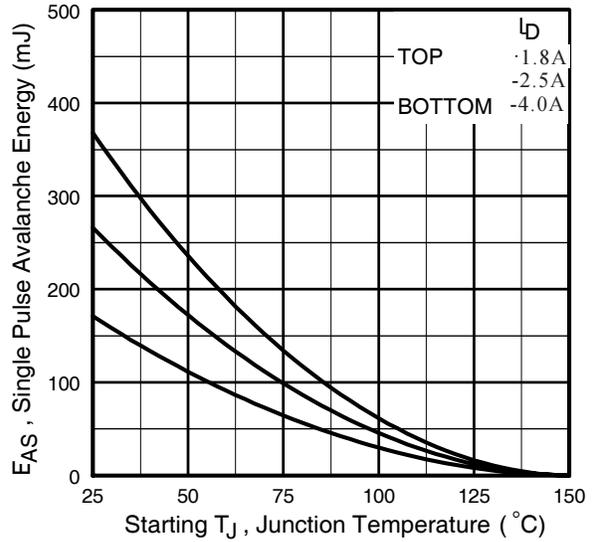


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

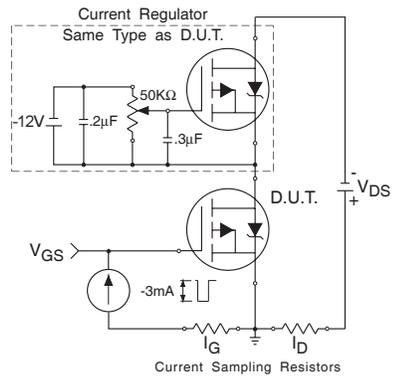
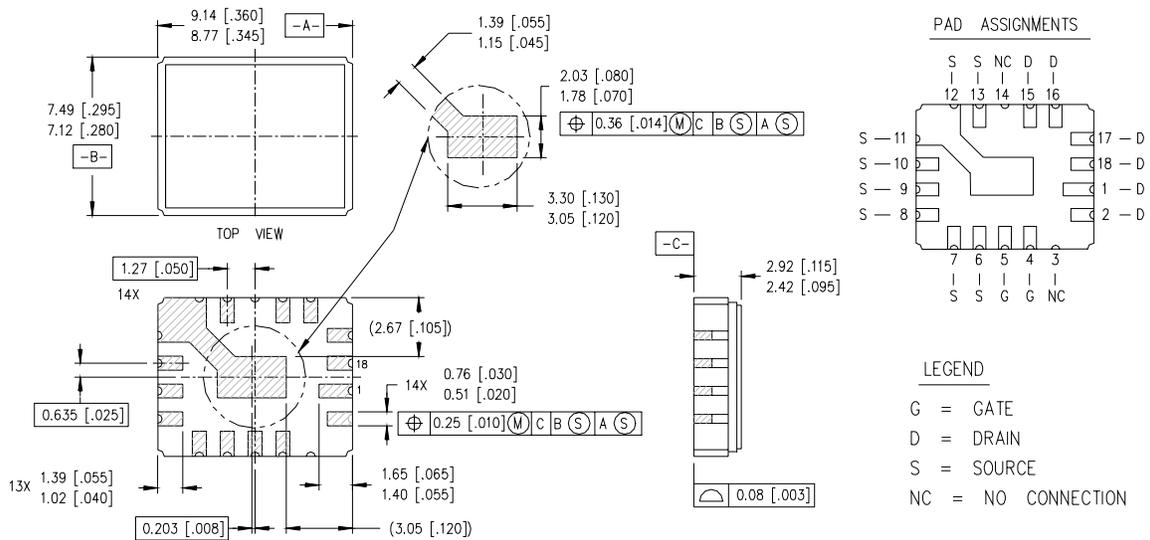


Fig 13b. Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -50V$, starting $T_J = 25^{\circ}C$, Peak $I_L = -4.0A$,
- ③ $I_{SD} \leq -4.0A$, $di/dt \leq -600A/\mu s$,
 $V_{DD} \leq -200V$, $T_J \leq 150^{\circ}C$
 Suggested $R_G = 7.5 \Omega$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions — LCC-18



- NOTES:
- DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
 - CONTROLLING DIMENSION: INCH.
 - DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].