

DESCRIPTION

FEATURES

- K4F170411C-B(F) (5V, 4K Ref.)
- K4F160411C-B(F) (5V, 2K Ref.)
- K4F170412C-B(F) (3.3V, 4K Ref.)
- K4F160412C-B(F) (3.3V, 2K Ref.)

- | Speed | 3.3V | | 5V | |
|-------|------|-----|-----|-----|
| | 4K | 2K | 4K | 2K |
| -50 | 324 | 396 | 495 | 605 |
| -60 | 288 | 360 | 440 | 550 |

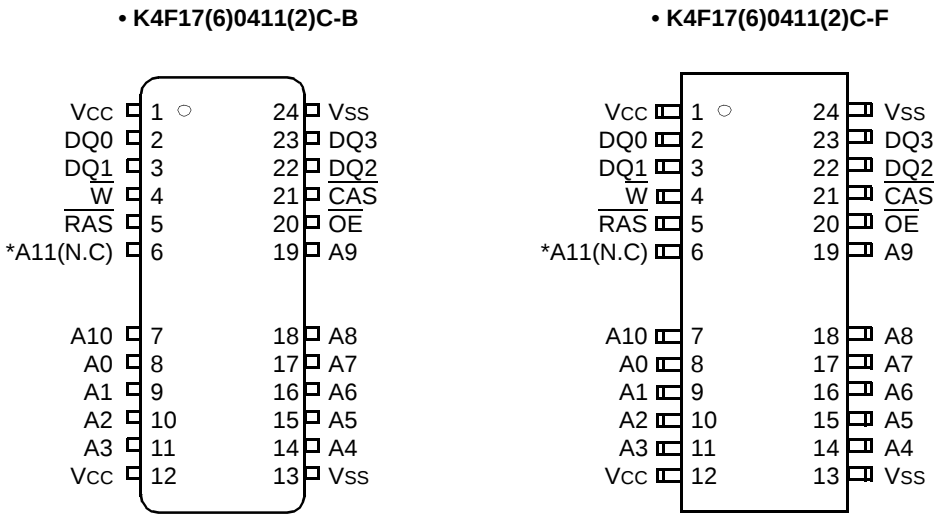
- | Part NO. | Vcc | Refresh cycle | Refresh period | | |
|------------|------|---------------|----------------|-------|--|
| | | | Nor- | L-ver | |
| K4F170411C | 5V | 4K | 64ms | 128ms | |
| K4F170412C | 3.3V | | | | |
| K4F160411C | 5V | 2K | 32ms | | |
| K4F160412C | 3.3V | | | | |

- | Speed | t _{RAC} | t _{CAC} | t _{RC} | t _{PC} | Remark |
|-------|------------------|------------------|-----------------|-----------------|---------|
| -50 | 50ns | 13ns | 90ns | 35ns | 5V/3.3V |
| -60 | 60ns | 15ns | 110ns | 40ns | 5V/3.3V |

The block diagram illustrates the VBB Generator and Memory Array interface. The VBB Generator is connected to Vcc and Vss. It provides a signal to the Control Clocks block, which also receives RAS, CAS, and W signals. The Control Clocks block is connected to the Refresh Timer, Refresh Control, Refresh Counter, Row Address Buffer, and Col. Address Buffer. The Refresh Timer is connected to the Refresh Control, which is connected to the Refresh Counter. The Refresh Counter is connected to the Row Address Buffer. The Row Address Buffer is connected to the Row Decoder. The Col. Address Buffer is connected to the Column Decoder. The Row Decoder and Column Decoder are connected to the Memory Array (4,194,304 x 4 Cells). The Memory Array is connected to the Sense Amps & I/O block. The Sense Amps & I/O block is connected to the Data in Buffer and Data out Buffer. The Data in Buffer is connected to DQ0 to DQ3. The Data out Buffer is connected to OE.



PIN CONFIGURATION (Top Views)



*A11 is N.C for K4F160411(2)C (5V/3.3V, 2K Ref. product)

B : 300mil 26(24) SOJ
F : 300mil 26(24) TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A10	Address Inputs (2K Product)
DQ0 - 3	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5V)
	Power(+3.3V)
N.C	No Connection (2K Ref. product)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	-55 to +150	°C
Power Dissipation	P _D	1	1	W
Short Circuit Output Current	I _{osAddress}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A= 0 to 70°C)

Parameter	Symbol	3.3V			5V			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3*1	2.4	-	V _{CC} +1.0*1	V
Input Low Voltage	V _{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns(3.3V), V_{CC}+2.0V/20ns(5V), Pulse width is measured at V_{CC}

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Max	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.3V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	uA
	Output High Voltage Level(I _{OH} =-2mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =2mA)	V _{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.5V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	uA
	Output High Voltage Level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max				Units
			K4F170412C	K4F160412C	K4F170411C	K4F160411C	
I _{CC1}	Don't care	-50 -60	90	110	90	110	mA
			80	100	80	100	mA
I _{CC2}	Normal L	Don't care	1	1	2	2	mA
			1	1	1	1	mA
I _{CC3}	Don't care	-50 -60	90	110	90	110	mA
			80	100	80	100	mA
I _{CC4}	Don't care	-50 -60	80	90	80	90	mA
			70	80	70	80	mA
I _{CC5}	Normal L	Don't care	0.5	0.5	1	1	mA
			200	200	250	250	uA
I _{CC6}	Don't care	-50 -60	90	110	90	110	mA
			80	100	80	100	mA
I _{CC7}	L	Don't care	250	250	300	300	uA
I _{CCS}	L	Don't care	200	200	250	250	uA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$, Address cycling @trc=min.)

I_{CC2} : Standby Current ($RAS=CAS=W=V_{IH}$)

I_{CC3}* : $\overline{RAS}$ -only Refresh Current ($\overline{CAS}=V_{IH}$, $\overline{RAS}$, Address cycling @trc=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}=V_{IL}$, $\overline{CAS}$, Address cycling @tpc=min.)

I_{CC5} : Standby Current ($RAS=CAS=W=V_{CC}-0.2V$)

I_{CC6}* : $\overline{CAS}$ -Before- $\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @trc=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})= $V_{CC}-0.2V$, Input low voltage(V_{IL})=0.2V, $\overline{CAS}=0.2V$,

DQ=Don't care, Trc=31.25us(4K/L-ver), 62.5us(2K/L-ver), TRAS=TRASmin~300ns

I_{CCS} : Self Refresh Current

$RAS=CAS=0.2V$, $\overline{W}=OE=A0 \sim A11=V_{CC}-0.2V$ or 0.2V,

DQ0 ~ DQ3= $V_{CC}-0.2V$, 0.2V or Open

***Note** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6} address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tpc.

K4F170411C, K4F160411C K4F170412C, K4F160412C

CMOS DRAM

CAPACITANCE (TA=25°C, VCC=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A11]	CIN1	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ3]	CDQ	-	7	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Test condition (5V device) : VCC=5.0V±10%, VIH/VIL=2.4/0.8V, VOH/VOL=2.4/0.4V

Test condition (3.3V device) : VCC=3.3V±0.3V, VIH/VIL=2.0/0.8V, VOH/VOL=2.0/0.8V

Parameter	Symbol	-50		-60		Units	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		ns	
Read-modify-write cycle time	t _{RWC}	133		155		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t _{CAC}		13		15	ns	3,4,5
Access time from column address	t _{AA}		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	0		0		ns	3
Output buffer turn-off delay	t _{OFF}	0	13	0	15	ns	6
Transition time (rise and fall)	t _T	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	t _{RP}	30		40		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	13		15		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	50		60		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5		5		ns	
Row address set-up time	t _{ASR}	0		0		ns	
Row address hold time	t _{RAH}	10		10		ns	
Column address set-up time	t _{ASC}	0		0		ns	
Column address hold time	t _{CAH}	10		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	25		30		ns	
Read command set-up time	t _{RCS}	0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		ns	8
Write command hold time	t _{WCH}	10		10		ns	
Write command pulse width	t _{WP}	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	13		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	13		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-50		-60		Units	Note
		Min	Max	Min	Max		
Data set-up time	tDS	0		0		ns	9
Data hold time	tDH	10		10		ns	9
Refresh period (2K, Normal)	tREF		32		32	ms	
Refresh period (4K, Normal)	tREF		64		64	ms	
Refresh period (L-ver)	tREF		128		128	ms	
Write command set-up time	tWCS	0		0		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		85		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	53		60		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35	ns	3
Fast Page cycle time	tPC	35		40		ns	
Fast Page read-modify-write cycle time	tPRWC	76		85		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page cycle)	tCP	10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	tRASP	50	200K	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		ns	
$\overline{\text{OE}}$ access time	tOEA		13		15	ns	
$\overline{\text{OE}}$ to data delay	tOED	13		15		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	13	0	15	ns	6
$\overline{\text{OE}}$ command hold time	tOEH	13		15		ns	
Write command set-up time (Test mode in)	tWTS	10		10		ns	11
Write command hold time (Test mode in)	tWTH	10		10		ns	11
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time($\overline{\text{C}}$ -B- $\overline{\text{R}}$ refresh)	tWRP	10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time($\overline{\text{C}}$ -B- $\overline{\text{R}}$ refresh)	tWRH	10		10		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tRASS	100		100		us	13,14,15
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tRPS	90		110		ns	13,14,15
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tCHS	-50		-50		ns	13,14,15

TEST MODE CYCLE

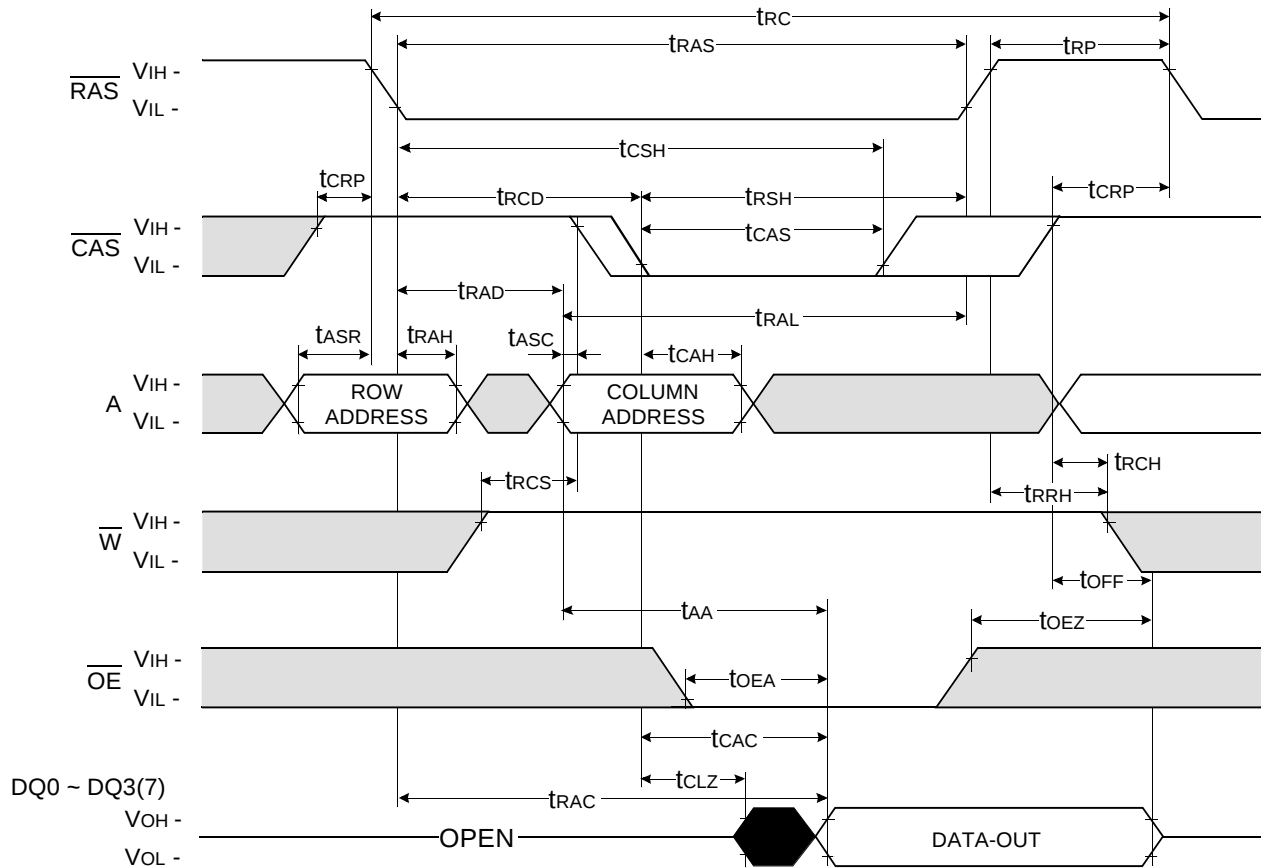
(Note 11)

Parameter	Symbol	-50		-60		Units	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	95		115		ns	
Read-modify-write cycle time	t _{RWC}	138		160		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		55		65	ns	3,4,10,12
Access time from $\overline{\text{CAS}}$	t _{CAC}		18		20	ns	3,4,5,12
Access time from column address	t _{AA}		30		35	ns	3,10,12
$\overline{\text{RAS}}$ pulse width	t _{RAS}	55	10K	65	10K	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	18	10K	20	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	18		20		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	55		65		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	30		35		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	41		45		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{RWD}	78		90		ns	7
Column address to $\overline{\text{W}}$ delay time	t _{AWD}	53		60		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	t _{CPWD}	58		65		ns	
Fast Page cycle time	t _{PC}	40		45		ns	
Fast Page read-modify-write cycle time	t _{PRWC}	81		90		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	t _{RASP}	55	200K	65	200K	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		35		40	ns	3
$\overline{\text{OE}}$ access time	t _{OEA}		18		20	ns	
$\overline{\text{OE}}$ to data delay	t _{OED}	18		20		ns	
$\overline{\text{OE}}$ command hold time	t _{OEH}	18		20		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only.
If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. $t_{\text{OFF}}(\text{min})$ and $t_{\text{OEZ}}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{W}}$ falling edge in read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only.
If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. If $t_{\text{RASS}} \geq 100\text{us}$, then $\overline{\text{RAS}}$ precharge time must use t_{RPS} instead of t_{RP} .
14. For $\overline{\text{RAS}}$ -only refresh and burst $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode, 4096(4K)/2048(2K) cycles of burst refresh must be executed within 64ms/32ms before and after self refresh, in order to meet refresh specification.
15. For distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ with 15.6us interval $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

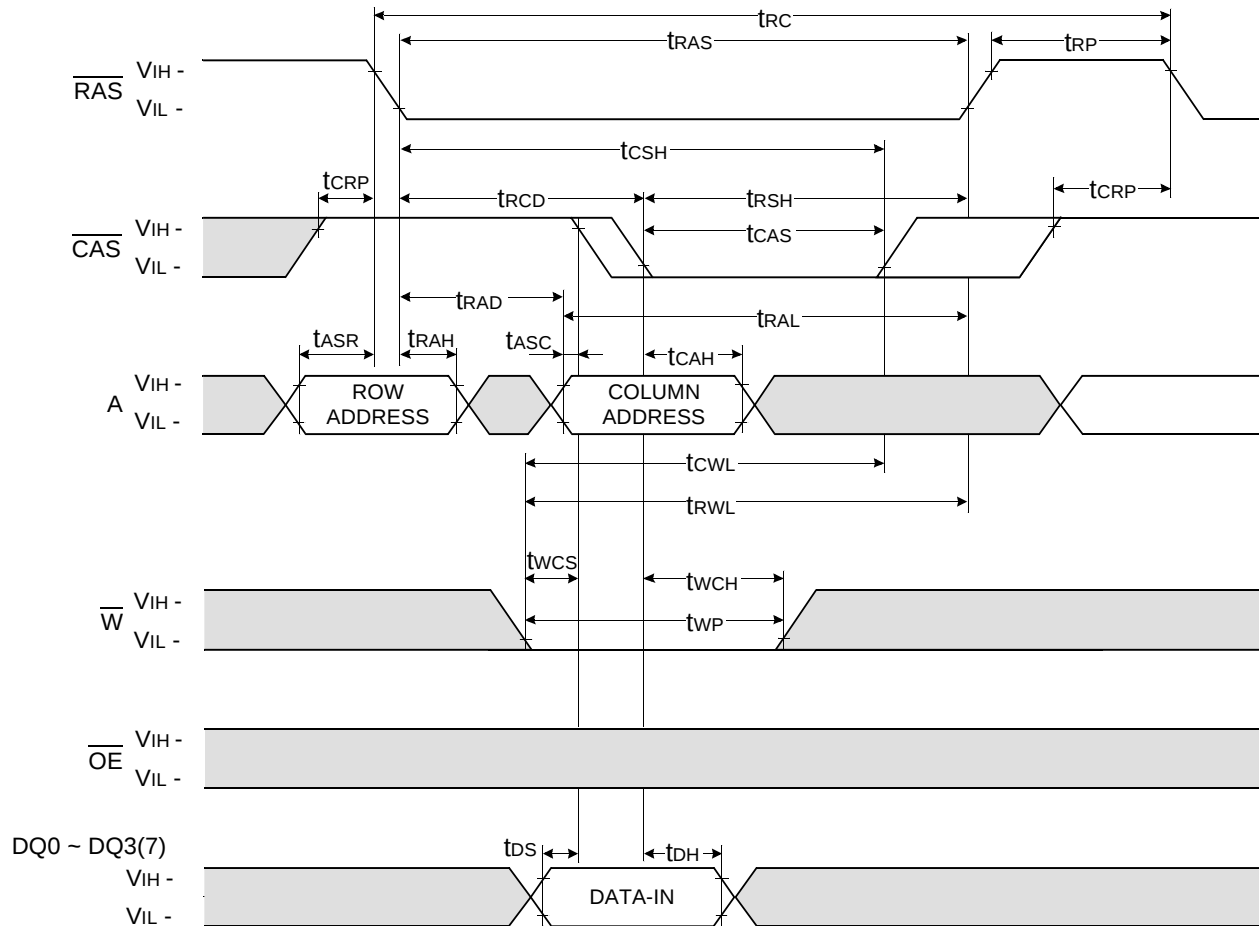
READ CYCLE



Don't care
Undefined

WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

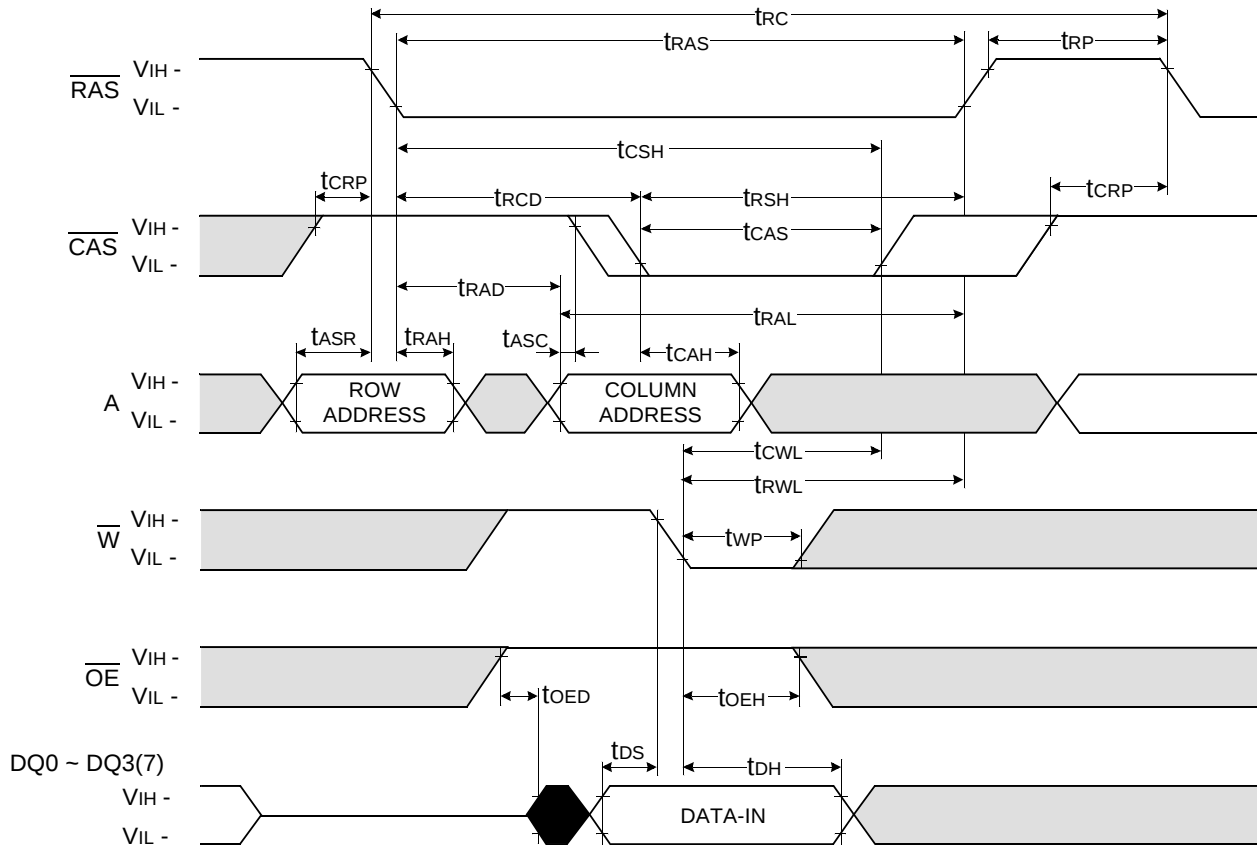


Don't care

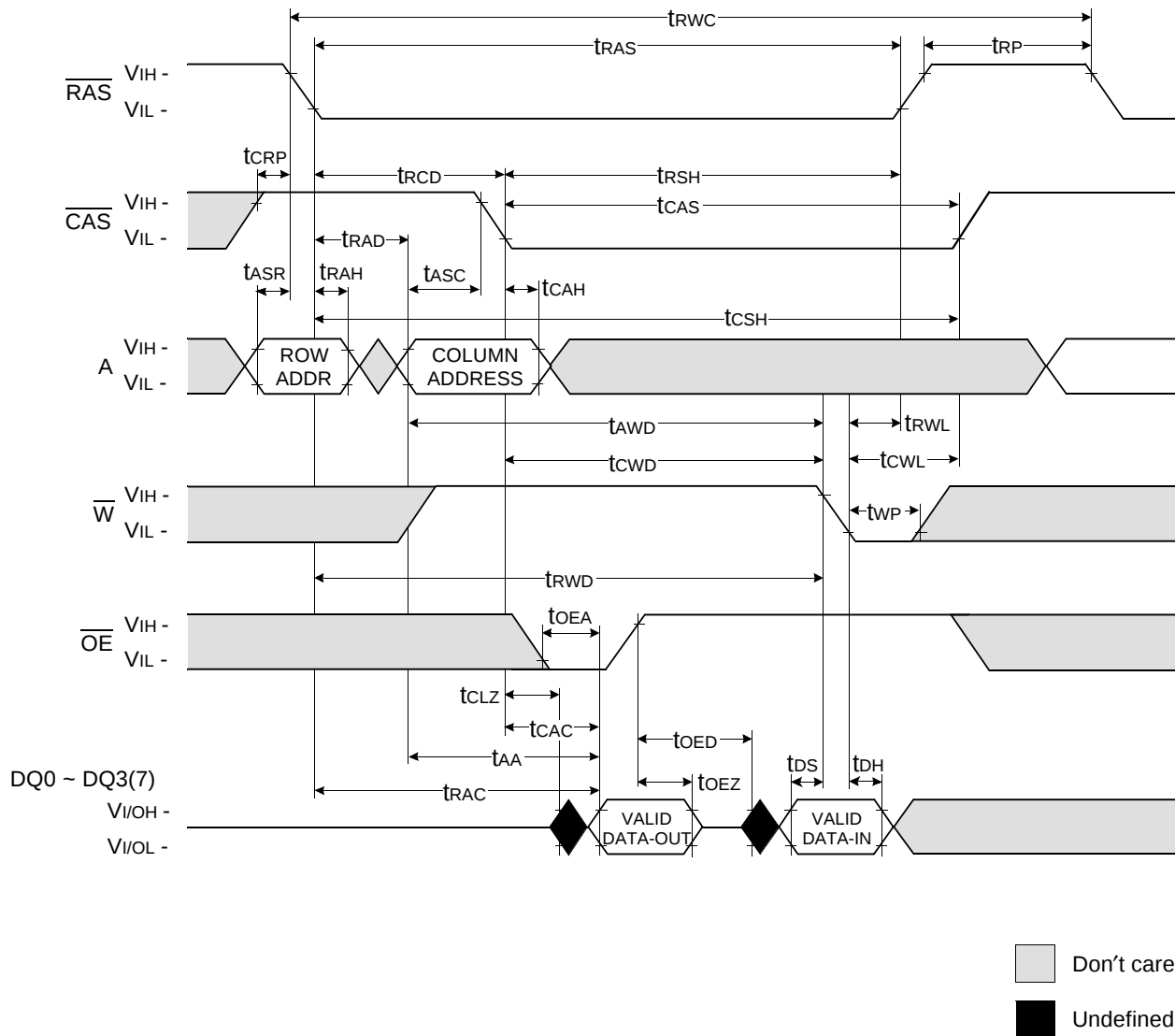
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WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

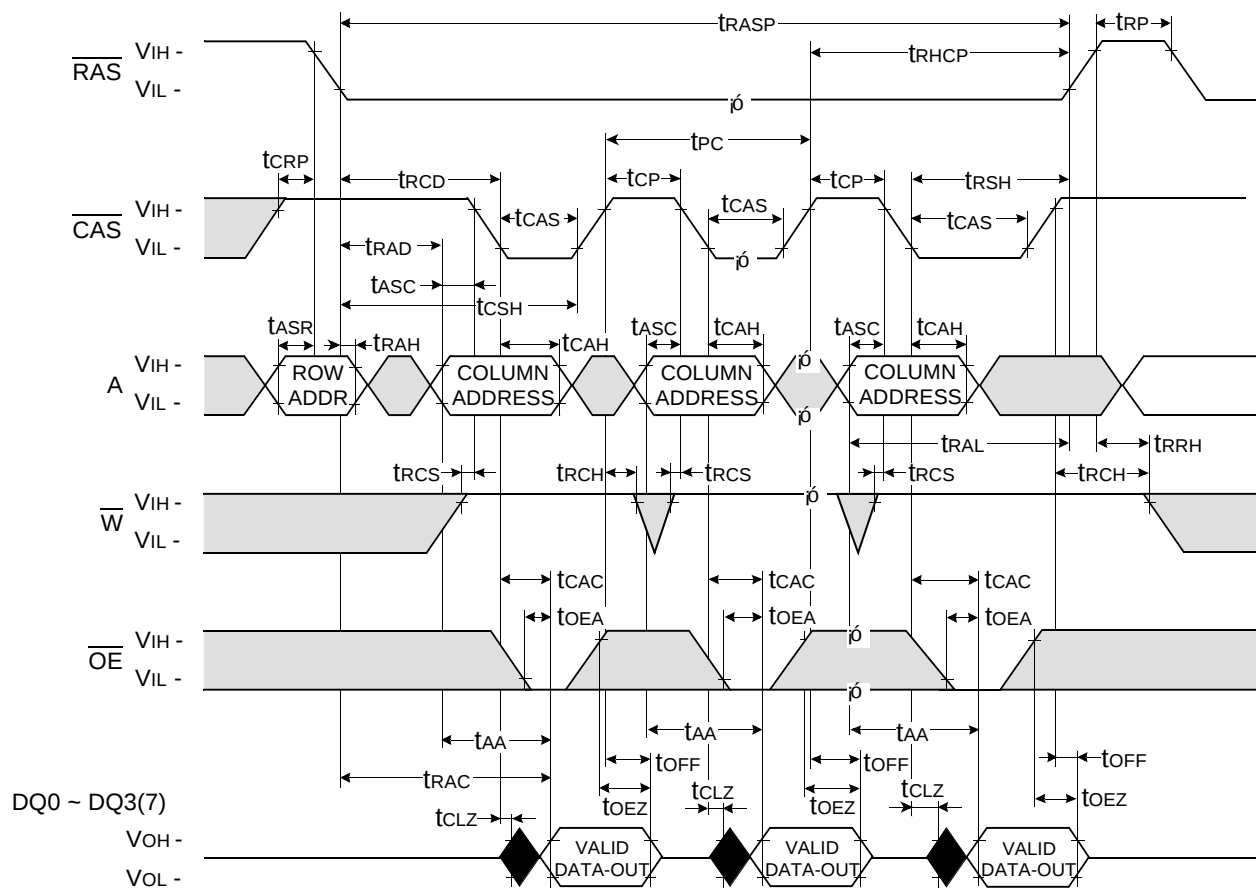
NOTE : DOUT = OPEN



READ - MODIFY - WRITE CYCLE



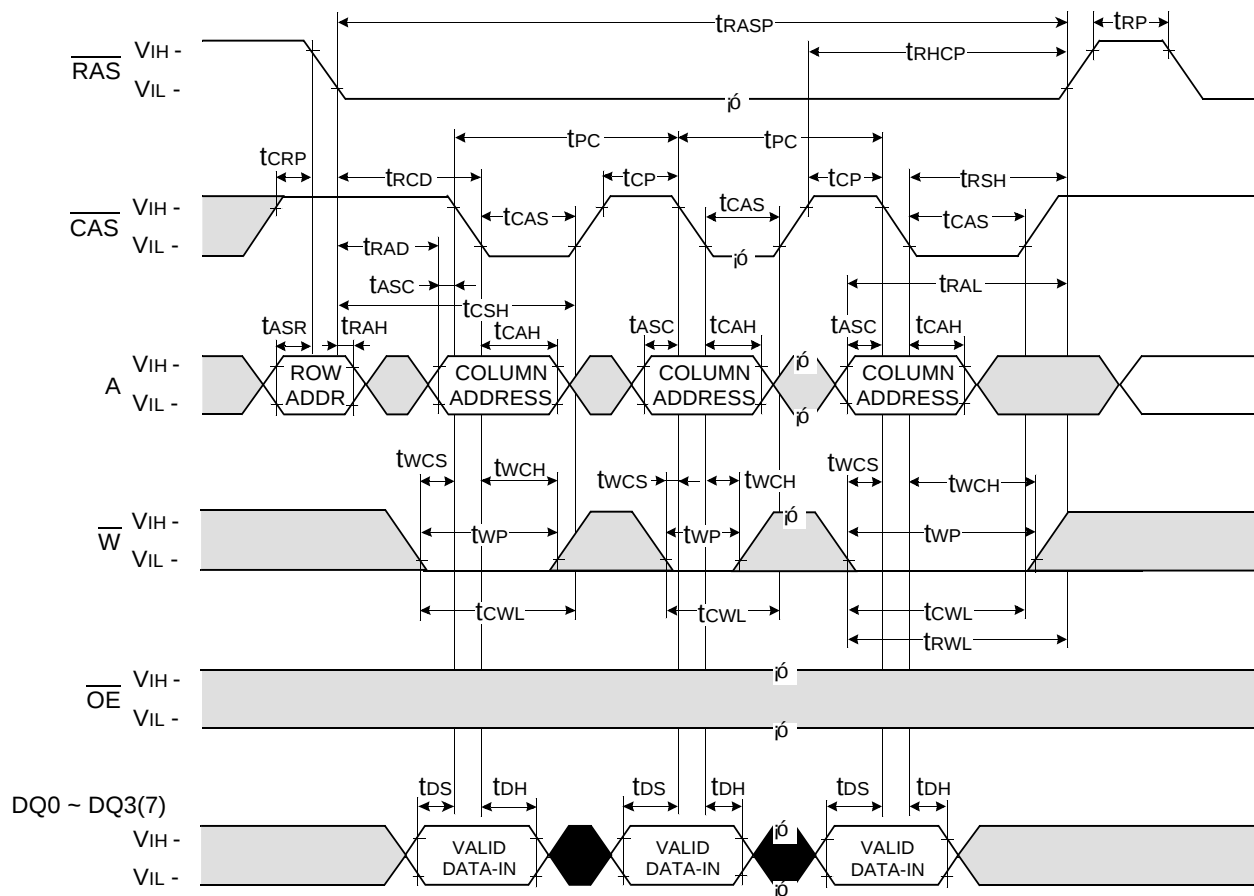
FAST PAGE READ CYCLE



Don't care
Undefined

FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



Don't care
Undefined

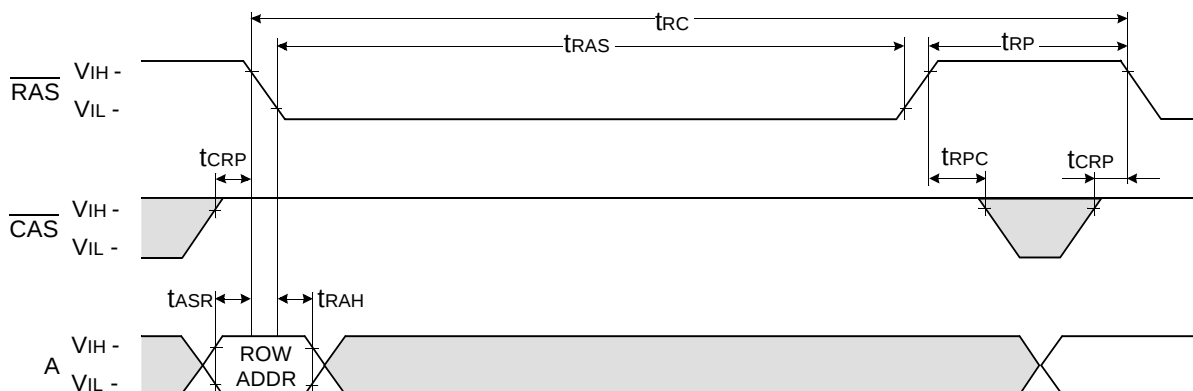
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$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE

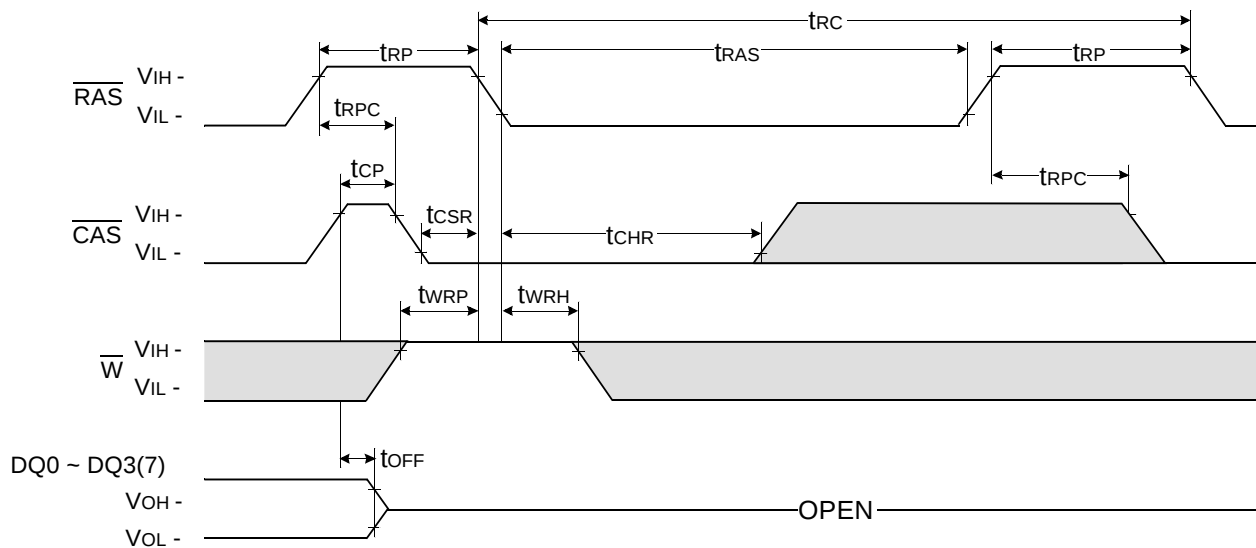
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



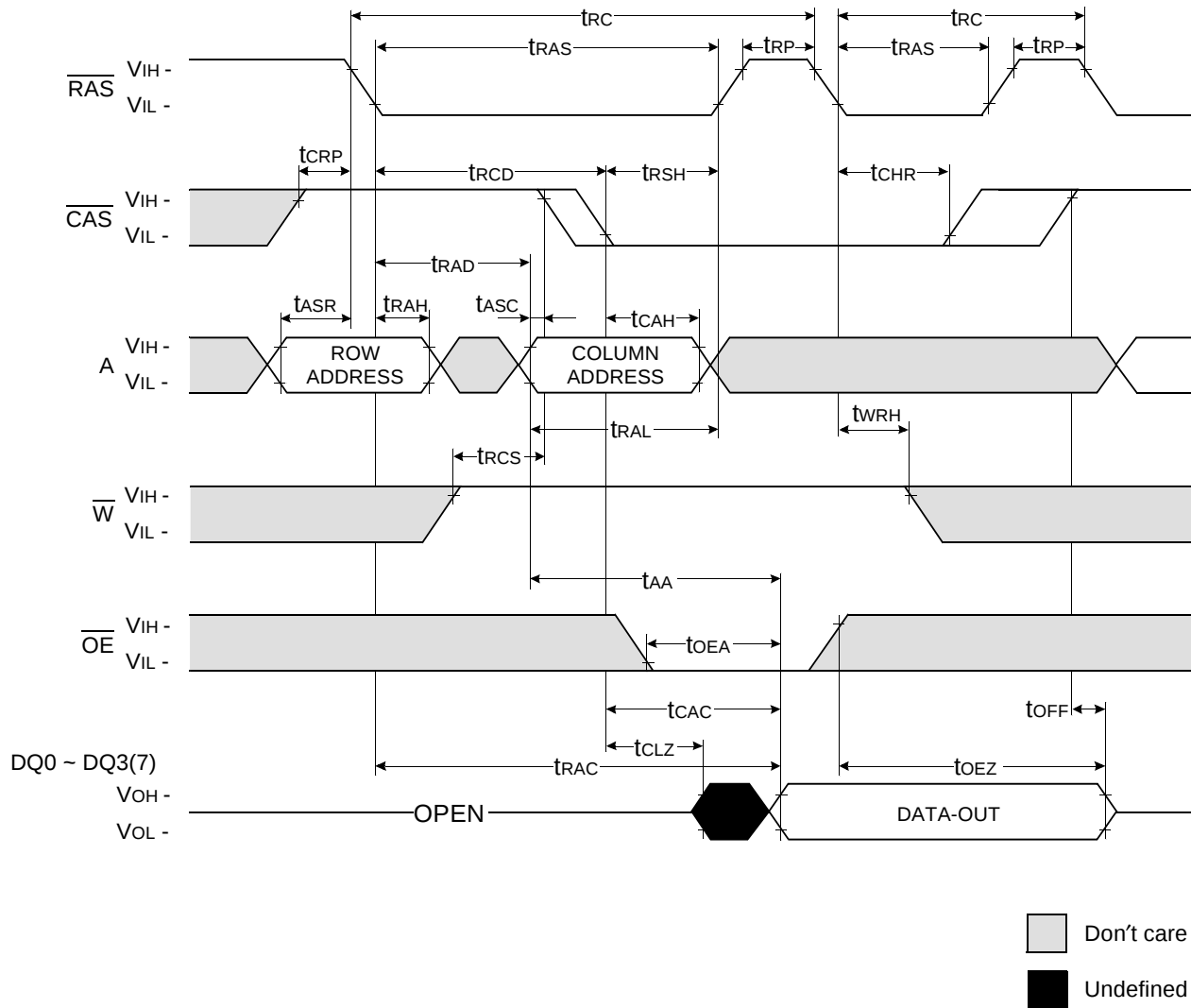
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



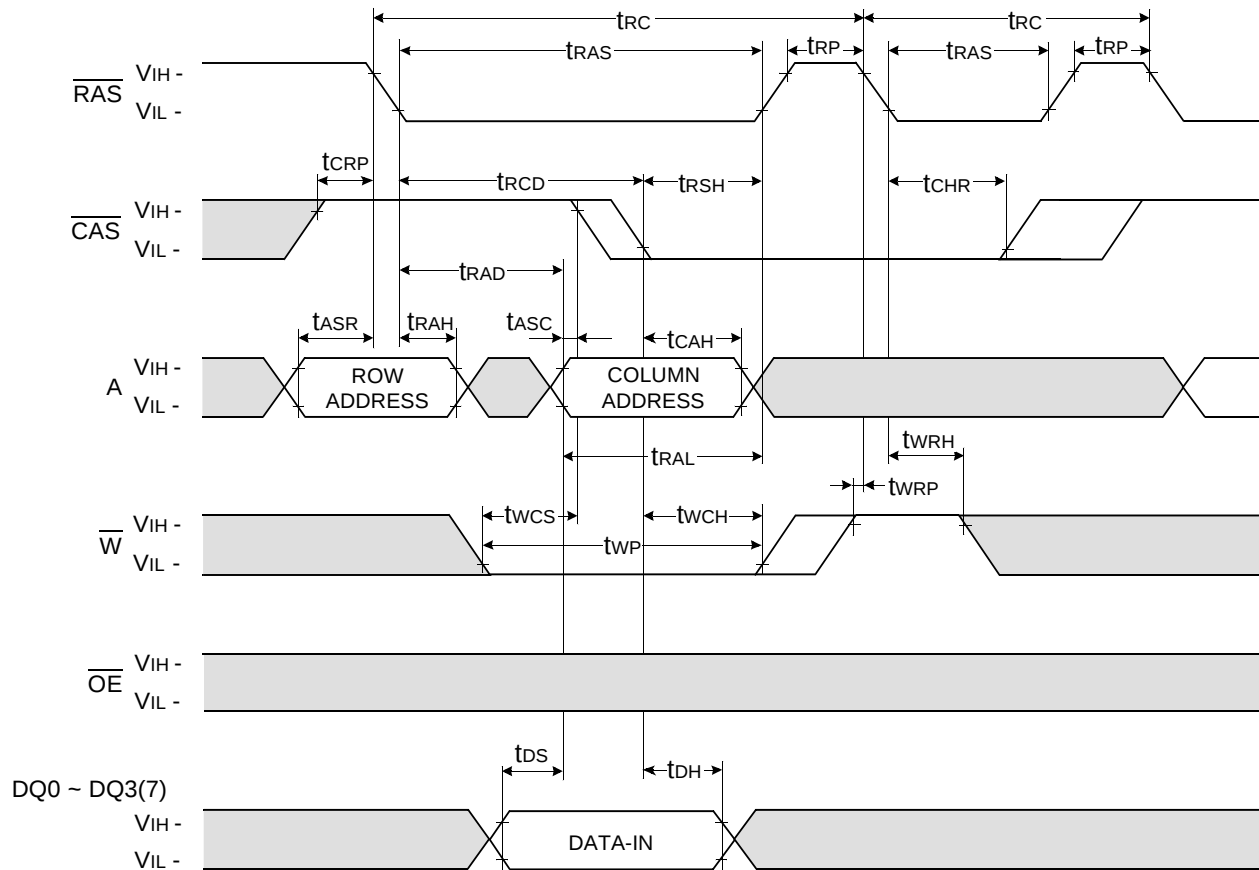
Don't care
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HIDDEN REFRESH CYCLE (READ)



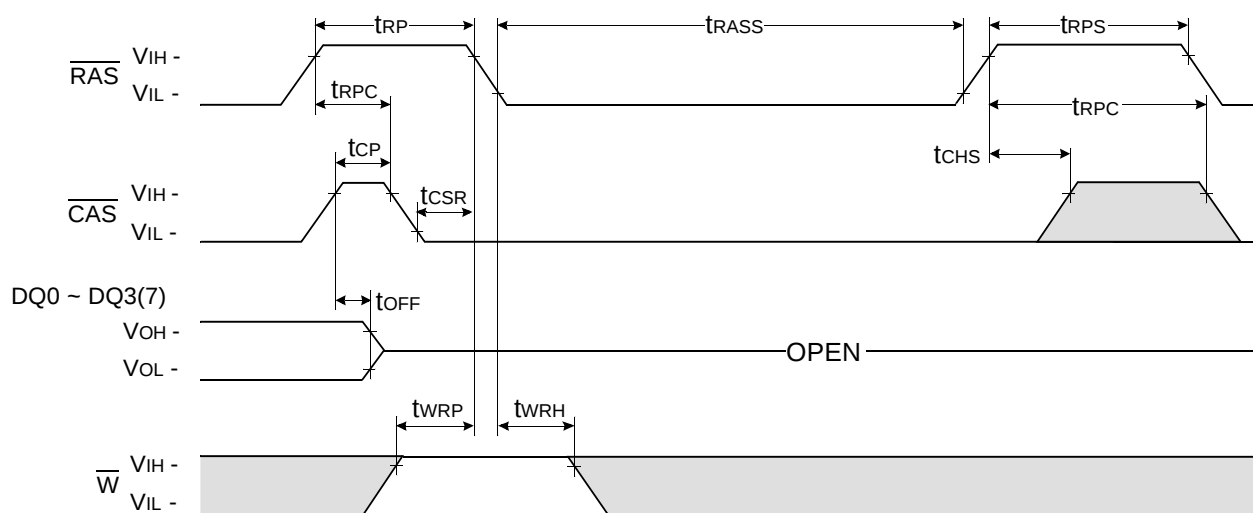
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN

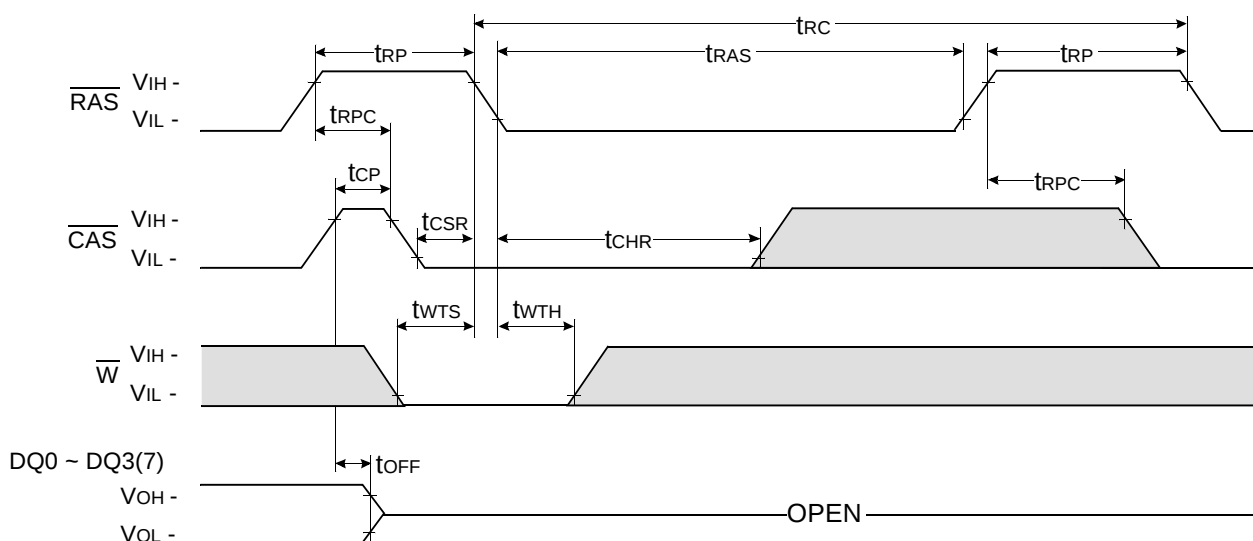


Don't care
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NOTE : $\overline{OE}$, A = Don't care



NOTE : $\overline{OE}$, A = Don't care

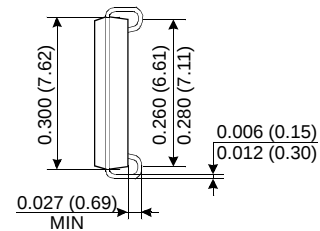
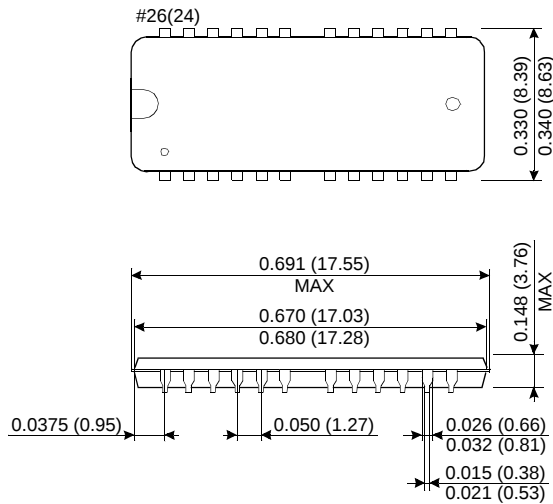


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PACKAGE DIMENSION

26(24) SOJ 300mil

Units : Inches (millimeters)



26(24) TSOP(II) 300mil

Units : Inches (millimeters)

