



KA7500C SMPS Controller

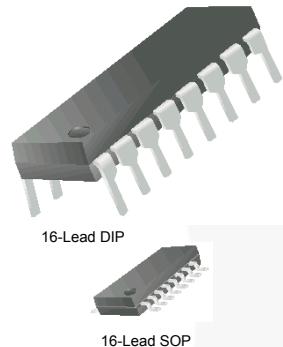
Features

- Internal Regulator Provides a Stable 5V Reference Supply Trimmed to $\pm 1\%$ Accuracy
- Uncommitted Output TR for 200mA Sink or Source Current
- Output Control for Push-Pull or Single-Ended Operation
- Variable Duty Cycle by Dead-Time Control (Pin 4) Complete PWM Control Circuit
- On-Chip Oscillator with Master or Slave Operation
- Internal Circuit Prohibits Double Pulse at Either Output

Description

The KA7500C is used for the control circuit of the pulse-width modulation switching regulator. The KA7500C consists of 5V reference voltage circuit, two error amplifiers, flip flop, an output control circuit, a PWM comparator, a dead-time comparator, and an oscillator.

This device can be operated in the switching frequency of 1kHz to 300kHz. The precision of voltage reference (V_{REF}) is improved up to $\pm 1\%$ with trimming. This provides a better output voltage regulation. The operating temperature range is $-25^{\circ}\text{C} \sim +85^{\circ}\text{C}$.



Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
KA7500C	-25 to $+85^{\circ}\text{C}$	RoHS	16-Lead Dual Inline Package (DIP)	Tube
KA7500CD			16-Lead Small Outline Package (SOP)	Tube
KA7500CDTF				Tape and Reel



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Block Diagram

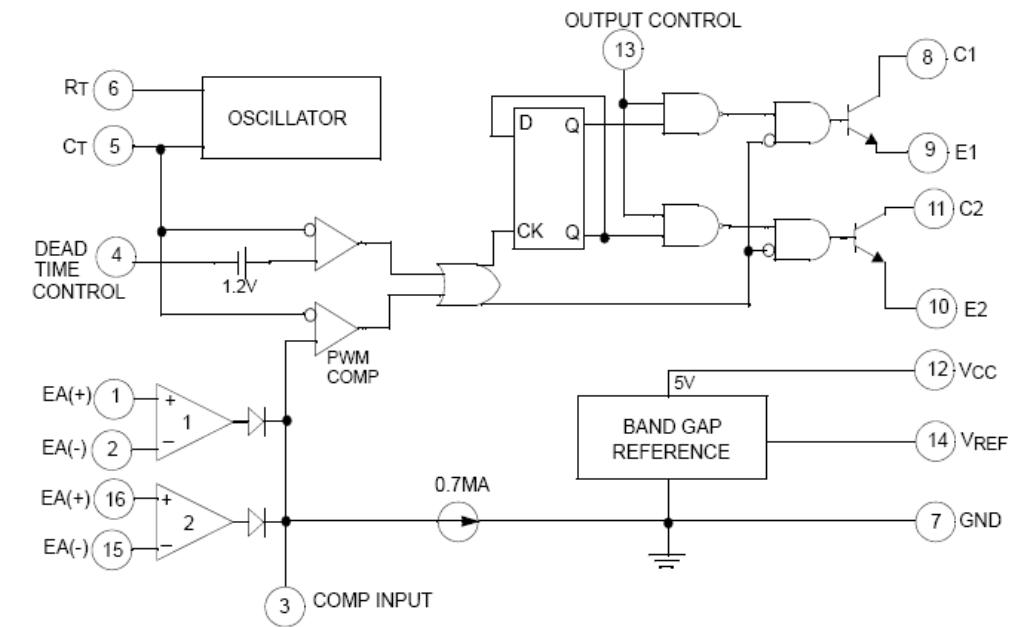


Figure 1. Block Diagram

Typical Application

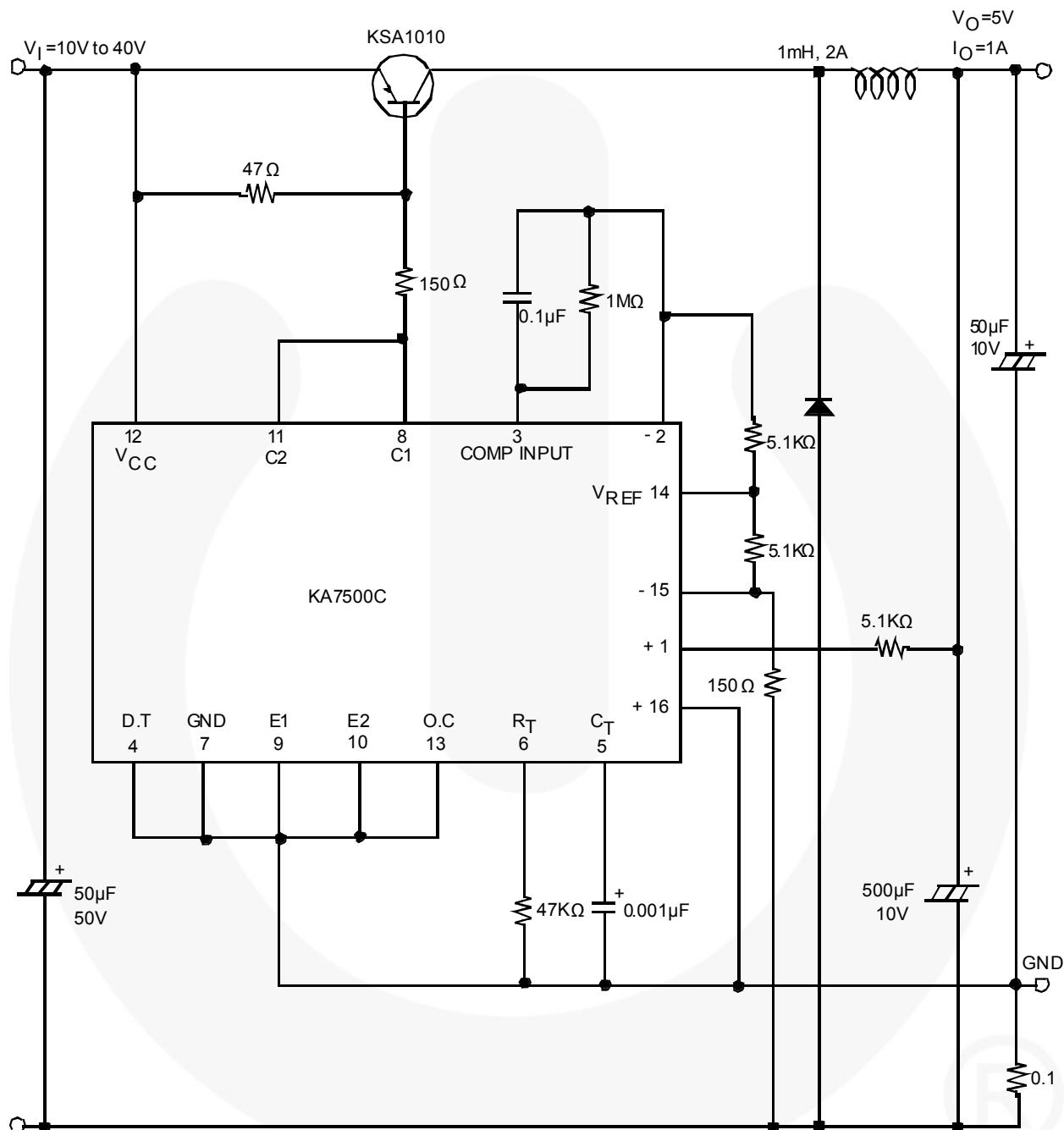


Figure 2. Pulse-Width Modulated Step-Down Converter

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage			42	V
V_C	Collector Supply Voltage			42	V
I_O	Output Current			250	mA
V_{IN}	Amplifier Input Voltage			$V_{CC} + 0.3$	V
P_D	Power Dissipation	KA7500C		1	W
		KA7500CD		0.9	
T_{OPR}	Operation Temperature Range		-25	+85	°C
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature			+125	°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	7	15	40	V
V_{C1}, V_{C2}	Collector Supply Voltage		30	40	V
I_{C1}, I_{C2}	Collector Output Current (Each Transition)			200	mA
V_{IN}	Amplifier Input Voltage	0.3		$V_{CC} - 2.0$	V
I_{FB}	Current Into Feedback Terminal			0.3	mA
I_{REF}	Reference Output Terminal			10	mA
R_T	Timing Resistor	1.8	30.0	500.0	KΩ
C_T	Timing Capacitor	0.0047	0.0010	10.0000	μA
f_{OSC}	Oscillator Frequency	1	40	200	kHz
V_{IN_PWM}	PWM Input Voltage (Pins 3, 4, and 13)	0.3		5.3	V

Electrical Characteristics

$V_{CC} = 20V$, $f = 10kHz$, $T_A = -25^\circ C$ to $+85^\circ C$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Reference Section						
V_{REF}	Reference Output Voltage	$I_{REF}=1mA$, $T_A=25^\circ C$ ⁽¹⁾	4.95	5.00	5.05	V
		$I_{REF}=1mA$	4.90	5.00	5.10	
R_{LINE}	Line Regulation	$V_{CC}=7V$ to $40V$		2	25	mV
R_{LOAD}	Load Regulation	$I_{REF}=1mA$ to $10mA$		1	15	mV
I_{SC}	Short-Circuit Output Current	$V_{REF}=0V$	10	35	50	mA
Oscillation Frequency						
f_{OSC}	Oscillation Frequency	$C_T=0.001\mu F$, $R_T=30K\Omega$		40.0		kHz
		$C_T=0.01\mu F$, $R_T=12K\Omega$, $T_A=25^\circ C$	9.2	10.0	10.8	
		$C_T=0.01\mu F$, $R_T=12K\Omega$, $T_A=T_{LOW}$ to T_{HIGH}	9.0		12.0	
$\Delta f/\Delta t$	Frequency Change with Temperature	$C_T=0.01\mu F$, $R_T=12K\Omega$			2	%
Dead-Time Control Section						
I_{BIAS}	Input Bias Current	$V_{CC}=15V$, $0V \leq V_4 \leq 5.25V$		-2	-10	µA
$D_{(MAX)}$	Maximum Duty Cycle	$V_{CC}=15V$, $V_4=0V$, OC $Pin=V_{REF}$	45			%
V_{ITH}	Input Threshold Voltage	Zero Duty Cycle		3.0	3.3	V
		Maximum Duty Cycle	0			
Error Amplifier Section						
V_{IO}	Input Offset Voltage	$V_3=2.5V$		2	10	mV
I_{IO}	Input Offset Current	$V_3=2.5V$		25	250	mA
I_{BIAS}	Input Bias Current	$V_3=2.5V$		0.2	1.0	µA
V_{CIM}	Common Mode Input Voltage	$7V \leq V_{CC} \leq 40V$	-0.3		V_{CC}	V
G_{VO}	Open-Loop Voltage Gain	$0.5V \leq V_3 \leq 3.5V$	70	95		dB
Bw	Unit-Gain Bandwidth			650		kHz
PWM Comparator Section						
V_{ITH}	Input Threshold Voltage	Zero Duty Cycle		4.0	4.5	V
I_{SINK}	Input Sink Current	$V_3=0.7V$	-0.3	-0.7		mA
Output Section						
$V_{CE(SAT)}$	Output Saturation Voltage Common Emitter	$V_E=0V$, $I_C=200mA$		1.0	1.3	V
$V_{CC(SAT)}$	Emitter-Follower	$V_C=15V$, $I_E=-200mA$		1.5	2.5	
$I_{C(OFF)}$	Collector Off-State Current	$V_{CC}=40V$, $V_{CE}=40V$		2	100	µA
$I_{E(OFF)}$	Emitter Off-State Current	$V_{CC}=V_C=40V$, $V_E=40V$			-100	
Total Device						
I_{CC}	Supply Current	$Pin6=V_{REF}$, $V_{CC}=15V$		6	10	mA
Output Switching Characteristics						
t_R	Rise Time, Common Emitter, Common Collector			100	200	ns
t_F	Fall Time, Common Emitter, Common Collector			25	100	

Note:

1. This is guaranteed where the marking code of the package surface is over 027.

Physical Dimensions

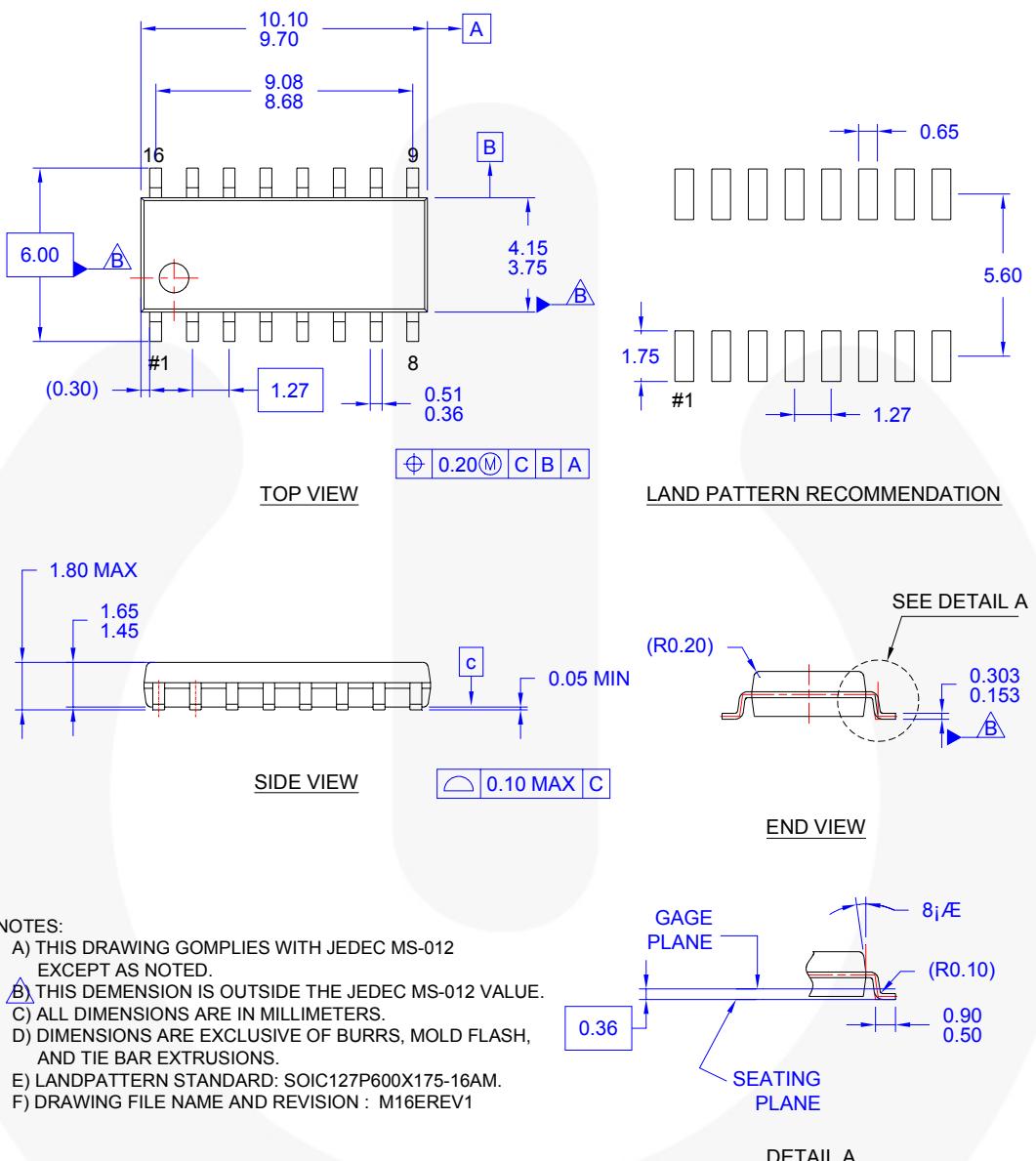
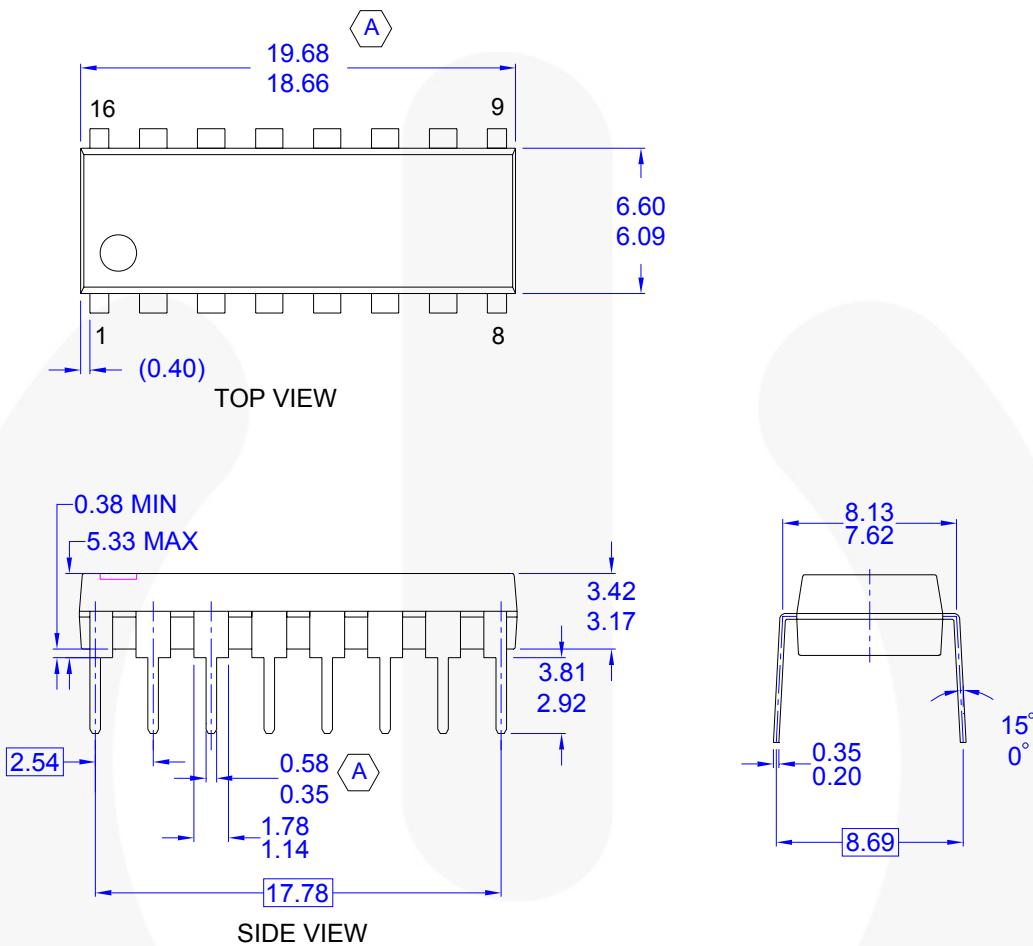


Figure 3. 16-Lead Small Outline Package (SOP)

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Physical Dimensions



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Figure 4. 16-Lead Dual Inline Package (DIP)

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