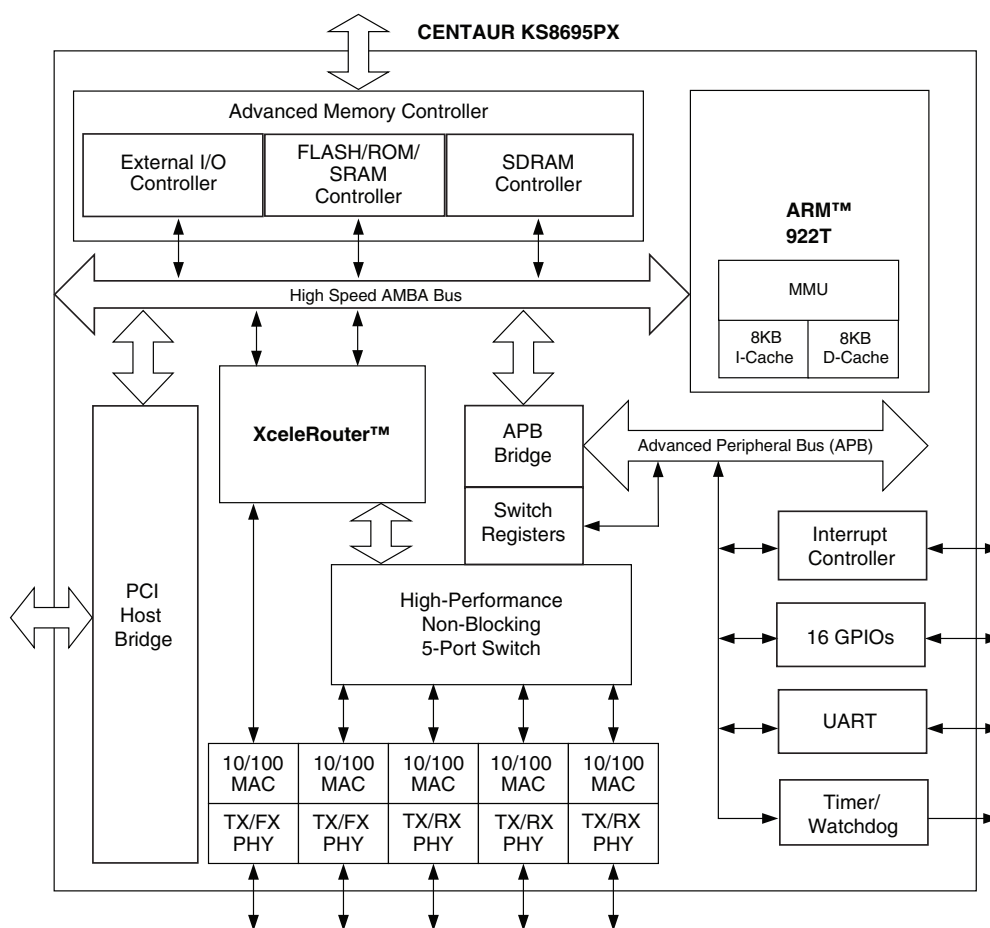


## General Description

The CENTAUR KS8695PX, Multi-Port PCI Gateway Solution, delivers a new level of networking integration, performance, and overall BOM cost savings, enabling original equipment manufacturers (OEMs) to provide customers with feature-rich, low-cost solutions for the residential gateway and small office environment.

- Integration of a PCI bridge allowing incorporation of a variety of productivity enhancing system interfaces, including the expanding 802.11 a/g/b wireless LAN.
- High-performance ARM™ CPU (ARM992T) with an 8KB I-cache, an 8KB D-cache, and a memory management unit (MMU) for Linux and WinCE® support.
- XceleRouter™ technology for WAN and LAN interfaces.
- Proven wire-speed switching technology that includes 802.1Q tag-based VLAN and quality of service (QoS) support.
- Five patented mixed-signal, low-powered Fast Ethernet transceivers with corresponding media access control (MAC) units.
- Advanced memory interface with programmable 8/16/32-bit data and 22-bit address bus with up to 64MB of total memory space for Flash, ROM, SRAM, SDRAM, and external peripherals.
- Protocol engine to accelerate packet processing.

## Functional Diagram



XceleRouter is a trademark of Micrel, Inc.; AMD is a registered trademark of Advanced Micro Devices, Inc.; ARM is a trademark of Advanced RISC Machines Ltd.; Intel is a registered trademark of Intel Corporation; WinCE is a registered trademark of Microsoft Corporation.

## Features

- The CENTAUR KS8695PX featuring XceleRouter technology is a single-chip multi-port PCI gateway solution with all the key components integrated for a high-performance, low-cost broadband gateway
- ARM922T High-Performance CPU Core
  - 185MIPS ARM922T core at 166MHz
  - 8KB I-cache and 8KB D-cache
  - Memory management unit (MMU) for Linux and WinCE®
  - 32-bit ARM and 16-bit thumb instruction sets for smaller memory footprints
- 33MHz 32-bit PCI Interface
  - version PCI 2.1
  - Supports bus mastership or guest-mode
  - Supports normal and memory-mapped I/O
  - Support for miniPCI and cardbus peripherals
- Integrated Ethernet Transceivers and Switch Engine
  - Five 10/100 Ethernet transceivers and five MACs (1P for WAN interface, 4P for LAN switching)
  - 100BASE-FX mode option on the WAN port and one LAN port
  - Automatic MDI/MDI-X crossover on all ports
  - Wire-speed, non-blocking switch
  - 802.1Q tag-based VLAN (16 VLANs, full range VID)
  - Port-based VLAN
  - QoS/CoS packet prioritization support: per port 802.1P and DiffServ-based
  - 64KB on-chip frame buffer SRAM
  - VLAN ID and 802.1P tag/untag option per port
  - 802.1D Spanning Tree Protocol support
  - Programmable rate-limiting per port: 0Mbps to 100Mbps, ingress and egress, rate options for high and low priority
  - Extensive MIB counter management support
  - IGMP snooping for multicast packet filtering
  - Dedicated 1K entry look-up engine
  - Port mirroring/monitoring/sniffing
  - Broadcast storm protection with % control global and per port basis
  - Full- and half-duplex flow control
- XceleRouter Technology
  - TCP/UDP/IP packet header checksum generation to offload CPU tasks
  - IPv4 packet filtering on checksum errors
  - Automatic error packet discard
  - DMA engine with burst-mode support for efficient WAN/LAN data transfers
  - FIFOs for back-to-back packet transfers
- Memory and External I/O Interfaces
  - 8/16/32-bit wide shared data path for Flash, ROM, SRAM, SDRAM, and external I/O
  - Total memory space up to 64MB
  - Intel®/AMD®-type Flash support

- Peripheral Support
  - 8/16/32-bit external I/O interface supporting PCMCIA or generic CPU/DSP host I/F
  - Sixteen general purpose input/output (GPIO)
  - Two 32-bit timer counters (one watchdog)
  - Interrupt controller
- System Design
  - Up to 166MHz CPU and 125MHz bus speed
  - 289 PBGA package (19mm x 19mm) saves board real estate
  - Two power supplies: 1.8V core and Ethernet RX supply, 3.3V I/O and Ethernet TX supply
  - Built-in LED controls
- Debugging
  - ARM922T JTAG debug interface
  - UART for console port or modem back-up
- Power Management
  - CPU and system clock speed step-down options
  - Low-power Ethernet transceivers
  - Per port power-down and Ethernet transmit disable
- Reference Hardware and Software Evaluation Kit
  - Hardware evaluation board (passes class B EMI)
  - Board support package including firmware source codes, linux kernel, and software stacks
  - Documentation for design and programming
  - Complete hardware and software reference designs available
- Commercial Temperature Range: 0°C to +70°C
- Available in 289-Pin PBGA

## Applications

- RG + combo 802.11a/b/g access point
- Multi-port broadband gateway
- Multi-port firewall and VPN appliances
- Combination wireless and wireline gateway
- Multi-port VoIP gateway
- Fiber-to-the-home managed CPE

## Ordering Information

| Part Number | Temperature Range | Package      |
|-------------|-------------------|--------------|
| KS8695PX    | 0°C to +70°C      | 289-Pin PBGA |

## Revision History

| Revision | Date     | Summary of Changes                                |
|----------|----------|---------------------------------------------------|
| 1.0      | 05/13/03 | Created.                                          |
| 1.1      | 07/06/04 | Copied to Micrel format and updated System Clock. |

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## System Level Applications

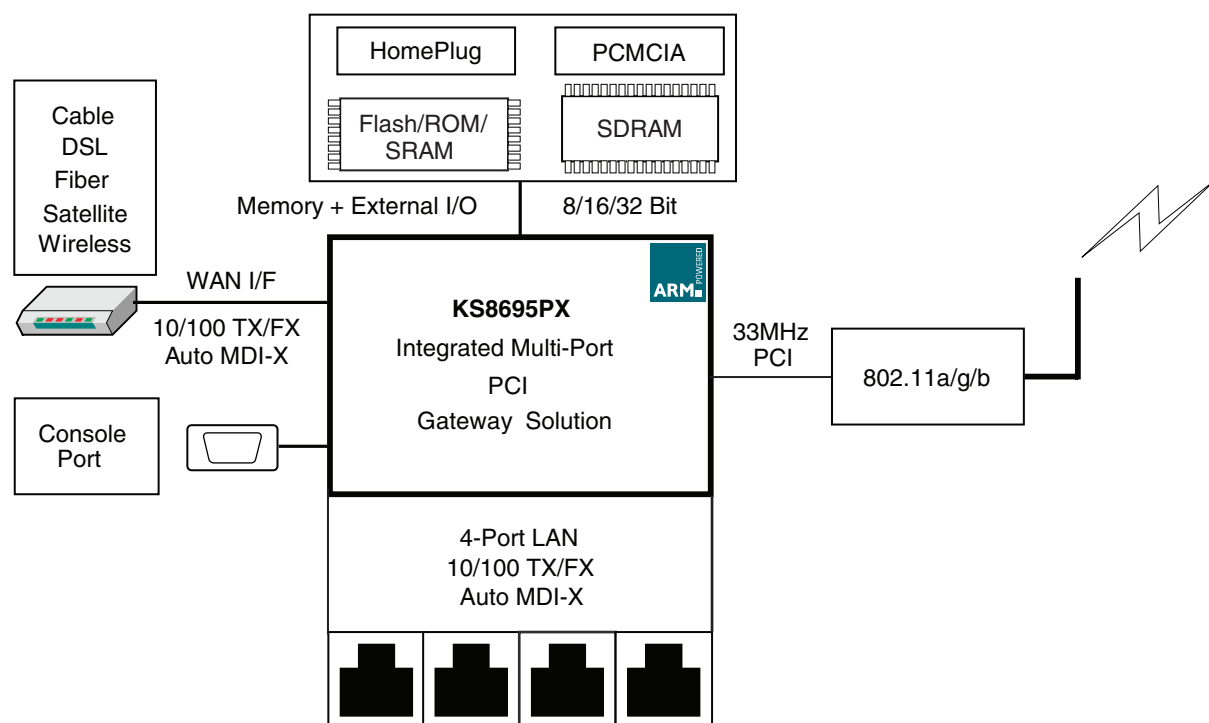


Figure 1. KS8695PX PCI Gateway System Options

## Pin Description

### Signal List Alphabetized by Name

| Pin Number | Pin Name   | Type <sup>(1)</sup> | Pin Function                                        |
|------------|------------|---------------------|-----------------------------------------------------|
| U4         | ADDR0      | O                   | Address Bit.                                        |
| T4         | ADDR1      | O                   | Address Bit.                                        |
| R3         | ADDR10     | O                   | Address Bit.                                        |
| P1         | ADDR11     | O                   | Address Bit.                                        |
| P2         | ADDR12     | O                   | Address Bit.                                        |
| N1         | ADDR13     | O                   | Address Bit.                                        |
| N2         | ADDR14     | O                   | Address Bit.                                        |
| N3         | ADDR15     | O                   | Address Bit.                                        |
| N4         | ADDR16     | O                   | Address Bit.                                        |
| M1         | ADDR17     | O                   | Address Bit.                                        |
| M2         | ADDR18     | O                   | Address Bit.                                        |
| M3         | ADDR19     | O                   | Address Bit.                                        |
| U3         | ADDR2      | O                   | Address Bit.                                        |
| P3         | ADDR20/BA0 | O                   | Address Bit/Bank Address Bit 0 for SDRAM Interface. |
| P4         | ADDR2/BA1  | O                   | Address Bit/Bank Address Bit 1 for SDRAM Interface. |
| T3         | ADDR3      | O                   | Address Bit.                                        |
| U2         | ADDR4      | O                   | Address Bit.                                        |
| U1         | ADDR5      | O                   | Address Bit.                                        |
| T1         | ADDR6      | O                   | Address Bit.                                        |
| T2         | ADDR7      | O                   | Address Bit.                                        |
| R1         | ADDR8      | O                   | Address Bit.                                        |
| R2         | ADDR9      | O                   | Address Bit.                                        |
| E3         | AGND       | Gnd                 | Analog Signal Ground.                               |
| H7         | AGND       | Gnd                 | Analog Signal Ground.                               |
| J7         | AGND       | Gnd                 | Analog Signal Ground.                               |
| K7         | AGND       | Gnd                 | Analog Signal Ground.                               |
| L7         | AGND       | Gnd                 | Analog Signal Ground.                               |
| D14        | CBEN0      | I/O                 | PCI Commands and Byte Enable 0. Active Low.         |
| A11        | CBEN1      | I/O                 | PCI Commands and Byte Enable 1. Active Low.         |
| B9         | CBEN2      | I/O                 | PCI Commands and Byte Enable 2. Active Low.         |
| A6         | CBEN3      | I/O                 | PCI Commands and Byte Enable 3. Active Low.         |
| B10        | CLKRUNN    | I/O                 | Cardbus Clock Run Request Signal. Active Low.       |
| U15        | DATA0      | I/O                 | External Data Bit.                                  |
| T15        | DATA1      | I/O                 | External Data Bit.                                  |
| U12        | DATA10     | I/O                 | External Data Bit.                                  |
| T12        | DATA11     | I/O                 | External Data Bit.                                  |

**Note:**

1. Gnd = Ground.

O = Output.

I/O = Bidirectional.

| Pin Number | Pin Name            | Type <sup>(1)</sup> | Pin Function                                                                      |
|------------|---------------------|---------------------|-----------------------------------------------------------------------------------|
| R12        | DATA12              | I/O                 | External Data Bit.                                                                |
| P12        | DATA13              | I/O                 | External Data Bit.                                                                |
| U11        | DATA14              | I/O                 | External Data Bit.                                                                |
| T11        | DATA15              | I/O                 | External Data Bit.                                                                |
| R11        | DATA16              | I/O                 | External Data Bit.                                                                |
| P11        | DATA17              | I/O                 | External Data Bit.                                                                |
| U10        | DATA18              | I/O                 | External Data Bit.                                                                |
| T10        | DATA19              | I/O                 | External Data Bit.                                                                |
| U14        | DATA2               | I/O                 | External Data Bit.                                                                |
| R10        | DATA20              | I/O                 | External Data Bit.                                                                |
| P10        | DATA21              | I/O                 | External Data Bit.                                                                |
| U9         | DATA22              | I/O                 | External Data Bit.                                                                |
| T9         | DATA23              | I/O                 | External Data Bit.                                                                |
| R9         | DATA24              | I/O                 | External Data Bit.                                                                |
| P9         | DATA25              | I/O                 | External Data Bit.                                                                |
| U8         | DATA26              | I/O                 | External Data Bit.                                                                |
| T8         | DATA27              | I/O                 | External Data Bit.                                                                |
| R8         | DATA28              | I/O                 | External Data Bit.                                                                |
| P8         | DATA29              | I/O                 | External Data Bit.                                                                |
| T14        | DATA3               | I/O                 | External Data Bit.                                                                |
| R7         | DATA30              | I/O                 | External Data Bit.                                                                |
| P7         | DATA31              | I/O                 | External Data Bit.                                                                |
| R14        | DATA4               | I/O                 | External Data Bit.                                                                |
| P14        | DATA5               | I/O                 | External Data Bit.                                                                |
| U13        | DATA6               | I/O                 | External Data Bit.                                                                |
| T13        | DATA7               | I/O                 | External Data Bit.                                                                |
| R13        | DATA8               | I/O                 | External Data Bit.                                                                |
| P13        | DATA9               | I/O                 | External Data Bit.                                                                |
| C11        | DEVSELN             | I/O                 | PCI Device Select Signal. Active Low.                                             |
| R16        | ECSN0               | O                   | External I/O Device Chip Select. Active Low.                                      |
| T16        | ECSN1               | O                   | External I/O Device Chip Select. Active Low.                                      |
| U16        | ECSN2               | O                   | External I/O Device Chip Select. Active Low.                                      |
| T17        | EROEN/<br>WRSTPLS   | O/I                 | ROM/SRAM/FLASH and External I/O Output Enable. Active Low. WRSTO Polarity Select. |
| M17        | ERWEN0/<br>TESTACK  | O                   | External I/O and ROM/SRAM/FLASH Write Byte Enable. Active Low.                    |
| N17        | ERWEN1/<br>TESTREQB | O                   | External I/O and ROM/SRAM/FLASH Write Byte Enable. Active Low.                    |
| P17        | ERWEN2/<br>TESTREQA | O                   | External I/O and ROM/SRAM/FLASH Write Byte Enable. Active Low.                    |

**Note:**

1. O = Output.

I/O = Bidirectional.

O/I = Output in normal mode; input pin during reset.

| Pin Number | Pin Name              | Type <sup>(1)</sup> | Pin Function                                                                    |
|------------|-----------------------|---------------------|---------------------------------------------------------------------------------|
| R17        | ERWEN3/<br>TICTESTENN | O                   | External I/O and ROM/SRAM/FLASH Write Byte Enable. Active Low.                  |
| P16        | EWAITN                | I                   | External Wait. Active Low.                                                      |
| D10        | FRAMEN                | I/O                 | PCI Bus Frame Signal. Active Low.                                               |
| A1         | GND                   | Gnd                 | Signal Ground.                                                                  |
| G7         | GND                   | Gnd                 | Signal Ground.                                                                  |
| G8         | GND                   | Gnd                 | Signal Ground.                                                                  |
| G9         | GND                   | Gnd                 | Signal Ground.                                                                  |
| G10        | GND                   | Gnd                 | Signal Ground.                                                                  |
| G11        | GND                   | Gnd                 | Signal Ground.                                                                  |
| H8         | GND                   | Gnd                 | Signal Ground.                                                                  |
| H9         | GND                   | Gnd                 | Signal Ground.                                                                  |
| H10        | GND                   | Gnd                 | Signal Ground.                                                                  |
| H11        | GND                   | Gnd                 | Signal Ground.                                                                  |
| J8         | GND                   | Gnd                 | Signal Ground.                                                                  |
| J9         | GND                   | Gnd                 | Signal Ground.                                                                  |
| J10        | GND                   | Gnd                 | Signal Ground.                                                                  |
| J11        | GND                   | Gnd                 | Signal Ground.                                                                  |
| K8         | GND                   | Gnd                 | Signal Ground.                                                                  |
| K9         | GND                   | Gnd                 | Signal Ground.                                                                  |
| K10        | GND                   | Gnd                 | Signal Ground.                                                                  |
| K11        | GND                   | Gnd                 | Signal Ground.                                                                  |
| L8         | GND                   | Gnd                 | Signal Ground.                                                                  |
| L9         | GND                   | Gnd                 | Signal Ground.                                                                  |
| L10        | GND                   | Gnd                 | Signal Ground.                                                                  |
| L11        | GND                   | Gnd                 | Signal Ground.                                                                  |
| C4         | GNT1N                 | O                   | PCI Bus Grant 2. Active Low. Output for Host Bridge Mode and Guest Bridge Mode. |
| C3         | NC                    | –                   | This pin must be left as no connect.                                            |
| C2         | NC                    | –                   | This pin must be left as no connect.                                            |
| G17        | GPIO0/EINT0           | I/O                 | General Purpose I/O Pin. External Interrupt Request Pin.                        |
| G16        | GPIO1/EINT1           | I/O                 | General Purpose I/O Pin. External Interrupt Request Pin.                        |
| K17        | GPIO10                | I/O                 | General Purpose I/O Pin.                                                        |
| K16        | GPIO11                | I/O                 | General Purpose I/O Pin.                                                        |
| K15        | GPIO12                | I/O                 | General Purpose I/O Pin.                                                        |
| K14        | GPIO13                | I/O                 | General Purpose I/O Pin.                                                        |
| L17        | GPIO14                | I/O                 | General Purpose I/O Pin.                                                        |

**Note:**

1. Gnd = Ground.

I = Input.

O = Output.

I/O = Bidirectional.



| Pin Number | Pin Name    | Type <sup>(1)</sup> | Pin Function                                                                |
|------------|-------------|---------------------|-----------------------------------------------------------------------------|
| L16        | GPIO15      | I/O                 | General Purpose I/O Pin.                                                    |
| H17        | GPIO2/EINT2 | I/O                 | General Purpose I/O Pin. External Interrupt Request Pin.                    |
| H16        | GPIO3/EINT3 | I/O                 | General Purpose I/O Pin. External Interrupt Request Pin.                    |
| H15        | GPIO4/TOUT0 | I/O                 | General Purpose I/O Pin. Timer 0 Output Pin.                                |
| H14        | GPIO5/TOUT1 | I/O                 | General Purpose I/O Pin. Timer 1 Output Pin.                                |
| J17        | GPIO6       | I/O                 | General Purpose I/O Pin.                                                    |
| J16        | GPIO7       | I/O                 | General Purpose I/O Pin.                                                    |
| J15        | GPIO8       | I/O                 | General Purpose I/O Pin.                                                    |
| J14        | GPIO9       | I/O                 | General Purpose I/O Pin.                                                    |
| D7         | IDSEL       | I                   | Initialization Device Select. Active High.                                  |
| A9         | IRDYN       | I/O                 | PCI Initiator Ready Signal. Active Low.                                     |
| F1         | ISET        | I                   | Set PHY Transmit Output Current. Connect to Ground with 3.01kΩ 1% Resistor. |
| B17        | L1LED0      | O                   | LAN Port 1 LED Programmable Indicator 0. Active Low.                        |
| B16        | L1LED1      | O                   | LAN Port 1 LED Programmable Indicator 1. Active Low.                        |
| C17        | L2LED0      | O                   | LAN Port 2 LED Programmable Indicator 0. Active Low.                        |
| C16        | L2LED1      | O                   | LAN Port 2 LED Programmable Indicator 1. Active Low.                        |
| D17        | L3LED0      | O                   | LAN Port 3 LED Programmable Indicator 0. Active Low.                        |
| D16        | L3LED1      | O                   | LAN Port 3 LED Programmable Indicator 1. Active Low.                        |
| E17        | L4LED0      | O                   | LAN Port 4 LED Programmable Indicator 0. Active Low.                        |
| E16        | L4LED1      | O                   | LAN Port 4 LED Programmable Indicator 1. Active Low.                        |
| H4         | LANRXM1     | I                   | LAN Port 1 PHY Receive Signal – (differential).                             |
| J4         | LANRXM2     | I                   | LAN Port 2 PHY Receive Signal – (differential).                             |
| K4         | LANRXM3     | I                   | LAN Port 3 PHY Receive Signal – (differential).                             |
| L4         | LANRXM4     | I                   | LAN Port 4 PHY Receive Signal – (differential).                             |
| H3         | LANRXP1     | I                   | LAN Port 1 PHY Receive Signal + (differential).                             |
| J3         | LANRXP2     | I                   | LAN Port 2 PHY Receive Signal + (differential).                             |
| K3         | LANRXP3     | I                   | LAN Port 3 PHY Receive Signal + (differential).                             |
| L3         | LANRXP4     | I                   | LAN Port 4 PHY Receive Signal + (differential).                             |
| H2         | LANTXM1     | O                   | LAN Port 1 PHY Transmit Signal – (differential).                            |
| J2         | LANTXM2     | O                   | LAN Port 2 PHY Transmit Signal – (differential).                            |
| K2         | LANTXM3     | O                   | LAN Port 3 PHY Transmit Signal – (differential).                            |
| L2         | LANTXM4     | O                   | LAN Port 4 PHY Transmit Signal – (differential).                            |
| H1         | LANTXP1     | O                   | LAN Port 1 PHY Transmit Signal + (differential).                            |
| J1         | LANTXP2     | O                   | LAN Port 2 PHY Transmit Signal + (differential).                            |
| K1         | LANTXP3     | O                   | LAN Port 3 PHY Transmit Signal + (differential).                            |
| L1         | LANTXP4     | O                   | LAN Port 4 PHY Transmit Signal + (differential).                            |
| E4         | M66EN       | I                   | PCI 66 MHz Enable.                                                          |
| D2         | MPCIACTN    | O                   | MiniPCI Active Signal. Active Low.                                          |
| A16        | PAD0        | I/O                 | PCI Address and Data 0.                                                     |

**Note:**

1. I = Input.

O = Output.

I/O = Bidirectional.

| Pin Number | Pin Name | Type <sup>(1)</sup> | Pin Function                                                             |
|------------|----------|---------------------|--------------------------------------------------------------------------|
| A15        | PAD1     | I/O                 | PCI Address and Data 1.                                                  |
| B13        | PAD10    | I/O                 | PCI Address and Data 10.                                                 |
| D13        | PAD11    | I/O                 | PCI Address and Data 11.                                                 |
| A12        | PAD12    | I/O                 | PCI Address and Data 12.                                                 |
| C12        | PAD13    | I/O                 | PCI Address and Data 13.                                                 |
| B12        | PAD14    | I/O                 | PCI Address and Data 14.                                                 |
| D12        | PAD15    | I/O                 | PCI Address and Data 15.                                                 |
| C9         | PAD16    | I/O                 | PCI Address and Data 16.                                                 |
| A8         | PAD17    | I/O                 | PCI Address and Data 17.                                                 |
| D9         | PAD18    | I/O                 | PCI Address and Data 18.                                                 |
| B8         | PAD19    | I/O                 | PCI Address and Data 19.                                                 |
| C15        | PAD2     | I/O                 | PCI Address and Data 2.                                                  |
| D8         | PAD20    | I/O                 | PCI Address and Data 20.                                                 |
| A7         | PAD21    | I/O                 | PCI Address and Data 21.                                                 |
| C7         | PAD22    | I/O                 | PCI Address and Data 22.                                                 |
| B7         | PAD23    | I/O                 | PCI Address and Data 23.                                                 |
| C6         | PAD24    | I/O                 | PCI Address and Data 24.                                                 |
| B6         | PAD25    | I/O                 | PCI Address and Data 25.                                                 |
| D6         | PAD26    | I/O                 | PCI Address and Data 26.                                                 |
| A5         | PAD27    | I/O                 | PCI Address and Data 27.                                                 |
| C5         | PAD28    | I/O                 | PCI Address and Data 28.                                                 |
| B5         | PAD29    | I/O                 | PCI Address and Data 29.                                                 |
| B15        | PAD3     | I/O                 | PCI Address and Data 3.                                                  |
| D5         | PAD30    | I/O                 | PCI Address and Data 30.                                                 |
| A4         | PAD31    | I/O                 | PCI Address and Data 31.                                                 |
| D15        | PAD4     | I/O                 | PCI Address and Data 4.                                                  |
| A14        | PAD5     | I/O                 | PCI Address and Data 5.                                                  |
| C14        | PAD6     | I/O                 | PCI Address and Data 6.                                                  |
| B14        | PAD7     | I/O                 | PCI Address and Data 7.                                                  |
| A13        | PAD8     | I/O                 | PCI Address and Data 8.                                                  |
| C13        | PAD9     | I/O                 | PCI Address and Data 9.                                                  |
| C8         | PAR      | I/O                 | PCI Parity.                                                              |
| D3         | PBMS     | I                   | PCI Bridge Mode Select. '1' = Host Bridge Mode. '0' = Guest Bridge Mode. |
| D4         | PCLK     | I                   | PCI Bus Clock.                                                           |
| A2         | PCLKOUT0 | O                   | PCI Clock Output 0.                                                      |
| B1         | PCLKOUT1 | O                   | PCI Clock Output 1.                                                      |
| C1         | NC       | –                   | This pin must be left as no connect.                                     |
| D1         | NC       | –                   | This pin must be left as no connect.                                     |
| B11        | PERRN    | I/O                 | PCI Parity Error Signal. Active Low.                                     |
| A3         | PRSTN    | I                   | PCI Reset. Active Low.                                                   |

**Note:**

1. I = Input.

O = Output.

I/O = Bidirectional.

| Pin Number | Pin Name            | Type <sup>(1)</sup> | Pin Function                                                                     |
|------------|---------------------|---------------------|----------------------------------------------------------------------------------|
| P15        | RCSN0               | O                   | ROM/SRAM/FLASH Chip Select. Active Low.                                          |
| R15        | RCSN1               | O                   | ROM/SRAM/FLASH Chip Select. Active Low.                                          |
| B4         | REQ1N               | I                   | PCI Bus Request 1. Active Low. Input for Host Bridge Mode and Guest Bridge Mode. |
| B3         | NC                  | –                   | This pin must be left as no connect.                                             |
| B2         | NC                  | –                   | This pin must be left as no connect.                                             |
| A17        | RESETN              | I                   | KS8695PX Chip Reset. Active Low.                                                 |
| T5         | SDCASN              | O                   | SDRAM Column Address Strobe, Active Low.                                         |
| P5         | SDCSN0              | O                   | SDRAM Chip Select. Active Low Chip Select Pins for SDRAM.                        |
| R4         | SDCSN1              | O                   | SDRAM Chip Select. Active Low Chip Select Pins for SDRAM.                        |
| T7         | SDICLK              | I                   | SDRAM Clock In.                                                                  |
| U7         | SDOCLK              | O                   | System/SDRAM Clock Out.                                                          |
| U6         | SDQM0               | O                   | SDRAM Data Input/Output Mask.                                                    |
| T6         | SDQM1               | O                   | SDRAM Data Input/Output Mask.                                                    |
| R6         | SDQM2               | O                   | SDRAM Data Input/Output Mask.                                                    |
| P6         | SDQM3               | O                   | SDRAM Data Input/Output Mask.                                                    |
| R5         | SDRASN              | O                   | SDRAM Row Address Strobe, Active Low.                                            |
| U5         | SDWEN               | O                   | SDRAM Write Enable. Active Low.                                                  |
| A10        | SERRN               | O                   | PCI System Error Signal. Active Low.                                             |
| D11        | STOPN               | I/O                 | PCI Stop Signal. Active Low.                                                     |
| G14        | TCK                 | I                   | JTAG Test Clock.                                                                 |
| F14        | TDI                 | I                   | JTAG Test Data In.                                                               |
| F15        | TDO                 | O                   | JTAG Test Data Out.                                                              |
| M4         | TEST1               | I                   | PHY Test Pin (factory test signal).                                              |
| F4         | TEST2               | I                   | PHY Test Pin (factory test signal).                                              |
| F17        | TESTEN              | I                   | Chip Test Enable (factory test signal).                                          |
| G15        | TMS                 | I                   | JTAG Test Mode Select                                                            |
| C10        | TRDYN               | I/O                 | PCI Target Ready Signal. Active Low.                                             |
| F16        | TRSTN               | I                   | JTAG Test Reset. Active Low.                                                     |
| M14        | UCTSN/<br>BISTEN    | I                   | UART Data Set Ready. Active Low. BIST Enable (factory test signal).              |
| L15        | UDCDN/<br>SCANEN    | I                   | UART Data Carrier Detect. Scan Enable (factory test signal).                     |
| M16        | UDSRN               | I                   | UART Data Set Ready. Active Low.                                                 |
| N15        | UDTRN/<br>DBGENN    | O                   | UART Data Terminal Ready. Active Low. Debug Enable (factory test signal).        |
| L14        | URIN/TSTRST         | I                   | UART Ring Indicator/Chip Test Reset (factory test signal).                       |
| M15        | URTSN/<br>CPUCLKSEL | O/I                 | UART Request to Send/CPU Clock Select.                                           |

**Note:**

1. I = Input.

O = Output.

I/O = Bidirectional.

O/I = Output in normal mode; input pin during reset.

| Pin Number | Pin Name | Type <sup>(1)</sup> | Pin Function                          |
|------------|----------|---------------------|---------------------------------------|
| N16        | URXD     | I                   | UART Receive Data.                    |
| N14        | UTXD     | O                   | UART Transmit Data.                   |
| E7         | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| E8         | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| E9         | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| E10        | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| F7         | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| F8         | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| F9         | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| F10        | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| M7         | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| M8         | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| M9         | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| H12        | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| H13        | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| J12        | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| J13        | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| K12        | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| K13        | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| N7         | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| N8         | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| N9         | VDD1.8   | Pwr                 | 1.8V Digital Core $V_{DD}$ .          |
| E11        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| E12        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| E13        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| F11        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| F12        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| F13        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| G12        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| G13        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| L12        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| L13        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| M10        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| M11        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| M12        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| M13        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| N10        | VDD3.3   | Pwr                 | 3.3V digital I/O Circuitry $V_{DD}$ . |
| N11        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| N12        | VDD3.3   | Pwr                 | 3.3V Digital I/O Circuitry $V_{DD}$ . |
| N13        | VDD3.3   | Pwr                 | 3.3V digital I/O Circuitry $V_{DD}$ . |

**Note:**

1. Pwr = Power.

I = Input.

O = Output.

| Pin Number | Pin Name          | Type <sup>(1)</sup> | Pin Function                                         |
|------------|-------------------|---------------------|------------------------------------------------------|
| E5         | VDDA1.8           | Pwr                 | 1.8V Analog V <sub>DD</sub> .                        |
| E6         | VDDA1.8           | Pwr                 | 1.8V Analog V <sub>DD</sub> .                        |
| F5         | VDDA1.8           | Pwr                 | 1.8V Analog V <sub>DD</sub> .                        |
| F6         | VDDA1.8           | Pwr                 | 1.8V Analog V <sub>DD</sub> .                        |
| G5         | VDDA1.8           | Pwr                 | 1.8V Analog V <sub>DD</sub> .                        |
| G6         | VDDA1.8           | Pwr                 | 1.8V Analog V <sub>DD</sub> .                        |
| H5         | VDDA1.8           | Pwr                 | 1.8V Analog V <sub>DD</sub> .                        |
| H6         | VDDA1.8           | Pwr                 | 1.8V Analog V <sub>DD</sub> .                        |
| J5         | VDDA1.8           | Pwr                 | 1.8V Analog V <sub>DD</sub> .                        |
| J6         | VDDA1.8           | Pwr                 | 1.8V Analog V <sub>DD</sub> .                        |
| K5         | VDDA3.3           | Pwr                 | 3.3V Analog V <sub>DD</sub> .                        |
| K6         | VDDA3.3           | Pwr                 | 3.3V Analog V <sub>DD</sub> .                        |
| L5         | VDDA3.3           | Pwr                 | 3.3V analog V <sub>DD</sub> .                        |
| L6         | VDDA3.3           | Pwr                 | 3.3V analog V <sub>DD</sub> .                        |
| M5         | VDDA3.3           | Pwr                 | 3.3V analog V <sub>DD</sub> .                        |
| M6         | VDDA3.3           | Pwr                 | 3.3V analog V <sub>DD</sub> .                        |
| N5         | VDDA3.3           | Pwr                 | 3.3V analog V <sub>DD</sub> .                        |
| N6         | VDDA3.3           | Pwr                 | 3.3V analog V <sub>DD</sub> .                        |
| F2         | WANFXSD           | I                   | WAN Fiber Signal Detect.                             |
| G4         | WANRXM            | I                   | WAN PHY Receive Signal – (differential).             |
| G3         | WANRXP            | I                   | WAN PHY Receive Signal + (differential).             |
| G2         | WANTXM            | O                   | WAN PHY Transmit Signal – (differential).            |
| G1         | WANTXP            | O                   | WAN PHY Transmit Signal + (differential).            |
| E15        | WLED0/<br>B0SIZE0 | O/I                 | WAN LED Programmable Indicator 0. Bank 0 Size Bit 0. |
| E14        | WLED1/<br>B0SIZE1 | O/I                 | WAN LED Programmable Indicator 1. Bank 0 Size Bit 1. |
| U17        | WRSTO             | O                   | Watchdog Timer Reset Output.                         |
| E1         | XCLK1             | I                   | External Clock In.                                   |
| E2         | XCLK2             | I                   | External Clock In (negative polarity).               |

**Note:**

1. Pwr = Power.

I = Input.

O = Output.

O/I = Output in normal mode; input pin during reset.

## Pin Description

|   | 1        | 2        | 3              | 4              | 5       | 6       | 7      | 8      | 9      | 10      | 11      | 12     | 13     | 14               | 15                  | 16              | 17               |
|---|----------|----------|----------------|----------------|---------|---------|--------|--------|--------|---------|---------|--------|--------|------------------|---------------------|-----------------|------------------|
| A | GND      | PCLKOUT0 | PRSTN          | PAD31          | PAD27   | CBEN3   | PAD21  | PAD17  | URDYN  | SERRN   | CBEN1   | PAD12  | PAD8   | PAD5             | PAD1                | PAD0            | RESETN           |
| B | PCLKOUT1 | NC       | NC             | REQ1N          | PAD29   | PAD25   | PAD23  | PAD19  | CBEN2  | CLKRUNN | PERRN   | PAD14  | PAD10  | PAD7             | PAD3                | L1LED1          | L1LED0           |
| C | NC       | NC       | NC             | GNT1N          | PAD28   | PAD24   | PAD22  | PAR    | PAD16  | TROYN   | DEVSELN | PAD13  | PAD9   | PAD6             | PAD2                | L2LED1          | L2LED0           |
| D | NC       | MPCIACTN | PMBS           | ECLK           | PAD30   | PAD26   | IOSEL  | PAD20  | PAD18  | FRAMEN  | STOPN   | PAD15  | PAD11  | CBEN0            | PAD4                | L3LED1          | L3LED0           |
| E | XCLK1    | XCLK2    | AGND           | M86EN          | VPLL1.8 | VDDA1.8 | VDD1.8 | VDD1.8 | VDD1.8 | VDD1.8  | VDD3.3  | VDD3.3 | VDD3.3 | WLED0/<br>BOSIZE |                     | L4LED1          | L4LED0           |
| F | RESET    | WANFXSD  | LAN<br>FXSD1   | TEST2          | VDDA1.8 | VDDA1.8 | VDD1.8 | VDD1.8 | VDD1.8 | VDD1.8  | VDD3.3  | VDD3.3 | VDD3.3 | TDI              | TDO                 | TRSTN           | TESTEN           |
| G | WANTXP   | WANTXM   | WANRXP         | WANRXM         | VDDA1.8 | VDDA1.8 | GND    | GND    | GND    | GND     | GND     | VDD3.3 | VDD3.3 | TCK              | TMS                 | GPIO1/<br>EINT1 | GPIO0/<br>EINT0  |
| H | LANTXP1  | LANTXM1  | LANRXP1        | LANRXM1        | VDDA1.8 | VDDA1.8 | AGND   | GND    | GND    | GND     | GND     | VDD1.8 | VDD1.8 | GPIO5/<br>TOUT1  | GPIO4/<br>TOUT0     | GPIO3/<br>EINT3 | GPIO2/<br>EINT2  |
| J | LANTXP2  | LANTXM2  | LANRXP2        | LANRXM2        | VDDA1.8 | VDDA1.8 | AGND   | GND    | GND    | GND     | GND     | VDD1.8 | VDD1.8 | GPIO9            | GPIO8               | GPIO7           | GPIO6            |
| K | LANTXP3  | LANTXM3  | LANRXP3        | LANRXM3        | VDDA3.3 | VDDA3.3 | AGND   | GND    | GND    | GND     | GND     | VDD1.8 | VDD1.8 | GPIO13           | GPIO12              | GPIO11          | GPIO10           |
| L | LANTXP4  | LANTXM4  | LANRXP4        | LANRXM4        | VDDA3.3 | VDDA3.3 | AGND   | GND    | GND    | GND     | GND     | VDD3.3 | VDD3.3 | URJN/<br>TSTST   | UDCN/<br>SCANEN     | GPIO15          | GPIO14           |
| M | ADDR17   | ADDR18   | ADDR19         | TEST1          | VDDA3.3 | VDDA3.3 | VDD1.8 | VDD1.8 | VDD1.8 | VDD3.3  | VDD3.3  | VDD3.3 | VDD3.3 | UCTSN/<br>BISTEN | URTSN/<br>CPUCLKSEL | UDSRN           | ERWEN0           |
| N | ADDR13   | ADDR14   | ADDR15         | ADDR16         | VDDA3.3 | VDDA3.3 | VDD1.8 | VDD1.8 | VDD1.8 | VDD3.3  | VDD3.3  | VDD3.3 | VDD3.3 | UTXD             | UDTRN               | URXD            | ERWEN1           |
| P | ADDR11   | ADDR12   | ADDR20/<br>BA0 | ADDR21/<br>BA1 | SDCSN0  | SDQM3   | DATA31 | DATA29 | DATA25 | DATA21  | DATA17  | DATA13 | DATA9  | DATA5            | RCSN0               | EWAITN          | ERWEN2           |
| R | ADDR8    | ADDR9    | ADDR10         | SDCSN1         | SDRASN  | SDQM2   | DATA30 | DATA28 | DATA24 | DATA20  | DATA16  | DATA12 | DATA8  | DATA4            | RCSN1               | ECSN0           | ERWEN3           |
| T | ADDR6    | ADDR7    | ADDR3          | ADDR1          | SDCASN  | SDQM1   | SDCLK  | DATA27 | DATA23 | DATA19  | DATA15  | DATA11 | DATA7  | DATA3            | DATA1               | ECSN1           | EREN/<br>WRSTPLS |
| U | ADDR5    | ADDR4    | ADDR2          | ADDR0          | SDWEN   | SDQM0   | SDCLKK | DATA26 | DATA22 | DATA18  | DATA14  | DATA10 | DATA6  | DATA2            | DATA0               | ECSN2           | WRSTO            |

PCI Signals

UART Signals

JTAG Signals

Miscellaneous

LED Drivers

Memory Interface

GPIO

Analog

VDD3.3

VDDA1.8

VDD1.8

GND

VDDA3.3

AGND

### Figure 2. KS8695PX Pin Mapping (Top View)

## Functional Description

### Introduction

Micrel's KS8695PX, a member of the CENTAUR line of integrated processors, is a high-performance router-on-a-chip solution for Ethernet and 802.11 a/g/b based embedded systems. Designed for use in communication's routers, it integrates a PCI to AHB bridge solution for interfacing with 32-bit PCI, miniPCI, and cardbus devices. The KS8695PX combines a proven third generation 5-port managed switch, an ARM9 RISC processor with MMU, and five physical transceiver units (PHYs) including their corresponding MAC units with Micrel's XceleRouter technology.

The KS8695PX is built around the 16/32-bit ARM922T RISC processor, which is a scalable, high-performance, microprocessor developed for highly integrated system-on-a-chip applications. It also offers a configurable 8KB I-cache and an 8KB D-cache that reduces memory access latency for high-performance applications. The simple, elegant, and fully static design of the KS8695PX is especially suitable for cost-effective, power-sensitive applications.

The KS8695PX contains five 10/100 PHYs: four are for the local area network (LAN) and one is for the wide area network (WAN). Connected to the PHYs are five corresponding MAC units with an integrated Layer 2 managed switch. The combining of the switch and the analog PHYs make the KS8695PX an extremely prudent solution for SOHO router applications, saving both board space and BOM costs. The Layer 2 switch contains a 16Kx32 SRAM on-chip memory for frame buffering. The embedded frame buffer memory is designed with a 1.4Gbps on-chip memory bus. This allows the KS8695PX to perform full non-blocking frame switching and/or routing on the fly for many applications.

For the media interface, the KS8695PX supports 10BASE-T and 100BASE-TX, as specified by the IEEE 802.3 standard, and 100 BASE-FX on the WAN port and on one LAN port.

The KS8695PX supports two modes of operation in the PCI bus environment: host bridge mode and guest bridge mode. In the host bridge mode, the ARM9 processor acts as the host of the entire system. It configures other PCI devices and coordinates their transactions, including initiating transactions between the PCI devices and AHB bus subsystem. In host bridge mode, all I/O registers, including those for the embedded switch, are configured by the ARM922T processor through the on-chip AMBA bus interface.

In guest bridge mode, all of the I/O registers are programmed by either the external host CPU on the PCI bus or the local ARM922T host processor through the AMBA bus. In guest bridge mode, the KS8695PX also functions as a slave on the PCI bus. The KS8695PX can be configured by either the ARM9 CPU or the PCI host CPU. In both cases, the KS8695PX memory subsystem is accessible from either the PCI host or the ARM9 CPU. Communications between the external host CPU and the ARM922T is accomplished through message passing or through shared memory.

### CPU Features

- 166MHz ARM922T RISC processor core
- On-chip AMBA bus 2.0 interfaces
- 16-bit thumb programming to relax memory requirement
- 8KB I-cache and 8KB D-cache
- Little-endian mode supported
- Configurable memory management unit
- Supports reduced CPU and system clock speed for power savings

### PCI to AHB Bridge Features

- Support 33MHz, 32-bit data PCI bus
- Integrated PCI bridge support for interfacing with 32-bit miniPCI or cardbus devices
- Independent AHB and PCI clock speed
- Supports 125MHz AHB speed
- Supports PCI revision 2.1 protocols
- Supports AHB bus 2.0 interfaces
- Supports both regular and memory-mapped I/O on the PCI interface
- Integrated PCI arbiter with power-on option to enable or disable
- Support Round Robin arbitration with three external PCI devices and one internal device
- Supports AHB burst transfers up to 16 data words
- Configurable PCI registers by host CPU ARM922T
- Supports bus mastership from PCI to AHB or AHB to PCI bus

### Switch Engine

- 5-Port 10/100 integrated switch with one WAN and four LAN physical layer transceivers
- 16Kx32 on-chip SRAM for frame buffering
- 1.4Gbps on-chip memory bandwidth for wire-speed frame switching
- 10Mbps and 100Mbps modes of operation for both full and half duplex

## Switch Engine (continued)

- Supports 802.1Q tag-based VLAN and port-based VLAN
- Supports 8.2,1p-based priority, DiffServ priority, and port-based priority
- Integrated address look-up engine, supports 1K absolute MAC addresses
- Automatic address learning, address aging, and address migration
- Broadcast storm protection
- Full-duplex IEEE 802.3x flow control
- Half-duplex back pressure flow control
- Supports IGMP snooping
- Spanning Tree Protocol support

## Advanced Memory Controller Features

- Supports glueless connection to two banks of ROM/SRAM/FLASH memory with programmable 8/16/32 bit data bus and programmable access timing
- Supports glueless connection to two SDRAM banks with programmable 8/16/32-bit data bus and programmable RAS/CAS latency
- Supports three external I/O banks with programmable 8/16/32-bit data bus and programmable access timing
- Programmable system clock speed for power management
- Automatic address line mapping for 8/16/32-bit accesses on Flash, ROM, SRAM, and SDRAM interfaces

## Direct Memory Access (DMA) Engines

- Independent MAC DMA engine with programmable burst mode for WAN port
- Independent MAC DMA engine with programmable burst mode for LAN ports
- Supports little-endian byte ordering for memory buffers and descriptors
- Contains large independent receive and transmit FIFOs (3KB receive/3KB transmit) for back-to-back packet receive, and guaranteed no under-run packet transmit
- Data alignment logic and scatter gather capability

## Protocol Engine/XceleRouter Technology

- Supports IPv4 IP header/TCP/UDP packet checksum generation for host CPU offloading
- Supports IPv4 packet filtering based on checksum errors

## Network Interface

- Features five MAC units and five PHY units
- Supports 10BASE-T and 100BASE-TX on all LAN ports and one WAN port. Also supports 100BASE-FX on the WAN port and on one LAN port
- Supports automatic CRC generation and checking
- Supports automatic error packet discard
- Supports IEEE 802.3 auto-negotiation algorithm of full-duplex and half-duplex operation for 10Mbps and 100Mbps
- Supports full/half-duplex operation on PHY interfaces
- Fully compliant with IEEE 802.3 Ethernet standards
- IEEE 802.3 full-duplex flow control and half-duplex backpressure collision flow control
- Supports MDI/MDI-X auto-crossover

## Peripherals

- Twenty-eight interrupt sources, including four external interrupt sources
- Normal or fast interrupt mode (IRQ, FIQ) supported
- Prioritized interrupt handling
- Sixteen programmable general purpose I/O. Pins individually configurable to input, output, or I/O mode for dedicated signals.
- Two programmable 32-bit timers with watchdog timer capability
- High-speed UART interface up to 115kbps

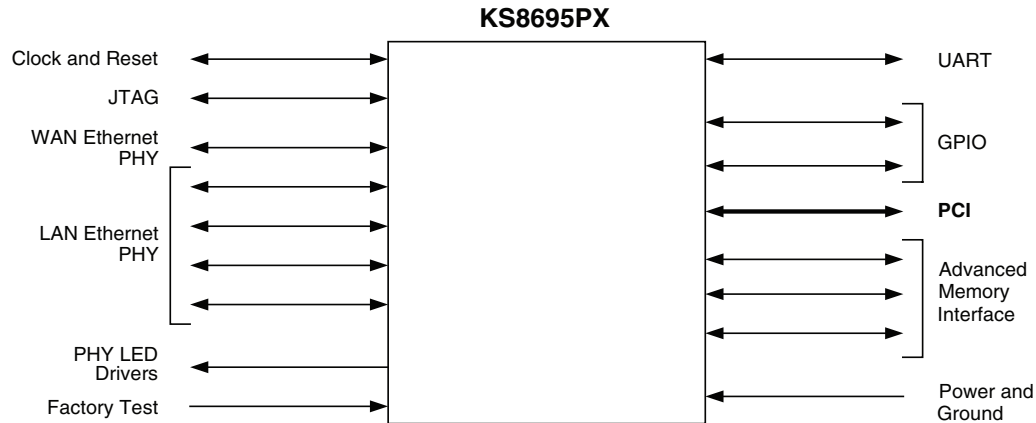
## Other Features

- Integrated PLL to generate CPU and system clocks
- JTAG development interface for ICE connection
- 19mm x 19mm 289-pin PBGA
- 1.8V CMOS for core and 3.3V for I/O



## Signal Description

### System Level Hardware Interfaces



**Figure 3. System Level Interfaces**

At the system level the KS8695PX features the following interfaces:

- Clock interface for crystal or external oscillator
- JTAG development interface
- One WAN Ethernet physical interface
- Four LAN Ethernet physical interfaces
- PHY LED drivers
- One high-speed UART interface
- Sixteen GPIO pins
- 33MHz, 32-bit PCI interface supporting three external masters
- Advanced memory interface
  - Programmable synchronous bus rate
  - Programmable asynchronous interface timing
  - Independently programmable data bus width for static and synchronous memory
  - Glueless connection to SDRAM
  - Glueless connection to flash memory or ROM
- Factory test
- Power and ground

### Configuration Pins

| Configuration          | Pin Name        | Pin #    | Settings                                                                                             |
|------------------------|-----------------|----------|------------------------------------------------------------------------------------------------------|
| Bank0 Flash Data Width | B0SIZE[1:0]     | E14, E15 | '00' = reserved<br>'01' = byte wide<br>'10' = half word wide (16 bits)<br>'11' = word wide (32 bits) |
| WRSTO Polarity         | EROEN/WRSTPLS   | U17      | '0' = active high<br>'1' = active low                                                                |
| CPU Clock Select       | URTSN/CPUCLKSEL | M15      | '0' = normal mode (PLL)<br>'1' = bypass internal PLL                                                 |
| PCI Bridge Mode        | PBMS            | D3       | '0' = guest bridge mode<br>'1' = host bridge mode                                                    |

**Table 1. Configuration Pins**

### Reset

The KS8695PX has a single reset input that can be driven by a system reset circuit or a simple power on reset circuit. The KS8695PX also features a reset output (WRSTO) that can be used to reset other devices in the system. WRSTO can be configured as either an active high reset or an active low reset through a strap-in option on pin U17, as shown in Table 1. The KS8695PX also has a built in watchdog timer. When the watchdog timer is programmed and the timer setting expires, the KS8695PX resets itself and also asserts WRSTO to reset the other devices in the system. Figure 3 shows a typical system using the KS8695PX WRSTO as the system reset.

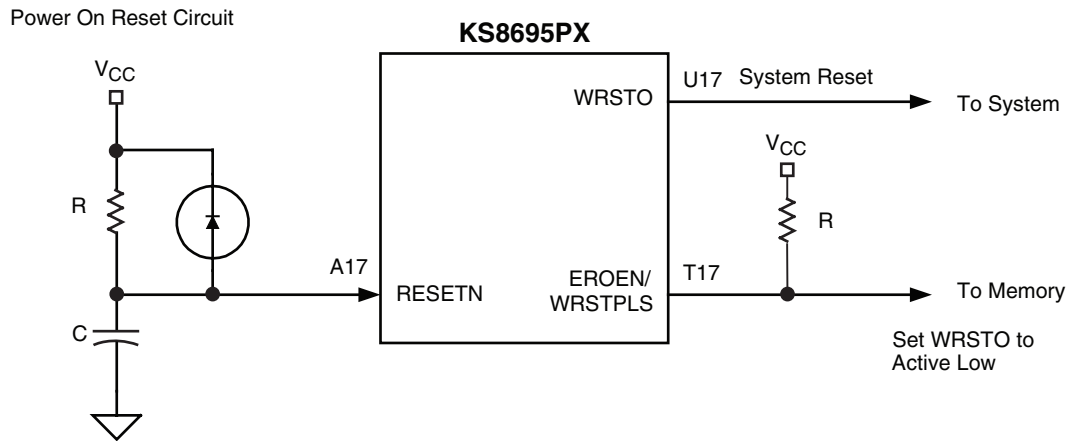


Figure 4. Example of a Reset Circuit

## System Clock

The clock to the KS8695PX is supplied by either a 25MHz  $\pm 50$ ppm crystal or by an oscillator. If an oscillator is used, it must be connected to the X1 input (pin E1) on the KS8695PX. If a crystal is used, it must be connected with a circuit similar to the one shown below. The 25MHz input clock is used by an internal PLL to generate the programmable SDOCLK. SDOCLK is the system clock and can be programmed from 25MHz to 125MHz using the system clock and bus control register at offset 0x0004. The CPUCLKSEL strap-in option on pin M15 needs to be pulled low for normal operation. SDCLK is used to register the data read from the SDRAM back into the KS8695PX. The system designer must ensure that SDRAM timing is met when routing SDOCLK back to SDICLK.

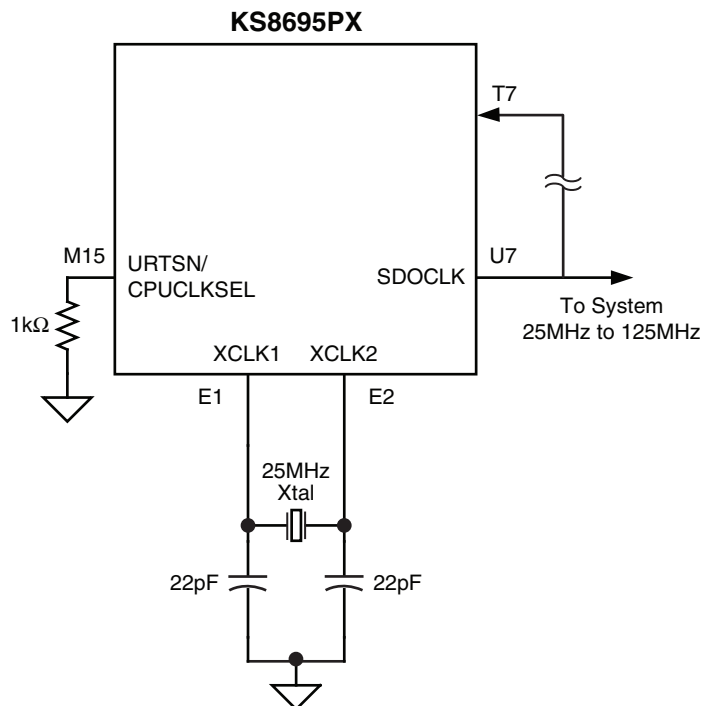


Figure 5. Typical Clock Circuit

## Memory Interface

The KS8695PX has a glueless interface for SDRAM and static memory, i.e. ROM, SRAM, and Flash. It supports up to two banks of static memory (Figure 6), up to two banks of SDRAM (Figure 7), and three banks of external I/O (Figure 8). The total address space for the KS8695PX is 64MB. This includes SDRAM, static memory, external I/O, and the KS8695PX's own 64KB of register space.

The memory interface for the SDRAM and static memory has a special automatic address mapping feature. This allows the designer to connect address bit 0 on the memory to ADDR[0] on the KS8695PX and address bit 1 on the memory to ADDR[1] on the memory, regardless of whether the designer is trying to achieve word, half word, or byte addressing.

The KS8695PX memory controller performs the address mapping internally. This permits the designer to use the maximum amount of address bits, instead of losing one or two bits because of address mapping. For external I/O, however, the designer still needs to take care of the address mapping (see Figure 8).

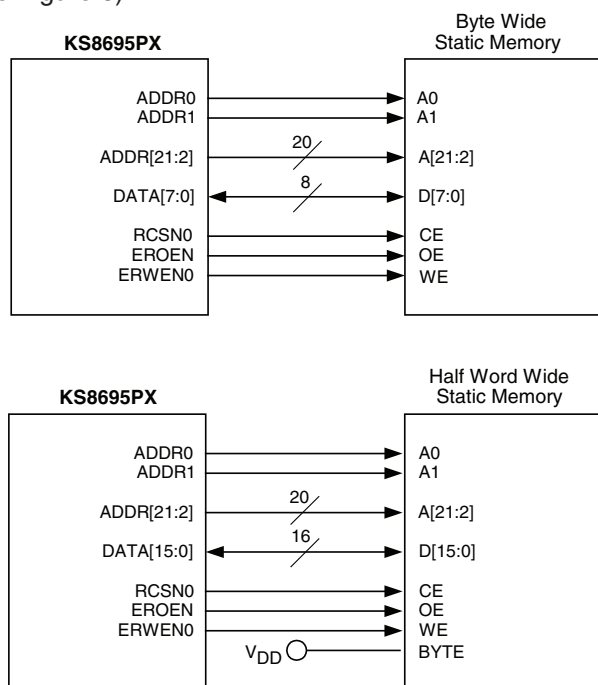


Figure 6. Static Memory Interface Examples

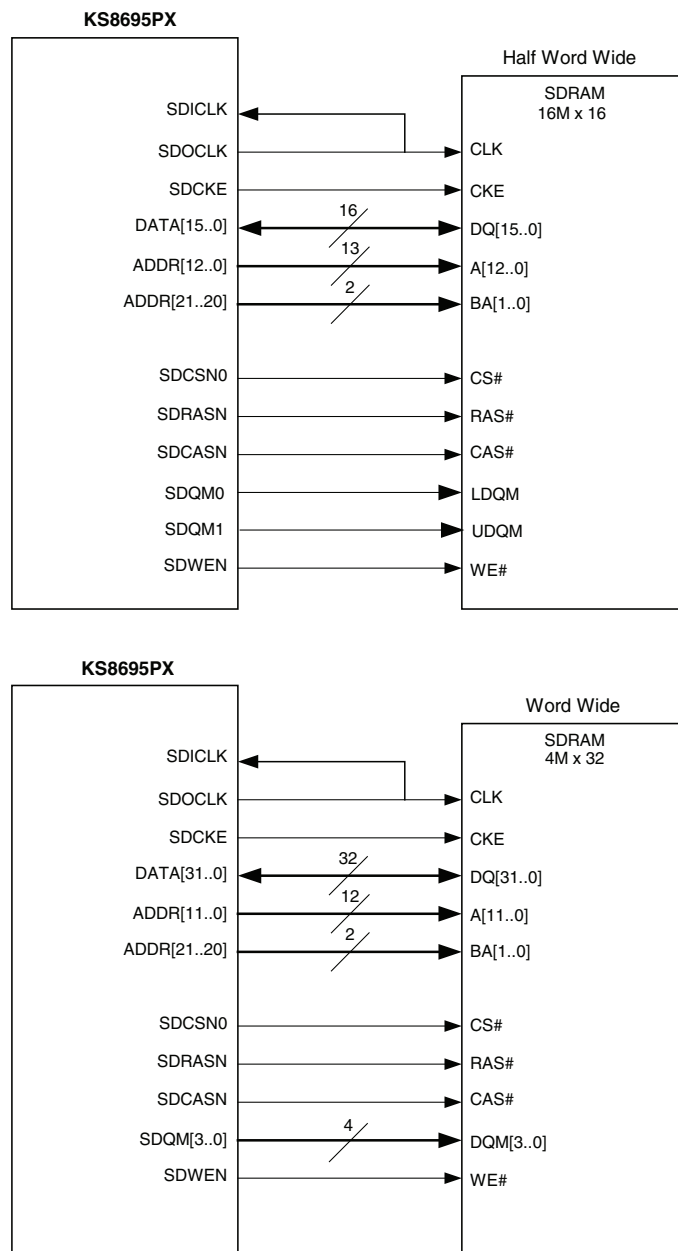
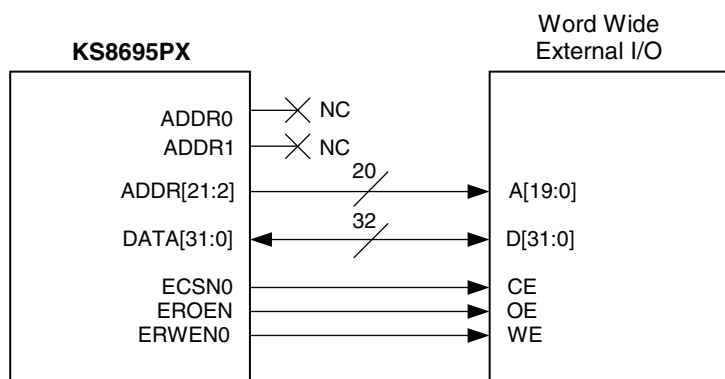
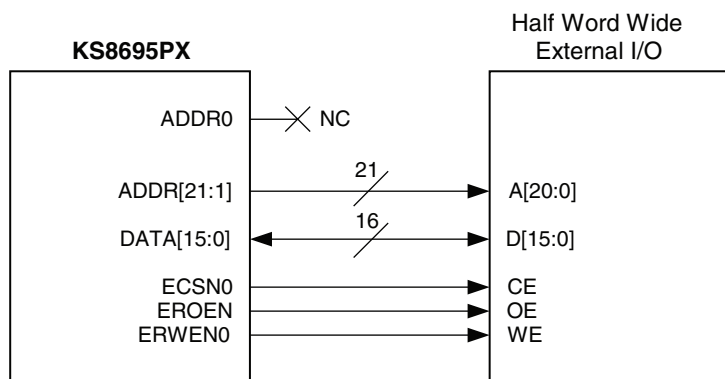
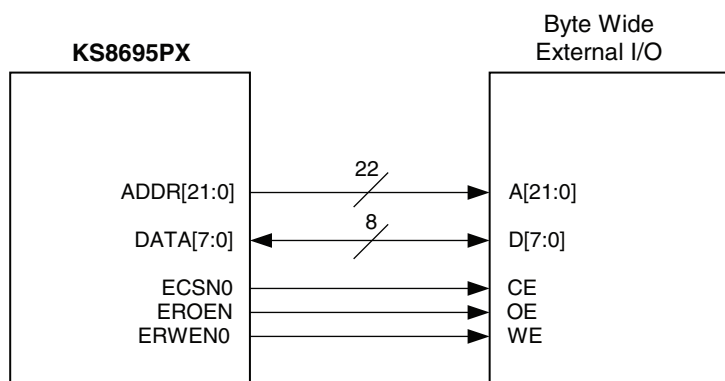


Figure 7. SDRAM Interface Examples



**Figure 8. External I/O Interface Examples**

## Signal Descriptions by Group

### Clock and Reset Pins

| Pin | Name                | I/O Type <sup>(1)</sup> | Description                                                                                                                                                                                                                                                                                                                                                                          |
|-----|---------------------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E1  | XCLK1/<br>CPUCLK    | I                       | External Clock In. This signal is used as the source clock for the transmit clock of the internal MAC and PHY. The clock frequency is 25MHz $\pm$ 50ppm. The XCLK1 signal is also used as the reference clock signal for the internal PLL to generate the 125MHz internal system clock.<br>CPUCLK: factory clock test input when the internal PLL is disabled (factory test signal). |
| E2  | XCLK2               | I                       | External Clock In. Used with XCLK1 pin when another polarity of crystal is needed. This is unused for a normal clock input.                                                                                                                                                                                                                                                          |
| M15 | URTSN/<br>CPUCLKSEL | O/I                     | Normal Mode: UART request to send. Active low output.<br>During reset: CPU clock select. Select CPU clock source. CPUCLKSEL=0 (normal mode), the internal PLL clock output is used as the CPU clock source.<br>CPUCLKSEL=1 (factory test signal): the external clock to the CPUCLK pin is used as the internal CPU clock source.                                                     |
| A17 | RESETN              | I                       | KS8695PX chip reset. Active low input asserted for at least 256 system clock (40ns) cycles to reset the KS8695PX. When in the reset state, all the output pins are tri-stated and all open drain signals are floating.                                                                                                                                                               |
| U17 | WRSTO               | O                       | Watchdog timer reset output. This signal is asserted for at least 200ms if RESETN is asserted or when the internal watchdog timer expires.                                                                                                                                                                                                                                           |
| T17 | EROEN/<br>WRSTPLS   | O/I                     | Normal Mode: ROM/SRAM/FLASH and External I/O output enable. Active low. When asserted, this signal controls the output enable port of the specified device.<br>During reset: Watchdog timer reset polarity setting. WRSTPLS=0, Active high; WRSTPLS=1, Active low. No default.                                                                                                       |

### JTAG Interface Pins

| Pin | Name  | I/O Type <sup>(1)</sup> | Description                  |
|-----|-------|-------------------------|------------------------------|
| G14 | TCK   | I                       | JTAG test clock.             |
| G15 | TMS   | I                       | JTAG test mode select.       |
| F14 | TDI   | I                       | JTAG test data in.           |
| F15 | TDO   | O                       | JTAG test data out.          |
| F16 | TRSTN | I                       | JTAG test reset. Active low. |

### WAN Ethernet Physical Interface Pins

| Pin | Name    | I/O Type <sup>(1)</sup> | Description                                                                                                |
|-----|---------|-------------------------|------------------------------------------------------------------------------------------------------------|
| G1  | WANTXP  | O                       | WAN PHY transmit signal + (differential).                                                                  |
| G2  | WANTXM  | O                       | WAN PHY transmit signal – (differential).                                                                  |
| G3  | WANRXP  | I                       | WAN PHY receive signal – (differential).                                                                   |
| G4  | WANRXM  | I                       | WAN PHY receive signal + (differential).                                                                   |
| G5  | WANFXSD | I                       | WAN fiber signal detect. Signal detect input when the WAN port is operated in 100BASE-FX 100Mb fiber mode. |

**Note:**

1. I = Input.

O = Output.

O/I = Output in normal mode; input pin during reset.

**LAN Ethernet Physical Interface Pins**

| Pin                  | Name                                     | I/O Type <sup>(1)</sup> | Description                                                                                                 |
|----------------------|------------------------------------------|-------------------------|-------------------------------------------------------------------------------------------------------------|
| H1<br>J1<br>K1<br>L1 | LANTXP1<br>LANTXP2<br>LANTXP3<br>LANTXP4 | I                       | LAN Port[4:1] PHY transmit signal + (differential).                                                         |
| H2<br>J2<br>K2<br>L2 | LANTXM1<br>LANTXM2<br>LANTXM3<br>LANTXM4 | I                       | LAN Port[4:1] PHY transmit signal – (differential).                                                         |
| H3<br>J3<br>K3<br>L3 | LANRXP1<br>LANRXP2<br>LANRXP3<br>LANRXP4 | O                       | LAN Port[4:1] PHY receive signal + (differential).                                                          |
| H4<br>J4<br>K4<br>L4 | LANTXM1<br>LANTXM2<br>LANTXM3<br>LANTXM4 | O                       | LAN Port[4:1] PHY receive signal – (differential).                                                          |
| F1                   | ISET                                     | I                       | Set PHY transmit output current. Connect to ground through a 3.01kΩ 1% resistor.                            |
| F3                   | LANFXSD1                                 | I                       | LAN fiber signal detect. Signal detect input when the LAN1 port is operated in 100BASE-FX 100Mb fiber mode. |

**PHY LED Drivers**

| Pin                      | Name                                 | I/O Type <sup>(1)</sup> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------------|--------------------------------------|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E15                      | WLED0/<br>B0SIZE0                    | O/I                     | Normal Mode: WAN LED indicator 0. Programmable via WAN misc. Control register bits [2:0].<br>'000' = Speed; '001' = Link; '010' = Full/half duplex; '011' = Collision;<br>'100' = TX/RX activity; '101' = Full-duplex collision; '110' = Link/Activity.<br>During reset: Bank 0 Data Access Size. Bank 0 is used for the boot program.<br>B0SIZE[1:0] are used to specify the size of the bank 0 data bus width as follows: '01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved. |
| E14                      | WLED1/<br>B0SIZE1                    | O/I                     | Normal Mode: WAN LED indicator 1. Programmable via WAN Misc. Control register bits [6:4].<br>'000' = Speed; '001' = Link; '010' = Full/half duplex; '011' = Collision;<br>'100' = TX/RX activity; '101' = Full-duplex collision; '110' = Link/Activity.<br>During reset: Bank 0 data access size. Bank 0 is used for the boot program.<br>B0SIZE[1:0] are used to specify the size of the bank 0 data bus width as follows: '01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved. |
| B17<br>C17<br>D17<br>E17 | L1LED0<br>L2LED0<br>L3LED0<br>L4LED0 | O                       | LAN Port[4:1] LED indicator 0. Programmable via switch control 0 register bits [27:25].<br>'000' = Speed; '001' = Link; '010' = Full/half duplex; '011' = Collision;<br>'100' = TX/RX activity; '101' = Full-duplex collision; '110' = Link/Activity.                                                                                                                                                                                                                                                |
| B16<br>C16<br>D16<br>E16 | L1LED1<br>L2LED1<br>L3LED1<br>L4LED1 | O                       | LAN Port[4:1] LED indicator 1. Programmable via switch control 0 register bits [24:22].<br>'000' = Speed; '001' = Link; '010' = Full/half duplex; '011' = Collision;<br>'100' = TX/RX activity; '101' = Full-duplex collision; '110' = Link/Activity.                                                                                                                                                                                                                                                |

**Note:**

1. I = Input.

O = Output.

O/I = Output in normal mode; input pin during reset.

**UART Pins**

| Pin | Name                | I/O Type <sup>(1)</sup> | Description                                                                                                                                                                                                                                                                                                                      |
|-----|---------------------|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| N16 | URXD                | I                       | UART receive data.                                                                                                                                                                                                                                                                                                               |
| N14 | UTXD                | O                       | UART transmit data.                                                                                                                                                                                                                                                                                                              |
| N15 | UDTRN/<br>DBGENN    | O                       | UART data terminal ready. Active low. Debug enable (factory test signal).                                                                                                                                                                                                                                                        |
| M16 | UDSRN               | I                       | UART data set ready. Active low.                                                                                                                                                                                                                                                                                                 |
| M15 | URTSN/<br>CPUCLKSEL | O/I                     | Normal mode: UART request to send. Active low output.<br>During reset: CPU clock select. Select CPU clock source. CPUCLKSEL=0 (normal mode), the internal PLL clock output is used as the CPU clock source.<br>CPUCLKSEL=1 (factory test signal), the external clock to the CPUCLK pin is used as the internal CPU clock source. |
| M14 | UCTSN/<br>BISTEN    | I                       | UART clear to send. BIST enable (factory test signal).                                                                                                                                                                                                                                                                           |
| L15 | UDCDN/<br>SCANEN    | I                       | UART data carrier detect. Scan enable (factory test signal).                                                                                                                                                                                                                                                                     |
| L14 | URIN/<br>TSTRST     | I                       | UART ring indicator. Chip test reset (factory test signal).                                                                                                                                                                                                                                                                      |

**General Purpose I/O Pins**

| Pin | Name            | I/O Type <sup>(1)</sup> | Description                                                                                                                                                                                                                         |
|-----|-----------------|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| G17 | GPIO0/<br>EINT0 | I/O                     | General purpose I/O pin. External interrupt request pin.                                                                                                                                                                            |
| G16 | GPIO1/<br>EINT1 | I/O                     | General purpose I/O pin. External interrupt request pin.                                                                                                                                                                            |
| H17 | GPIO2/<br>EINT2 | I/O                     | General purpose I/O pin. External interrupt request pin.                                                                                                                                                                            |
| H16 | GPIO3/<br>EINT3 | I/O                     | General purpose I/O pin. External interrupt request pin.                                                                                                                                                                            |
| H15 | GPIO4/<br>TOUT0 | I/O                     | General purpose I/O pin. Timer 0 output pin.                                                                                                                                                                                        |
| H14 | GPIO5/<br>TOUT1 | I/O                     | General purpose I/O pin. Timer 1 output pin.                                                                                                                                                                                        |
| J17 | GPIO6           | I/O                     | General purpose I/O pin.                                                                                                                                                                                                            |
| J16 | GPIO7           | I/O                     | General purpose I/O pin.                                                                                                                                                                                                            |
| J15 | GPIO8           | I/O                     | General purpose I/O pin.                                                                                                                                                                                                            |
| J14 | GPIO9           | I/O                     | General purpose I/O pin.                                                                                                                                                                                                            |
| K17 | GPIO10          | I/O                     | General purpose I/O pin.                                                                                                                                                                                                            |
| K16 | GPIO11          | I/O                     | General purpose I/O pin.                                                                                                                                                                                                            |
| K15 | GPIO12          | I/O                     | General purpose I/O pin.                                                                                                                                                                                                            |
| K14 | GPIO13          | I/O                     | General purpose I/O pin.                                                                                                                                                                                                            |
| L17 | GPIO14          | I/O                     | General purpose I/O pin.                                                                                                                                                                                                            |
| L16 | GPIO15          | I/O                     | General purpose I/O pin.                                                                                                                                                                                                            |
| A3  | PRSTN           | I                       | PCI Reset. Active low. This signal is an input used to reset the KS8695PX PCI logic. If the KS8695PX is the host, use the RESETN signal to drive this input. If the KS8695PX is a guest, use the system reset to drive this signal. |

**Note:**

1. I = Input.

O = Output.

I/O = Bidirectional.

O/I = Output in normal mode; input pin during reset.

**General Purpose I/O Pins (continued)**

| Pin                                                                                                                                                                                                          | Name                                                                                                                                                                                                                                                                               | I/O Type <sup>(1)</sup> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D4                                                                                                                                                                                                           | PCLK                                                                                                                                                                                                                                                                               | I                       | PCI bus clock. This signal provides the timing for the PCI bus transactions. This signal is used to drive the PCI bus interface and the internal PCI logic. All PCI bus signals are sampled on the rising edges of the PCLK. PCLK can operate from 20MHz to 33MHz. For host mode, use a PCLKOUT signal to drive this input. In guest mode, use the system PCI clock to drive this input.                                                                                                                   |
| C2                                                                                                                                                                                                           | NC                                                                                                                                                                                                                                                                                 | –                       | No connect.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| C3                                                                                                                                                                                                           | NC                                                                                                                                                                                                                                                                                 | –                       | No connect.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| C4                                                                                                                                                                                                           | GNT1N                                                                                                                                                                                                                                                                              | O                       | PCI bus grant 1. Active low. In host bridge mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the device connected to REQ1N. In guest bridge mode, this signal is an output to indicate that the KS8695PX is requesting to access the PCI bus as a PCI master. In guest bridge mode, this is basically the KS8695PX's request output.                                                                                                                                |
| B2                                                                                                                                                                                                           | NC                                                                                                                                                                                                                                                                                 | –                       | No connect.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| B3                                                                                                                                                                                                           | NC                                                                                                                                                                                                                                                                                 | –                       | No connect.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| B4                                                                                                                                                                                                           | REQ1N                                                                                                                                                                                                                                                                              | I                       | PCI bus request 1. Active low. In host bridge mode, this is an input signal from the external PCI device to request PCI bus access. In guest bridge mode, this is an input signal from an external PCI bus arbiter granting access to the bus. In guest bridge, this is basically the KS8695PX's grant input.                                                                                                                                                                                              |
| A4<br>D5<br>B5<br>C5<br>A5<br>D6<br>B6<br>C6<br>B7<br>C7<br>A7<br>D8<br>B8<br>D9<br>A8<br>C9<br>D12<br>B12<br>C12<br>A12<br>D13<br>B13<br>C13<br>A13<br>B14<br>C14<br>A14<br>D15<br>B15<br>C15<br>A15<br>A16 | PAD31<br>PAD30<br>PAD29<br>PAD28<br>PAD27<br>PAD26<br>PAD25<br>PAD24<br>PAD23<br>PAD22<br>PAD21<br>PAD20<br>PAD19<br>PAD18<br>PAD17<br>PAD16<br>PAD15<br>PAD14<br>PAD13<br>PAD12<br>PAD11<br>PAD10<br>PAD9<br>PAD8<br>PAD7<br>PAD6<br>PAD5<br>PAD4<br>PAD3<br>PAD2<br>PAD1<br>PAD0 | I/O                     | 32-Bit PCI address and data. PCI bus transactions consist of an address phase followed by one or more data phases. Address and data signals are multiplexed on the same pins. For a PCI write transaction, the source of the data is the KS8695PX. For a PCI read transaction, the data source is the target. The KS8695PX supports both read and write burst transactions. In the case of a read transaction, a special data turn around cycle is needed between the address phase and the data phase(s). |

**Note:**

1. I = Input.

O = Output.

I/O = Bidirectional.



**General Purpose I/O Pins (continued)**

| Pin                    | Name                             | I/O Type <sup>(1)</sup> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|------------------------|----------------------------------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A6<br>B9<br>A11<br>D14 | CBEN3<br>CBEN2<br>CBEN1<br>CBEN0 | I/O                     | PCI commands and byte enable. Active low.<br>The PCI command and byte enable signals are multiplexed on the same pins. During the first clock cycle of a PCI transaction, the CBEN bus contains the command for the transaction. The PCI transaction consists of the address phases and one or more data phases. During the data phases of the transaction, the bus carries the byte enable for the current data phases.                                                                                                 |
| C8                     | PAR                              | I/O                     | Parity. PCI bus parity is even across PAD[31:0] and CBEN[3:0]. The KS8695PX generates PAR during the address phase and write data phases as a bus master and during read data phases as a target. It checks for correct PAR during the read data phase as a bus master, during every address phase as a bus slave, and during write data phases as a target.                                                                                                                                                             |
| D10                    | FRAMEN                           | I/O                     | PCI bus frame signal. Active low. FRAMEN is an indication of an active PCI bus cycle. It is asserted at the beginning of a PCI transaction, i.e. the address phase, and deasserted before the final transfer of the data phase of the transaction.                                                                                                                                                                                                                                                                       |
| A9                     | IRDYN                            | I/O                     | PCI initiator ready signal. Active low. This signal is asserted by a PCI master to indicate a valid data phase on the PAD bus during data phases of a write transaction. During a read transaction, it indicates that the master is ready to accept data from the target. A target monitors the IRDYN signal when a data phase is completed on any rising edge of the PCI clock when both IRDYN and TRDYN are asserted. Wait cycles are inserted until both IRDYN and TRDYN are asserted together.                       |
| C10                    | TRDYN                            | I/O                     | PCI target ready signal. Active low. This signal is asserted by a PCI slave to indicate a valid data phase on the PAD bus during a read transaction. During a write transaction, it indicates that the slave is ready to accept data from the target. A PCI initiator monitors the TRDYN signal when a data phase is completed on any rising edge of the PCI clock when both IRDYN and TRDYN are asserted. Wait cycles are inserted until both IRDYN and TRDYN are asserted together.                                    |
| C11                    | DEVSELN                          | I/O                     | PCI device select signal. Active low. This signal is asserted when the KS8695PX is selected as a target during a bus transaction. When the KS8695PX is the initiator of the current bus access, it expects the target to assert DEVSELN within five PCI bus cycles, confirming the access. If the target does not assert DEVSELN within the required bus cycles, the KS8695PX aborts the bus cycle. To meet the timing requirement, the KS8695PX asserts this signal in a medium speed decode timing. ( two bus cycles). |
| D7                     | IDSEL                            | I                       | Initialization device select. Active high. It is used as a chip select during configuration read and write transactions.                                                                                                                                                                                                                                                                                                                                                                                                 |
| D11                    | STOPN                            | I/O                     | PCI stop signal. Active low. This signal is asserted by the PCI target to indicate to the bus master that it is terminating the current transaction. The KS8695PX responds to the assertion of STOPN when it is the bus master, either to disconnect, retry, or abort the transaction.                                                                                                                                                                                                                                   |
| B11                    | PERRN                            | I/O                     | PCI parity error signal. Active low. The KS8695PX asserts PERRN when it checks and detects a bus parity error. When it generates the PAR output, the KS8695PX monitors for any reported parity error on PERRN. When the KS8695PX is the bus master and a parity error is detected, the KS8695PX sets error bits in the control status registers. It completes the current data burst transaction, and then stops the operation. After the host clears the system error, the KS8695PX continues its operation.            |
| A10                    | SERRN                            | O                       | PCI system error signal. Active low. If an address parity error is detected, the KS8695PX asserts the SERRN signal two clocks after the failing address.                                                                                                                                                                                                                                                                                                                                                                 |
| E4                     | M66EN                            | I                       | PCI 66MHz enable. When asserted, this signal indicates the PCI bus segment is operating at 66MHz. This pin is mainly used in guest bridge mode when the PCLK is driven by an external host bridge.                                                                                                                                                                                                                                                                                                                       |

**Note:**

1. I = Input.

O = Output.

I/O = Bidirectional.

**General Purpose I/O Pins (continued)**

| Pin | Name     | I/O Type <sup>(1)</sup> | Description                                                                                                                                                                                                                                                          |
|-----|----------|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D1  | NC       | –                       | No connect.                                                                                                                                                                                                                                                          |
| C1  | NC       | –                       | No connect.                                                                                                                                                                                                                                                          |
| B1  | PCLKOUT1 | O                       | PCI clock output 1.                                                                                                                                                                                                                                                  |
| A2  | PCLKOUT0 | O                       | PCI clock output 0.                                                                                                                                                                                                                                                  |
| B10 | CLKRUNN  | I/O                     | This is a cardbus only signal. The CLKRUNN signal is used by portable cardbus devices to request that the system turn on the bus clock. Output is always active in cardbus and miniPCI modes.                                                                        |
| D2  | MPCIACTN | O                       | MiniPCI active. This signal is asserted by the PCI device to indicate that its current function requires full system performance. MPCIACTN is an open drain output signal. In miniPCI mode, this signal is always low.                                               |
| D3  | PBMS     | I                       | PCI bridge mode select. This selects the operating mode for the PCI bridge. When PBMS is high, the host bridge mode is selected and the on-chip PCI bus arbiter is enabled. When PBMS is low, the guest bridge mode is selected and the on-chip arbiter is disabled. |

**Advanced Memory Interface (SDRAM/ROM/FLASH/SRAM/EXTERNAL I/O)**

| Pin                                                                                                                  | Name                                                                                                                                                                                                                               | I/O Type <sup>(1)</sup> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| T7                                                                                                                   | SDICLK                                                                                                                                                                                                                             | I                       | SDRAM Clock In: SDRAM clock input for the SDRAM memory controller interface.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| U7                                                                                                                   | SDOCLK                                                                                                                                                                                                                             | O                       | System/SDRAM Clock Out: Output of the internal system clock, it is also used as the clock signal for SDRAM interface.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| P4                                                                                                                   | ADDR21/BA1                                                                                                                                                                                                                         | O                       | Address Bit 21/Bank Address Input 1: Address bit 21 for asynchronous accesses. Bank Address Input bit 1 for SDRAM accesses.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| P3                                                                                                                   | ADDR20/BA0                                                                                                                                                                                                                         | O                       | Address Bit 20/Bank Address Input 0: Address bit 20 for asynchronous accesses. Bank Address Input bit 0 for SDRAM accesses.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| M3<br>M2<br>M1<br>N4<br>N3<br>N2<br>N1<br>P2<br>P1<br>R3<br>R2<br>R1<br>T2<br>T1<br>U1<br>U2<br>T3<br>U3<br>T4<br>U4 | ADDR[19]<br>ADDR[18]<br>ADDR[17]<br>ADDR[16]<br>ADDR[15]<br>ADDR[14]<br>ADDR[13]<br>ADDR[12]<br>ADDR[11]<br>ADDR[10]<br>ADDR[9]<br>ADDR[8]<br>ADDR[7]<br>ADDR[6]<br>ADDR[5]<br>ADDR[4]<br>ADDR[3]<br>ADDR[2]<br>ADDR[1]<br>ADDR[0] | O                       | Address Bus: The 22-bit address bus (including ADDR[21:20] above) covers 4M word memory space shared by ROM/SRAM/FLASH, SDRAM, and external I/O banks. During the SDRAM cycles, the internal address bus is used to generate RAS and CAS addresses for the SDRAM. The number of column address bits in the SDRAM banks can be programmed from 8 to 11 bits via the SDRAM control registers. ADDR[12:0] are the SDRAM address and ADDR[21:20] are the SDRAM bank address. During other cycles, the ADDR[21:0] is the byte address of the data transfer. For SDRAM and FLASH/ROM/SRAM, connect all address lines, i.e. A0 to A0, A1 to A1, etc. The memory controller automatically handles address line adjustments for the 8/16/32 bit accesses. For external I/O devices, the user needs to connect address lines for 8/16/32 bit accesses. |

**Note:**

1. I = Input.

O = Output.

I/O = Bidirectional.

**Advanced Memory Interface (SDRAM/ROM/FLASH/SRAM/EXTERNAL I/O)**

| Pin                                                                                                                                                                                                                | Name                                                                                                                                                                                                                                                                                                                                                                               | I/O Type <sup>(1)</sup> | Description                                                                                                                                                                                                                                                                                                                                 |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P7<br>R7<br>P8<br>R8<br>T8<br>U8<br>P9<br>R9<br>T9<br>U9<br>P10<br>R10<br>T10<br>U10<br>P11<br>R11<br>T11<br>U11<br>P12<br>R12<br>T12<br>U12<br>P13<br>R13<br>T13<br>U13<br>P14<br>R14<br>T14<br>U14<br>T15<br>U15 | DATA[31]<br>DATA[30]<br>DATA[29]<br>DATA[28]<br>DATA[27]<br>DATA[26]<br>DATA[25]<br>DATA[24]<br>DATA[23]<br>DATA[22]<br>DATA[21]<br>DATA[20]<br>DATA[19]<br>DATA[18]<br>DATA[17]<br>DATA[16]<br>DATA[15]<br>DATA[14]<br>DATA[13]<br>DATA[12]<br>DATA[11]<br>DATA[10]<br>DATA[9]<br>DATA[8]<br>DATA[7]<br>DATA[6]<br>DATA[5]<br>DATA[4]<br>DATA[3]<br>DATA[2]<br>DATA[1]<br>DATA[0] | I/O                     | External Data Bus. 32-Bit bi-directional data bus for data transfer. The KS8695PX also supports 8-bit and 16-bit data bus widths.                                                                                                                                                                                                           |
| R4<br>P5                                                                                                                                                                                                           | SDCSN[1]<br>SDCSN[0]                                                                                                                                                                                                                                                                                                                                                               | O                       | SDRAM Chip Select: Active low chip select pins for SDRAM. The KS8695PX supports up to two SDRAM banks. One SDCSN output is provided for each bank.                                                                                                                                                                                          |
| R5                                                                                                                                                                                                                 | SDRASN                                                                                                                                                                                                                                                                                                                                                                             | O                       | SDRAM Row Address Strobe: Active low. The row address strobe pin for SDRAM.                                                                                                                                                                                                                                                                 |
| T5                                                                                                                                                                                                                 | SDCASN                                                                                                                                                                                                                                                                                                                                                                             | O                       | SDRAM Column Address Strobe: Active low. The column address strobe pin for SDRAM.                                                                                                                                                                                                                                                           |
| U5                                                                                                                                                                                                                 | SDWEN                                                                                                                                                                                                                                                                                                                                                                              | O                       | SDRAM Write Enable: Active low. The write enable signal for SDRAM.                                                                                                                                                                                                                                                                          |
| P6<br>R6<br>T6<br>U6                                                                                                                                                                                               | SDQM[3]<br>SDQM[2]<br>SDQM[1]<br>SDQM[0]                                                                                                                                                                                                                                                                                                                                           | O                       | SDRAM Data Input/Output Mask: Data input/output mask signals for SDRAM. The SDQM is sampled high and is an output mask signal for write accesses and an output enable signal for read accesses. Input data are masked during a write cycle. The SDQM0/1/2/3 correspond to DATA[7:0], DATA[15:8], DATA[23:16] and DATA[31:24], respectively. |
| U16<br>T16<br>R16                                                                                                                                                                                                  | ECSN[2]<br>ECSN[1]<br>ECSN[0]                                                                                                                                                                                                                                                                                                                                                      | O                       | External I/O Device Chip Select: Active low. Three external I/O banks are provided for external memory mapped I/O operations. Each I/O bank stores up to 16KB. The ECSNx signals indicate which of the three I/O banks is selected.                                                                                                         |
| P16                                                                                                                                                                                                                | EWAITN                                                                                                                                                                                                                                                                                                                                                                             | I                       | External Wait: Active low. This signal is asserted when an external I/O device or a ROM/SRAM/FLASH bank needs more access cycles than those defined in the corresponding control register.                                                                                                                                                  |
| R15<br>P15                                                                                                                                                                                                         | RCSN[1]<br>RCSN[0]                                                                                                                                                                                                                                                                                                                                                                 | O                       | ROM/SRAM/FLASH Chip Select: Active low. The KS8695PX can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks.                                                                                                                                        |

**Note:**

1. I = Input.

O = Output.

I/O = Bidirectional.

| Pin | Name                  | I/O Type <sup>(1)</sup> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----|-----------------------|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| T17 | EROEN/<br>WRSTPLS     | O/I                     | Normal mode: External I/O and ROM/SRAM/FLASH output enable: Active low. When asserted, this signal controls the output enable port of the specified memory device.<br>During reset: Watchdog timer reset polarity setting. WRSTPLS=0, active low; WRSTPLS = 1, active high. No default.                                                                                                                                                                                                   |
| M17 | ERWEN0/<br>TESTACK    | O                       | External I/O and ROM/SRAM/FLASH write byte enable: Active low. When asserted, the ERWENx controls the byte write enable of the memory device (except SDRAM). ARM CPU test signal (factory test signal).                                                                                                                                                                                                                                                                                   |
| N17 | ERWEN1/<br>TESTREQB   | O                       | External I/O and ROM/SRAM/FLASH write byte enable: Active low. When asserted, the ERWENx controls the byte write enable of the memory device (except SDRAM). ARM CPU test signal (factory test signal).                                                                                                                                                                                                                                                                                   |
| P17 | ERWEN2/<br>TESTREQA   | O                       | External I/O and ROM/SRAM/FLASH write byte enable: Active low. When asserted, the ERWENx controls the byte write enable of the memory device except SDRAM). ARM CPU test signal (factory test signal).                                                                                                                                                                                                                                                                                    |
| R17 | ERWEN3/<br>TICTESTENN | O                       | External I/O and ROM/SRAM/FLASH write byte enable. Active low. When asserted, the ERWENx controls the byte write enable of the memory device (except SDRAM). ARM CPU test signal (factory test signal).                                                                                                                                                                                                                                                                                   |
| E15 | WLED0/<br>B0SIZE0     | O/I                     | Normal mode: WAN LED indicator 0: Programmable via WAN misc. Control register bits [2:0].<br>000 = Speed; 001 = Link; 010 = Full/half duplex; 011 = Collision;<br>100 = TX/RX activity; 101 = Full-duplex collision; 110 = Link/Activity.<br>During reset: Bank 0 data access size. Bank 0 is used for the boot program.<br>B0SiZE[1:0] are used to specify the size of the bank 0 data bus width as follows:<br>'01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved. |
| E14 | WLED1/<br>B0SIZE1     | O/I                     | Normal mode: WAN LED indicator 1: Programmable via WAN Misc. Control register bits [6:4].<br>000 = Speed; 001 = Link; 010 = Full/half duplex; 011 = Collision;<br>100 = TX/RX activity; 101 = Full-duplex collision; 110 = Link/Activity.<br>During reset: Bank 0 data access size. Bank 0 is used for the boot program.<br>B0SiZE[1:0] are used to specify the size of the bank 0 data bus width as follows:<br>'01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved. |

## Factory Test Pins

| Pin | Name   | I/O Type <sup>(1)</sup> | Description                                                     |
|-----|--------|-------------------------|-----------------------------------------------------------------|
| F7  | TESTEN | I                       | Chip test enable: (factory test signal), pull down if not used. |
| M4  | TEST1  | I                       | PHY test pin: (factory test signal).                            |
| F4  | TEST2  | I                       | PHY test pin: (factory test signal).                            |

### Note:

1. I = Input.

O = Output.

O/I = Output in normal mode; input pin during reset.

**Power and Ground Pins**

| Pin                                                                                                                          | Name    | I/O Type <sup>(1)</sup> | Description                  |
|------------------------------------------------------------------------------------------------------------------------------|---------|-------------------------|------------------------------|
| E5<br>E6<br>F5<br>F6<br>G5<br>G6<br>H5<br>H6<br>J5<br>J6                                                                     | VDDA1.8 | P                       | 1.8V analog $V_{DD}$ .       |
| E7<br>E8<br>E9<br>E10<br>F7<br>F8<br>F9<br>F10<br>M7<br>M8<br>M9<br>H12<br>H13<br>J12<br>J13<br>K12<br>K13<br>N7<br>N8<br>N9 | VDD1.8  | P                       | 1.8V digital core $V_{DD}$ . |
| K5<br>K6<br>L5<br>L6<br>M5<br>M6<br>N5<br>N6                                                                                 | VDDA3.3 | P                       | 3.3V analog $V_{DD}$ .       |
| E11<br>E12<br>E13<br>F11<br>F12<br>F13<br>G12<br>G13<br>L12<br>L13<br>M10<br>M11<br>M12<br>M13<br>N10<br>N11<br>N12<br>N13   | VDDA3.3 | P                       | 3.3V digital I/O $V_{DD}$ .  |

**Note:**

1. P = Power.

| Pin                                                                                                                                        | Name | I/O Type <sup>(1)</sup> | Description    |
|--------------------------------------------------------------------------------------------------------------------------------------------|------|-------------------------|----------------|
| E3<br>H7<br>J7<br>K7<br>L7                                                                                                                 | AGND | Gnd                     | Analog Ground. |
| A1<br>G7<br>G8<br>G9<br>G10<br>G11<br>H8<br>H9<br>H10<br>H11<br>J8<br>J9<br>J10<br>J11<br>K8<br>K9<br>K10<br>K11<br>L8<br>L9<br>L10<br>L11 | GND  | Gnd                     | Ground.        |

**Note:**

1. P = Power.

## Address Map and Register Description

### Memory Map

Upon power up, the KS8695PX memory map is configured as shown below.

| Address Range           | Region | Description                                  |
|-------------------------|--------|----------------------------------------------|
| 0x03FF0000 – 0x03FFFFFF | 64KB   | KS8695PX System Configuration Register Space |
| 0x02000000 – 0x03FEFFFF | 32MB   | Not Configured                               |
| 0x00000000 – 0x01FFFFFF | 32MB   | Flash Bank 0                                 |

### Memory Map Example

The default base address for the KS8695PX system configuration registers is 0x03ff0000. After power up, the user is free to remap the memory for their specific application. The following is an example of the memory space remapped for operation.

| Address Range           | Region | Description                                  |
|-------------------------|--------|----------------------------------------------|
| 0x03FF0000 – 0x03FFFFFF | 64KB   | KS8695PX System Configuration Register Space |
| 0x03E00000 – 0x03FEFFFF | 2MB    | Disabled, Not Used                           |
| 0x03200000 – 0x036FFFFF | 5MB    | Space (External I/O)                         |
| 0x02C00000 – 0x031FFFFF | 6MB    | Reserved FLASH Space, Not Used               |
| 0x02800000 – 0x02BFFFFF | 4MB    | FLASH                                        |
| 0x02000000 – 0x027FFFFF | 8MB    | Disabled, Not Used                           |
| 0x00000000 – 0x01FFFFFF | 32MB   | SDRAM                                        |

### Register Description

The KS8695PX system configuration registers (SCRs) are located in a block of 64KB in the host memory address space. After power up and initialization, the user can remap the SCRs to a desired offset. The SCRs are 32 bits wide. They are 32 bit word-aligned and must be accessed using word instructions.

The AHB-PCI bridge configuration registers are also included in the SCRs. A subset of the AHB-PCI bridge configuration registers is also accessible to an external PCI host when the KS8695PX is configured in PCI guest mode. Refer to the detailed Register Description document for additional information, including bit definitions. If you don't have this document, contact your local Micrel Field Application Engineer or salesperson.

| Register Type        | Address Range           |
|----------------------|-------------------------|
| System Configuration | 0x03FFFFFF – 0x03FEFFFF |
| External I/O Bank 2  | 0x03FEFFFF – 0x039FFFFF |
| External I/O Bank 1  | 0x039FFFFF – 0x035FFFFF |
| External I/O Bank 0  | 0x035FFFFF – 0x031FFFFF |
| Not Used             | 0x031FFFFF – 0x02FFFFFF |
| Flash Bank 0 – 4MB   | 0x02FFFFFF – 0x027FFFFF |
| Not Used             | 0x027FFFFF – 0x00FFFFFF |
| SDRAM 16MB           | 0x00FFFFFF – 0x00000000 |

| Address Range   | Register Type                |
|-----------------|------------------------------|
| 0x0000 – 0x0004 | System Configuration         |
| 0x2000 – 0x2224 | PCI-AHB Bridge Configuration |
| 0x4000 – 0x4040 | Memory Controller Interface  |
| 0x6000 – 0x60FC | WAN DMA                      |
| 0x8000 – 0x80FC | LAN DMA                      |
| 0xA000 – 0xA0FC | Reserved                     |
| 0xE000 – 0xA0FC | UART Registers               |
| 0xE200 – 0xE234 | Interrupt Controller         |
| 0xE400 – 0xE410 | Timer Registers              |
| 0xE600 – 0xE608 | General Purpose I/O          |
| 0xE800 – 0xE850 | Switch Engine Configuration  |
| 0xEA00 – 0xEA18 | Miscellaneous                |

**Absolute Maximum Ratings<sup>(1)</sup>**

## Supply Voltage

|                                             |                |
|---------------------------------------------|----------------|
| (V <sub>DDA1.8</sub> , V <sub>DD1.8</sub> ) | –0.5V to +2.4V |
| (V <sub>DDA3.3</sub> , V <sub>DD3.3</sub> ) | –0.5V to +4.0V |

Input Voltage (all inputs) ..... –0.5V to +4.0V

Output Voltage (all outputs) ..... –0.5V to +4.0V

Lead Temperature (soldering, 10sec.) ..... 270°C

Storage Temperature (T<sub>S</sub>) ..... –55°C to +150°C**Operating Ratings<sup>(2)</sup>**

## Supply Voltage

|                                                            |                |
|------------------------------------------------------------|----------------|
| (V <sub>DDA1.8</sub> , V <sub>DD1.8</sub> )                | +1.7V to +1.9V |
| (V <sub>DDA3.3</sub> , V <sub>DD3.3</sub> ) <sup>(3)</sup> | +3.0V to +3.6V |

Ambient Temperature (T<sub>A</sub>) ..... –0°C to +70°CJunction Temperature (T<sub>J</sub>) ..... 150°CPackage Thermal Resistance<sup>(4)</sup>PBGA (θ<sub>JA</sub>) No Air Flow ..... 29.86°C/W

1m/s ..... 21.86°C/W

2m/s ..... 21.54°C/W

(θ<sub>JC</sub>) No Air Flow ..... 8.34°C/W

Stresses greater than those give above can cause permanent damage to the device. Operation of the device at the stated or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level.

**Electrical Characteristics<sup>(5)</sup>**

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------|-----------|-----------|-----|-----|-----|-------|
|--------|-----------|-----------|-----|-----|-----|-------|

Total Supply Current (including TX output driver current)

100BASE-TX Operation: All ports 100% Utilization, SDOCLK = 125MHz

|                   |                          |                             |  |       |  |   |
|-------------------|--------------------------|-----------------------------|--|-------|--|---|
| I <sub>TX</sub>   | 100BASE-TX (Analog TX)   | V <sub>DDA3.3</sub> = +3.3V |  | 0.243 |  | A |
| I <sub>RX</sub>   | 100BASE-TX (Analog RX)   | V <sub>DDA1.8</sub> = +1.8V |  | 0.124 |  | A |
| I <sub>DDIO</sub> | 100BASE-T (Digital I/O)  | V <sub>DD3.3</sub> = +3.3V  |  | 0.033 |  | A |
| I <sub>DDC</sub>  | 100BASE-T (Digital Core) | V <sub>DD1.8</sub> = +1.8V  |  | 0.235 |  | A |

10BASE-TX Operation: All ports 100% Utilization, SDOCLK = 125MHz

|                   |                         |                             |  |       |  |   |
|-------------------|-------------------------|-----------------------------|--|-------|--|---|
| I <sub>TX</sub>   | 10BASE-T (Analog TX)    | V <sub>DDA3.3</sub> = +3.3V |  | 0.328 |  | A |
| I <sub>RX</sub>   | 10BASE-T (Analog RX)    | V <sub>DDA1.8</sub>         |  | 0.072 |  | A |
| I <sub>DDIO</sub> | 10BASE-T (Digital I/O)  | V <sub>DD3.3</sub> = +3.3V  |  | 0.025 |  | A |
| I <sub>DDC</sub>  | 10BASE-T (Digital Core) | V <sub>DD1.8</sub> = +1.8V  |  | 0.234 |  | A |

Auto-Negotiation Mode: SDOCLK = 125MHz

|                   |                         |                             |  |        |  |   |
|-------------------|-------------------------|-----------------------------|--|--------|--|---|
| I <sub>TX</sub>   | 10BASE-T (Transmitter)  | V <sub>DDA3.3</sub> = +3.3V |  | 0.046  |  | A |
| I <sub>RX</sub>   | 10BASE-T (Analog RX)    | V <sub>DDA1.8</sub>         |  | 0.07   |  | A |
| I <sub>DDIO</sub> | 10BASE-T (Digital I/O)  | V <sub>DD3.3</sub> = +3.3V  |  | 0.021  |  | A |
| I <sub>DDC</sub>  | 10BASE-T (Digital Core) | V <sub>DD1.8</sub> = +1.8V  |  | 0.0233 |  | A |

TTL Inputs (PCI, LED, Memory Interface, UART)

|                 |                                                |                                            |      |  |      |    |
|-----------------|------------------------------------------------|--------------------------------------------|------|--|------|----|
| V <sub>IH</sub> | Input High Voltage                             | 1/2V <sub>DDA3.3</sub>                     | +0.4 |  |      | V  |
| V <sub>IL</sub> | Input Low Voltage                              | 1/2V <sub>DDA3.3</sub>                     |      |  | –0.4 | V  |
| I <sub>IN</sub> | Input Current<br>(Excluding pull-up/pull-down) | V <sub>IN</sub> = GND = V <sub>DD3.3</sub> | –10  |  | 10   | μA |

TTL Outputs (PCI, LED, Memory Interface, UART)

|                 |                          |                                            |      |  |      |    |
|-----------------|--------------------------|--------------------------------------------|------|--|------|----|
| V <sub>OH</sub> | Output High Voltage      | I <sub>OH</sub> = –8mA; V <sub>DD3.3</sub> | +0.4 |  |      | V  |
| V <sub>OL</sub> | Output Low Voltage       | I <sub>OL</sub> = 8mA                      |      |  | +0.4 | V  |
| I <sub>OZ</sub> | Output Tri-state Leakage |                                            |      |  | 10   | μA |

**Notes:**

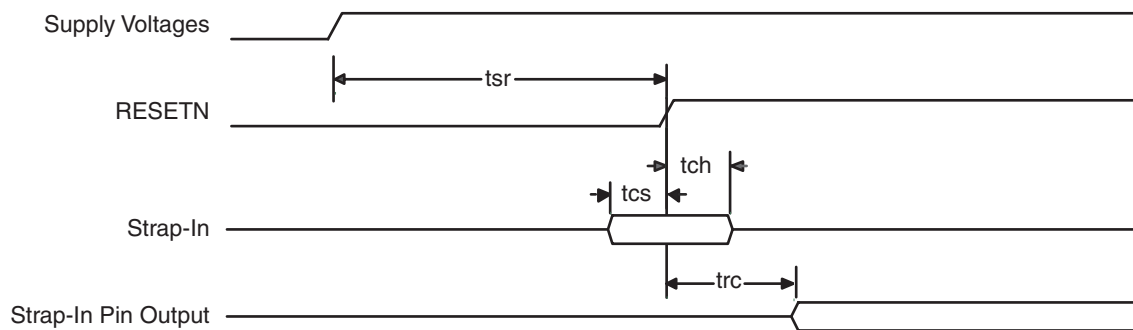
- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (Ground to V<sub>DD</sub>).
- V<sub>DDA</sub> or V<sub>DD</sub> can operate from either a 2.5V or 3.3V supply.
- No heat spreader in package.
- Specification for packaged product only.



| Symbol                                                                                     | Parameter                        | Condition                                           | Min  | Typ | Max       | Units         |
|--------------------------------------------------------------------------------------------|----------------------------------|-----------------------------------------------------|------|-----|-----------|---------------|
| TTL Outputs (PCI, LED, Memory Interface, UART)                                             |                                  |                                                     |      |     |           |               |
| $V_{OH}$                                                                                   | Output High Voltage              | $I_{OH} = -8\text{mA}$ ; $V_{DD3.3}$                | +0.4 |     |           | V             |
| $V_{OL}$                                                                                   | Output Low Voltage               | $I_{OL} = 8\text{mA}$                               |      |     | +0.4      | V             |
| $I_{OZ}$                                                                                   | Output Tri-state Leakage         |                                                     |      |     | 10        | $\mu\text{A}$ |
| 100BASE-TX Transmit (measured differentially after 1:1 transformer)                        |                                  |                                                     |      |     |           |               |
| $V_O$                                                                                      | Peak Differential Output Voltage | 100 $\Omega$ termination on the differential output | 0.95 |     | 1.05      | V             |
| $V_{IMB}$                                                                                  | Output Voltage Imbalance         | 100 $\Omega$ termination on the differential output |      |     | 2         | %             |
| $t_r, t_f$                                                                                 | Rise/Fall Time                   |                                                     | 3    |     | 5         | ns            |
|                                                                                            | Rise/Fall Time Imbalance         |                                                     | 0    |     | 0.5       | ns            |
|                                                                                            | Duty Cycle Distortion            |                                                     |      |     | $\pm 0.5$ | ns            |
|                                                                                            | Overshoot                        |                                                     |      |     | 5         | %             |
| $V_{SET}$                                                                                  | Reference Voltage of ISET        |                                                     |      | 0.5 |           | V             |
|                                                                                            | Output Jitters                   | Peak-to-peak                                        |      | 0.7 | 1.4       | ns            |
| 10BASE-T Receive                                                                           |                                  |                                                     |      |     |           |               |
| $V_{SQ}$                                                                                   | Squelch Threshold                | 5MHz square wave                                    |      | 400 |           | mV            |
| 10BASE-T Transmit (measured differentially after 1:1 transformer) $V_{DDAT} = 2.5\text{V}$ |                                  |                                                     |      |     |           |               |
| $V_P$                                                                                      | Peak Differential Output Voltage | 100 $\Omega$ termination on the differential output |      | 2.3 |           | V             |
|                                                                                            | Jitters Added                    | 100 $\Omega$ termination on the differential output |      |     | $\pm 3.5$ | ns            |
|                                                                                            | Rise/Fall Time                   |                                                     |      | 28  | 30        | ns            |

## Timing Diagrams

For PCI timing, please refer to the PCI specification, version 2.1.



**Figure 9. Reset Timing**

| Symbol   | Parameter                            | Min | Typ | Max | Units |
|----------|--------------------------------------|-----|-----|-----|-------|
| $t_{SR}$ | Stable supply voltages to reset high | 10  |     |     | ns    |
| $t_{CS}$ | Configuration set-up time            | 50  |     |     | ns    |
| $t_{CH}$ | Configuration hold time              | 50  |     |     | ns    |
| $t_{RC}$ | Reset to strap-in pin output         | 50  |     |     | ns    |

**Table 2. Reset Timing Parameters**

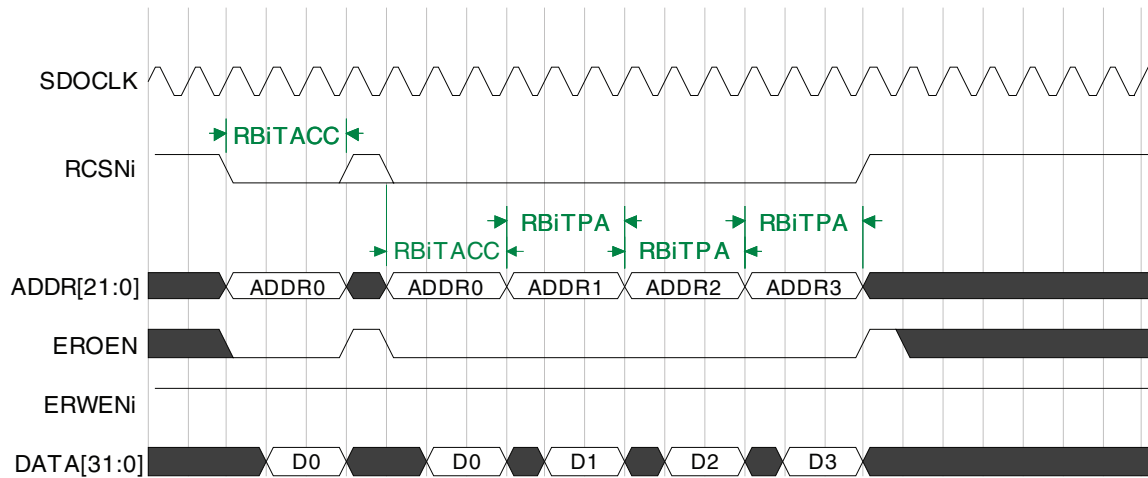


Figure 10. Static Memory Read Cycle

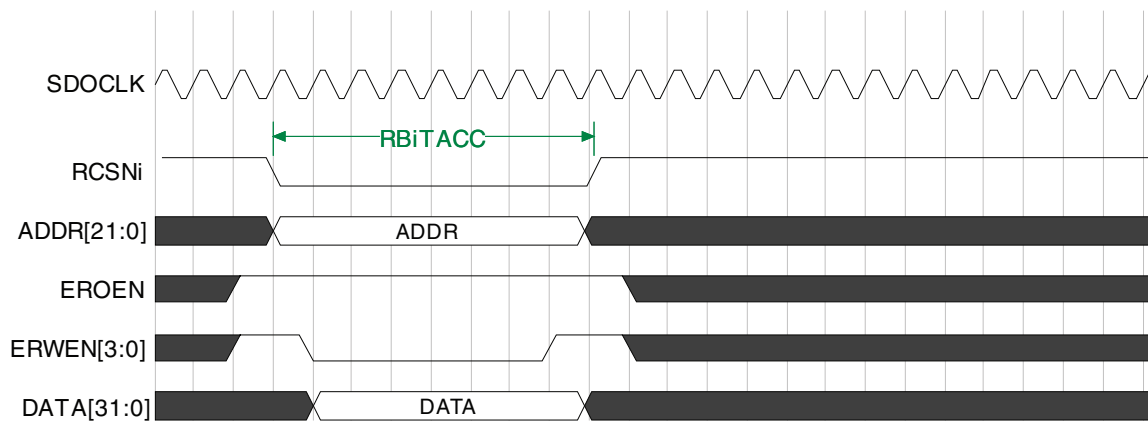


Figure 11. Static Memory Write Cycle

| Symbol  | Parameter <sup>(1)</sup>             | Registers |
|---------|--------------------------------------|-----------|
| RBiTACC | Programmable bank i access time      | 0x4010    |
| RBiTPA  | Programmable bank i page access time | 0x4014    |

Table 3. Static Memory Timing Parameters

**Note:**

1. "i" Refers to chip select parameters 0 and 1.

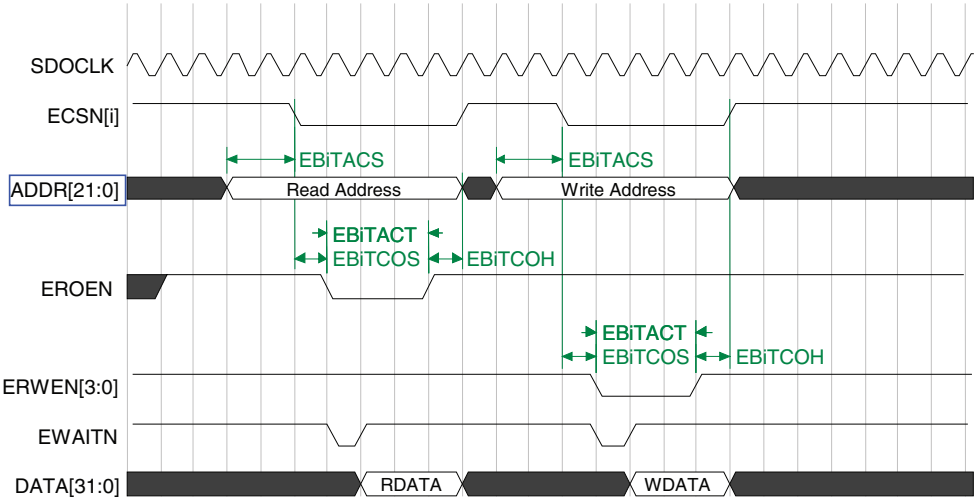


Figure 12. External I/O Read and Write Cycles

| Symbol  | Parameter <sup>(1)</sup>                                   | Registers              |
|---------|------------------------------------------------------------|------------------------|
| EBiTACS | Programmable bank i address setup time before chip select  | 0x4000, 0x4004, 0x4008 |
| EBiTACT | Programmable bank i write enable/output enable access time | 0x4000, 0x4004, 0x4008 |
| EBiTCOS | Programmable bank i chip select setup time before OEN      | 0x4000, 0x4004, 0x4008 |
| EBiTCOH | Programmable bank i chip select hold time                  | 0x4000, 0x4004, 0x4008 |

Table 4. External I/O Timing Parameters

**Note:**  
1. "i" Refers to chip select parameters 0, 1, or 2.

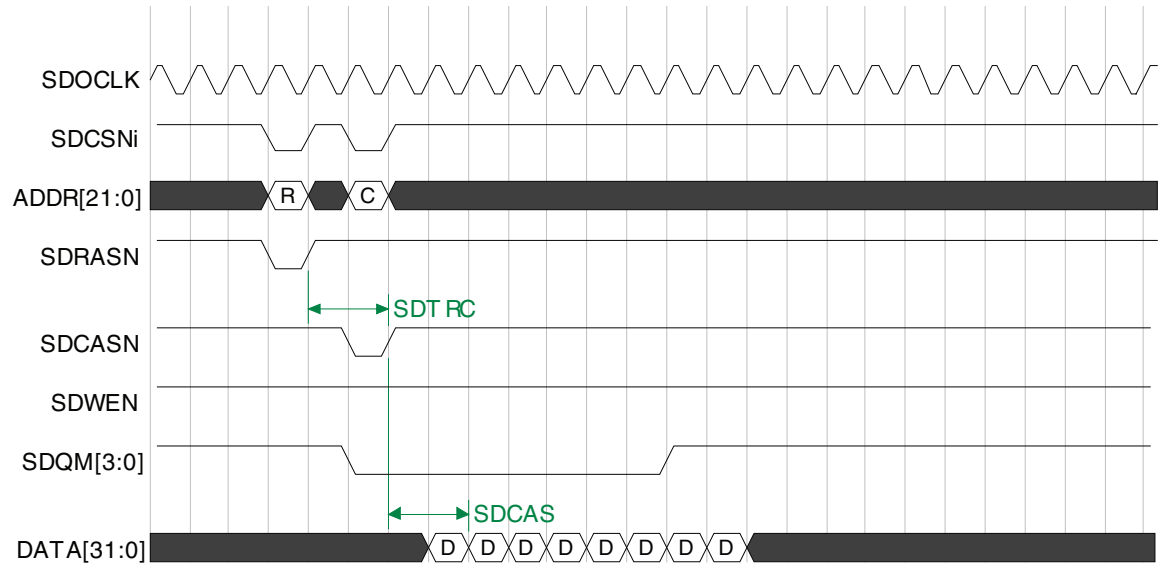


Figure 13. SDRAM Read Timing

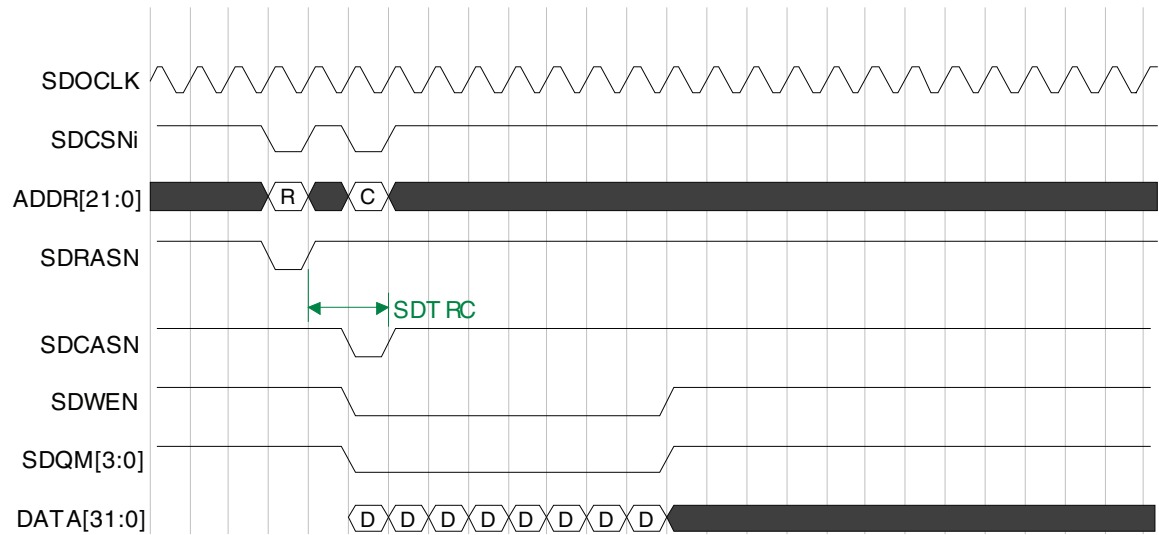
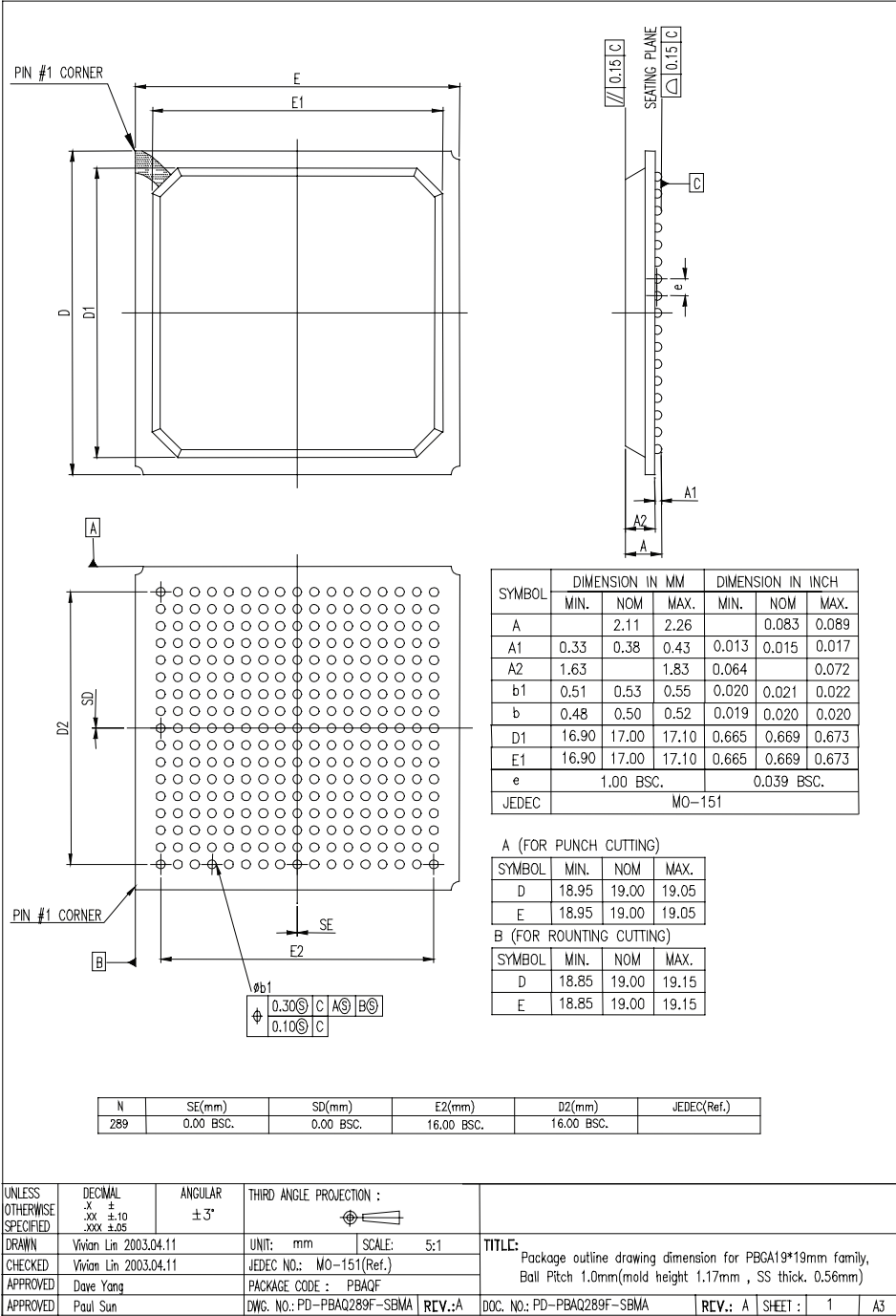


Figure 14. SDRAM Write Timing

| Symbol | Parameter                             | Registers |
|--------|---------------------------------------|-----------|
| SDTRC  | Programmable SDRAM RAS to CAS latency | 0x4038    |
| SDCAS  | Programmable SDRAM CAS latency        | 0x4038    |

Table 5. SDRAM Timing Parameters

Package Information



289-Pin PBGA

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