LAN9312

High Performance Two Port 10/100 Managed Ethernet Switch with 32-Bit Non-PCI CPU Interface

PRODUCT FEATURES

Datasheet

Highlights

- High performance and full featured 2 port switch with VLAN, QoS packet prioritization, Rate Limiting, IGMP monitoring and management functions
- Easily interfaces to most 32-bit embedded CPU's
- Unique Virtual PHY feature simplifies software development by mimicking the multiple switch ports as a single port MAC/PHY
- Integrated IEEE 1588 Hardware Time Stamp Unit

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions
- Digital video recorders
- VoIP/Video phone systems
- Home gateways
- Test/Measurement equipment
- Industrial automation systems

Key Benefits

- Ethernet Switch Fabric
  - 32K buffer RAM
  - 1K entry forwarding table
  - Port based IEEE 802.1Q VLAN support (16 groups)
    - Programmable IEEE 802.1Q tag insertion/removal
  - IEEE 802.1d spanning tree protocol support
  - QoS/CoS Packet prioritization
    - 4 dynamic QoS queues per port
    - Input priority determined by VLAN tag, DA lookup, TOS, DIFFSERV or port default value
    - Programmable class of service map based on input priority
    - Remapping of 802.1Q priority field on per port basis
    - Programmable rate limiting at the ingress/egress ports with random early discard, per port / priority
  - IGMP v1/v2/v3 monitoring for Multicast packet filtering
  - Programmable filter by MAC address
- Switch Management
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic on any ports or port pairs
  - Fully compliant statistics (MIB) gathering counters
  - Control registers configurable on-the-fly
- Ports
  - 2 internal 10/100 PHYs with HP Auto-MDIX support
  - Fully compliant with IEEE 802.3 standards
  - 10BASE-T and 100BASE-TX support
  - Full and half duplex support
  - Full duplex flow control
  - Backpressure (forced collision) half duplex flow control
  - Automatic flow control based on programmable levels
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding
  - 2K Jumbo packet support
  - Programmable interframe gap, flow control pause value
  - Full transmit/receive statistics
  - Auto-negotiation
  - Automatic MDI/MDI-X
  - Loop-back mode
- High-performance host bus interface
  - Provides in-band network communication path
  - Access to management registers
  - Simple, SRAM-like interface
  - 32-bit data bus
  - Big, little, and mixed endian support
  - Large TX and RX FIFO's for high latency applications
  - Programmable water marks and threshold levels
  - Host interrupt support
- IEEE 1588 Hardware Time Stamp Unit
  - Global 64-bit tunable clock
  - Master or slave mode per port
  - Time stamp on TX or RX of Sync and Delay_req packets per port, Timestamp on GPIO
  - 64-bit timer comparator event generation (GPIO or IRQ)
- Comprehensive Power Management Features
  - Wake on LAN
  - Wake on link status change (energy detect)
  - Magic packet wakeup
  - Wakeup indicator event signal
- Other Features
  - General Purpose Timer
  - Serial EEPROM interface (I^2C master or Microwire™ master) for non-managed configuration
  - Programmable GPIOs/LEDs
- Single 3.3V power supply
- Available in Commercial Temp. Range

Order Numbers:

LAN9312-NU For 128-Pin, VTQFP Lead-Free RoHS Compliant Package (0 TO 70°C Temp Range)

LAN9312-NZW For 128-Pin, XVTQFP Lead-Free RoHS Compliant Package (0 TO 70°C Temp Range)

LAN9312-NU-TR For 128-Pin, VTQFP Lead-Free RoHS Compliant Package (0 TO 70°C Temp Range)

LAN9312-NZW-TR For 128-Pin, XVTQFP Lead-Free RoHS Compliant Package (0 TO 70°C Temp Range)

TR indicates tape & reel option.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

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Chapter 1 Preface

1.1 General Terms

100BT	100BASE-T (100Mbps Fast Ethernet, IEEE 802.3u)
ADC	Analog-to-Digital Converter
ALR	Address Logic Resolution
BLW	Baseline Wander
BM	Buffer Manager - Part of the switch fabric
BPDU	Bridge Protocol Data Unit - Messages which carry the Spanning Tree Protocol information
Byte	8-bits
CSMA/CD	Carrier Sense Multiple Access / Collision Detect
CSR	Control and Status Registers
CTR	Counter
DA	Destination Address
DWORD	32-bits
EPC	EEPROM Controller
FCS	Frame Check Sequence - The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction.
FIFO	First In First Out buffer
FSM	Finite State Machine
GPIO	General Purpose I/O
HBI	Host Bus Interface. The physical bus connecting the LAN9312 to the host. Also referred to as the Host Bus.
HBIC	Host Bus Interface Controller. The hardware module that interfaces the LAN9312 to the HBI.
Host	External system (Includes processor, application software, etc.)
IGMP	Internet Group Management Protocol
Inbound	Refers to data input to the LAN9312 from the host
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true, and the status bit is cleared by writing a zero.
lsb	Least Significant Bit
LSB	Least Significant Byte
MDI	Medium Dependant Interface
MDIX	Media Independent Interface with Crossover

MII	Media Independent Interface
MIIM	Media Independent Interface Management
MIL	MAC Interface Layer
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
msb	Most Significant Bit
MSB	Most Significant Byte
NRZI	Non Return to Zero Inverted. This encoding method inverts the signal for a “1” and leaves the signal unchanged for a “0”
N/A	Not Applicable
NC	No Connect
OUI	Organizationally Unique Identifier
Outbound	Refers to data output from the LAN9312 to the host
PIO cycle	Program I/O cycle. An SRAM-like read or write cycle on the HBI.
PISO	Parallel In Serial Out
PLL	Phase Locked Loop
PTP	Precision Time Protocol
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RTC	Real-Time Clock
SA	Source Address
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame.
SIPO	Serial In Parallel Out
SMI	Serial Management Interface
SQE	Signal Quality Error (also known as “heartbeat”)
SSD	Start of Stream Delimiter
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
UUID	Universally Unique IDentifier
WORD	16-bits

1.2 Buffer Types

Table 1.1 describes the pin buffer type notation used in Chapter 3, "Pin Description and Configuration," on page 26 and throughout this document.

Table 1.1 Buffer Types

BUFFER TYPE	DESCRIPTION
IS	Schmitt-triggered Input
O8	Output with 8mA sink and 8mA source
OD8	Open-drain output with 8mA sink
O12	Output with 12mA sink and 12mA source
OD12	Open-drain output with 12mA sink
PU	50uA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the LAN9312. When connected to a load that must be pulled high, an external resistor must be added.
PD	50uA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the LAN9312. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AO	Analog output
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

1.3 Register Nomenclature

Table 1.2 describes the register bit attribute notation used throughout this document.

Table 1.2 Register Bit Types

REGISTER BIT TYPE NOTATION	REGISTER BIT DESCRIPTION
R	**Read:** A register or bit with this attribute can be read.
W	**Read:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
WC	**Write One to Clear:** writing a one clears the value. Writing a zero has no effect
WAC	**Write Anything to Clear:** writing anything clears the value.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
SS	**Self-Setting:** Contents are self-setting after being cleared. Writes of one have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** Bits with this attribute will stay high until the bit is read. After it is read, the bit will either remain high if the high condition remains, or will go low if the high condition has been removed. If the bit has not been read, the bit will remain high regardless of a change to the high condition. This mode is used in some Ethernet PHY registers.
NASR	**Not Affected by Software Reset.** The state of NASR bits do not change on assertion of a software reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

Many of these register bit notations can be combined. Some examples of this are shown below:

- **R/W:** Can be written. Will return current setting on a read.
- **R/WAC:** Will return current setting on a read. Writing anything clears the bit.

Chapter 2 Introduction

2.1 General Description

The LAN9312 is a full featured, 2 port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9312 combines all the functions of a 10/100 switch system, including the switch fabric, packet buffers, buffer manager, media access controllers (MACs), PHY transceivers, and host bus interface. The LAN9312 complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol specification and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications.

At the core of the LAN9312 is the high performance, high efficiency 3 port Ethernet switch fabric. The switch fabric contains a 3 port VLAN layer 2 switch engine that supports untagged, VLAN tagged, and priority tagged frames. The switch fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed, and a 1K entry forwarding table provides ample room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the buffer manager block within the switch fabric. All aspects of the switch fabric are managed via the switch fabric configuration and status registers, which are indirectly accessible via the memory mapped system control and status registers.

The LAN9312 provides 2 switched ports. Each port is fully compliant with the IEEE 802.3 standard and all internal MACs and PHYs support full/half duplex 10BASE-T and 100BASE-TX operation. The LAN9312 provides 2 on-chip PHYs, 1 Virtual PHY and 3 MACs. The Virtual PHY and the Host MAC are used to connect the LAN9312 switch fabric to the host bus interface. All ports support automatic or manual full duplex flow control or half duplex backpressure (forced collision) flow control. Automatic 32-bit CRC generation/checking and automatic payload padding are supported to further reduce CPU overhead. 2K jumbo packet (2048 byte) support allows for oversized packet transfers, effectively increasing throughput while deceasing CPU load. All MAC and PHY related settings are fully configurable via their respective registers within the LAN9312.

The integrated Host Bus Interface (HBI) easily interfaces to most 32-bit embedded CPU's via a simple SRAM like interface, enabling switch fabric access via the internal Host MAC and allowing full control over the LAN9312 via memory mapped system control and status registers. The HBI supports 32-bit operation with big, little, and mixed endian operations. Four separate FIFO mechanisms (TX/RX Data FIFO's, TX/RX Status FIFO's) interface the HBI to the Host MAC and facilitate the transferring of packet data and status information between the host CPU and the switch fabric. The LAN9312 also provides power management features which allow for wake on LAN, wake on link status change (energy detect), and magic packet wakeup detection. A configurable host interrupt pin allows the device to inform the host CPU of any internal interrupts.

The LAN9312 contains an I^2C/Microwire master EEPROM controller for connection to an optional EEPROM. This allows for the storage and retrieval of static data. The internal EEPROM Loader can be optionally configured to automatically load stored configuration settings from the EEPROM into the LAN9312 at reset.

In addition to the primary functionality described above, the LAN9312 provides additional features designed for extended functionality. These include a configurable 16-bit General Purpose Timer (GPT), a 32-bit 25MHz free running counter, a 12-bit configurable GPIO/LED interface, and IEEE 1588 time stamping on all ports and select GPIOs. The IEEE time stamp unit provides a 64-bit tunable clock for accurate PTP timing and a timer comparator to allow time based interrupt generation.

The LAN9312's performance, features and small size make it an ideal solution for many applications in the consumer electronics and industrial automation markets. Targeted applications include: set top boxes (cable, satellite and IP), digital televisions, digital video recorders, voice over IP and video phone systems, home gateways, and test and measurement equipment.

2.2 Block Diagram

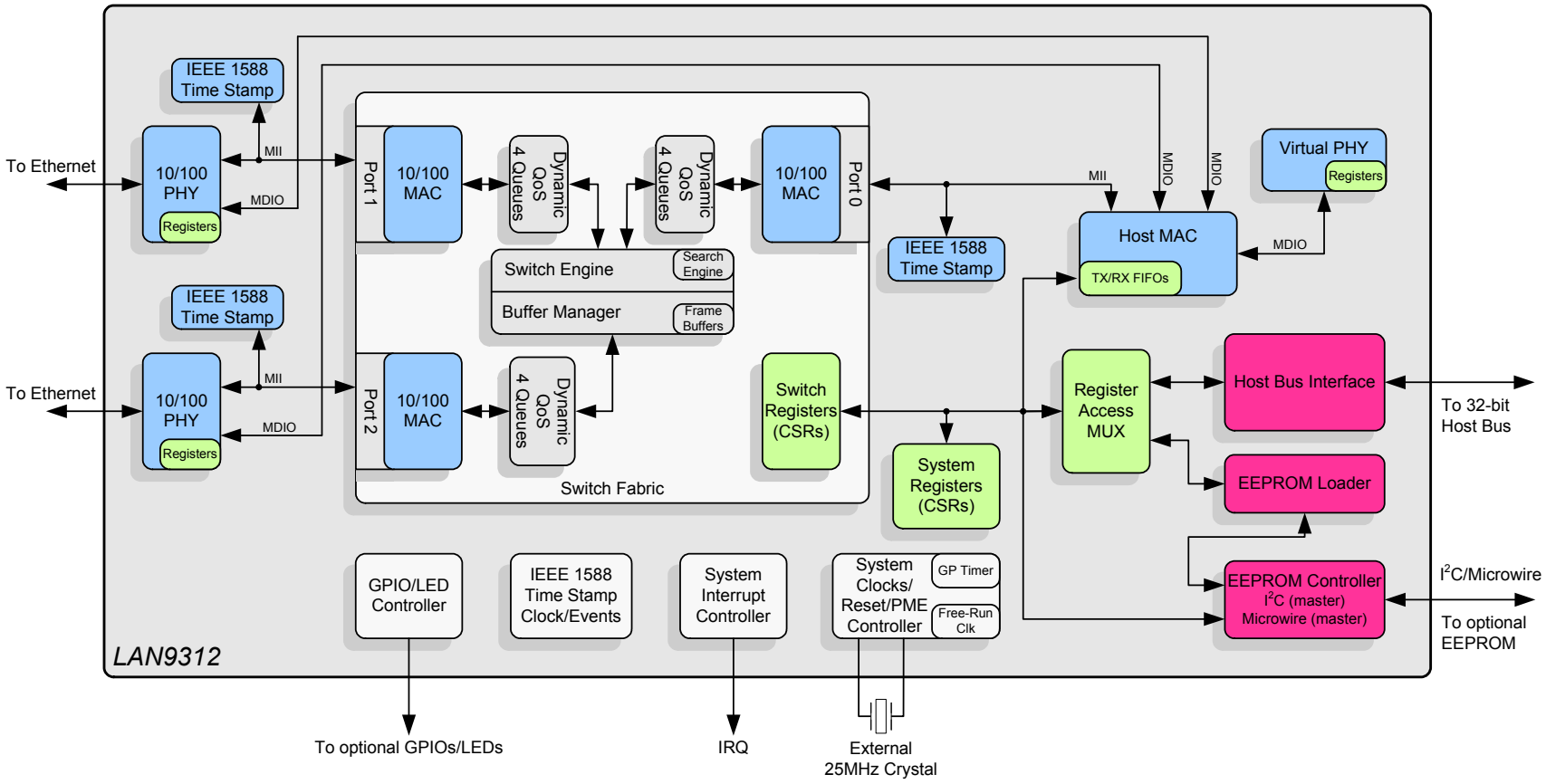


Figure 2.1 Internal LAN9312 Block Diagram

2.2.1 System Clocks/Reset/PME Controller

A clock module contained within the LAN9312 generates all the system clocks required by the device. This module interfaces directly with the external 25MHz crystal/oscillator to generate the required clock divisions for each internal module, with the exception of the 1588 clocks, which are generated in the 1588 Time Stamp Clock/Events module. A 16-bit general purpose timer and 32-bit free-running clock are provided by this module for general purpose use.

The LAN9312 reset events are categorized as chip-level resets, multi-module resets, and single-module resets.

A chip-level reset is initiated by assertion of any of the following input events:

- **Power-On Reset**
- **nRST Pin Reset**

A multi-module reset is initiated by assertion of the following:

- **Digital Reset** - DIGITAL_RST (bit 0) in the Reset Control Register (RESET_CTL)
  - Resets all LAN9312 sub-modules except the Ethernet PHYs (Port 1 PHY, Port 2 PHY, and Virtual PHY)
- **Soft Reset** - SRST (bit 0) in the Hardware Configuration Register (HW_CFG)
  - Resets the HBI, Host MAC, and System CSRs below address 100h

A single-module reset is initiated by assertion of the following:

- **Port 2 PHY Reset** - PHY2_RST (bit 2) in the Reset Control Register (RESET_CTL) or Reset (bit 15) in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x)
  - Resets the Port 2 PHY
- **Port 1 PHY Reset** - PHY1_RST (bit 1) in the Reset Control Register (RESET_CTL) or Reset (bit 15) in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x)
  - Resets the Port 1 PHY
- **Virtual PHY Reset** - VPHY_RST (bit 0) in the Reset Control Register (RESET_CTL), (bit 10) in the Power Management Control Register (PMT_CTRL), or Reset (bit 15) in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL)
  - Resets the Virtual PHY

The LAN9312 supports numerous power management and wakeup features. The Port 1 & 2 PHYs provide general power-down and energy detect power-down modes, which allow a reduction in PHY power consumption. The Host MAC provides wake-up frame detection and magic packet detection modes. The LAN9312 can be programmed to issue an external wake signal (PME) via several methods, including wake on LAN, wake on link status change (energy detect), and magic packet wakeup. The PME signal is ideal for triggering system power-up using remote Ethernet wakeup events.

2.2.2 System Interrupt Controller

The LAN9312 provides a multi-tier programmable interrupt structure which is controlled by the System Interrupt Controller. At the top level are the Interrupt Status Register (INT_STS) and Interrupt Enable Register (INT_EN). These registers aggregate and control all interrupts from the various LAN9312 sub-modules. The LAN9312 is capable of generating interrupt events from the following:

- **1588 Time Stamp**
- **Switch Fabric**
- **Ethernet PHYs**
- **GPIOs**
- **Host MAC (FIFOs, power management)**
- **General Purpose Timer**

- **Software (general purpose)**

A dedicated programmable IRQ interrupt output pin is provided for external indication of any LAN9312 interrupts. The IRQ pin is controlled via the Interrupt Configuration Register (IRQ_CFG), which allows configuration of the IRQ buffer type, polarity, and de-assertion interval.

2.2.3 Switch Fabric

The Switch Fabric consists of the following major function blocks:

- **10/100 MACs**
  There is one 10/100 Ethernet MAC per switch fabric port, which provides basic 10/100 Ethernet functionality, including transmission deferral, collision back-off/retry, TX/RX FCS checking/generation, TX/RX pause flow control, and transmit back pressure. The 10/100 MACs act as an interface between the switch engine and the 10/100 PHYs (for ports 1 and 2). The port 0 10/100 MAC interfaces the switch engine to the Host MAC. Each 10/100 MAC includes RX and TX FIFOs and per port statistic counters.
- **Switch Engine**
  This block, consisting of a 3 port VLAN layer 2 switching engine, provides the control for all forwarding/filtering rules and supports untagged, VLAN tagged, and priority tagged frames. The switch engine provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, and port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. A 1K entry forwarding table provides ample room for MAC address forwarding tables.
- **Buffer Manager**
  This block controls the free buffer space, multi-level transmit queues, transmission scheduling, and packet dropping of the switch fabric. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed. Each port is allocated 1a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block.
- **Switch CSRs**
  This block contains all switch related control and status registers, and allows all aspects of the switch fabric to be managed. These registers are indirectly accessible via the memory mapped system control and status registers

2.2.4 Ethernet PHYs

The LAN9312 contains three PHYs: Port 1 PHY, Port 2 PHY and a Virtual PHY. The Port 1 & 2 PHYs are identical in functionality and each connect their corresponding Ethernet signal pins to the switch fabric MAC of their respective port. These PHYs interface with their respective MAC via an internal MII interface. The Virtual PHY provides the virtual functionality of a PHY and allows connection of the Host MAC to port 0 of the switch fabric as if it was connected to a single port PHY. All PHYs comply with the IEEE 802.3 Physical Layer for Twisted Pair Ethernet and can be configured for full/half duplex 100 Mbps (100BASE-TX) or 10Mbps (10BASE-T) Ethernet operation. All PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set.

2.2.5 Host Bus Interface (HBI)

The Host Bus Interface (HBI) module provides a high-speed asynchronous SRAM-like slave interface that facilitates communication between the LAN9312 and a host system. The HBI allows access to the System CSRs and handles byte swapping based on the dynamic endianess select. The HBI interfaces to the switch fabric via the Host MAC, which contains the TX/RX Data and Status FIFOs, Host MAC registers and power management features. The main features of the HBI are:

- **Asynchronous 32-bit Host Bus Interface**
  - Host Data Bus Endianess Control
  - Direct FIFO Access Modes

- **System CSRs Access**
- **Interrupt Support**

2.2.6 Host MAC

The Host MAC incorporates the essential protocol requirements for operating an Ethernet/IEEE 802.3-compliant node and provides an interface between the Host Bus Interface (HBI) and the Ethernet PHYs and Switch Fabric. On the front end, the Host MAC interfaces to the HBI via 2 sets of FIFO's (TX Data FIFO, TX Status FIFO, RX Data FIFO, RX Status FIFO). The FIFOs are a conduit between the HBI and the Host MAC through which all transmitted and received data and status information is passed. An additional bus is used to access the Host MAC CSR's via the Host MAC CSR Interface Command Register (MAC_CSR_CMD) and Host MAC CSR Interface Data Register (MAC_CSR_DATA) system registers.

On the back end, the Host MAC interfaces with the 10/100 Ethernet PHY's (Virtual PHY, Port 1 PHY, Port 2 PHY) via an internal SMI (Serial Management Interface) bus. This allows the Host MAC access to the PHY's internal registers via the Host MAC MII Access Register (HMAC_MII_ACC) and Host MAC MII Data Register (HMAC_MII_DATA). The Host MAC interfaces to the Switch Engine Port 0 via an internal MII (Media Independent Interface) connection allowing for incoming and outgoing Ethernet packet transfers.

The Host MAC can operate at either 100Mbps or 10Mbps in both half-duplex or full-duplex modes. When operating in half-duplex mode, the Host MAC complies fully with Section 4 of ISO/IEC 8802-3 (ANSI/IEEE standard) and ANSI/IEEE 802.3 standards. When operating in full-duplex mode, the Host MAC complies with IEEE 802.3 full-duplex operation standard.

2.2.7 EEPROM Controller/Loader

The EEPROM Controller is an I^2C/Microwire master module which interfaces an optional external EEPROM with the system register bus and the EEPROM Loader. Multiple types (I^2C/Microwire) and sizes of external EEPROMs are supported. Configuration of the EEPROM type and size are accomplished via the eeprom_type_strap and eeprom_size_strap[1:0] configuration straps respectively. Various commands are supported for each EEPROM type, allowing for the storage and retrieval of static data. The I^2C interface conforms to the Philips *I^2C-Bus Specification*.

The EEPROM Loader module interfaces to the EEPROM Controller, Ethernet PHYs, and the system CSRs. The EEPROM Loader provides the automatic loading of configuration settings from the EEPROM into the LAN9312 at reset. The EEPROM Loader runs upon a pin reset (nRST), power-on reset (POR), digital reset (DIGITAL_RST bit in the Reset Control Register (RESET_CTL)), or upon the issuance of a RELOAD command via the EEPROM Command Register (E2P_CMD).

2.2.8 1588 Time Stamp

The IEEE 1588 Time Stamp modules provide hardware support for the IEEE 1588 Precision Time Protocol (PTP), allowing clock synchronization with remote Ethernet devices, packet time stamping, and time driven event generation. Time stamping is supported on all ports, with an individual IEEE 1588 Time Stamp module connected to each port via the MII bus. Any port may function as a master or a slave clock per the IEEE 1588 specification, and the LAN9312 as a whole may function as a boundary clock.

A 64-bit tunable clock is provided that is used as the time source for all IEEE 1588 time stamp related functions. The IEEE 1588 Clock/Events block provides IEEE 1588 clock comparison based interrupt generation and time stamp related GPIO event generation. Two LAN9312 GPIO pins (GPIO[8:9]) can be used to trigger a time stamp capture when configured as an input, or output a signal from the GPIO based on an IEEE 1588 clock target compare event when configured as an output. All features of the IEEE 1588 hardware time stamp unit can be monitored and configured via their respective IEEE 1588 configuration and status registers (CSRs).

2.2.9 GPIO/LED Controller

The LAN9312 provides 12 configurable general-purpose input/output pins which are controlled via this module. These pins can be individually configured via the GPIO/LED CSRs to function as inputs, push-pull outputs, or open drain outputs and each is capable of interrupt generation with configurable polarity. Two of the GPIO pins (GPIO[9:8]) can be used for IEEE 1588 timestamp functions, allowing GPIO driven 1588 time clock capture when configured as an input, or GPIO output generation based on an IEEE 1588 clock target compare event.

In addition, 8 of the GPIO pins can be alternatively configured as LED outputs. These pins, GPIO[7:0] (nP1LED[3:0] and nP2LED[3:0]), may be enabled to drive Ethernet status LEDs for external indication of various attributes of the switch ports.

2.3 System Configuration

In a typical application, the LAN9312 Host Bus Interface (HBI) is connected to the host microprocessor/microcontroller via the asynchronous 32-bit interface, allowing access to the LAN9312 system configuration and status registers. The LAN9312 utilizes the internal Host MAC to provide a network path for the host CPU. The LAN9312 may share the host bus with additional system memory and/or peripherals. For more information on the HBI, refer to Chapter 8, "Host Bus Interface (HBI)," on page 99.

The 2 Ethernet ports of the LAN9312 must be connected to Auto-MDIX style magnetics for proper operation on the Ethernet network. Refer to the SMSC Application Note 8.13 “Suggested Magnetics” for further details.

The LAN9312 also supports optional EEPROM and GPIOs/LEDs. When an EEPROM is connected, the EEPROM loader can be used to load the initial device configuration from the external EEPROM via the I^2C/Microwire interface.

A system configuration diagram of the LAN9312 in a typical embedded environment can be seen in Figure 2.2.

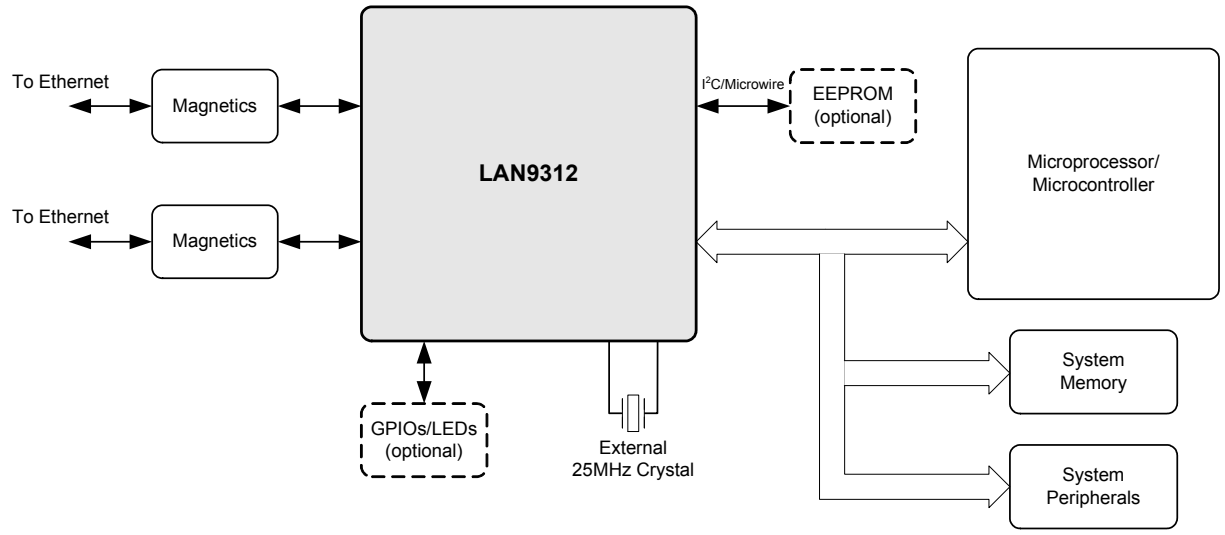


Figure 2.2 System Block Diagram

Chapter 3 Pin Description and Configuration

3.1 Pin Diagrams

3.1.1 128-VTQFP Pin Diagram

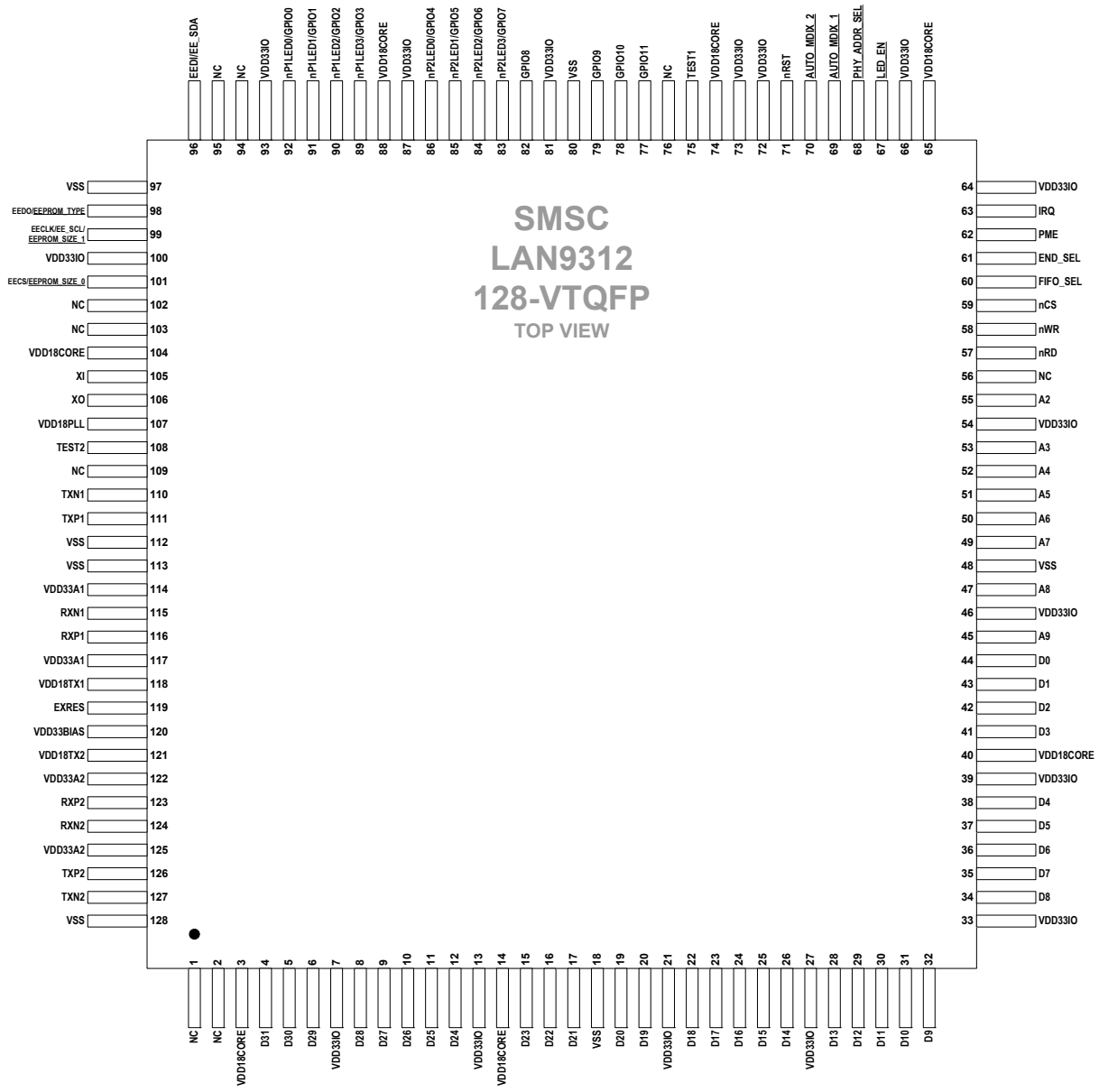
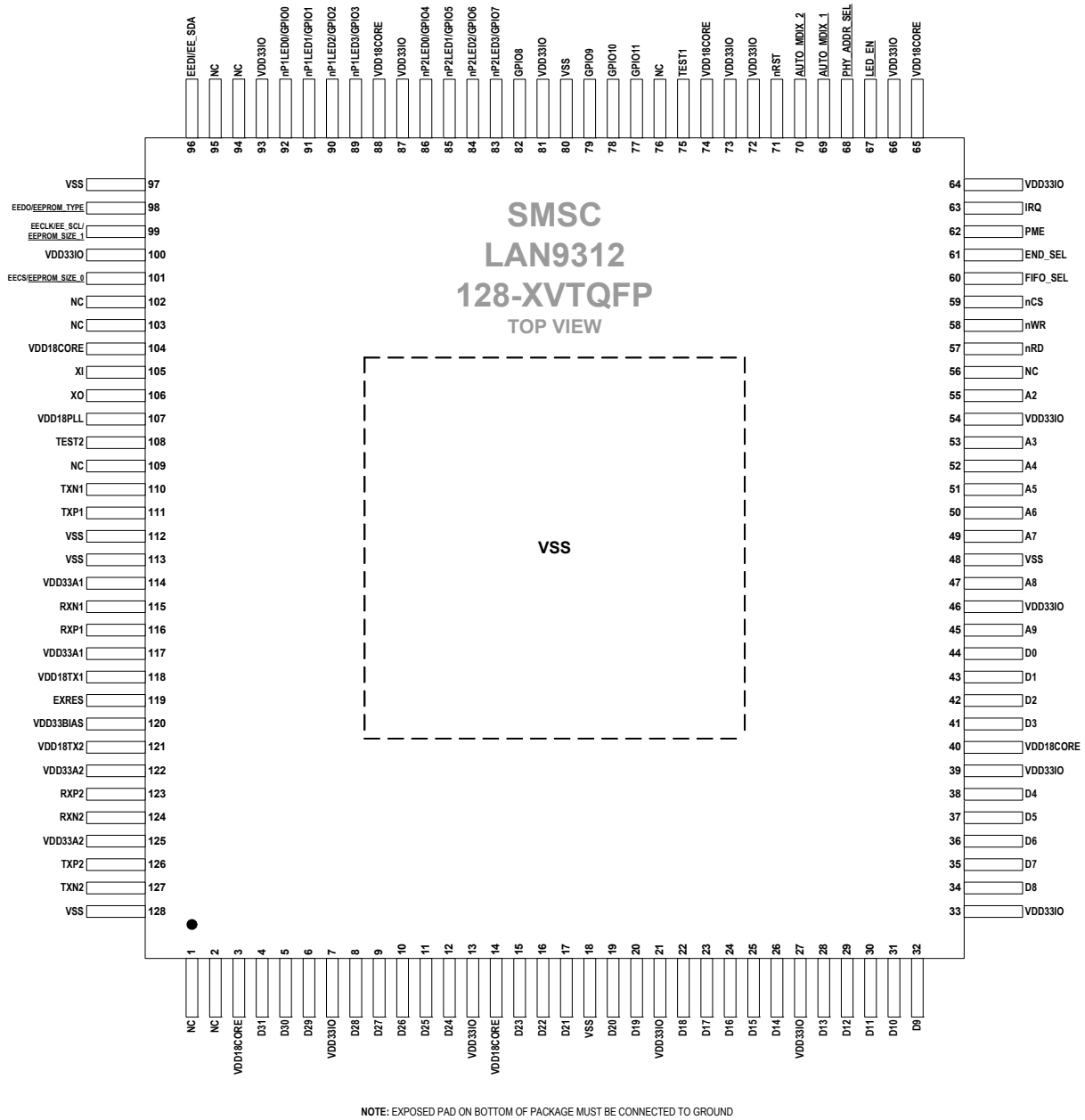


Figure 3.1 LAN9312 128-VTQFP Pin Assignments (TOP VIEW)

3.1.2 128-XVTQFP Pin Diagram



NOTE: EXPOSED PAD ON BOTTOM OF PACKAGE MUST BE CONNECTED TO GROUND

Figure 3.2 LAN9312 128-XVTQFP Pin Assignments (TOP VIEW)

3.2 Pin Descriptions

This section contains the descriptions of the LAN9312 pins. The pin descriptions have been broken into functional groups as follows:

- LAN Port 1 Pins
- LAN Port 2 Pins
- LAN Port 1 & 2 Power and Common Pins
- Host Bus Interface Pins
- EEPROM Pins
- Dedicated Configuration Strap Pins
- Miscellaneous Pins
- PLL Pins
- Core and I/O Power and Ground Pins
- No-Connect Pins

Note: A list of buffer type definitions is provided in Section 1.2, "Buffer Types," on page 18.

Table 3.1 LAN Port 1 Pins

PIN	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
89-92	Port 1 LED Indicators	nP1LED[3:0]	OD12	**LED Indicators:** When configured as LED outputs via the LED Configuration Register (LED_CFG), these pins are open-drain, active low outputs and the pull-ups and input buffers are disabled. The functionality of each pin is determined via the LED_CFG[9:8] bits.
	General Purpose I/O Data	GPIO[3:0]	IS/O12/ OD12 (PU)	**General Purpose I/O Data:** When configured as GPIO via the LED Configuration Register (LED_CFG), these general purpose signals are fully programmable as either push-pull outputs, open-drain outputs or Schmitt-triggered inputs by writing the General Purpose I/O Configuration Register (GPIO_CFG) and General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). The pull-ups are enabled in GPIO mode. The input buffers are disabled when set as an output. **Note:** See Chapter 13, "GPIO/LED Controller," on page 162 for additional details.
110	Port 1 Ethernet TX Negative	TXN1	AIO	**Ethernet TX Negative:** Negative output of Port 1 Ethernet transmitter. See Note 3.1 for additional information.
111	Port 1 Ethernet TX Positive	TXP1	AIO	**Ethernet TX Positive:** Positive output of Port 1 Ethernet transmitter. See Note 3.1 for additional information.
115	Port 1 Ethernet RX Negative	RXN1	AIO	**Ethernet RX Negative:** Negative input of Port 1 Ethernet receiver. See Note 3.1 for additional information.
116	Port 1 Ethernet RX Positive	RXP1	AIO	**Ethernet RX Positive:** Positive input of Port 1 Ethernet receiver. See Note 3.1 for additional information.

Note 3.1 The pin names for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

Table 3.2 LAN Port 2 Pins

PIN	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
83-86	Port 2 LED Indicators	nP2LED[3:0]	OD12	**LED indicators:** When configured as LED outputs via the LED Configuration Register (LED_CFG), these pins are open-drain, active low outputs and the pull-ups and input buffers are disabled. The functionality of each pin is determined via the LED_CFG[9:8] bits.
	General Purpose I/O Data	GPIO[7:4]	IS/O12/ OD12 (PU)	**General Purpose I/O Data:** When configured as GPIO via the LED Configuration Register (LED_CFG), these general purpose signals are fully programmable as either push-pull outputs, open-drain outputs or Schmitt-triggered inputs by writing the General Purpose I/O Configuration Register (GPIO_CFG) and General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). The pull-ups are enabled in GPIO mode. The input buffers are disabled when set as an output. **Note:** See Chapter 13, "GPIO/LED Controller," on page 162 for additional details.
127	Port 2 Ethernet TX Negative	TXN2	AIO	**Ethernet TX Negative:** Negative output of Port 2 Ethernet transmitter. See Note 3.2 for additional information.
126	Port 2 Ethernet TX Positive	TXP2	AIO	**Ethernet TX Positive:** Positive output of Port 2 Ethernet transmitter. See Note 3.2 for additional information.
124	Port 2 Ethernet RX Negative	RXN2	AIO	**Ethernet RX Negative:** Negative input of Port 2 Ethernet receiver. See Note 3.2 for additional information.
123	Port 2 Ethernet RX Positive	RXP2	AIO	**Ethernet RX Positive:** Positive input of Port 2 Ethernet receiver. See Note 3.2 for additional information.

Note 3.2 The pin names for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

Table 3.3 LAN Port 1 & 2 Power and Common Pins

PIN	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
119	Bias Reference	EXRES	AI	**Bias Reference:** Used for internal bias circuits. Connect to an external 12.4K ohm, 1% resistor to ground.
114,117	+3.3V Port 1 Analog Power Supply	VDD33A1	P	**+3.3V Port 1 Analog Power Supply** Refer to the LAN9312 reference schematic for additional connection information.

Table 3.3 LAN Port 1 & 2 Power and Common Pins (continued)

PIN	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
122,125	+3.3V Port 2 Analog Power Supply	VDD33A2	P	**+3.3V Port 2 Analog Power Supply** Refer to the LAN9312 reference schematic for additional connection information.
120	+3.3V Master Bias Power Supply	VDD33BIAS	P	**+3.3V Master Bias Power Supply** Refer to the LAN9312 reference schematic for additional connection information.
121	Port 2 Transmitter +1.8V Power Supply	VDD18TX2	P	**Port 2 Transmitter +1.8V Power Supply:** This pin is supplied from the internal PHY voltage regulator. This pin must be tied to the VDD18TX1 pin for proper operation. Refer to the LAN9312 reference schematic for additional connection information.
118	Port 1 Transmitter +1.8V Power Supply	VDD18TX1	P	**Port 1 Transmitter +1.8V Power Supply:** This pin must be connected directly to the VDD18TX2 pin for proper operation. Refer to the LAN9312 reference schematic for additional connection information.

Table 3.4 Host Bus Interface Pins

PIN	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
4-6, 8-12, 15-17,19, 20,22-26, 28-32, 34-38, 41-44	Host Bus Data	D[31:0]	IS/O8	**Host Bus Data High:** Bits 31-0 of the Host Bus 32-bit data port. **Note:** Big and little endianess is supported.
45,47, 49-53, 55	Host Bus Address	A[9:2]	IS	**Host Bus Address:** 9-bit Host Bus Address Port used to select Internal CSR's and TX and RX FIFO's. **Note:** The A0 and A1 bits are not used because the LAN9312 must be accessed on DWORD boundaries.
57	Read Strobe	nRD	IS	**Read Strobe:** Active low strobe to indicate a read cycle. This signal is qualified by the nCS chip select.
58	Write Strobe	nWR	IS	**Write Strobe:** Active low strobe to indicate a write cycle. This signal is qualified by the nCS chip select.
59	Chip Select	nCS	IS	**Chip Select:** Active low signal used to qualify read and write operations.

Table 3.4 Host Bus Interface Pins (continued)

PIN	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
60	Data FIFO Direct Access Select	FIFO_SEL	IS	**Data FIFO Direct Access Select:** When driven high, all accesses to the LAN9312 are directed to the RX and TX Data FIFO's. All reads are from the RX Data FIFO, and all writes are to the TX Data FIFO. In this mode, the address input is ignored. Refer to Section 14.1.3, "Direct FIFO Access Mode," on page 167 for additional information.
61	Endianess Select	END_SEL	IS	**Endianess Select:** When this signal is set high, big endian mode is selected. When low, little endian mode is selected. This signal may be dynamically changed or held static. Refer to Chapter 8, "Host Bus Interface (HBI)," on page 99 for additional information.

Note: Refer to Chapter 8, "Host Bus Interface (HBI)," on page 99 for additional information regarding the use of these signals.

Table 3.5 EEPROM Pins

PIN	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
96	EEPROM Microwire Data Input	EEDI	IS (PD)	**EEPROM Microwire Data Input (EEDI):** In Microwire EEPROM mode (EEPROM_TYPE = 0), this pin is the Microwire EEPROM serial data input.
	EEPROM I^2C Serial Data Input/Output	EE_SDA	IS/OD8	**EEPROM I^2C Serial Data Input/Output (EE_SDA):** In I^2C EEPROM mode (EEPROM_TYPE = 1), this pin is the I^2C EEPROM serial data input/output. **Note:** If I^2C is selected, an external pull-up is required when using an EEPROM and is recommended if no EEPROM is attached.
98	EEPROM Microwire Data Output	EEDO	O8	**EEPROM Microwire Data Output:** In Microwire EEPROM mode (EEPROM_TYPE = 0), this pin is the Microwire EEPROM serial data output. **Note:** In I^2C mode (EEPROM_TYPE=1), this pin is not used and is driven low. **Note:** When not using a Microwire or I^2C EEPROM, an external pull-down resistor is recommended on this pin.
	EEPROM Type Strap	EEPROM_TYPE	IS Note 3.3	**EEPROM Type Strap:** Configures the EEPROM type. See Note 3.4 **0 = Microwire Mode** **1 = I^2C Mode** **Note:** When not using a Microwire or I^2C EEPROM, an external pull-down resistor is recommended on this pin.

Table 3.5 EEPROM Pins (continued)

PIN	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
99	EEPROM Microwire Serial Clock	EECLK	O8	**EEPROM Microwire Serial Clock (EECLK):** In Microwire EEPROM mode (EEPROM_TYPE = 0), this pin is the Microwire EEPROM clock output.
	EEPROM I^2C Serial Clock	EE_SCL	IS/OD8	**EEPROM I^2C Serial Clock (EE_SCL):** In I^2C EEPROM mode (EEPROM_TYPE=1), this pin is the I^2C EEPROM clock input/open-drain output. **Note:** If I^2C is selected, an external pull-up is required when using an EEPROM and is recommended if no EEPROM is attached.
	EEPROM Size Strap 1	EEPROM_SIZE_1	IS Note 3.5	**EEPROM Size Strap 1:** Configures the high bit of the EEPROM size range as specified in Section 10.2, "I2C/Microwire Master EEPROM Controller," on page 137. This bit is not used for I^2C EEPROMs. See Note 3.4.
101	EEPROM Microwire Chip Select	EECS	O8	**EEPROM Microwire Chip Select:** In Microwire EEPROM mode (EEPROM_TYPE = 0), this pin is the Microwire EEPROM chip select output. **Note:** In I^2C mode (EEPROM_TYPE=1), this pin is not used and is driven low.
	EEPROM Size Strap 0	EEPROM_SIZE_0	IS Note 3.3	**EEPROM Size Strap 0:** Configures the low bit of the EEPROM size range as specified in Section 10.2, "I2C/Microwire Master EEPROM Controller," on page 137. See Note 3.4.

Note 3.3 The IS buffer type is valid only during the time specified in Section 15.5.2, "Reset and Configuration Strap Timing," on page 445.

Note 3.4 Configuration strap values are latched on power-on reset or nRST de-assertion. Configuration strap pins are identified by an underlined symbol name. Refer to Section 4.2.4, "Configuration Straps," on page 40 for more information.

Note 3.5 The IS buffer type is valid only during the time specified in Section 15.5.2, "Reset and Configuration Strap Timing," on page 445 and when in I^2C mode.

Table 3.6 Dedicated Configuration Strap Pins

<table>
<tr><th>PIN</th><th>NAME</th><th>SYMBOL</th><th>BUFFER TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>67</td><td>LED Enable Strap</td><td>LED_EN</td><td>IS
(PU)</td><td>LED Enable Strap: Configures the default value for the LED_EN bits in the LED Configuration Register (LED_CFG). When latched low, all 8 LED/GPIO pins are configured as GPIOs. When latched high, all 8 LED/GPIO pins are configured as LEDs. See Note 3.6.</td></tr>
<tr><td>68</td><td>PHY Address Strap</td><td>PHY_ADDR_SEL</td><td>IS
(PU)</td><td>PHY Address Select Strap: Configures the default MII management address values for the PHYs (Virtual, Port 1, and Port 2) as detailed in Section 7.1.1, "PHY Addressing," on page 82.

<table><tr><th>PHY_ADDR_SEL VALUE</th><th>VIRTUAL PHY ADDRESS</th><th>PORT 1 PHY ADDRESS</th><th>PORT 2 PHY ADDRESS</th></tr><tr><td>0</td><td>0</td><td>1</td><td>2</td></tr><tr><td>1</td><td>1</td><td>2</td><td>3</td></tr></table>
See Note 3.6.</td></tr>
<tr><td>69</td><td>Port 1 Auto-MDIX Enable Strap</td><td>AUTO_MDIX_1</td><td>IS
(PU)</td><td>Port 1 Auto-MDIX Enable Strap: Configures the Auto-MDIX functionality on Port 1. When latched low, Auto-MDIX is disabled. When latched high, Auto-MDIX is enabled.

See Note 3.6.</td></tr>
<tr><td>70</td><td>Port 2 Auto-MDIX Enable Strap</td><td>AUTO_MDIX_2</td><td>IS
(PU)</td><td>Port 2 Auto-MDIX Enable Strap: Configures the Auto-MDIX functionality on Port 2. When latched low, Auto-MDIX is disabled. When latched high, Auto-MDIX is enabled.

See Note 3.6.</td></tr>
</table>

Note: For more information on configuration straps, refer to Section 4.2.4, "Configuration Straps," on page 40. Additional strap pins, which share functionality with the EEPROM pins, are described in Table 3.5.

Note 3.6 Configuration strap values are latched on power-on reset or nRST de-assertion. Configuration strap pins are identified by an underlined symbol name. Some configuration straps can be overridden by values from the EEPROM Loader. Refer to Section 4.2.4, "Configuration Straps," on page 40 for more information.

Table 3.7 Miscellaneous Pins

PIN	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
77-79, 82	General Purpose I/O Data	GPIO[11:8]	IS/OD12/ O12 (PU) Note 3.7	**General Purpose I/O Data:** These general purpose signals are fully programmable as either push-pull outputs, open-drain outputs, or Schmitt-triggered inputs by writing the General Purpose I/O Configuration Register (GPIO_CFG) and General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). For more information, refer to Chapter 13, "GPIO/LED Controller," on page 162. **Note:** The remaining GPIO[7:0] pins share functionality with the LED output pins, as described in Table 3.1 and Table 3.2.
63	Interrupt Output	IRQ	O8/OD8	**Interrupt Output:** Interrupt request output. The polarity, source and buffer type of this signal is programmable via the Interrupt Configuration Register (IRQ_CFG). For more information, refer to Chapter 5, "System Interrupts," on page 49.
71	System Reset Input	nRST	IS (PU)	**System Reset Input:** This active low signal allows external hardware to reset the LAN9312. The LAN9312 also contains an internal power-on reset circuit. Thus, this signal may be left unconnected if an external hardware reset is not needed. When used, this signal must adhere to the reset timing requirements as detailed in Section 15.5.2, "Reset and Configuration Strap Timing," on page 445. **Note:** The LAN9312 must always be read at least once after power-up or reset to ensure that write operations function properly.
75	Test 1	TEST1	AI	**Test 1:** This pin must be tied to VDD33IO for proper operation.
108	Test 2	TEST2	AI	**Test 2:** This pin must be tied to VDD33IO for proper operation.
62	Power Management Event	PME	O8/OD8	**Power Management Event:** When programmed accordingly, this signal is asserted upon detection of a wakeup event. The polarity and buffer type of this signal is programmable via the PME_EN bit of the Power Management Control Register (PMT_CTRL). Refer to Chapter 4, "Clocking, Resets, and Power Management," on page 36 for additional information on the LAN9312 power management features.

Note 3.7 The input buffers are enabled when configured as GPIO inputs only.

Table 3.8 PLL Pins

PIN	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
107	PLL +1.8V Power Supply	VDD18PLL	P	**PLL +1.8V Power Supply:** This pin must be connected to VDD18CORE for proper operation. Refer to the LAN9312 reference schematic for additional connection information.
105	Crystal Input	XI	ICLK	**Crystal Input:** External 25MHz crystal input. This signal can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected.
106	Crystal Output	XO	OCLK	**Crystal Output:** External 25MHz crystal output.

Table 3.9 Core and I/O Power and Ground Pins

PIN	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
7,13,21,27, 33,39,46, 54,64,66, 72,73,81, 87,93,100	+3.3V I/O Power	VDD33IO	P	**+3.3V Power Supply for I/O Pins and Internal Regulator** Refer to the LAN9312 reference schematic for additional connection information.
3,14,40,65, 74,88,104	Digital Core +1.8V Power Supply Output	VDD18CORE	P	**Digital Core +1.8V Power Supply Output:** +1.8V power from the internal core voltage regulator. All VDD18CORE pins must be tied together for proper operation. Refer to the LAN9312 reference schematic for additional connection information.
18,48,80, 97,112,113, 128 Note 3.8	Common Ground	VSS	P	**Common Ground**

Note 3.8 Plus external pad for 128-XVTQFP package only

Table 3.10 No-Connect Pins

PIN	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1,2,56, 76,94,95, 102,103, 109	No Connect	NC	-	**No Connect:** These pins must be left floating for normal device operation.

Chapter 4 Clocking, Resets, and Power Management

4.1 Clocks

The LAN9312 includes a clock module which provides generation of all system clocks as required by the various sub-modules of the device. The LAN9312 requires a fixed-frequency 25MHz clock source for use by the internal clock oscillator and PLL. This is typically provided by attaching a 25MHz crystal to the XI and XO pins as specified in Section 15.6, "Clock Circuit," on page 454. Optionally, this clock can be provided by driving the XI input pin with a single-ended 25MHz clock source. If a single-ended source is selected, the clock input must run continuously for normal device operation. The internal PLL generates a fixed 200MHz base clock which is used to derive all LAN9312 sub-system clocks.

In addition to the sub-system clocks, the clock module is also responsible for generating the clocks used for the general purpose timer and free-running clock. Refer to Chapter 12, "General Purpose Timer & Free-Running Clock," on page 161 for additional details.

Note: Crystal specifications are provided in Table 15.15, “LAN9312Crystal Specifications,” on page 454.

4.2 Resets

The LAN9312 provides multiple hardware and software reset sources, which allow varying levels of the LAN9312 to be reset. All resets can be categorized into three reset types as described in the following sections:

- Chip-Level Resets
  - —Power-On Reset (POR)
  - —nRST Pin Reset
- Multi-Module Resets
  - —Digital Reset (DIGITAL_RST)
  - —Soft Reset (SRST)
- Single-Module Resets
  - —Port 2 PHY Reset
  - —Port 1 PHY Reset
  - —Virtual PHY Reset

The LAN9312 supports the use of configuration straps to allow automatic custom configurations of various LAN9312 parameters. These configuration strap values are set upon de-assertion of all chip-level resets and can be used to easily set the default parameters of the chip at power-on or pin (nRST) reset. Refer to Section 4.2.4, "Configuration Straps," on page 40 for detailed information on the usage of these straps.

Note: The LAN9312 EEPROM Loader is run upon a power-on reset, nRST pin reset, and digital reset. Refer to Section 10.2.4, "EEPROM Loader," on page 149 for additional information.

Table 4.1 summarizes the effect of the various reset sources on the LAN9312. Refer to the following sections for detailed information on each of these reset types.

Table 4.1 Reset Sources and Affected LAN9312 Circuitry

RESET SOURCE	SYSTEM CLOCKS/RESET/PME	SYS INTERRUPTS	SWITCH FABRIC	ETHERNET PHYS	HBI	HOST MAC	EEPROM CONTROLLER	1588 TIME STAMP	GPIO/LED CONTROLLER	CONFIG. STRAPS LATCHED	EEPROM LOADER RUN
POR	X	X	X	X	X	X	X	X	X	X	X
nRST Pin	X	X	X	X	X	X	X	X	X	X	X
Digital Reset	X	X	X		X	X	X	X	X		X
Soft Reset					X	X					Note 4.1
Port 2 PHY				X							
Port 1 PHY				X							
Virtual PHY				X							

Note 4.1 In the case of a soft reset, the EEPROM Loader is run, but loads only the MAC address into the Host MAC. No other values are loaded by the EEPROM Loader in this case.

4.2.1 Chip-Level Resets

A chip-level reset event activates all internal resets, effectively resetting the entire LAN9312. Configuration straps are latched, and the EEPROM Loader is run as a result of chip-level resets. A chip-level reset is initiated by assertion of any of the following input events:

- Power-On Reset (POR)
- nRST Pin Reset

Chip-level reset completion/configuration can be determined by polling the READY bit of the Hardware Configuration Register (HW_CFG) or Power Management Control Register (PMT_CTRL) until it is set. When set, the READY bit indicates that the reset has completed and the device is ready to be accessed.

With the exception of the Hardware Configuration Register (HW_CFG), Power Management Control Register (PMT_CTRL), Byte Order Test Register (BYTE_TEST), and Reset Control Register (RESET_CTL), read access to any internal resources is forbidden while the READY bit is cleared. Writes to any address are invalid until the READY bit is set.

Note: The LAN9312 must be read at least once after any chip-level reset to ensure that write operations function properly.

4.2.1.1 Power-On Reset (POR)

A power-on reset occurs whenever power is initially applied to the LAN9312, or if the power is removed and reapplied to the LAN9312. This event resets all circuitry within the device. Configuration straps are latched, and the EEPROM Loader is run as a result of this reset.

A POR reset typically takes approximately 23mS, plus additional time (91uS for I^2C, 28uS for Microwire) per byte of data loaded from the EEPROM via the EEPROM Loader. A full EEPROM load (64KB for I^2C, 2KB for Microwire) will complete in approximately 6.0 seconds for I^2C EEPROM, and 80mS for Microwire EEPROM.

4.2.1.2 nRST Pin Reset

Driving the nRST input pin low initiates a chip-level reset. This event resets all circuitry within the device. Use of this reset input is optional, but when used, it must be driven for the period of time specified in Section 15.5.2, "Reset and Configuration Strap Timing," on page 445. Configuration straps are latched, and the EEPROM Loader is run as a result of this reset.

A nRST pin reset typically takes approximately 760uS, plus additional time (91uS for I^2C, 28uS for Microwire) per byte of data loaded from the EEPROM via the EEPROM Loader. A full EEPROM load (64KB for I^2C, 2KB for Microwire) will complete in approximately 6.0 seconds for I^2C EEPROM, and 58mS for Microwire EEPROM.

Note: The nRST pin is pulled-high internally. If unused, this signal can be left unconnected. Do not rely on internal pull-up resistors to drive signals external to the device.

Please refer to Section Table 3.7, "Miscellaneous Pins," on page 34 for a description of the nRST pin.

4.2.2 Multi-Module Resets

Multi-module resets activate multiple internal resets, but do not reset the entire chip. Configuration straps are *not* latched upon multi-module resets. A multi-module reset is initiated by assertion of the following:

- Digital Reset (DIGITAL_RST)
- Soft Reset (SRST)

Chip-level reset completion/configuration can be determined by polling the READY bit of the Hardware Configuration Register (HW_CFG) or Power Management Control Register (PMT_CTRL) until it is set. When set, the READY bit indicates that the reset has completed and the device is ready to be accessed.

With the exception of the Hardware Configuration Register (HW_CFG), Power Management Control Register (PMT_CTRL), Byte Order Test Register (BYTE_TEST), and Reset Control Register (RESET_CTL), read access to any internal resources is forbidden while the READY bit is cleared. Writes to any address are invalid until the READY bit is set.

Note: The digital reset and soft reset do not reset register bits designated as NASR.

Note: The LAN9312 must be read at least once after a multi-module reset to ensure that write operations function properly.

4.2.2.1 Digital Reset (DIGITAL_RST)

A digital reset is performed by setting the DIGITAL_RST bit of the Reset Control Register (RESET_CTL). A digital reset will reset all LAN9312 sub-modules except the Ethernet PHYs (Port 1 PHY, Port 2 PHY, and Virtual PHY). The EEPROM Loader will automatically run following this reset. Configuration straps are *not* latched as a result of a digital reset.

A digital reset typically takes approximately 760uS, plus additional time (91uS for I^2C, 28uS for Microwire) per byte of data loaded from the EEPROM via the EEPROM Loader. A full EEPROM load

(64KB for I^2C, 2KB for Microwire) will complete in approximately 6.0 seconds for I^2C EEPROM, and 58mS for Microwire EEPROM.

4.2.2.2 Soft Reset (SRST)

A soft reset is performed by setting the SRST bit of the Hardware Configuration Register (HW_CFG). A soft reset will reset the HBI, Host MAC, and System CSRs below address 100h. The soft reset also clears any TX or RX errors in the Host MAC transmitter and receiver (TXE/RXE). This reset does *not* latch the configuration straps. On soft reset, the EEPROM Loader is run, but loads only the MAC address into the Host MAC. No other values are loaded by the EEPROM Loader in this case.

A soft reset typically takes 590uS, plus an additional time (550uS for I^2C, 170uS for Microwire) when data is loaded from the EEPROM via the EEPROM Loader.

4.2.3 Single-Module Resets

A single-module reset will reset only the specified module. Single-module resets do *not* latch the configuration straps or initiate the EEPROM Loader. A single-module reset is initiated by assertion of the following:

- Port 2 PHY Reset
- Port 1 PHY Reset
- Virtual PHY Reset

4.2.3.1 Port 2 PHY Reset

A Port 2 PHY reset is performed by setting the PHY2_RST bit of the Reset Control Register (RESET_CTL) or the Reset bit in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). Upon completion of the Port 2 PHY reset, the PHY2_RST and Reset bits are automatically cleared. No other modules of the LAN9312 are affected by this reset.

In addition to the methods above, the Port 2 PHY is automatically reset after returning from a PHY power-down mode. This reset differs in that the PHY power-down mode reset does not reload or reset any of the PHY registers. Refer to Section 7.2.9, "PHY Power-Down Modes," on page 94 for additional information.

Port 2 PHY reset completion can be determined by polling the PHY2_RST bit in the Reset Control Register (RESET_CTL) or the Reset bit in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) until it clears. Under normal conditions, the PHY2_RST and Reset bit will clear approximately 110uS after the Port 2 PHY reset occurrence.

Note: When using the Reset bit to reset the Port 2 PHY, register bits designated as NASR are not reset.

Refer to Section 7.2.10, "PHY Resets," on page 95 for additional information on Port 2 PHY resets.

4.2.3.2 Port 1 PHY Reset

A Port 1 PHY reset is performed by setting the PHY1_RST bit of the Reset Control Register (RESET_CTL) or the Reset bit in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). Upon completion of the Port 1 PHY reset, the PHY1_RST and Reset bits are automatically cleared. No other modules of the LAN9312 are affected by this reset.

In addition to the methods above, the Port 1 PHY is automatically reset after returning from a PHY power-down mode. This reset differs in that the PHY power-down mode reset does not reload or reset any of the PHY registers. Refer to Section 7.2.9, "PHY Power-Down Modes," on page 94 for additional information.

Port 1 PHY reset completion can be determined by polling the PHY1_RST bit in the Reset Control Register (RESET_CTL) or the Reset bit in the Port x PHY Basic Control Register

(PHY_BASIC_CONTROL_x) until it clears. Under normal conditions, the PHY1_RST and Reset bit will clear approximately 110uS after the Port 1 PHY reset occurrence.

Note: When using the Reset bit to reset the Port 1 PHY, register bits designated as NASR are not reset.

Refer to Section 7.2.10, "PHY Resets," on page 95 for additional information on Port 1 PHY resets.

4.2.3.3 Virtual PHY Reset

A Virtual PHY reset is performed by setting the VPHY_RST bit of the Reset Control Register (RESET_CTL), VPHY_RST bit in the Power Management Control Register (PMT_CTRL), or Reset in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). No other modules of the LAN9312 are affected by this reset.

Virtual PHY reset completion can be determined by polling the VPHY_RST bit in the Reset Control Register (RESET_CTL), the VPHY_RST bit in the Power Management Control Register (PMT_CTRL), or the Reset bit in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) until it clears. Under normal conditions, the VPHY_RST and Reset bit will clear approximately 1uS after the Virtual PHY reset occurrence.

Refer to Section 7.3.2, "Virtual PHY Resets," on page 98 for additional information on Virtual PHY resets.

4.2.4 Configuration Straps

Configuration straps allow various features of the LAN9312 to be automatically configured to user defined values. Configuration straps can be organized into two main categories: hard-straps and soft-straps. Both hard-straps and soft-straps are latched upon Power-On Reset (POR) or pin reset (nRST). The primary difference between these strap types is that soft-strap default values can be overridden by the EEPROM Loader, while hard-straps cannot.

Configuration straps which have a corresponding external pin include internal resistors in order to prevent the signal from floating when unconnected. If a particular configuration strap is connected to a load, an external pull-up or pull-down resistor should be used to augment the internal resistor to ensure that it reaches the required voltage level prior to latching. The internal resistor can also be overridden by the addition of an external resistor.

Note: The system designer must guarantee that configuration strap pins meet the timing requirements specified in Section 15.5.2, "Reset and Configuration Strap Timing," on page 445. If configuration strap pins are not at the correct voltage level prior to being latched, the LAN9312 may capture incorrect strap values.

4.2.4.1 Soft-Straps

Soft-strap values are latched on the release of POR or nRST and are overridden by values from the EEPROM Loader (when an EEPROM is present). These straps are used as direct configuration values or as defaults for CPU registers. Some, but not all, soft-straps have an associated pin. Those that do not have an associated pin, have a tie off default value. All soft-strap values can be overridden by the EEPROM Loader. Table 4.2 provides a list of all soft-straps and their associated pin or default value. Straps which have an associated pin are also fully defined in Chapter 3, "Pin Description and Configuration," on page 26. Refer to Section 10.2.4, "EEPROM Loader," on page 149 for information on the operation of the EEPROM Loader and the loading of strap values.

Upon setting the DIGITAL_RST bit in the Reset Control Register (RESET_CTL) or upon issuing a RELOAD command via the EEPROM Command Register (E2P_CMD), these straps return to their original latched (non-overridden) values if an EEPROM is no longer attached or has been erased. The associated pins are not re-sampled. (i.e. The value latched on the pin during the last POR or nRST will be used, not the value on the pin during the digital reset or RELOAD command issuance). If it is desired to re-latch the current configuration strap pin values, a POR or nRST must be issued.

Table 4.2 Soft-Strap Configuration Strap Definitions

STRAP NAME	DESCRIPTION	PIN / DEFAULT VALUE
LED_en_strap[7:0]	**LED Enable Straps:** Configures the default value for the LED_EN bits in the LED Configuration Register (LED_CFG). A high value configures the associated LED/GPIO pin as a LED. A low value configures the associated LED/GPIO pin as a GPIO. **Note:** One pin configures the default for all 8 LED/GPIOs, but 8 separate bits are loaded by the EEPROM Loader, allowing individual control over each LED/GPIO.	LED_EN
LED_fun_strap[1:0]	**LED Function Straps:** Configures the default value for the LED_FUN bits in the LED Configuration Register (LED_CFG). When configured low, the corresponding bit will be cleared. When configured high, the corresponding bit will be set.	00b
auto_mdix_strap_1	**Port 1 Auto-MDIX Enable Strap:** Configures the default value for the Auto-MDIX functionality on Port 1 when the AMDIXCTL bit in the Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x) is cleared. When configured low, Auto-MDIX is disabled. When configured high, Auto-MDIX is enabled. **Note:** If AMDIXCTL is set, this strap had no effect.	AUTO_MDIX_1
manual_mdix_strap_1	**Port 1 Manual MDIX Strap:** Configures MDI(0) or MDIX(1) for Port 1 when the auto_mdix_strap_1 is low and the AMDIXCTL bit of the Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x) is cleared.	0b
autoneg_strap_1	**Port 1 Auto Negotiation Enable Strap:** Configures the default value for the Auto-Negotiation (PHY_AN) enable bit in the PHY_BASIC_CTRL_1 register (See Section 14.4.2.1). When configured low, auto-negotiation is disabled. When configured high, auto-negotiation is enabled. This strap also affects the default value of the following bits: ▪ PHY_SPEED_SEL_LSB and PHY_DUPLEX bits of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) ▪ 10BASE-T Full Duplex (bit 6) and 10BASE-T Half Duplex (bit 5) bits of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) ▪ MODE[2:0] bits of the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) Refer to the respective register definition sections for additional information.	1b

Table 4.2 Soft-Strap Configuration Strap Definitions (continued)

STRAP NAME	DESCRIPTION	PIN / DEFAULT VALUE
speed_strap_1	**Port 1 Speed Select Strap:** Configures the default value for the Speed Select LSB (PHY_SPEED_SEL_LSB) bit in the PHY_BASIC_CTRL_1 register (See Section 14.4.2.1). When configured low, 10 Mbps is selected. When configured high, 100 Mbps is selected. This strap also affects the default value of the following bits: ▪ PHY_SPEED_SEL_LSB bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) ▪ 10BASE-T Full Duplex (bit 6) and 10BASE-T Half Duplex (bit 5) bits of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) ▪ MODE[2:0] bits of the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) Refer to the respective register definition sections for additional information.	1b
duplex_strap_1	**Port 1 Duplex Select Strap:** Configures the default value for the Duplex Mode (PHY_DUPLEX) bit in the PHY_BASIC_CTRL_1 register (See Section 14.4.2.1). When configured low, half-duplex is selected. When configured high, full-duplex is selected. This strap also affects the default value of the following bits: ▪ PHY_DUPLEX bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) ▪ 10BASE-T Full Duplex (bit 6) of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) ▪ MODE[2:0] bits of the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) Refer to the respective register definition sections for additional information.	1b
BP_EN_strap_1	**Port 1 Backpressure Enable Strap:** Configures the default value for the Port 1 Backpressure Enable (BP_EN_1) bit of the Port 1 Manual Flow Control Register (MANUAL_FC_1). When configured low, backpressure is disabled. When configured high, backpressure is enabled.	1b
FD_FC_strap_1	**Port 1 Full-Duplex Flow Control Enable Strap:** Configures the default value of the Port 1 Full-Duplex Transmit Flow Control Enable (TX_FC_1) and Port 1 Full-Duplex Receive Flow Control Enable (RX_FC_1) bits in the Port 1 Manual Flow Control Register (MANUAL_FC_1), which are used when manual full-duplex control is selected. When configured low, full-duplex Pause packet detection and generation are disabled. When configured high, full-duplex Pause packet detection and generation are enabled.	1b

Table 4.2 Soft-Strap Configuration Strap Definitions (continued)

STRAP NAME	DESCRIPTION	PIN / DEFAULT VALUE
manual_FC_strap_1	**Port 1 Manual Flow Control Enable Strap:** Configures the default value of the Port 1 Full-Duplex Manual Flow Control Select (MANUAL_FC_1) bit in the Port 1 Manual Flow Control Register (MANUAL_FC_1). When configured low, flow control is determined by auto-negotiation (if enabled), and symmetric PAUSE is advertised (bit 10 of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) is set). When configured high, flow control is determined by the Port 1 Full-Duplex Transmit Flow Control Enable (TX_FC_1) and Port 1 Full-Duplex Receive Flow Control Enable (RX_FC_1) bits, and symmetric PAUSE is not advertised (bit 10 of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) is cleared).	0b
auto_mdix_strap_2	**Port 2 Auto-MDIX Enable Strap:** Configures the default value for the Auto-MDIX functionality on Port 2 when the AMDIXCTL bit in the Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x) is cleared. When configured low, Auto-MDIX is disabled. When configured high, Auto-MDIX is enabled. **Note:** If AMDIXCTL is set, this strap had no effect.	AUTO_MDIX_2
manual_mdix_strap_2	**Port 2 Manual MDIX Strap:** Configures MDI(0) or MDIX(1) for Port 2 when the auto_mdix_strap_2 is low and the AMDIXCTL bit of the Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x) is cleared.	0b
autoneg_strap_2	**Port 2 Auto Negotiation Enable Strap:** Configures the default value for the Auto-Negotiation (PHY_AN) enable bit in the PHY_BASIC_CTRL_2 register (See Section 14.4.2.1). When configured low, auto-negotiation is disabled. When configured high, auto-negotiation is enabled. This strap also affects the default value of the following bits: ▪ PHY_SPEED_SEL_LSB and PHY_DUPLEX bits of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) ▪ 10BASE-T Full Duplex (bit 6) and 10BASE-T Half Duplex (bit 5) bits of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) ▪ MODE[2:0] bits of the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) Refer to the respective register definition sections for additional information.	1b

Table 4.2 Soft-Strap Configuration Strap Definitions (continued)

STRAP NAME	DESCRIPTION	PIN / DEFAULT VALUE
speed_strap_2	**Port 2 Speed Select Strap:** Configures the default value for the Speed Select LSB (PHY_SPEED_SEL_LSB) bit in the PHY_BASIC_CTRL_2 register (See Section 14.4.2.1). When configured low, 10 Mbps is selected. When configured high, 100 Mbps is selected. This strap also affects the default value of the following bits: ▪ PHY_SPEED_SEL_LSB bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) ▪ 10BASE-T Full Duplex (bit 6) and 10BASE-T Half Duplex (bit 5) bits of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) ▪ MODE[2:0] bits of the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) Refer to the respective register definition sections for additional information.	1b
duplex_strap_2	**Port 2 Duplex Select Strap:** Configures the default value for the Duplex Mode (PHY_DUPLEX) bit in the PHY_BASIC_CTRL_2 register (See Section 14.4.2.1). When configured low, half-duplex is selected. When configured high, full-duplex is selected. This strap also affects the default value of the following bits: ▪ PHY_DUPLEX bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) ▪ 10BASE-T Full Duplex (bit 6) of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) ▪ MODE[2:0] bits of the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) Refer to the respective register definition sections for additional information.	1b
BP_EN_strap_2	**Port 2 Backpressure Enable Strap:** Configures the default value for the Port 2 Backpressure Enable (BP_EN_2) bit of the Port 2 Manual Flow Control Register (MANUAL_FC_2). When configured low, backpressure is disabled. When configured high, backpressure is enabled.	1b
FD_FC_strap_2	**Port 2 Full-Duplex Flow Control Enable Strap:** Configures the default value of the Port 2 Full-Duplex Transmit Flow Control Enable (TX_FC_2) and Port 2 Full-Duplex Receive Flow Control Enable (RX_FC_2) bits in the Port 2 Manual Flow Control Register (MANUAL_FC_2), which are used when manual full-duplex control is selected. When configured low, full-duplex Pause packet detection and generation are disabled. When configured high, full-duplex Pause packet detection and generation are enabled.	1b

Table 4.2 Soft-Strap Configuration Strap Definitions (continued)

STRAP NAME	DESCRIPTION	PIN / DEFAULT VALUE
manual_FC_strap_2	**Port 2 Manual Flow Control Enable Strap:** Configures the default value of the Port 2 Full-Duplex Manual Flow Control Select (MANUAL_FC_2) bit in the Port 2 Manual Flow Control Register (MANUAL_FC_2). When configured low, flow control is determined by auto-negotiation (if enabled), and symmetric PAUSE is advertised (bit 10 of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) is set). When configured high, flow control is determined by the Port 2 Full-Duplex Transmit Flow Control Enable (TX_FC_2) and Port 2 Full-Duplex Receive Flow Control Enable (RX_FC_2) bits, and symmetric PAUSE is not advertised (bit 10 of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) is cleared).	0b
BP_EN_strap_mii	**Port 0(Host MAC) Backpressure Enable Strap:** Configures the default value for the Port 0 Backpressure Enable (BP_EN_MII) bit of the Port 0(Host MAC) Manual Flow Control Register (MANUAL_FC_MII). When configured low, backpressure is disabled. When configured high, backpressure is enabled.	1b
FD_FC_strap_mii	**Port 0(Host MAC) Full-Duplex Flow Control Enable Strap**: Configures the default of the TX_FC_MII and RX_FC_MII bits in the Port 0(Host MAC) Manual Flow Control Register (MANUAL_FC_MII) which are used when manual full-duplex flow control is selected. When configured low, flow control is disabled on RX/TX. When configured high, flow control is enabled on RX/TX.	1b
manual_FC_strap_mii	**Port 0(Host MAC) Manual Flow Control Enable Strap:** Configures the default value of the MANUAL_FC_MII bit in the Port 0(Host MAC) Manual Flow Control Register (MANUAL_FC_MII). When configured low, flow control is determined by Virtual Auto-Negotiation (if enabled). When configured high, flow control is determined by TX_FC_MII and RX_FC_MII bits in the Port 0(Host MAC) Manual Flow Control Register (MANUAL_FC_MII).	0b
SQE_test_disable_strap_mii	**SQE Heartbeat Disable Strap:** Configures the Signal Quality Error (Heartbeat) test function by controlling the default value of the SQEOFF (bit 0) of the Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS). When configured low, SQEOFF defaults to 0 and SQE test is enabled. When configured high, SQEOFF defaults to 1 and SQE test is disabled.	0b

4.2.4.2 Hard-Straps

Hard-straps are latched upon Power-On Reset (POR) or pin reset (nRST) only. Unlike soft-straps, hard-straps always have an associated pin and cannot be overridden by the EEPROM Loader. These straps are used as either direct configuration values or as register defaults. Table 4.3 provides a list of all hard-straps and their associated pin. These straps, along with their pin assignments are also fully defined in Chapter 3, "Pin Description and Configuration," on page 26.

Table 4.3 Hard-Strap Configuration Strap Definitions

<table>
<tr><th>STRAP NAME</th><th>DESCRIPTION</th><th>PIN</th></tr>
<tr><td>eeprom_type_strap</td><td>EEPROM Type Strap: Configures the EEPROM type.

0 = Microwire Mode
1 = I²C Mode</td><td>EEPROM_TYPE</td></tr>
<tr><td>eeprom_size_strap[1:0]</td><td>EEPROM Size Strap [1:0]: Configures the EEPROM size range as specified in Section 10.2, "I2C/Microwire Master EEPROM Controller," on page 137.</td><td>EEPROM_SIZE_[1:0]</td></tr>
<tr><td>phy_addr_sel_strap</td><td>PHY Address Select Strap: Configures the default MII management address values for the PHYs and Virtual PHY as detailed in Section 7.1.1, "PHY Addressing," on page 82.

<table>
<tr><th>PHY_ADDR_SEL_STRAP VALUE</th><th>VIRTUAL PHY ADDRESS</th><th>PORT 1 PHY ADDRESS</th><th>PORT 2 PHY ADDRESS</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>1</td><td>2</td><td>3</td></tr>
</table>
</td><td>PHY_ADDR_SEL</td></tr>
</table>

4.3 Power Management

The LAN9312 Port 1 and Port 2 PHYs and the Host MAC support several power management and wakeup features.

The LAN9312 can be programmed to issue an external wake signal (PME) via several methods, including wake on LAN, wake on link status change (energy detect), and magic packet wakeup. The PME signal is ideal for triggering system power-up using remote Ethernet wakeup events. A simplified diagram of the logic that controls the PME and PME_INT signals can be seen in Figure 4.1.

The PME module handles the latching of the Port 1 & 2 PHY Energy-Detect Status (ED_STS1 and ED_STS2) and Wake-On LAN Status (WOL_STS) bits of the Power Management Control Register (PMT_CTRL). This module also masks the status bits with the corresponding enable bits (ED_EN1, ED_EN2, WOL_EN) and combines the results together to generate the PME_INT status bit in the Interrupt Status Register (INT_STS). The PME_INT status bit is then masked with the PME_EN bit and conditioned before becoming the PME output pin.

The PME output characteristics can be configured via the PME_TYPE, PME_IND, and PME_POL bits of the Power Management Control Register (PMT_CTRL). These bits allow the PME to be open-drain, active high push-pull, or active-low push-pull and configure the output to be continuous, or pulse for 50mS.

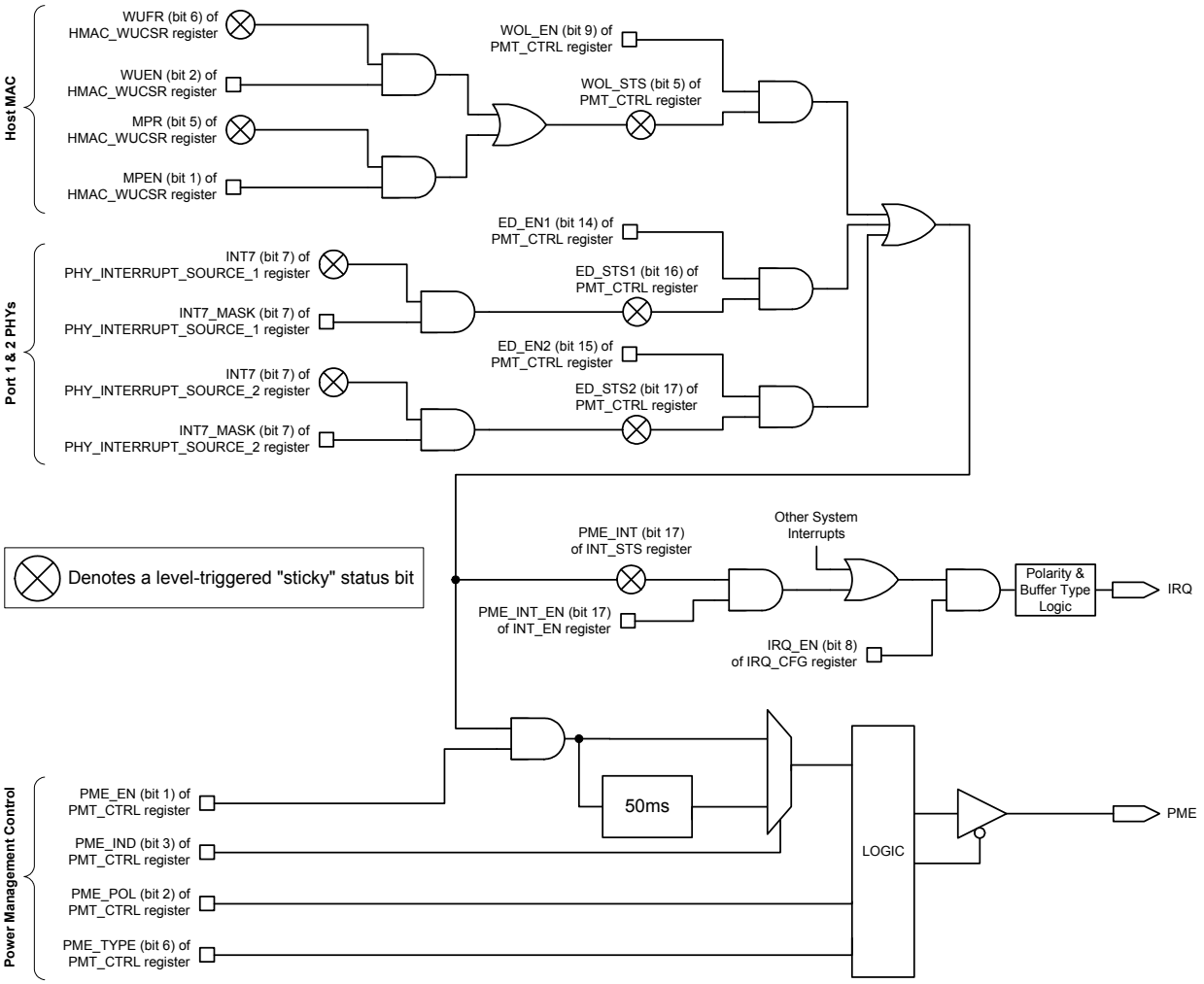


Figure 4.1 PME and PME_INT Signal Generation

4.3.1 Port 1 & 2 PHY Power Management

The Port 1 & 2 PHYs provide independent general power-down and energy-detect power-down modes which reduce PHY power consumption. General power-down mode provides power savings by powering down the entire PHY, except the PHY management control interface. General power-down mode must be manually enabled and disabled as described in Section 7.2.9.1, "PHY General Power-Down," on page 95.

In energy-detect power-down mode, the PHY will resume from power-down when energy is seen on the cable (typically from link pulses). If the ENERGYON interrupt (INT7) of either PHYs Port x PHY Interrupt Mask Register (PHY_INTERRUPT_MASK_x) is unmasked, then the corresponding PHY will generate an interrupt. These interrupts are reflected in the Interrupt Status Register (INT_STS) bit 27 (PHY_INT2) for the Port 2 PHY, and bit 26 (PHY_INT1) for the Port 1 PHY. These interrupts can be used to trigger the IRQ interrupt output pin, as described in Section 5.2.3, "Ethernet PHY Interrupts," on page 52. Refer to Section 7.2.9.2, "PHY Energy Detect Power-Down," on page 95 for details on the operation and configuration of the PHY energy-detect power-down mode.

The Port 1 & 2 PHY energy-detect events are capable of asserting the PME output by additionally setting the PME_EN and ED_EN2 (Port 2 PHY) or ED_EN1 (Port 1 PHY) bits of the Power Management Control Register (PMT_CTRL).

4.3.2 Host MAC Power Management

The Host MAC provides wake-up frame and magic packet detection modes. When enabled in the Host MAC Wake-up Control and Status Register (HMAC_WUCSR) (via the WUEN bit for wake-up frames, and the MPEN bit for magic packets), detection of wake-up frames or magic packets causes the WUFR and MPR bits of the HMAC_WUCSR register to set, respectively. If either of the WUFR and MPR bits are set, the WOL_STS bit of the Power Management Control Register (PMT_CTRL) will be set. These events can enable PME output assertion by additionally setting the PME_EN bit of the Power Management Control Register (PMT_CTRL).

The IRQ interrupt output can be triggered by a wake-up frame or magic packet as described in Section 5.2.6, "Power Management Interrupts," on page 53.

Refer to Section 9.5, "Wake-up Frame Detection," on page 116 and Section 9.5.1, "Magic Packet Detection," on page 118 for additional details on these features.

Chapter 5 System Interrupts

5.1 Functional Overview

This chapter describes the system interrupt structure of the LAN9312. The LAN9312 provides a multi-tier programmable interrupt structure which is controlled by the System Interrupt Controller. The programmable system interrupts are generated internally by the various LAN9312 sub-modules and can be configured to generate a single external host interrupt via the IRQ interrupt output pin. The programmable nature of the host interrupt provides the user with the ability to optimize performance dependent upon the application requirements. The IRQ interrupt buffer type, polarity, and de-assertion interval are modifiable. The IRQ interrupt can be configured as an open-drain output to facilitate the sharing of interrupts with other devices. All internal interrupts are maskable and capable of triggering the IRQ interrupt.

5.2 Interrupt Sources

The LAN9312 is capable of generating the following interrupt types:

- 1588 Time Stamp Interrupts (Port 2,1,0 and GPIO 9,8)
- Switch Fabric Interrupts (Buffer Manager, Switch Engine, and Port 2,1,0 MACs)
- Ethernet PHY Interrupts (Port 1,2 PHYs)
- GPIO Interrupts (GPIO[11:0])
- Host MAC Interrupts (FIFOs)
- Power Management Interrupts
- General Purpose Timer Interrupt (GPT)
- Software Interrupt (General Purpose)
- Device Ready Interrupt

All interrupts are accessed and configured via registers arranged into a multi-tier, branch-like structure, as shown in Figure 5.1. At the top level of the LAN9312 interrupt structure are the Interrupt Status Register (INT_STS), Interrupt Enable Register (INT_EN), and Interrupt Configuration Register (IRQ_CFG).

The Interrupt Status Register (INT_STS) and Interrupt Enable Register (INT_EN) aggregate and enable/disable all interrupts from the various LAN9312 sub-modules, combining them together to create the IRQ interrupt. These registers provide direct interrupt access/configuration to the Host MAC, General Purpose Timer, software, and device ready interrupts. These interrupts can be monitored, enabled/disabled, and cleared, directly within these two registers. In addition, interrupt event indications are provided for the 1588 Time Stamp, Switch Fabric, Port 1 & 2 Ethernet PHYs, Power Management, and GPIO interrupts. These interrupts differ in that the interrupt sources are generated and cleared in other sub-block registers. The INT_STS register does not provide details on what specific event within the sub-module caused the interrupt, and requires the software to poll an additional sub-module interrupt register (as shown in Figure 5.1) to determine the exact interrupt source and clear it. For interrupts which involve multiple registers, only after the interrupt has been serviced and cleared at its source will it be cleared in the INT_STS register.

The Interrupt Configuration Register (IRQ_CFG) is responsible for enabling/disabling the IRQ interrupt output pin as well as configuring its properties. The IRQ_CFG register allows the modification of the IRQ pin buffer type, polarity, and de-assertion interval. The de-assertion timer guarantees a minimum interrupt de-assertion period for the IRQ output and is programmable via the INT_DEAS field of the Interrupt Configuration Register (IRQ_CFG). A setting of all zeros disables the de-assertion timer. The de-assertion interval starts when the IRQ pin de-asserts, regardless of the reason.

Note: The de-assertion timer does not apply to the PME interrupt. Assertion of the PME interrupt does not affect the de-assertion timer.

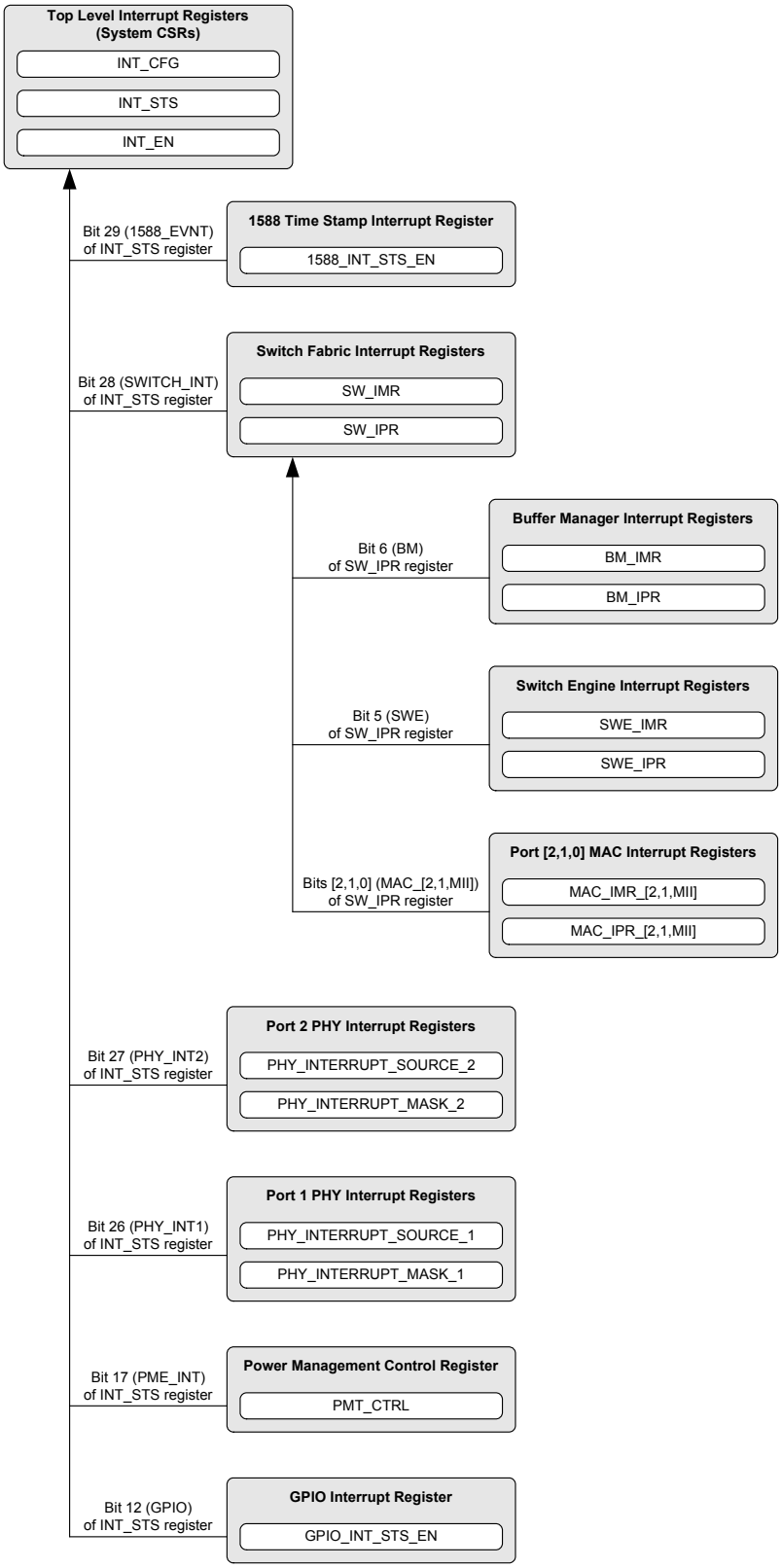


Figure 5.1 Functional Interrupt Register Hierarchy

The following sections detail each category of interrupts and their related registers. Refer to Chapter 14, "Register Descriptions," on page 166 for bit-level definitions of all interrupt registers.

5.2.1 1588 Time Stamp Interrupts

Multiple 1588 Time Stamp interrupt sources are provided by the LAN9312. The top-level 1588_EVNT (bit 29) of the Interrupt Status Register (INT_STS) provides indication that a 1588 interrupt event occurred in the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN).

The 1588 Interrupt Status and Enable Register (1588_INT_STS_EN) provides enabling/disabling and status of all 1588 interrupt conditions. These include TX/RX 1588 clock capture indication on Ports 2,1,0, 1588 clock capture for GPIO[8:9] events, as well as 1588 timer interrupt indication.

In order for a 1588 interrupt event to trigger the external IRQ interrupt pin, the desired 1588 interrupt event must be enabled in the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN), bit 29 (1588_EVNT_EN) of the Interrupt Enable Register (INT_EN) must be set, and IRQ output must be enabled via bit 8 (IRQ_EN) of the Interrupt Configuration Register (IRQ_CFG).

For additional details on the 1588 Time Stamp interrupts, refer to Section 11.6, "IEEE 1588 Interrupts," on page 160.

5.2.2 Switch Fabric Interrupts

Multiple Switch Fabric interrupt sources are provided by the LAN9312 in a three-tiered register structure as shown in Figure 5.1. The top-level SWITCH_INT (bit 28) of the Interrupt Status Register (INT_STS) provides indication that a Switch Fabric interrupt event occurred in the Switch Engine Interrupt Pending Register (SWE_IPR).

In turn, the Switch Engine Interrupt Pending Register (SWE_IPR) and Switch Engine Interrupt Mask Register (SWE_IMR) provide status and enabling/disabling of all Switch Fabric sub-modules interrupts (Buffer Manager, Switch Engine, and Port 2,1,0 MACs).

The low-level Switch Fabric sub-module interrupt pending and mask registers of the Buffer Manager, Switch Engine, and Port 2,1,0 MACs provide multiple interrupt sources from their respective sub-modules. These low-level registers provide the following interrupt sources:

- **Buffer Manager** (Buffer Manager Interrupt Mask Register (BM_IMR) and Buffer Manager Interrupt Pending Register (BM_IPR))
  —Status B Pending
  —Status A Pending
- **Switch Engine** (Switch Engine Interrupt Mask Register (SWE_IMR) and Switch Engine Interrupt Pending Register (SWE_IPR))
  —Interrupt Pending
- **Port 2,1,0 MACs** (Port x MAC Interrupt Mask Register (MAC_IMR_x) and Port x MAC Interrupt Pending Register (MAC_IPR_x))
  —No currently supported interrupt sources. These registers are reserved for future use.

In order for a Switch Fabric interrupt event to trigger the external IRQ interrupt pin, the following must be configured:

- The desired Switch Fabric sub-module interrupt event must be enabled in the corresponding mask register (Buffer Manager Interrupt Mask Register (BM_IMR) for the Buffer Manager, Switch Engine Interrupt Mask Register (SWE_IMR) for the Switch Engine, and/or Port x MAC Interrupt Mask Register (MAC_IMR_x) for the Port 2,1,0 MACs)
- The desired Switch Fabric sub-module interrupt event must be enabled in the Switch Engine Interrupt Mask Register (SWE_IMR)
- Bit 28 (SWITCH_INT_EN) of the Interrupt Enable Register (INT_EN) must be set
- IRQ output must be enabled via bit 8 (IRQ_EN) of the Interrupt Configuration Register (IRQ_CFG)

For additional details on the Switch Fabric interrupts, refer to Section 6.6, "Switch Fabric Interrupts," on page 81.

5.2.3 Ethernet PHY Interrupts

The Port 1 and Port 2 PHYs each provide a set of identical interrupt sources. The top-level PHY_INT1 (bit 26) and PHY_INT2 (bit 27) of the Interrupt Status Register (INT_STS) provides indication that a PHY interrupt event occurred in the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x).

Port 1 and Port 2 PHY interrupts are enabled/disabled via their respective Port x PHY Interrupt Mask Register (PHY_INTERRUPT_MASK_x). The source of a PHY interrupt can be determined and cleared via the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x). The Port 1 and Port 2 PHYs are each capable of generating unique interrupts based on the following events:

- ENERGYON Activated
- Auto-Negotiation Complete
- Remote Fault Detected
- Link Down (Link Status Negated)
- Auto-Negotiation LP Acknowledge
- Parallel Detection Fault
- Auto-Negotiation Page Received

In order for a Port 1 or Port 2 interrupt event to trigger the external IRQ interrupt pin, the desired PHY interrupt event must be enabled in the corresponding Port x PHY Interrupt Mask Register (PHY_INTERRUPT_MASK_x), the PHY_INT1(Port 1 PHY) and/or PHY_INT2(Port 2 PHY) bits of the Interrupt Enable Register (INT_EN) must be set, and IRQ output must be enabled via bit 8 (IRQ_EN) of the Interrupt Configuration Register (IRQ_CFG).

For additional details on the Ethernet PHY interrupts, refer to Section 7.2.8.1, "PHY Interrupts," on page 94.

5.2.4 GPIO Interrupts

Each GPIO[11:0] of the LAN9312 is provided with its own interrupt. The top-level GPIO (bit 12) of the Interrupt Status Register (INT_STS) provides indication that a GPIO interrupt event occurred in the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN). The General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN) provides enabling/disabling and status of each GPIO[11:0] interrupt.

In order for a GPIO interrupt event to trigger the external IRQ interrupt pin, the desired GPIO interrupt must be enabled in the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN), bit 12 (GPIO_EN) of the Interrupt Enable Register (INT_EN) must be set, and IRQ output must be enabled via bit 8 (IRQ_EN) of the Interrupt Configuration Register (IRQ_CFG).

For additional details on the GPIO interrupts, refer to Section 13.2.2, "GPIO Interrupts," on page 163.

5.2.5 Host MAC Interrupts

The top-level Interrupt Status Register (INT_STS), and Interrupt Enable Register (INT_EN) provide the status and enabling/disabling of multiple Host MAC related interrupts. All Host MAC interrupts are monitored and configured directly within these two registers. The following Host MAC related interrupt events are supported:

- TX Stopped
- RX Stopped
- RX Dropped Frame Counter Halfway

- TX IOC
- RX DMA
- TX Status FIFO Overflow
- Receive Watchdog Time-Out
- Receiver Error
- Transmitter Error
- TX Data FIFO Underrun
- TX Data FIFO Overrun
- TX Data FIFO Available
- TX Status FIFO Full
- TX Status FIFO Level
- RX Dropped Frame
- RX Data FIFO Level
- RX Status FIFO Full
- RX Status FIFO Level

In order for a Host MAC interrupt event to trigger the external IRQ interrupt pin, the desired Host MAC interrupt event must be enabled in the Interrupt Enable Register (INT_EN), and IRQ output must be enabled via bit 8 (IRQ_EN) of the Interrupt Configuration Register (IRQ_CFG).

Refer to the Interrupt Status Register (INT_STS) on page 174 and Chapter 9, "Host MAC," on page 112 for additional information on bit definitions and Host MAC operation.

5.2.6 Power Management Interrupts

Multiple Power Management Event interrupt sources are provided by the LAN9312. The top-level PME_INT (bit 17) of the Interrupt Status Register (INT_STS) provides indication that a Power Management interrupt event occurred in the Power Management Control Register (PMT_CTRL).

The Power Management Control Register (PMT_CTRL) provides enabling/disabling and status of all Power Management conditions. These include energy-detect on the Port 1/2 PHYs, and Wake-On-LAN (wake-up frame or magic packet) detection by the Host MAC.

In order for a Power Management interrupt event to trigger the external IRQ interrupt pin, the desired Power Management interrupt event must be enabled in the Power Management Control Register (PMT_CTRL) (bits 15, 14, and/or 9), bit 17 (PME_INT_EN) of the Interrupt Enable Register (INT_EN) must be set, and IRQ output must be enabled via bit 8 (IRQ_EN) of the Interrupt Configuration Register (IRQ_CFG).

For additional details on power management, refer to Section 4.3, "Power Management," on page 46.

5.2.7 General Purpose Timer Interrupt

A General Purpose Timer (GPT) interrupt is provided in the top-level Interrupt Status Register (INT_STS) and Interrupt Enable Register (INT_EN) (bit 19). This interrupt is issued when the General Purpose Timer Configuration Register (GPT_CFG) wraps past zero to FFFFh, and is cleared when bit 19 of the Interrupt Status Register (INT_STS) is written with 1.

In order for a General Purpose Timer interrupt event to trigger the external IRQ interrupt pin, the GPT must be enabled via the bit 29 (TIMER_EN) in the General Purpose Timer Configuration Register (GPT_CFG), bit 19 of the Interrupt Enable Register (INT_EN) must be set, and IRQ output must be enabled via bit 8 (IRQ_EN) of the Interrupt Configuration Register (IRQ_CFG).

For additional details on the General Purpose Timer, refer to Section 12.1, "General Purpose Timer," on page 161.

5.2.8 Software Interrupt

A general purpose software interrupt is provided in the top level Interrupt Status Register (INT_STS) and Interrupt Enable Register (INT_EN). The SW_INT interrupt (bit 31) of the Interrupt Status Register (INT_STS) is generated when SW_INT_EN (bit 31) of the Interrupt Enable Register (INT_EN) is set. This interrupt provides an easy way for software to generate an interrupt, and is designed for general software usage.

5.2.9 Device Ready Interrupt

A device ready interrupt is provided in the top-level Interrupt Status Register (INT_STS) and Interrupt Enable Register (INT_EN). The READY interrupt (bit 30) of the Interrupt Status Register (INT_STS) indicates that the LAN9312 is ready to be accessed after a power-up or reset condition. Writing a 1 to this bit in the Interrupt Status Register (INT_STS) will clear it.

In order for a device ready interrupt event to trigger the external IRQ interrupt pin, bit 30 of the Interrupt Enable Register (INT_EN) must be set, and IRQ output must be enabled via bit 8 (IRQ_EN) of the Interrupt Configuration Register (IRQ_CFG).

Chapter 6 Switch Fabric

6.1 Functional Overview

At the core of the LAN9312 is the high performance, high efficiency 3 port Ethernet switch fabric. The switch fabric contains a 3 port VLAN layer 2 switch engine that supports untagged, VLAN tagged, and priority tagged frames. The switch fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed, and a 1K entry forwarding table provides room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the buffer manager block within the switch fabric. All aspects of the switch fabric are managed via the switch fabric configuration and status registers (CSR), which are indirectly accessible via the memory mapped system control and status registers.

The switch fabric consists of four major block types:

- Switch Fabric CSRs - These registers provide access to various switch fabric parameters for configuration and monitoring.
- 10/100 Ethernet MACs - A total of three MACs are included in the switch fabric which provide basic 10/100 Ethernet functionality for each switch fabric port.
- Switch Engine (SWE) - This block is the core of the switch fabric and provides VLAN layer 2 switching for all three switch ports.
- Buffer Manager (BM) - This block provides control of the free buffer space, transmit queues, and scheduling.

Refer to Figure 2.1 Internal LAN9312 Block Diagram on page 21 for details on the interconnection of the switch fabric blocks within the LAN9312.

6.2 Switch Fabric CSRs

The switch fabric CSRs provide register level access to the various parameters of the switch fabric. Switch fabric related registers can be classified into two main categories based upon their method of access: direct and indirect.

The directly accessible switch fabric registers are part of the main system CSRs of the LAN9312 and are detailed in Section 14.2.6, "Switch Fabric," on page 229. These registers provide switch fabric manual flow control (Ports 0-2), data/command registers (for access to the indirect switch fabric registers), and switch MAC address configuration.

The indirectly accessible switch fabric registers reside within the switch fabric and must be accessed indirectly via the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) and Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD), or the set of Switch Fabric CSR Interface Direct Data Register (SWITCH_CSR_DIRECT_DATA). The indirectly accessible switch fabric CSRs provide full access to the many configurable parameters of the switch engine, buffer manager, and each switch port. The switch fabric CSRs are detailed in Section 14.5, "Switch Fabric Control and Status Registers," on page 308.

For detailed descriptions of all switch fabric related registers, refer to Chapter 14, "Register Descriptions," on page 166.

6.2.1 Switch Fabric CSR Writes

To perform a write to an individual switch fabric register, the desired data must first be written into the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA). The write cycle is initiated by performing a single write to the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) with CSR_BUSY (bit 31) set, the CSR_ADDRESS field (bits 15:0) set to the desired register address, the R_nW (bit 30) cleared, the AUTO_INC and AUTO_DEC fields cleared, and the desired CSR byte enable bits selected (bits 19:16). The completion of the write cycle is indicated by the clearing of the CSR_BUSY bit.

A second write method may be used which utilizes the auto increment/decrement function of the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) for writing sequential register addresses. When using this method, the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) must first be written with the auto increment(AUTO_INC) or auto decrement(AUTO_DEC) bit set, the CSR_ADDRESS field written with the desired register address, the R_nW bit cleared, and the desired CSR byte enable bits selected (typically all set). The write cycles are then initiated by writing the desired data into the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA). The completion of the write cycle is indicated by the clearing of the CSR_BUSY bit, at which time the address in the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) is incremented or decremented accordingly. The user may then initiate a subsequent write cycle by writing the desired data into the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA).

The third write method is to use the direct data range write function. Writes within the Switch Fabric CSR Interface Direct Data Register (SWITCH_CSR_DIRECT_DATA) address range automatically set the appropriate register address, set all four byte enable bits (CSR_BE[3:0]), clears the R_nW bit, and sets the CSR_BUSY bit of the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD). The completion of the write cycle is indicated by the clearing of the CSR_BUSY bit. Since the address range of the switch fabric CSRs exceeds that of the Switch Fabric CSR Interface Direct Data Register (SWITCH_CSR_DIRECT_DATA) address range, a sub-set of the switch fabric CSRs are mapped to the Switch Fabric CSR Interface Direct Data Register (SWITCH_CSR_DIRECT_DATA) address range as detailed in Table 14.3, “Switch Fabric CSR to SWITCH_CSR_DIRECT_DATA Address Range Map,” on page 240.

Figure 6.1 illustrates the process required to perform a switch fabric CSR write. The minimum wait periods as specified in Table 8.1, “Read After Write Timing Rules,” on page 102 are required where noted.

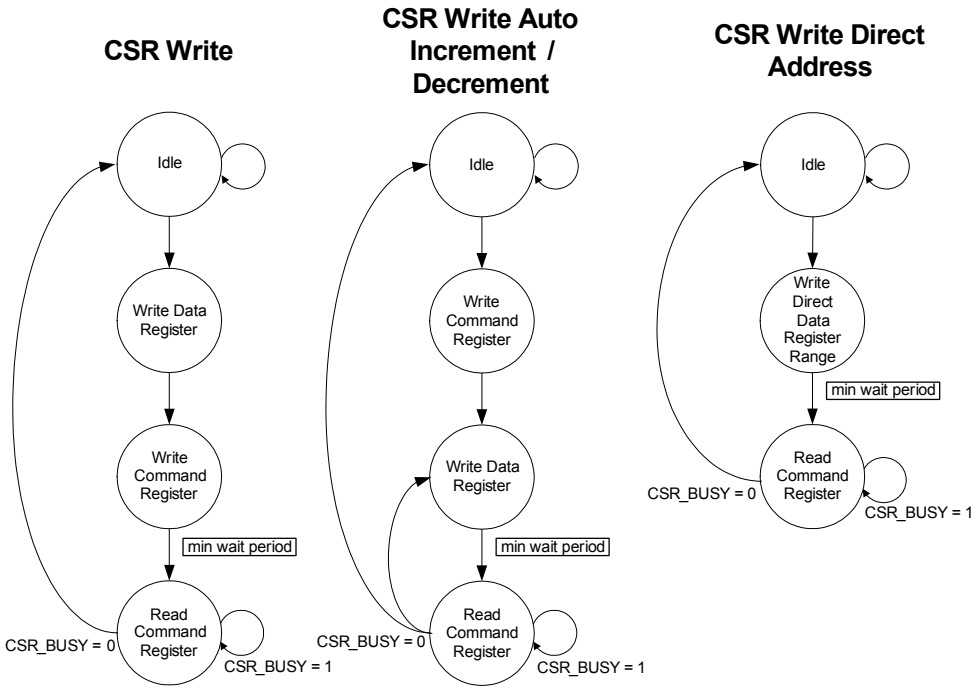


Figure 6.1 Switch Fabric CSR Write Access Flow Diagram

6.2.2 Switch Fabric CSR Reads

To perform a read of an individual switch fabric register, the read cycle must be initiated by performing a single write to the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) with CSR_BUSY (bit 31) set, the CSR_ADDRESS field (bits 15:0) set to the desired register address, the R_nW (bit 30) set, and the AUTO_INC and AUTO_DEC fields cleared. Valid data is available for reading when the CSR_BUSY bit is cleared, indicating that the data can be read from the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA).

A second read method may be used which utilizes the auto increment/decrement function of the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) for reading sequential register addresses. When using this method, the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) must first be written with the auto increment(AUTO_INC) or auto decrement(AUTO_DEC) bit set, the CSR_ADDRESS field written with the desired register address, and the R_nW bit set. The completion of a read cycle is indicated by the clearing of the CSR_BUSY bit, at which time the data can be read from the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA). When the data is read, the address in the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) is incremented or decremented accordingly, and another read cycle is started automatically. The user should clear the AUTO_INC and AUTO_DEC bits before reading the last data to avoid an unintended read cycle.

Figure 6.2 illustrates the process required to perform a switch fabric CSR read. The minimum wait periods as specified in Table 8.1, “Read After Write Timing Rules,” on page 102 are required where noted.

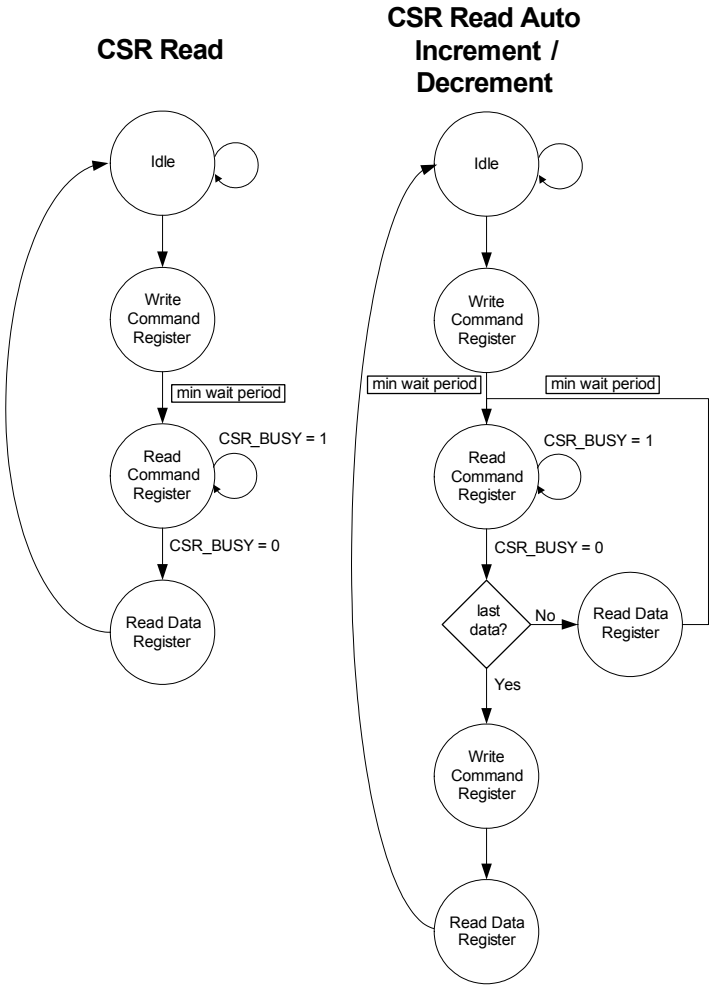


Figure 6.2 Switch Fabric CSR Read Access Flow Diagram

6.2.3 Flow Control Enable Logic

Each switch fabric port (0,1,2) is provided with two flow control enable inputs per port, one for transmission and one for reception. Flow control on transmission allows the transmitter to generate back pressure in half-duplex mode, and pause packets in full-duplex. Flow control in reception enables the reception of pause packets to pause transmissions.

The state of these enables is based on the state of the ports duplex and Auto-negotiation settings and the values of the corresponding Manual Flow Control register (Port 1 Manual Flow Control Register (MANUAL_FC_1), Port 2 Manual Flow Control Register (MANUAL_FC_2), or Port 0(Host MAC) Manual Flow Control Register (MANUAL_FC_MII)). Table 6.1 details the switch fabric flow control enable logic.

When in half-duplex mode, the transmit flow control (back pressure) enable is determined directly by the BP_EN_x bit of the ports manual flow control register. When Auto-negotiation is disabled, or the MANUAL_FC_x bit of the ports manual flow control register is set, the switch port flow control enables during full-duplex are determined by the TX_FC_x and RX_FC_x bits of the ports manual flow control

register. When Auto-negotiation is enabled and the MANUAL_FC_x bit is cleared, the switch port flow control enables during full-duplex are determined by Auto-negotiation.

Note: The flow control values in the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) and Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) are not affected by the values of the manual flow control register. Refer to Section 7.2.5.1, "PHY Pause Flow Control," on page 92 and Section 7.3.1.3, "Virtual PHY Pause Flow Control," on page 98 for additional information on PHY and Virtual PHY flow control settings respectively.

Table 6.1 Switch Fabric Flow Control Enable Logic

CASE	MANUAL_FC_X	AN ENABLE	AN COMPLETE	LP AN ABLE	DUPLEX	AN PAUSE ADVERTISEMENT (Note 6.2)	AN ASYM PAUSE ADVERTISEMENT (Note 6.2)	LP PAUSE ABILITY (Note 6.2)	LP ASYM PAUSE ABILITY (Note 6.2)	RX FLOW CONTROL ENABLE	TX FLOW CONTROL ENABLE
-	1	X	X	X	Half	X	X	X	X	0	BP_EN_x
-	X	0	X	X	Half	X	X	X	X	0	BP_EN_x
-	1	X	X	X	Full	X	X	X	X	RX_FC_x	TX_FC_x
-	X	0	X	X	Full	X	X	X	X	RX_FC_x	TX_FC_x
1	0	1	0	X	X	X	X	X	X	0	0
2	0	1	1	0	Half (Note 6.1)	X	X	X	X	0	BP_EN_x
3	0	1	1	1	Half	X	X	X	X	0	BP_EN_x
4	0	1	1	1	Full	0	0	X	X	0	0
5	0	1	1	1	Full	0	1	0	X	0	0
6	0	1	1	1	Full	0	1	1	0	0	0
7	0	1	1	1	Full	0	1	1	1	0	1
8	0	1	1	1	Full	1	0	0	X	0	0
9	0	1	1	1	Full	1	X	1	X	1	1
10	0	1	1	1	Full	1	1	0	0	0	0
11	0	1	1	1	Full	1	1	0	1	1	0

Note 6.1 If Auto-negotiation is enabled and complete, but the link partner is not Auto-negotiation capable, half-duplex is forced via the parallel detect function.

Note 6.2 For the Port 1 and Port 2 PHYs, these are the bits from the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) and Port x PHY Auto-Negotiation Link Partner Base Page Ability Register (PHY_AN_LP_BASE_ABILITY_x). For the Virtual PHY, these are the local/partner swapped outputs from the bits in the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) and Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY). Refer to Section 7.3.1, "Virtual PHY Auto-Negotiation," on page 96 for more information.

Per Table 6.1, the following cases are possible:

- **Case 1** - Auto-negotiation is still in progress. Since the result is not yet established, flow control is disabled.
- **Case 2** - Auto-negotiation is enabled and unsuccessful (link partner not Auto-negotiation capable). The link partner ability is undefined, effectively a don't-care value, in this case. The duplex setting will default to half-duplex in this case. Flow control is determined by the BP_EN_x bit.
- **Case 3** - Auto-negotiation is enabled and successful with half-duplex as a result. The link partner ability is undefined since it only applies to full-duplex operation. Flow control is determined by the BP_EN_x bit.
- **Cases 4-11** -Auto-negotiation is enabled and successful with full-duplex as the result. In these cases, the advertisement registers and the link partner ability controls the RX and TX enables. These cases match IEEE 802.3 Annex 28B.3.
  - **Cases 4,5,6,8,10** - No flow control enabled
  - **Case 7** - Asymmetric pause towards partner (away from switch port)
  - **Case 9** - Symmetric pause
  - **Case 11** - Asymmetric pause from partner (towards switch port)

6.3 10/100 Ethernet MACs

The switch fabric contains three 10/100 MAC blocks, one for each switch port (0,1,2). The 10/100 MAC provides the basic 10/100 Ethernet functionality, including transmission deferral and collision back-off/retry, receive/transmit FCS checking and generation, receive/transmit pause flow control, and transmit back pressure. The 10/100 MAC also includes RX and TX FIFOs and per port statistic counters.

6.3.1 Receive MAC

The receive MAC (IEEE 802.3) sublayer decomposes Ethernet packets acquired via the internal MII interface by stripping off the preamble sequence and Start of Frame Delimiter (SFD). The receive MAC checks the FCS, the MAC Control Type, and the byte count against the drop conditions. The packet is stored in the RX FIFO as it is received.

The receive MAC determines the validity of each received packet by checking the Type field, FCS, and oversize or undersize conditions. All bad packets will be either immediately dropped or marked (at the end) as bad packets.

Oversized packets are normally truncated at 1519 or 1523 (VLAN tagged) octets and marked as erroneous. The MAC can be configured to accept packets up to 2048 octets (inclusive), in which case the oversize packets are truncated at 2048 bytes and marked as erroneous.

Undersized packets are defined as packets with a length less than the minimum packet size. The minimum packet size is defined to be 64 bytes, exclusive of preamble sequence and SFD.

The FCS and length/type fields of the frame is checked to detect if the packet has a valid MAC control frame. When the MAC receives a MAC control frame with a valid FCS and determines the operation code is a pause command (Flow Control frame), the MAC will load its internal pause counter with the Number_of_Slots variable from the MAC control frame just received. Anytime the internal pause counter is zero, the transmit MAC will be allowed to transmit (XON). If the internal pause counter is not zero, the receive MAC will not allow the transmit MAC to transmit (XOFF). When the transmit MAC detects an XOFF condition it will continue to transmit the current packet, terminating transmission after the current packet has been transmitted until receiving the XON condition from the receive MAC. The pause counter will begin to decrement at then end of the current transmission, or immediately if no transmission is underway. If another pause command is received while the transmitter is already in pause, the new pause time indicated by the Flow Control packet will be loaded into the pause counter.

The pause function is enabled by either Auto-negotiation, or manually as discussed in Section 6.2.3, "Flow Control Enable Logic," on page 58. Pause frames are consumed by the MAC and not sent to the switch engine. Non-pause control frames are optionally filtered or forwarded.

When the receive FIFO is full and additional data continues to be received, an overrun condition occurs and the frame is discarded (FIFO space recovered) or marked as a bad frame.

The receive MAC can be disabled from receiving all frames by clearing the RX Enable bit of the Port x MAC Receive Configuration Register (MAC_RX_CFG_x).

The size of the RX FIFO is 256 bytes. If a bad packet with less than 64 bytes is received, it will be flushed from the FIFO automatically and the FIFO space recovered. Packets equal to or larger than 64 bytes with an error will be marked and reported to the switch engine. The switch engine will subsequently drop the packet.

6.3.1.1 Receive Counters

The receive MAC gathers statistics on each packet and increments the related counter registers. The following receive counters are supported for each switch fabric port. Refer to Table 14.12, “Indirectly Accessible Switch Control and Status Registers,” on page 308 and Section 14.5.2.3 through Section 14.5.2.22 for detailed descriptions of these counters.

- Total undersized packets (Section 14.5.2.3, on page 325)
- Total packets 64 bytes in size (Section 14.5.2.4, on page 326)
- Total packets 65 through 127 bytes in size (Section 14.5.2.5, on page 327)
- Total packets 128 through 255 bytes in size (Section 14.5.2.6, on page 328)
- Total packets 256 through 511 bytes in size (Section 14.5.2.7, on page 329)
- Total packets 512 through 1023 bytes in size (Section 14.5.2.8, on page 330)
- Total packets 1024 through maximum bytes in size (Section 14.5.2.9, on page 331)
- Total oversized packets (Section 14.5.2.10, on page 332)
- Total OK packets (Section 14.5.2.11, on page 333)
- Total packets with CRC errors (Section 14.5.2.12, on page 334)
- Total multicast packets (Section 14.5.2.13, on page 335)
- Total broadcast packets (Section 14.5.2.14, on page 336)
- Total MAC Pause packets (Section 14.5.2.15, on page 337)
- Total fragment packets (Section 14.5.2.16, on page 338)
- Total jabber packets (Section 14.5.2.17, on page 339)
- Total alignment errors (Section 14.5.2.18, on page 340)
- Total bytes received from all packets (Section 14.5.2.19, on page 341)
- Total bytes received from good packets (Section 14.5.2.20, on page 342)
- Total packets with a symbol error (Section 14.5.2.21, on page 343)
- Total MAC control packets (Section 14.5.2.22, on page 344)

6.3.2 Transmit MAC

The transmit MAC generates an Ethernet MAC frame from TX FIFO data. This includes generating the preamble and SFD, calculating and appending the frame checksum value, optionally padding undersize packets to meet the minimum packet requirement size (64 bytes), and maintaining a standard inter-frame gap time during transmit.

The transmit MAC can operate at 10/100Mbps, half- or full-duplex, and with or without flow control depending on the state of the transmission. In half-duplex mode the transmit MAC meets CSMA/CD IEEE 802.3 requirements. The transmit MAC will re-transmit if collisions occur during the first 64 bytes (normal collisions), or will discard the packet if collisions occur after the first 64 bytes (late collisions). The transmit MAC follows the standard truncated binary exponential back-off algorithm, collision and jamming procedures.

The transmit MAC pre-pends the standard preamble and SFD to every packet from the FIFO. The transmit MAC also follows as default, the standard Inter-Frame Gap (IFG). The default IFG is 96 bit times and can be adjusted via the IFG Config field of the Port x MAC Transmit Configuration Register (MAC_TX_CFG_x).

Packet padding and cyclic redundant code (FCS) calculation may be optionally performed by the transmit MAC. The auto-padding process automatically adds enough zeros to packets shorter than 64 bytes. The auto-padding and FCS generation is controlled via the TX Pad Enable bit of the Port x MAC Transmit Configuration Register (MAC_TX_CFG_x).

The transmit FIFO acts as a temporary buffer between the transmit MAC and the switch engine. The FIFO logic manages the re-transmission for normal collision conditions or discards the frames for late or excessive collisions.

When in full-duplex mode, the transmit MAC uses the flow-control algorithm specified in IEEE 802.3. MAC pause frames are used primarily for flow control packets, which pass signalling information between stations. MAC pause frames have a unique type of 8808h, and a pause op-code of 0001h. The MAC pause frame contains the pause value in the data field. The flow control manager will auto-adapt the procedure based on traffic volume and speed to avoid packet loss and unnecessary pause periods.

When in half-duplex mode, the MAC uses a back pressure algorithm. The back pressure algorithm is based on a forced collision and an aggressive back-off algorithm.

6.3.2.1 Transmit Counters

The transmit MAC gathers statistics on each packet and increments the related counter registers. The following transmit counters are supported for each switch fabric port. Refer to Table 14.12, “Indirectly Accessible Switch Control and Status Registers,” on page 308 and Section 14.5.2.25 through Section 14.5.2.42 for detailed descriptions of these counters.

- Total packets deferred (Section 14.5.2.25, on page 347)
- Total pause packets (Section 14.5.2.26, on page 348)
- Total OK packets (Section 14.5.2.27, on page 349)
- Total packets 64 bytes in size (Section 14.5.2.28, on page 350)
- Total packets 65 through 127 bytes in size (Section 14.5.2.29, on page 351)
- Total packets 128 through 255 bytes in size (Section 14.5.2.30, on page 352)
- Total packets 256 through 511 bytes in size (Section 14.5.2.31, on page 353)
- Total packets 512 through 1023 bytes in size (Section 14.5.2.32, on page 354)
- Total packets 1024 through maximum bytes in size (Section 14.5.2.33, on page 355)
- Total undersized packets (Section 14.5.2.34, on page 356)
- Total bytes transmitted from all packets (Section 14.5.2.35, on page 357)

- Total broadcast packets (Section 14.5.2.36, on page 358)
- Total multicast packets (Section 14.5.2.37, on page 359)
- Total packets with a late collision (Section 14.5.2.38, on page 360)
- Total packets with excessive collisions (Section 14.5.2.39, on page 361)
- Total packets with a single collision (Section 14.5.2.40, on page 362)
- Total packets with multiple collisions (Section 14.5.2.41, on page 363)
- Total collision count (Section 14.5.2.42, on page 364)

6.4 Switch Engine (SWE)

The switch engine (SWE) is a VLAN layer 2 (link layer) switching engine supporting 3 ports. The SWE supports the following types of frame formats: untagged frames, VLAN tagged frames, and priority tagged frames. The SWE supports both the 802.3 and Ethernet II frame formats.

The SWE provides the control for all forwarding/filtering rules. It handles the address learning and aging, and the destination port resolution based upon the MAC address and VLAN of the packet. The SWE implements the standard bridge port states for spanning tree and provides packet metering for input rate control. It also implements port mirroring, broadcast throttling, and multicast pruning and filtering. Packet priorities are supported based on the IPv4 TOS bits and IPv6 Traffic Class bits using a DIFFSERV Table mapping, the non-DIFFSERV mapped IPv4 precedence bits, VLAN priority using a per port Priority Regeneration Table, DA based static priority, and Traffic Class mapping to one of 4 QoS transmit priority queues.

The following sections detail the various features of the switch engine.

6.4.1 MAC Address Lookup Table

The Address Logic Resolution (ALR) maintains a 1024 entry MAC Address Table. The ALR searches the table for the destination MAC address. If the search finds a match, the associated data is returned indicating the destination port or ports, whether to filter the packet, the packets priority (used if enabled), and whether to override the ingress and egress spanning tree port state. Figure 6.3 displays the ALR table entry structure. Refer to the Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0) and Switch Engine ALR Write Data 1 Register (SWE_ALR_WR_DAT_1) for detailed descriptions of these bits.

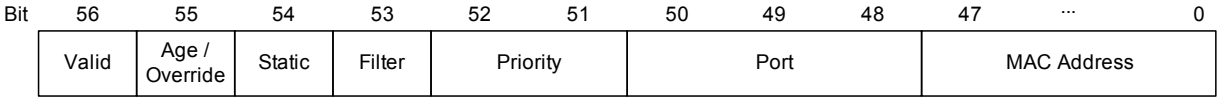


Figure 6.3 ALR Table Entry Structure

6.4.1.1 Learning/Aging/Migration

The ALR adds new MAC addresses upon ingress along with the associated receive port.

If the source MAC address already exists, the entry is refreshed. This action serves two purposes. First, if the source port has changed due to a network reconfiguration (migration), it is updated. Second, each instance the entry is refreshed, the aging status bit is set, keeping the entry active. Learning can be disabled per port via the Enable Learning on Ingress field of the Switch Engine Port Ingress Configuration Register (SWE_PORT_INGRSS_CFG).

During each aging period, the ALR scans the learned MAC addresses. For entries which have the aging status bit set, the ALR simply clears the bit. As mentioned above, if a MAC address is subsequently refreshed, the aging bit will be set again and the process would repeat. If a learned entry already had its aging status bit cleared (by a previous scan), the ALR will instead remove the learned entry. Therefore, if two scans occur before a MAC address is refreshed, the entry will be aged and removed. Each aging period is approximately 5 minutes. Therefore an entry will be aged and removed at a minimum of 5 minutes, and a maximum of 10 minutes.

6.4.1.2 Static Entries

If a MAC address entry is manually added by the host CPU, it can be (and typically is) marked as static. Static entries are not subjected to the aging process. Static entries also cannot be changed by the learning process (including migration).

6.4.1.3 Multicast Pruning

The destination port that is returned as a result of a destination MAC address lookup may be a single port or any combination of ports. The latter is used to setup multicast address groups. An entry with a multicast MAC address would be entered manually by the host CPU with the appropriate destination port(s). Typically, the Static bit should also be set to prevent automatic aging of the entry.

6.4.1.4 Address Filtering

Filtering can be performed on a destination MAC address. Such an entry would be entered manually by the host CPU with the Filter bit active. Typically, the Static bit should also be set to prevent automatic aging of the entry.

6.4.1.5 Spanning Tree Port State Override

A special spanning tree port state override setting can be applied to MAC address entries. When the host CPU manually adds an entry with both the Static and Age bits set, packets with a matching destination address will bypass the spanning tree port state and will be forwarded. This feature is typically used to allow the reception of the BPDU packets while a port is in the non-forwarding state. Refer to Section 6.4.5, "Spanning Tree Support," on page 70 for additional details.

6.4.1.6 MAC Destination Address Lookup Priority

If enabled in the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG), the transmit priority for static MAC address entries is taken from the associated data of that entry.

6.4.1.7 Host Access

The ALR contains a learning engine that is used by the host CPU to add, delete, and modify the MAC Address Table. This engine is accessed by using the Switch Engine ALR Command Register (SWE_ALR_CMD), Switch Engine ALR Command Status Register (SWE_ALR_CMD_STS), Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0), and Switch Engine ALR Write Data 1 Register (SWE_ALR_WR_DAT_1).

The following procedure should be followed in order to add, delete, and modify the ALR entries:

1. Write the Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0) and Switch Engine ALR Write Data 1 Register (SWE_ALR_WR_DAT_1) with the desired MAC address and control bits.

   Note: An entry can be deleted by setting the Valid and Static bits to 0.
2. Write the Switch Engine ALR Command Register (SWE_ALR_CMD) register with 0004h (Make Entry)
3. Poll the Make Pending bit in the Switch Engine ALR Command Status Register (SWE_ALR_CMD_STS) until it is cleared.
4. Write the Switch Engine ALR Command Register (SWE_ALR_CMD) with 0000h.

The ALR contains a search engine that is used by the host to read the MAC Address Table. This engine is accessed by using the Switch Engine ALR Command Register (SWE_ALR_CMD), Switch Engine ALR Read Data 0 Register (SWE_ALR_RD_DAT_0), and Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1).

Note: The entries read are not necessarily in the same order as they were learned or manually added.

The following procedure should be followed in order to read the ALR entries:

1. Write the Switch Engine ALR Command Register (SWE_ALR_CMD) with 0002h (Get First Entry).
2. Write the Switch Engine ALR Command Register (SWE_ALR_CMD) with 0000h (Clear the Get First Entry Bit)
3. Poll the Valid and End of Table bits in the Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1) until either are set.
4. If the Valid bit is set, then the entry is valid and the data from the Switch Engine ALR Read Data 0 Register (SWE_ALR_RD_DAT_0) and Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1) can be stored.
5. If the End of Table bit is set, then exit.
6. Write the Switch Engine ALR Command Register (SWE_ALR_CMD) with 0001h (Get Next Entry).
7. Write the Switch Engine ALR Command Register (SWE_ALR_CMD) with 0000h (Clear the Get Next Entry bit)
8. Go to step 3.

Note: Refer to Section 14.5.3.1, on page 367 through Section 14.5.3.6, on page 374 for detailed definitions of these registers.

6.4.2 Forwarding Rules

Upon ingress, packets are filtered or forwarded based on the following rules:

- If the destination port equals the source port (local traffic), the packet is filtered.
- If the source port is not in the forwarding state, the packet is filtered (unless the Spanning Tree Port State Override is in effect).
- If the destination port is not in the forwarding state, the packet is filtered (unless the Spanning Tree Port State Override is in effect).
- If the Filter bit for the Destination Address is set in the ALR table, the packet is filtered.
- If the packet has a unicast destination MAC address which is not found in the ALR table and the Drop Unknown bit is set, the packet is filtered.
- If the packet has a multicast destination MAC address which is not found in the ALR table and the Filter Multicast bit is set, the packet is filtered.
- If the packet has a broadcast destination MAC address and the Broadcast Storm Control level has been reached, the packet is discarded.
- If Drop on Yellow is set, the packet is colored Yellow, and randomly selected, it is discarded.
- If Drop on Red is set and the packet is colored Red, it is discarded.
- If the destination address was not found in the ALR table (an unknown or a broadcast) and the Broadcast Buffer Level is exceeded, the packet is discarded.
- If there is insufficient buffer space, the packet is discarded.

When the switch is enabled for VLAN support, these following rules also apply:

- If the packet is untagged or priority tagged and the Admit Only VLAN bit for the ingress port is set, the packet is filtered.
- If the packet is tagged and has a VID equal to FFFh, it is filtered.
- If Enable Membership Checking on Ingress is set, Admit Non Member is cleared, and the source port is not a member of the incoming VLAN, the packet is filtered.
- If Enable Membership Checking on Ingress is set and the destination port is not a member of the incoming VLAN, the packet is filtered.
- If the destination address was not found in the ALR table (as unknown or broadcast) and the VLAN broadcast domain containment resulted in zero valid destination ports, the packet is filtered.

Note: For the last three cases, if the VID is not in the VLAN table, the VLAN is considered foreign and the membership result is NULL. A NULL membership will result in the packet being filtered if Enable Membership Checking is set. A NULL membership will also result in the packet being filtered if the destination address is not found in the ALR table (since the packet would have no destinations).

6.4.3 Transmit Priority Queue Selection

The transmit priority queue may be selected from five options. As shown in Figure 6.4, the priority may be based on:

- the static value for the destination address in the ALR table
- the precedence bits in the IPv4 TOS octet
- the DIFFSERV mapping table indexed by the IPv4 TOS octet or the IPv6 Traffic Class octet
- the VLAN tag priority field using the per port Priority Regeneration table
- the port default

The last four options listed are sent through the Traffic Class table which maps the selected priority to one of the four output queues. The static value from the ALR table directly specifies the queue.

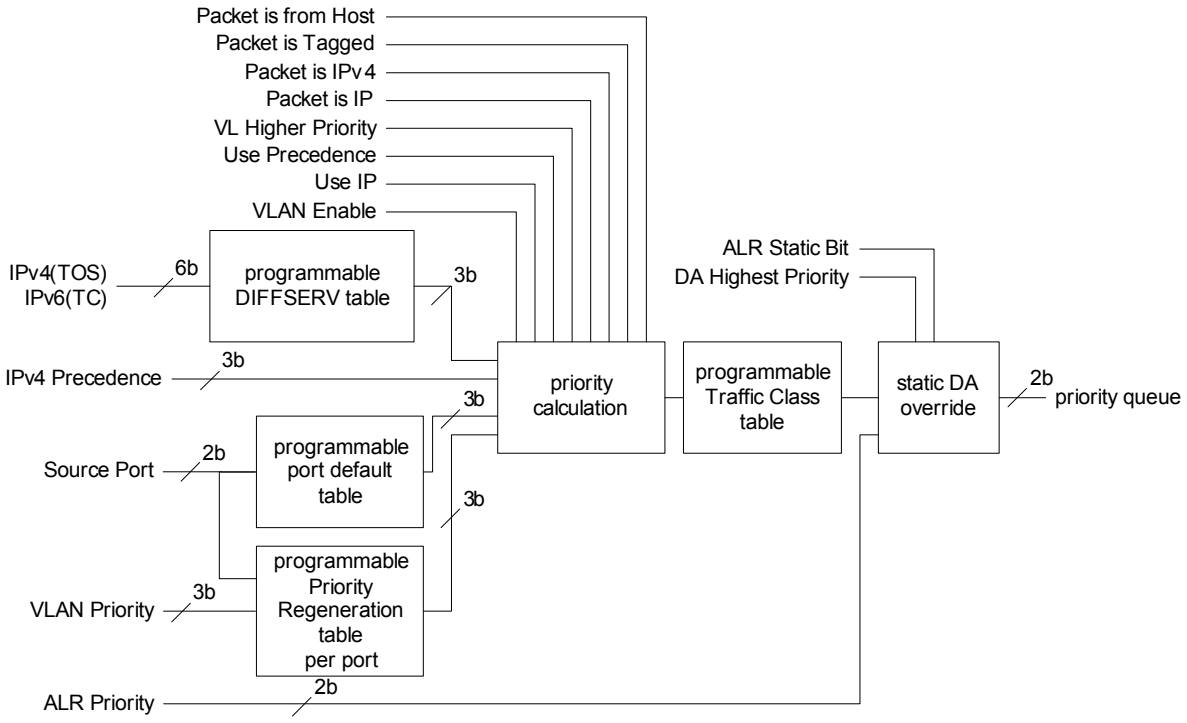


Figure 6.4 Switch Engine Transmit Queue Selection

The transmit queue priority is based on the packet type and device configuration as shown in Figure 6.5. Refer to Section 14.5.3.16, "Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG)," on page 384 for definitions of the configuration bits.

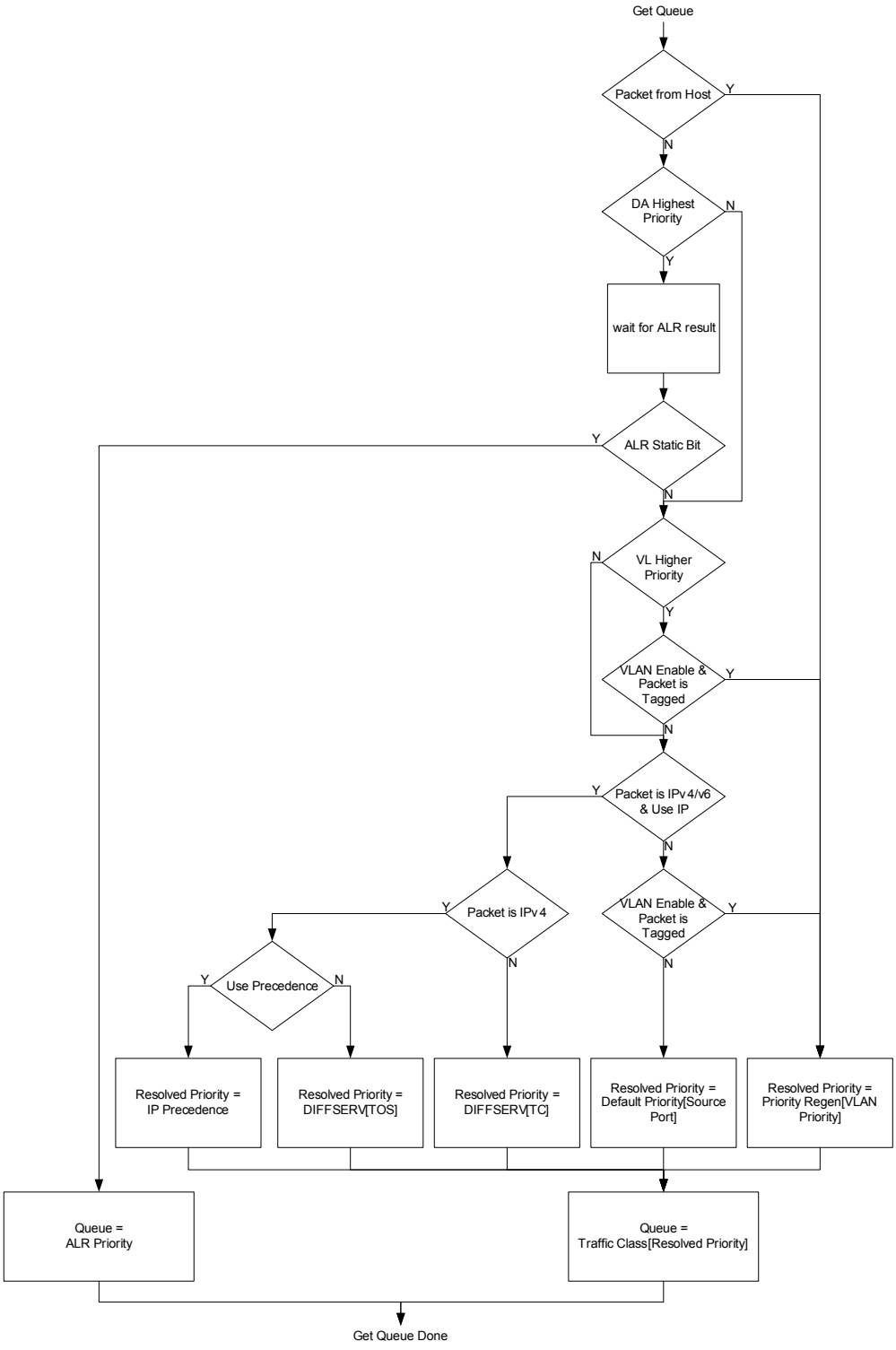


Figure 6.5 Switch Engine Transmit Queue Calculation

6.4.3.1 Port Default Priority

As detailed in Figure 6.5, the default priority is based on the ingress ports priority bits in its port VID value. The PVID table is read and written by using the Switch Engine VLAN Command Register (SWE_VLAN_CMD), Switch Engine VLAN Write Data Register (SWE_VLAN_WR_DATA), Switch Engine VLAN Read Data Register (SWE_VLAN_RD_DATA), and Switch Engine VLAN Command Status Register (SWE_VLAN_CMD_STS). Refer to Section 14.5.3.8, on page 376 through Section 14.5.3.11, on page 379 for detailed VLAN register descriptions.

6.4.3.2 IP Precedence Based Priority

The transmit priority queue can be chosen based on the Precedence bits of the IPv4 TOS octet. This is supported for tagged and non-tagged packets for both type field and length field encapsulations. The Precedence bits are the three most significant bits of the IPv4 TOS octet.

6.4.3.3 DIFFSERV Based Priority

The transmit priority queue can be chosen based on the DIFFSERV usage of the IPv4 TOS or IPv6 Traffic Class octet. This is supported for tagged and non-tagged packets for both type field and length field encapsulations.

The DIFFSERV table is used to determine the packet priority from the 6-bit Differentiated Services (DS) field. The DS field is defined as the six most significant bits of the IPv4 TOS octet or the IPv6 Traffic Class octet and is used as an index into the DIFFSERV table. The output of the DIFFSERV table is then used as the priority. This priority is then passed through the Traffic Class table to select the transmit priority queue.

Note: The DIFFSERV table is not initialized upon reset or power-up. If DIFFSERV is enabled, then the full table must be initialized by the host.

The DIFFSERV table is read and written by using the Switch Engine DIFFSERV Table Command Register (SWE_DIFFSERV_TBL_CFG), Switch Engine DIFFSERV Table Write Data Register (SWE_DIFFSERV_TBL_WR_DATA), Switch Engine DIFFSERV Table Read Data Register (SWE_DIFFSERV_TBL_RD_DATA), and Switch Engine DIFFSERV Table Command Status Register (SWE_DIFFSERV_TBL_CMD_STS). Refer to Section 14.5.3.12, on page 380 through Section 14.5.3.15, on page 383 for detailed DIFFSERV register descriptions.

6.4.3.4 VLAN Priority

As detailed in Figure 6.5, the transmit priority queue can be taken from the priority field of the VLAN tag. The VLAN priority is sent through a per port Priority Regeneration table, which is used to map the VLAN priority into a user defined priority.

The Priority Regeneration table is programmed by using the Switch Engine Port 0 Ingress VLAN Priority Regeneration Table Register (SWE_INGRSS_REGEN_TBL_MII), Switch Engine Port 1 Ingress VLAN Priority Regeneration Table Register (SWE_INGRSS_REGEN_TBL_1), and Switch Engine Port 2 Ingress VLAN Priority Regeneration Table Register (SWE_INGRSS_REGEN_TBL_2). Refer to Section 14.5.3.33, on page 403 through Section 14.5.3.35, on page 405 for detailed descriptions of these registers.

6.4.4 VLAN Support

The switch engine supports 16 active VLANs out of a possible 4096. The VLAN table contains the 16 active VLAN entries, each consisting of the VID, the port membership, and un-tagging instructions.

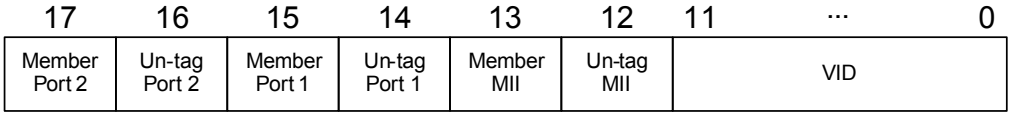


Figure 6.6 VLAN Table Entry Structure

On ingress, if a packet has a VLAN tag containing a valid VID (not 000h or FFFh), the VID table is searched. If the VID is found, the VLAN is considered active and the membership and un-tag instruction is used. If the VID is not found, the VLAN is considered foreign and the membership result is NULL. A NULL membership will result in the packet being filtered if Enable Membership Checking is set. A NULL membership will also result in the packet being filtered if the destination address is not found in the ALR table (since the packet would have no destinations).

On ingress, if a packet does not have a VLAN tag or if the VLAN tag contains VID with a value of 0 (priority tag), the packet is assigned a VLAN based on the Port Default VID (PVID) and Priority. The PVID is then used to access the above VLAN table.

The VLAN membership of the packet is used for ingress and egress checking and for VLAN broadcast domain containment. The un-tag instructions are used at egress on ports defined as hybrid ports.

Refer to Section 14.5.3.8, on page 376 through Section 14.5.3.11, on page 379 for detailed VLAN register descriptions.

6.4.5 Spanning Tree Support

Hardware support for the Spanning Tree Protocol (STP) and the Rapid Spanning Tree Protocol (RSTP) includes a per port state register as well as the override bit in the MAC Address Table entries (Section 6.4.1.5, on page 64) and the host CPU port special tagging (Section 6.4.10, on page 75).

The Switch Engine Port State Register (SWE_PORT_STATE) is used to place a port into one of the modes as shown in Table 6.2. Normally only Port 1 and Port 2 are placed into modes other than forwarding. Port 0 should normally be left in forwarding mode.

Table 6.2 Spanning Tree States

Port State	Hardware Action	Software Action
01 - Blocking (also used for disabled)	Received packets on the port are discarded. Transmissions to the port are blocked. Learning on the port is disabled.	The MAC Address Table should be programmed with entries that the host CPU needs to receive (e.g. the BPDU address). The static and override bits should be set. The host CPU should not send any packets to the port in this state. The host CPU should discard received packets from this port when in the Disabled state. **Note:** There is no hardware distinction between the Blocking and Disabled states.

Table 6.2 Spanning Tree States (continued)

Port State	Hardware Action	Software Action
11 - Listening	Received packets on the port are discarded. Transmissions to the port are blocked. Learning on the port is disabled.	The MAC Address Table should be programmed with entries that the host CPU needs to receive (e.g. the BPDU address). The static and override bits should be set. The host CPU may send packets to the port in this state.
10 - Learning	Received packets on the port are discarded. Transmissions to the port are blocked. Learning on the port is enabled.	The MAC Address Table should be programmed with entries that the host CPU needs to receive (e.g. the BPDU address). The static and override bits should be set. The host CPU may send packets to the port in this state.
00 - Forwarding	Received packets on the port are forwarded normally. Transmissions to the port are sent normally. Learning on the port is enabled.	The MAC Address Table should be programmed with entries that the host CPU needs to receive (e.g. the BPDU address). The static and override bits should be set. The host CPU may send packets to the port in this state.

6.4.6 Ingress Flow Metering and Coloring

The LAN9312 supports hardware ingress rate limiting by metering packet streams and marking packets as either Green, Yellow, or Red according to three traffic parameters: Committed Information Rate (CIR), Committed Burst Size (CBS), and Excess Burst Size (EBS). A packet is marked Green if it does not exceed the CBS, Yellow if it exceeds to CBS but not the EBS, or Red otherwise.

Ingress flow metering and coloring is enabled via the Ingress Rate Enable bit in the Switch Engine Ingress Rate Configuration Register (SWE_INGRSS_RATE_CFG). Once enabled, each incoming packet is classified into a stream. Streams are defined as per port (3 streams), per priority (8 streams), or per port & priority (24 streams) as selected via the Rate Mode bits in the Switch Engine Ingress Rate Configuration Register (SWE_INGRSS_RATE_CFG). Each stream can have a different CIR setting. All streams share common CBS and EBS settings. CIR, CBS, and EBS are programmed via the Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD) and Switch Engine Ingress Rate Write Data Register (SWE_INGRSS_RATE_WR_DATA).

Each stream is metered according to RFC 2697. At the rate set by the CIR, two token buckets are credited per stream. First, the Committed Burst bucket is incremented up to the maximum set by the CBS. Once the Committed Burst bucket is full, the Excess Burst bucket is incremented up to the maximum set by the EBS. The CIR rate is specified in time per byte. The value programmed is in approximately 20 nS per byte increments. Typical values are listed in Table 6.3. When a port is receiving at 10Mbps, any setting faster than 39 has the effect of not limiting the rate.

Table 6.3 Typical Ingress Rate Settings

CIR Setting	Time Per Byte	Bandwidth
0-3	80 nS	100 Mbps
4	100 nS	80 Mbps
5	120 nS	67 Mbps
6	140 nS	57 Mbps
7	160 nS	50 Mbps
9	200 nS	40 Mbps
12	260 nS	31 Mbps
19	400 nS	20 Mbps
39	800 nS	10 Mbps
79	1600 nS	5 Mbps
160	3220 nS	2.5 Mbps
402	8060 nS	1 Mbps
804	16100 nS	500 Kbps
1610	32220 nS	250 Kbps
4028	80580 nS	100 Kbps
8056	161140 nS	50 Kbps

After each packet is received, the bucket is decremented. If the Committed Burst bucket has sufficient tokens, it is debited and the packet is colored Green. If the Committed Burst bucket lacks sufficient tokens for the packet, the Excess Burst bucket is checked. If the Excess Burst bucket has sufficient tokens, it is debited, the packet is colored Yellow and is subjected to random discard. If the Excess Burst bucket lacks sufficient tokens for the packet, the packet is colored Red and is discarded.

Note: All of the token buckets are initialized to the default value of 1536. If lower values are programmed into the CBS and EBS parameters, the token buckets will need to be normally depleted below these values before the values have any affect on limiting the maximum value of the token buckets.

Refer to Section 14.5.3.25, on page 394 through Section 14.5.3.29, on page 399 for detailed register descriptions.

6.4.6.1 Ingress Flow Calculation

Based on the flow monitoring mode, an ingress flow definition can include the ingress priority. This is calculated similarly to the transmit queue with the exception that the Priority Regeneration and the Traffic Class table are not used. As shown in Figure 6.7, the priority can be based on:

- The precedence bits in the IPv4 TOS octet
- The DIFFSERV mapping table indexed by the IPv4 TOS octet or the IPv6 Traffic Class octet
- The VLAN tag priority field (but not through the per port Priority Regeneration table)
- The port default

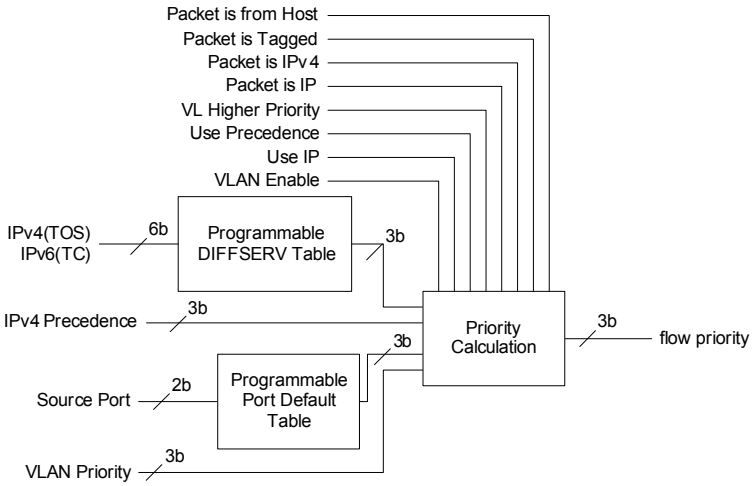


Figure 6.7 Switch Engine Ingress Flow Priority Selection

The ingress flow calculation is based on the packet type and the device configuration as shown in Figure 6.8.

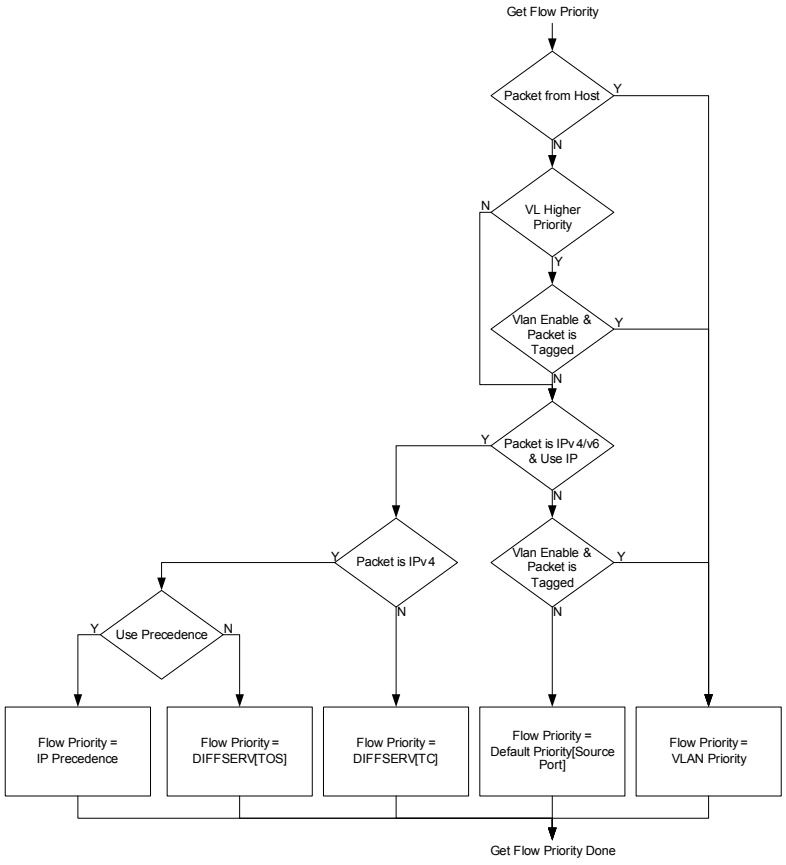


Figure 6.8 Switch Engine Ingress Flow Priority Calculation

6.4.7 Broadcast Storm Control

In addition to ingress rate limiting, the LAN9312 supports hardware broadcast storm control on a per port basis. This feature is enabled via the Switch Engine Broadcast Throttling Register (SWE_BCST_THROT). The allowed rate per port is specified as the number of bytes multiplied by 64 allowed to be received every 1.72 mS interval. Packets that exceed this limit are dropped. Typical values are listed in Table 6.4. When a port is receiving at 10Mbps, any setting above 34 has the effect of not limiting the rate.

Table 6.4 Typical Broadcast Rate Settings

Broadcast Throttle Level	Bandwidth
252	75 Mbps
168	50 Mbps
134	40 Mbps
67	20 Mbps
34	10 Mbps
17	5 Mbps
8	2.4 Mbps
4	1.2 Mbps
3	900 Kbps
2	600 Kbps
1	300 Kbps

In addition to the rate limit, the Buffer Manager Broadcast Buffer Level Register (BM_BCST_LVL) specifies the maximum number of buffers that can be used by broadcasts, multicasts, and unknown unicasts.

6.4.8 IPv4 IGMP Support

The LAN9312 provides Internet Group Management Protocol (IGMP) hardware support using two mechanisms: IGMP monitoring and Multicast Pruning.

On ingress, if IGMP packet monitoring is enabled in the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG), IGMP *multicast* packets are trapped and redirected to the IGMP monitoring port (typically set to the port to which the host CPU is connected). IGMP packets are identified as IPv4 packets with a protocol of 2. Both Ethernet and IEEE 802.3 frame formats are supported as are VLAN tagged packets.

Once the IGMP packets are received by the host CPU, the host software can decide which port or ports need to be members of the multicast group. This group is then added to the ALR table as detailed in Section 6.4.1.3, "Multicast Pruning," on page 64. The host software should also forward the original IGMP packet if necessary.

Normally, packets are never transmitted back to the receiving port. For IGMP monitoring, this may optionally be enabled via the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG). This function would be used if the monitoring port wished to participate in the IGMP group without the need to perform special handling in the transmit portion of the driver software.

Note: Most forwarding rules are skipped when a packet is monitored. However, a packet is still filtered if:

- The source port is not in the forwarding state (unless Spanning Tree Port State Override is in effect.
- VLAN's are enabled, the packet is untagged or priority tagged, and the Admit Only VLAN bit for the ingress port is set.
- VLAN's are enabled and the packet is tagged and had a VID equal to FFFh.
- VLAN's are enabled, Enabled Membership Checking on Ingress is set, Admit Non Member is cleared, and the source port is not a member of the incoming VLAN.

6.4.9 Port Mirroring

The LAN9312 supports port mirroring where packets received or transmitted on a port or ports can also be copied onto another "sniffer" port.

Port mirroring is configured using the Switch Engine Port Mirroring Register (SWE_PORT_MIRROR). Multiple mirrored ports can be defined, but only one sniffer port can be defined.

When receive mirroring is enabled, packets that are forwarded from a port designated as a mirrored port are also transmitted by the sniffer port. For example, Port 2 is setup to be a mirrored port and Port 0 is setup to be the sniffer port. If a packet is received on Port 2 with a destination of Port 1, it is forwarded to both Port 1 and Port 0.

When transmit mirroring is enabled, packets that are forwarded to a port designated as a mirrored port are also transmitted by the sniffer port. For example, Port 2 is setup to be a mirrored port and Port 0 is setup to be the sniffer port. If a packet is received on Port 1 with a destination of Port 2, it is forwarded to both Port 2 and Port 0.

Note: A packet will never be transmitted out of the receiving port. A receive packet is not normally mirrored if it is filtered. This can optionally be enabled.

6.4.10 Host CPU Port Special Tagging

The Switch Engine Ingress Port Type Register (SWE_INGRSS_PORT_TYP) and Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE) are used to enable a special VLAN tag that is used by the host CPU. This special tag is used to specify the port(s) where packets from the CPU should be sent, and to indicate which port received the packet that was forwarded to the CPU.

6.4.10.1 Packets from the Host CPU

The Switch Engine Ingress Port Type Register (SWE_INGRSS_PORT_TYP) configures the switch to use the special VLAN tag in packets from the host CPU as a destination port indicator. A setting of 11b should be used on the port that is connected to the host CPU (typically Port 0). A setting of 00b should be used on the normal network ports.

The special VLAN tag is a normal VLAN tag where the VID field is used as the destination port indicator. If VID bit 3 is zero, then bits 0 and 1 specify the destination port (0, 1, 2) or broadcast (3). If VID bit 3 is one, then the normal ALR lookup is performed and learning is performed on the source address. The PRI field from the VLAN tag is used as the packet priority.

Upon egress from the destination port(s), the special tag is removed. If a regular VLAN tag needs to be sent as part of the packet, then it should be part of the packet data from the host CPU port or set as an unused bit in the VID field.

Note: When specifying Port 0 as the destination port, the VID will be set to 0. A VID of 0 is normally considered a priority tagged packet. Such a packet will be filtered if Admit Only VLAN is set on the host CPU port. Either avoid setting Admit Only VLAN on the host CPU port or set an unused bit in the VID field.

Note: The maximum size tagged packet that can normally be sent into a switch port (from the Host MAC) is 1522 bytes. Since the special tag consumes four bytes of the packet length, the outgoing packet is limited to 1518 bytes, even if it contains a regular VLAN tag as part of the packet data. If a larger outgoing packet is required, the Jumbo2K bit in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x) of Port 0 should be set.

6.4.10.2 Packets to the Host CPU

The Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE) configures the switch to add the special VLAN tag in packets to the host CPU as a source port indicator. A setting of 11b should be used only on the port that is connected to the host CPU (typically Port 0). Other settings can be used on the normal network ports as needed.

The special VLAN tag is a normal VLAN tag where bits 0 and 1 of the VID field specify the source port (0, 1, or 2).

Upon egress from the host CPU port, the special tag is added. If a regular VLAN tag already exists, it is not deleted. Instead it will follow the special tag.

Note: Since the special tag adds four bytes to the length of the packet, it is possible for a normally tagged, maximum size, incoming packet to become 1526 bytes in length. In order for the Host MAC to receive this length packet without indicating a length error, the Host MAC VLAN2 Tag Register (HMAC_VLAN2) in the Host MAC should be set to 8100h and the Host MAC VLAN1 Tag Register (HMAC_VLAN1) should be set to a value other than 8100h. This configuration will allow frames up to 1538 bytes in length to be received.

Note: Since the special tag adds four bytes to the length of the packet, it is possible for a normally tagged, maximum size, incoming jumbo packet to become 2052 bytes in length. This packet will be received by the Host MAC with the following conditions:

- The receive status will indicate Frame Too Long
- Up to four bytes of the end of packet may be truncated (the maximum receive length at the Host MAC is 2048).

6.4.11 Counters

A counter is maintained per port that contains the number of MAC address that were not learned or were overwritten by a different address due to MAC Address Table space limitations. These counters are accessible via the following registers:

- Switch Engine Port 0 Learn Discard Count Register (SWE_LRN_DISCRD_CNT_MII)
- Switch Engine Port 1 Learn Discard Count Register (SWE_LRN_DISCRD_CNT_1)
- Switch Engine Port 2 Learn Discard Count Register (SWE_LRN_DISCRD_CNT_2)

A counter is maintained per port that contains the number of packets filtered at ingress. This count includes packets filtered due to broadcast throttling, but does not include packets dropped due to ingress rate limiting. These counters are accessible via the following registers:

- Switch Engine Port 0 Ingress Filtered Count Register (SWE_FILTERED_CNT_MII)
- Switch Engine Port 1 Ingress Filtered Count Register (SWE_FILTERED_CNT_1)
- Switch Engine Port 2 Ingress Filtered Count Register (SWE_FILTERED_CNT_2)

6.5 Buffer Manager (BM)

The buffer manager (BM) provides control of the free buffer space, the multiple priority transmit queues, transmission scheduling, and packet dropping. VLAN tag insertion and removal is also performed by the buffer manager. The following sections detail the various features of the buffer manager.

6.5.1 Packet Buffer Allocation

The packet buffer consists of 32KB of RAM that is dynamically allocated in 128 byte blocks as packets are received. Up to 16 blocks may be used per packet, depending on the packet length. The blocks are linked together as the packet is received. If a packet is filtered, dropped, or contains a receive error, the buffers are reclaimed.

6.5.1.1 Buffer Limits and Flow Control Levels

The BM keeps track of the amount of buffers used per each ingress port. These counts are used to generate flow control (half-duplex backpressure or full-duplex pause frames) and to limit the amount of buffer space that can be used by any individual receiver (hard drop limit). The flow control and drop limit thresholds are dynamic and adapt based on the current buffer usage. Based on the number of active receiving ports, the drop level and flow control pause and resume thresholds adjust between fixed settings and two user programmable levels via the Buffer Manager Drop Level Register (BM_DROP_LVL), Buffer Manager Flow Control Pause Level Register (BM_FC_PAUSE_LVL), and Buffer Manager Flow Control Resume Level Register (BM_FC_RESUME_LVL) respectively.

The BM also keeps a count of the number of buffers that are queued for multiple ports (broadcast queue). This count is compared against the Buffer Manager Broadcast Buffer Level Register (BM_BCST_LVL), and if the configured drop level is reached or exceeded, subsequent packets are dropped.

6.5.2 Random Early Discard (RED)

Based on the ingress flow monitoring detailed in Section 6.4.6, "Ingress Flow Metering and Coloring," on page 71, packets are colored as Green, Yellow, or Red. Packets colored Red are always discarded if the Drop on Red bit in the Buffer Manager Configuration Register (BM_CFG) is set. If the Drop on Yellow bit in the Buffer Manager Configuration Register (BM_CFG) is set, packets colored Yellow are randomly discarded based on the moving average number of buffers used by the ingress port.

The probability of a discard is programmable into the Random Discard Weight table via the Buffer Manager Random Discard Table Command Register (BM_RNDM_DSCRD_TBL_CMD), Buffer Manager Random Discard Table Write Data Register (BM_RNDM_DSCRD_TBL_WDATA), and Buffer Manager Random Discard Table Read Data Register (BM_RNDM_DSCRD_TBL_RDATA). The Random Discard Weight table contains sixteen entries, each 10-bits wide. Each entry corresponds to a range of the average number of buffers used by the ingress port. Entry 0 is for 0 to 15 buffers, entry 1 is for 16 to 31 buffers, etc. The probability for each entry us set in 1/1024's. For example, a setting of 1 is 1-in-1024, or approximately 0.1%. A setting of all ones (1023) is 1023-in-1024, or approximately 99.9%.

Refer to Section 14.5.4.10, "Buffer Manager Random Discard Table Command Register (BM_RNDM_DSCRD_TBL_CMD)," on page 421 for additional details on writing and reading the Random Discard Weight table.

6.5.3 Transmit Queues

Once a packet has been completely received, it is queued for transmit. There are four queues per transmit port, one for each level of transmit priority. Each queue is virtual (if there are no packets for that port/priority, the queue is empty), and dynamic (a queue may be any length if there is enough memory space). When a packet is read from the memory and sent out to the corresponding port, the used buffers are released.

6.5.4 Transmit Priority Queue Servicing

When a transmit queue is non-empty, it is serviced and the packet is read from the buffer RAM and sent to the transmit MAC. If there are multiple queues that require servicing, one of two methods may be used: fixed priority ordering, or weighted round-robin ordering. If the Fixed Priority Queue Servicing bit in the Buffer Manager Configuration Register (BM_CFG) is set, a strict order, fixed priority is selected. Transmit queue 3 has the highest priority, followed by 2, 1, and 0. If the Fixed Priority Queue Servicing bit in the Buffer Manager Configuration Register (BM_CFG) is cleared, a weighted round-robin order is followed. Assuming all four queues are non-empty, the service is weighted with a 9:4:2:1 ratio (queue 3,2,1,0). The servicing is blended to avoid burstiness (e.g. queue 3, then queue 2, then queue 3, etc.).

6.5.5 Egress Rate Limiting (Leaky Bucket)

For egress rate limiting, the leaky bucket algorithm is used on each output priority queue. For each output port, the bandwidth that is used by each priority queue can be limited. If any egress queue receives packets faster than the specified egress rate, packets will be accumulated in the packet memory. After the memory is used, packet dropping or flow control will be triggered.

Note: Egress rate limiting occurs before the Transmit Priority Queue Servicing, such that a lower priority queue will be serviced if a higher priority queue is being rate limited.

The egress limiting is enabled per priority queue. After a packet is selected to be sent, its length is recorded. The switch then waits a programmable amount of time, scaled by the packet length, before servicing that queue once again. The amount of time per byte is programmed into the Buffer Manager Egress Rate registers (refer to Section 14.5.4.14 through Section 14.5.4.19 for detailed register definitions). The value programmed is in approximately 20 nS per byte increments. Typical values are listed in Table 6.5. When a port is transmitting at 10 Mbps, any setting above 39 has the effect of not limiting the rate.

Table 6.5 Typical Egress Rate Settings

EGRESS RATE SETTING	TIME PER BYTE	BANDWIDTH @ 64 BYTE PACKET	BANDWIDTH @ 512 BYTE PACKET	BANDWIDTH @ 1518 BYTE PACKET
0-3	80 nS	76 Mbps (Note 6.3)	96 Mbps (Note 6.3)	99 Mbps (Note 6.3)
4	100 nS	66 Mbps	78 Mbps	80 Mbps
5	120 nS	55 Mbps	65 Mbps	67 Mbps
6	140 nS	48 Mbps	56 Mbps	57 Mbps
7	160 nS	42 Mbps	49 Mbps	50 Mbps
9	200 nS	34 Mbps	39 Mbps	40 Mbps
12	260 nS	26 Mbps	30 Mbps	31 Mbps
19	400 nS	17 Mbps	20 Mbps	20 Mbps
39	800 nS	8.6 Mbps	10 Mbps	10 Mbps
78	1580 nS	4.4 Mbps	5 Mbps	5 Mbps
158	3180 nS	2.2 Mbps	2.5 Mbps	2.5 Mbps
396	7940 nS	870 Kbps	990 Kbps	1 Mbps
794	15900 nS	440 Kbps	490 Kbps	500 Kbps
1589	31800 nS	220 Kbps	250 Kbps	250 Kbps
3973	79480 nS	87 Kbps	98 Kbps	100 Kbps
7947	158960 nS	44 Kbps	49 Kbps	50 Kbps

Note 6.3 These are the unlimited max bandwidths when IFG and preamble are taken into account.

6.5.6 Adding, Removing, and Changing VLAN Tags

Based on the port configuration and the received packet formation, a VLAN tag can be added to, removed from, or modified in a packet. There are four received packet type cases: non-tagged, priority-tagged, normal-tagged, and CPU special-tagged. There are also four possible settings for an egress port: dumb, access, hybrid, and CPU. In addition, each VLAN table entry can specify the removal of the VLAN tag (the entry's un-tag bit).

The tagging/un-tagging rules are specified as follows:

- **Dumb Port** - This port type generally does not change the tag.
  When a received packet is non-tagged, priority-tagged, or normal-tagged, the packet passes untouched.
  When a packet is received special-tagged from a CPU port, the special tag is removed.
- **Access Port** - This port type generally does not support tagging.
  When a received packet in non-tagged, the packet passes untouched.
  When a received packet is priority-tagged or normal-tagged, the tag is removed.
  When a received packet is special-tagged from a CPU port, the special tag is removed.
- **CPU Port** - Packets transmitted from this port type generally contain a special tag. Special tags are described in detail in Section 6.4.10, "Host CPU Port Special Tagging," on page 75.
- **Hybrid Port** - Generally, this port type supports a mix of normal-tagged and non-tagged packets. It is the most complex, but most flexible port type.

For clarity, the following details the incoming un-tag instruction. As described in Section 6.4.4, "VLAN Support," on page 70, the un-tag instruction is one of three un-tag bits from the applicable entry in the VLAN table, selected by the ingress port number. The entry in the VLAN table is either the VLAN from the received packet or the ingress ports default VID.

- When a received packet is non-tagged, a new VLAN tag is added if two conditions are met. First, the Insert Tag bit for the egress port in the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE) must be set. Second, the un-tag instruction associated with the ingress ports default VID must be cleared. The VLAN tag that is added will have a VID and Priority taken from the *ingress* ports default VID and priority.
- When a received packet is priority-tagged, either the tag is removed or it is modified.
  If the un-tag instruction associated with the ingress ports default VID is set, then the tag is removed.
  Otherwise, the tag is modified. The VID of the new VLAN tag is changed to the *ingress* ports default VID. If the Change Priority bit in the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE) for the egress port is set, then the Priority field of the new VLAN tag is also changed to the *ingress* ports default priority.
- When a received packet is normal-tagged, either the tag is removed, modified, or passed.
  If the un-tag instruction associated with the VID in the received packet is set, then the tag is removed.
  Else, if the Change Tag bit in the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE) for the egress port is clear, the packet is untouched.
  Else, if both the Change VLAN ID and the Change Priority bits in the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE) for the egress port are clear, the packet passes untouched.
  Otherwise, the tag is modified. If the Change VLAN ID bit for the egress port is set, the VOD of the new VLAN tag is changed to the *egress* ports default ID. If the Change Priority bit for the egress port is set, the Priority field of the new VLAN is changed to the *egress* ports default priority.
- When a packet is received special-tagged from a CPU port, the special tag is removed.

Hybrid tagging is summarized in Figure 6.9.

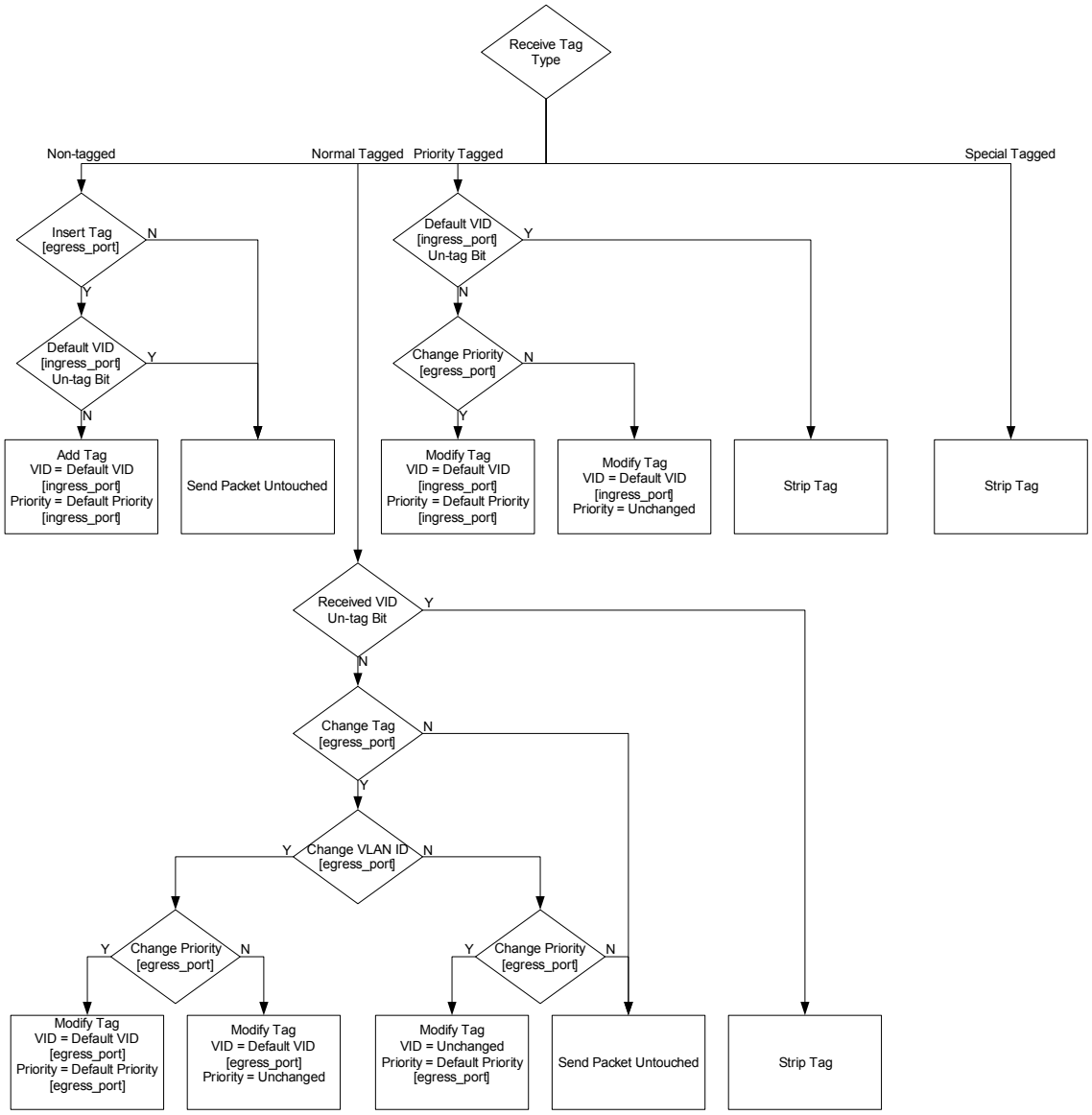


Figure 6.9 Hybrid Port Tagging and Un-tagging

The default VLAN ID and priority of each port may be configured via the following registers:

- Buffer Manager Port 0 Default VLAN ID and Priority Register (BM_VLAN_MII)
- Buffer Manager Port 1 Default VLAN ID and Priority Register (BM_VLAN_1)
- Buffer Manager Port 2 Default VLAN ID and Priority Register (BM_VLAN_2)

6.5.7 Counters

A counter is maintained per port that contains the number of packets dropped due to buffer space limits and ingress rate limit discarding (Red and random Yellow dropping). These counters are accessible via the following registers:

- Buffer Manager Port 0 Drop Count Register (BM_DRP_CNT_SRC_MII)
- Buffer Manager Port 1 Drop Count Register (BM_DRP_CNT_SRC_1)
- Buffer Manager Port 2 Drop Count Register (BM_DRP_CNT_SRC_2)

A counter is maintained per port that contains the number of packets dropped due solely to ingress rate limit discarding (Red and random Yellow dropping). This count value can be subtracted from the drop counter, as described above, to obtain the drop counts due solely to buffer space limits. The ingress rate drop counters are accessible via the following registers:

- Buffer Manager Port 0 Ingress Rate Drop Count Register (BM_RATE_DRP_CNT_SRC_MII)
- Buffer Manager Port 1 Ingress Rate Drop Count Register (BM_RATE_DRP_CNT_SRC_1)
- Buffer Manager Port 2 Ingress Rate Drop Count Register (BM_RATE_DRP_CNT_SRC_2)

6.6 Switch Fabric Interrupts

The switch fabric is capable of generating multiple maskable interrupts from the buffer manager, switch engine, and MACs. These interrupts are detailed in Section 5.2.2, "Switch Fabric Interrupts," on page 51.

Chapter 7 Ethernet PHYs

7.1 Functional Overview

The LAN9312 contains three PHYs: Port 1 PHY, Port 2 PHY and a Virtual PHY. The Port 1 & 2 PHYs are identical in functionality and each connect their corresponding Ethernet signal pins to the switch fabric MAC of their respective port. These PHYs interface with their respective MAC via an internal MII interface. The Virtual PHY provides the virtual functionality of a PHY and allows connection of the Host MAC to port 0 of the switch fabric as if it was connected to a single port PHY. All PHYs comply with the IEEE 802.3 Physical Layer for Twisted Pair Ethernet and can be configured for full/half duplex 100 Mbps (100BASE-TX) or 10Mbps (10BASE-T) Ethernet operation. All PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set and can be configured indirectly via the Host MAC, or directly via the memory mapped Virtual PHY registers. Refer to Section 14.4, "Ethernet PHY Control and Status Registers" for details on the Ethernet PHY registers.

The LAN9312 Ethernet PHYs are discussed in detail in the following sections:

- Section 7.2, "Port 1 & 2 PHYs," on page 83
- Section 7.3, "Virtual PHY," on page 96

7.1.1 PHY Addressing

Each individual PHY is assigned a unique default PHY address via the phy_addr_sel_strap configuration strap as shown in Table 7.1. In addition, the Port 1 PHY and Port 2 PHY addresses can be changed via the PHY Address (PHYADD) field in the Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x). For proper operation, all LAN9312 PHY addresses must be unique. No check is performed to assure each PHY is set to a different address. Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 40.

Table 7.1 Default PHY Serial MII Addressing

PHY_ADDR_SEL_STRAP	VIRTUAL PHY DEFAULT ADDRESS VALUE	PORT 1 PHY DEFAULT ADDRESS VALUE	PORT 2 PHY DEFAULT ADDRESS VALUE
0	0	1	2
1	1	2	3

7.2 Port 1 & 2 PHYs

Functionally, each PHY can be divided into the following sections:

- 100BASE-TX Transmit and 100BASE-TX Receive
- 10BASE-T Transmit and 10BASE-T Receive
- PHY Auto-negotiation
- HP Auto-MDIX
- MII MAC Interface
- PHY Management Control

Note 7.1 Because the Port 1 PHY and Port 2 PHY are functionally identical, this section will describe them as the “Port x PHY”, or simply “PHY”. Wherever a lowercase “x” has been appended to a port or signal name, it can be replaced with “1” or “2” to indicate the Port 1 or Port 2 PHY respectively. All references to “PHY” in this section can be used interchangeably for both the Port 1 & 2 PHYs. This nomenclature excludes the Virtual PHY.

A block diagram of the Port x PHYs main components can be seen in Figure 7.1.

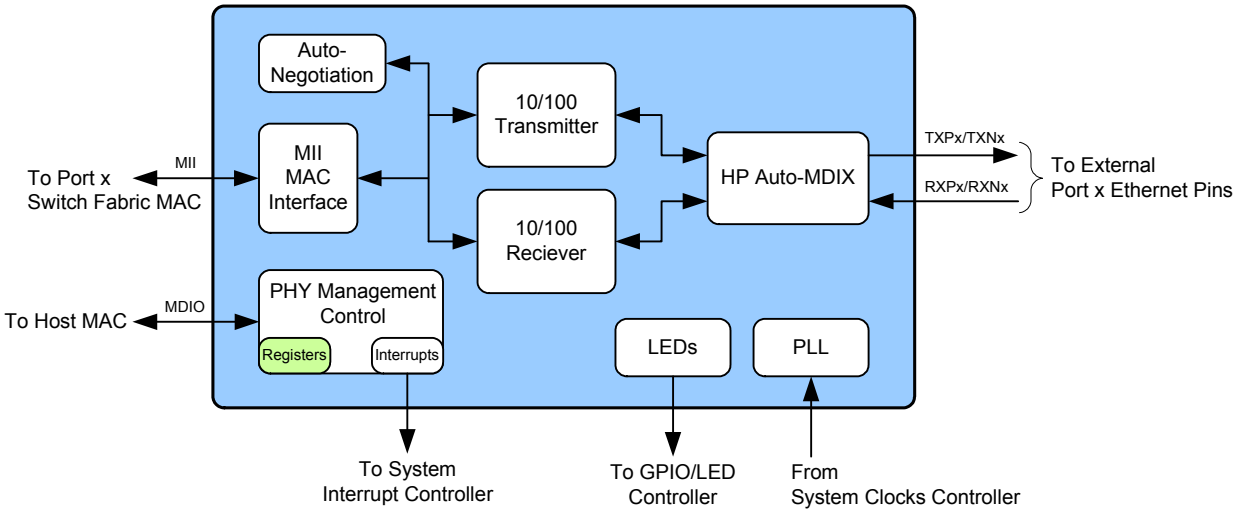


Figure 7.1 Port x PHY Block Diagram

7.2.1 100BASE-TX Transmit

The 100BASE-TX transmit data path is shown in Figure 7.2. Shaded blocks are those which are internal to the PHY. Each major block is explained in the following sections.

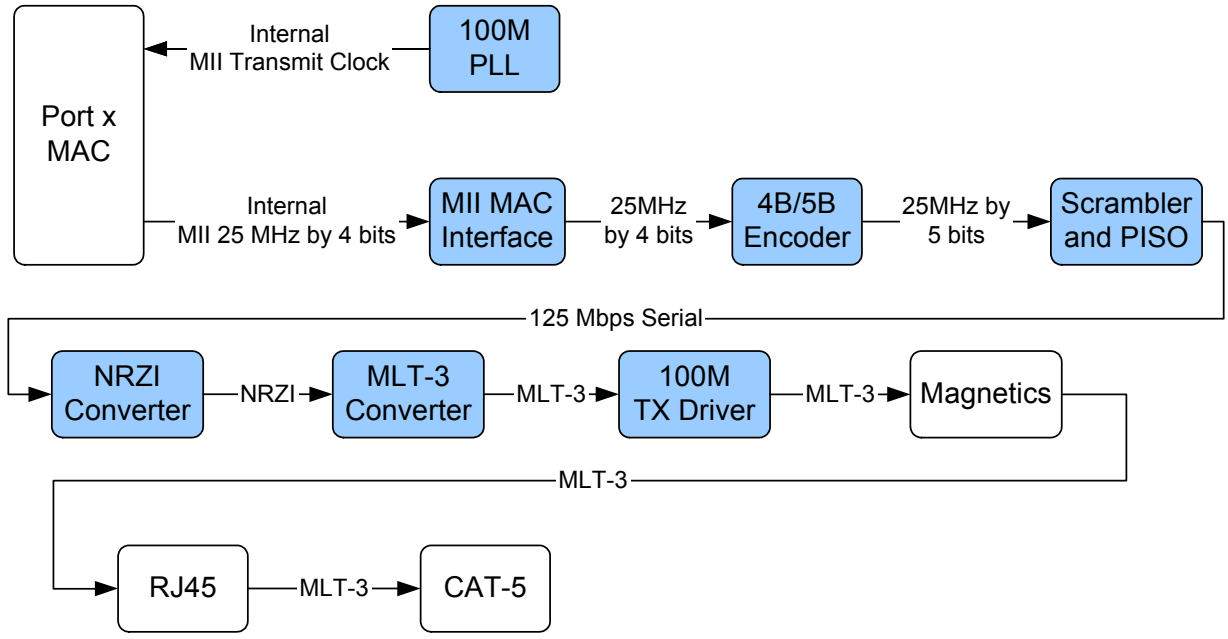


Figure 7.2 100BASE-TX Transmit Data Path

7.2.1.1 MII MAC Interface

For a transmission, the switch fabric MAC drives the transmit data to the PHYs MII MAC Interface. The MII MAC Interface is described in detail in Section 7.2.7, "MII MAC Interface".

Note: The PHY is connected to the switch fabric MAC via standard MII signals. Refer to the IEEE 802.3 specification for additional details.

7.2.1.2 4B/5B Encoder

The transmit data passes from the MII block to the 4B/5B Encoder. This block encodes the data from 4-bit nibbles to 5-bit symbols (known as “code-groups”) according to Table 7.2. Each 4-bit data-nibble is mapped to 16 of the 32 possible code-groups. The remaining 16 code-groups are either used for control information or are not valid.

The first 16 code-groups are referred to by the hexadecimal values of their corresponding data nibbles, 0 through F. The remaining code-groups are given letter designations with slashes on either side. For example, an IDLE code-group is /I/, a transmit error code-group is /H/, etc.

Table 7.2 4B/5B Code Table

CODE GROUP	SYM	RECEIVER INTERPRETATION			TRANSMITTER INTERPRETATION		
11110	0	0	0000	DATA	0	0000	DATA
01001	1	1	0001		1	0001	
10100	2	2	0010		2	0010	
10101	3	3	0011		3	0011	
01010	4	4	0100		4	0100	
01011	5	5	0101		5	0101	
01110	6	6	0110		6	0110	
01111	7	7	0111		7	0111	
10010	8	8	1000		8	1000	
10011	9	9	1001		9	1001	
10110	A	A	1010		A	1010	
10111	B	B	1011		B	1011	
11010	C	C	1100		C	1100	
11011	D	D	1101		D	1101	
11100	E	E	1110		E	1110	
11101	F	F	1111		F	1111	
11111	/I/	IDLE			Sent after /T/R/ until the MII Transmitter Enable signal (TXEN) is received		
11000	/J/	First nibble of SSD, translated to “0101” following IDLE, else MII Receive Error (RXER)			Sent for rising MII Transmitter Enable signal (TXEN)		
10001	/K/	Second nibble of SSD, translated to “0101” following J, else MII Receive Error (RXER)			Sent for rising MII Transmitter Enable signal (TXEN)		
01101	/T/	First nibble of ESD, causes de-assertion of CRS if followed by /R/, else assertion of MII Receive Error (RXER)			Sent for falling MII Transmitter Enable signal (TXEN)		
00111	/R/	Second nibble of ESD, causes de-assertion of CRS if following /T/, else assertion of MII Receive Error (RXER)			Sent for falling MII Transmitter Enable signal (TXEN)		
00100	/H/	Transmit Error Symbol			Sent for rising MII Transmit Error (TXER)		
00110	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)			INVALID		
11001	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)			INVALID		
00000	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)			INVALID		

Table 7.2 4B/5B Code Table (continued)

CODE GROUP	SYM	RECEIVER INTERPRETATION	TRANSMITTER INTERPRETATION
00001	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID
00010	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID
00011	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID
00101	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID
01000	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID
01100	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID
10000	/V/	INVALID, MII Receive Error (RXER) if during MII Receive Data Valid (RXDV)	INVALID

7.2.1.3 Scrambler and PISO

Repeated data patterns (especially the IDLE code-group) can have power spectral densities with large narrow-band peaks. Scrambling the data helps eliminate these peaks and spread the signal power more uniformly over the entire channel bandwidth. This uniform spectral density is required by FCC regulations to prevent excessive EMI from being radiated by the physical wiring. The scrambler also performs the Parallel In Serial Out conversion (PISO) of the data.

The seed for the scrambler is generated from the PHY address, ensuring that each PHY will have its own scrambler sequence. For more information on PHY addressing, refer to Section 7.1.1, "PHY Addressing".

7.2.1.4 NRZI and MLT-3 Encoding

The scrambler block passes the 5-bit wide parallel data to the NRZI converter where it becomes a serial 125MHz NRZI data stream. The NRZI is then encoded to MLT-3. MLT-3 is a tri-level code where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.

7.2.1.5 100M Transmit Driver

The MLT-3 data is then passed to the analog transmitter, which drives the differential MLT-3 signal on output pins TXPx and TXNx (where “x” is replaced with “1” for the Port 1 PHY, or “2” for the Port 2 PHY), to the twisted pair media across a 1:1 ratio isolation transformer. The 10BASE-T and 100BASE-TX signals pass through the same transformer so that common “magnetics” can be used for both. The transmitter drives into the 100Ω impedance of the CAT-5 cable. Cable termination and impedance matching require external components.

7.2.1.6 100M Phase Lock Loop (PLL)

The 100M PLL locks onto the reference clock and generates the 125MHz clock used to drive the 125 MHz logic and the 100BASE-TX Transmitter.

7.2.2 100BASE-TX Receive

The 100BASE-TX receive data path is shown in Figure 7.3. Shaded blocks are those which are internal to the PHY. Each major block is explained in the following sections.

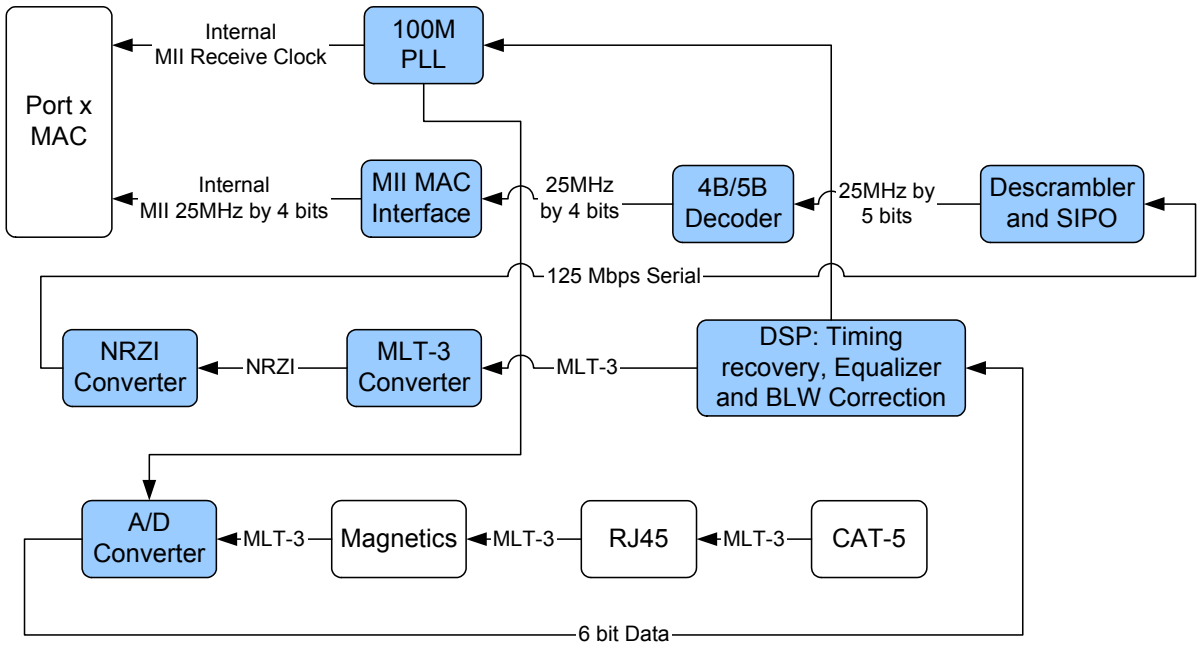


Figure 7.3 100BASE-TX Receive Data Path

7.2.2.1 A/D Converter

The MLT-3 data from the cable is fed into the PHY on inputs RXPx and RXNx (where “x” is replaced with “1” for the Port 1 PHY, or “2” for the Port 2 PHY) via a 1:1 ratio transformer. The ADC samples the incoming differential signal at a rate of 125M samples per second. Using a 64-level quantizer, 6 digital bits are generated to represent each sample. The DSP adjusts the gain of the A/D Converter (ADC) according to the observed signal levels such that the full dynamic range of the ADC can be used.

7.2.2.2 DSP: Equalizer, BLW Correction and Clock/Data Recovery

The 6 bits from the ADC are fed into the DSP block. The equalizer in the DSP section compensates for phase and amplitude distortion caused by the physical channel (magnetics, connectors, and CAT-5 cable). The equalizer can restore the signal for any good-quality CAT-5 cable between 1m and 150m.

If the DC content of the signal is such that the low-frequency components fall below the low frequency pole of the isolation transformer, then the droop characteristics of the transformer will become significant and Baseline Wander (BLW) on the received signal will result. To prevent corruption of the received data, the PHY corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD defined “killer packet” with no bit errors.

The 100M PLL generates multiple phases of the 125MHz clock. A multiplexer, controlled by the timing unit of the DSP, selects the optimum phase for sampling the data. This is used as the received recovered clock. This clock is used to extract the serial data from the received signal.

7.2.2.3 NRZI and MLT-3 Decoding

The DSP generates the MLT-3 recovered levels that are fed to the MLT-3 converter. The MLT-3 is then converted to an NRZI data stream.

7.2.2.4 Descrambler and SIPO

The descrambler performs an inverse function to the scrambler in the transmitter and also performs the Serial In Parallel Out (SIPO) conversion of the data.

During reception of IDLE (/I/) symbols. the descrambler synchronizes its descrambler key to the incoming stream. Once synchronization is achieved, the descrambler locks on this key and is able to descramble incoming data.

Special logic in the descrambler ensures synchronization with the remote PHY by searching for IDLE symbols within a window of 4000 bytes (40us). This window ensures that a maximum packet size of 1514 bytes, allowed by the IEEE 802.3 standard, can be received with no interference. If no IDLE-symbols are detected within this time-period, receive operation is aborted and the descrambler re-starts the synchronization process.

The de-scrambled signal is then aligned into 5-bit code-groups by recognizing the /J/K/ Start-of-Stream Delimiter (SSD) pair at the start of a packet. Once the code-word alignment is determined, it is stored and utilized until the next start of frame.

7.2.2.5 5B/4B Decoding

The 5-bit code-groups are translated into 4-bit data nibbles according to the 4B/5B table shown in Table 7.2. The translated data is presented on the internal MII RXD[3:0] signal lines to the switch fabric MAC. The SSD, /J/K/, is translated to “0101 0101” as the first 2 nibbles of the MAC preamble. Reception of the SSD causes the PHY to assert the RXDV signal, indicating that valid data is available on the RXD bus. Successive valid code-groups are translated to data nibbles. Reception of either the End of Stream Delimiter (ESD) consisting of the /T/R/ symbols, or at least two /I/ symbols causes the PHY to de-assert carrier sense and RXDV. These symbols are not translated into data.

7.2.2.6 Receiver Errors

During a frame, unexpected code-groups are considered receive errors. Expected code groups are the DATA set (0 through F), and the /T/R/ (ESD) symbol pair. When a receive error occurs, the internal MII’s RXER signal is asserted and arbitrary data is driven onto the internal receive data bus (RXD) to the switch fabric MAC. Should an error be detected during the time that the /J/K/ delimiter is being decoded (bad SSD error), RXER is asserted and the value 1110b is driven onto the internal receive data bus (RXD) to the switch fabric MAC. Note that the internal MII’s data valid signal (RXDV) is not yet asserted when the bad SSD occurs.

7.2.2.7 MII MAC Interface

For reception, the 4-bit data nibbles are sent to the MII MAC Interface block where they are sent via MII to the switch fabric MAC. The MII MAC Interface is described in detail in Section 7.2.7, "MII MAC Interface".

Note: The PHY is connected to the switch fabric MAC via standard MII signals. Refer to the IEEE 802.3 specification for additional details.

7.2.3 10BASE-T Transmit

Data to be transmitted comes from the switch fabric MAC. The 10BASE-T transmitter receives 4-bit nibbles from the internal MII at a rate of 2.5MHz and converts them to a 10Mbps serial data stream. The data stream is then Manchester-encoded and sent to the analog transmitter, which drives a signal onto the twisted pair via the external magnetics.

10BASE-T transmissions use the following blocks:

- MII MAC Interface (digital)
- 10M TX Driver (digital/analog)
- 10M PLL (analog)

7.2.3.1 MII MAC Interface

For a transmission, the switch fabric MAC drives the transmit data to the PHYs MII MAC Interface. The MII MAC Interface is described in detail in Section 7.2.7, "MII MAC Interface".

Note: The PHY is connected to the switch fabric MAC via standard MII signals. Refer to the IEEE 802.3 specification for additional details.

7.2.3.2 10M TX Driver and PLL

The 4-bit wide data is sent to the 10M TX Driver block. The nibbles are converted to a 10Mbps serial NRZI data stream. The 10M PLL locks onto the external clock or internal oscillator and produces a 20MHz clock. This is used to Manchester encode the NRZ data stream. When no data is being transmitted (TXEN is low), the 10M TX Driver block outputs Normal Link Pulses (NLPs) to maintain communications with the remote link partner. The manchester encoded data is sent to the analog transmitter where it is shaped and filtered before being driven out as a differential signal across the TXPx and TXNx outputs (where “x” is replaced with “1” for the Port 1 PHY, or “2” for the Port 2 PHY).

7.2.4 10BASE-T Receive

The 10BASE-T receiver gets the Manchester-encoded analog signal from the cable via the magnetics. It recovers the receive clock from the signal and uses this clock to recover the NRZI data stream. This 10M serial data is converted to 4-bit data nibbles which are passed to the controller across the internal MII at a rate of 2.5MHz.

10BASE-T reception uses the following blocks:

- Filter and SQUELCH (analog)
- 10M RX (digital/analog)
- MII MAC Interface (digital)
- 10M PLL (analog)

7.2.4.1 Filter and Squelch

The Manchester signal from the cable is fed into the PHY on inputs RXPx and RXNx (where “x” is replaced with “1” for Port 1, or “2” for Port 2) via 1:1 ratio magnetics. It is first filtered to reduce any out-of-band noise. It then passes through a SQUELCH circuit. The SQUELCH is a set of amplitude and timing comparators that normally reject differential voltage levels below 300mV and detect and recognize differential voltages above 585mV.

7.2.4.2 10M RX and PLL

The output of the SQUELCH goes to the 10M RX block where it is validated as Manchester encoded data. The polarity of the signal is also checked. If the polarity is reversed (local RXP is connected to RXN of the remote partner and vice versa), then this is identified and corrected. The reversed condition

is indicated by the flag “XPOL“, bit 4 in Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x). The 10M PLL locks onto the received Manchester signal and generates the received 20MHz clock from it. Using this clock, the Manchester encoded data is extracted and converted to a 10MHz NRZI data stream. It is then converted from serial to 4-bit wide parallel data.

The RX10M block also detects valid 10BASE-T IDLE signals - Normal Link Pulses (NLPs) - to maintain the link.

7.2.4.3 MII MAC Interface

For reception, the 4-bit data nibbles are sent to the MII MAC Interface block where they are sent via MII to the switch fabric MAC. The MII MAC Interface is described in detail in Section 7.2.7, "MII MAC Interface".

Note: The PHY is connected to the switch fabric MAC via standard MII signals. Refer to the IEEE 802.3 specification for additional details.

7.2.4.4 Jabber Detection

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition, that results in holding the TXEN input for an extended period of time. Special logic is used to detect the jabber state and abort the transmission to the line, within 45ms. Once TXEN is deasserted, the logic resets the jabber condition.

7.2.5 PHY Auto-negotiation

The purpose of the auto-negotiation function is to automatically configure the PHY to the optimum link parameters based on the capabilities of its link partner. Auto-negotiation is a mechanism for exchanging configuration information between two link-partners and automatically selecting the highest performance mode of operation supported by both sides. Auto-negotiation is fully defined in clause 28 of the IEEE 802.3 specification and is enabled by setting bit 12 (PHY_AN) of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x).

The advertised capabilities of the PHY are stored in the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x). The PHY contains the ability to advertise 100BASE-TX and 10BASE-T in both full or half-duplex modes. Besides the connection speed, the PHY can advertise remote fault indication and symmetric or asymmetric pause flow control as defined in the IEEE 802.3 specification. The LAN9312 does not support “Next Page” capability. Many of the default advertised capabilities of the PHY are determined via configuration straps as shown in Section 14.4.2.5, "Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x)," on page 294. Refer to Section 4.2.4, "Configuration Straps," on page 40 for additional details on how to use the LAN9312 configuration straps.

Once auto-negotiation has completed, information about the resolved link and the results of the negotiation process are reflected in the speed indication bits in the Port x PHY Special Control/Status Register (PHY_SPECIAL_CONTROL_STATUS_x), as well as the Port x PHY Auto-Negotiation Link Partner Base Page Ability Register (PHY_AN_LP_BASE_ABILITY_x).

The auto-negotiation protocol is a purely physical layer activity and proceeds independently of the MAC controller.

The following blocks are activated during an Auto-negotiation session:

- Auto-negotiation (digital)
- 100M ADC (analog)
- 100M PLL (analog)
- 100M equalizer/BLW/clock recovery (DSP)
- 10M SQUELCH (analog)

- 10M PLL (analog)
- 10M TX Driver (analog)

Auto-negotiation is started by the occurrence of any of the following events:

- Power-On Reset (POR)
- Hardware reset (nRST)
- PHY Software reset (via Reset Control Register (RESET_CTL), or bit 15 of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x))
- PHY Power-down reset (Section 7.2.9, "PHY Power-Down Modes," on page 94)
- PHY Link status down (bit 2 of the Port x PHY Basic Status Register (PHY_BASIC_STATUS_x) is cleared)
- Setting the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x), bit 9 high (auto-neg restart)
- Digital Reset (via bit 0 of the Reset Control Register (RESET_CTL))
- Issuing an EEPROM Loader RELOAD command (Section 10.2.4, "EEPROM Loader," on page 149)

Note: Refer to Section 4.2, "Resets," on page 36 for information on these and other system resets.

On detection of one of these events, the PHY begins auto-negotiation by transmitting bursts of Fast Link Pulses (FLP). These are bursts of link pulses from the 10M TX Driver. They are shaped as Normal Link Pulses and can pass uncorrupted down CAT-3 or CAT-5 cable. A Fast Link Pulse Burst consists of up to 33 pulses. The 17 odd-numbered pulses, which are always present, frame the FLP burst. The 16 even-numbered pulses, which may be present or absent, contain the data word being transmitted. Presence of a data pulse represents a “1”, while absence represents a “0”.

The data transmitted by an FLP burst is known as a “Link Code Word.” These are defined fully in IEEE 802.3 clause 28. In summary, the PHY advertises 802.3 compliance in its selector field (the first 5 bits of the Link Code Word). It advertises its technology ability according to the bits set in the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x).

There are 4 possible matches of the technology abilities. In the order of priority these are:

- 100M Full Duplex (highest priority)
- 100M Half Duplex
- 10M Full Duplex
- 10M Half Duplex (lowest priority)

If the full capabilities of the PHY are advertised (100M, full-duplex), and if the link partner is capable of 10M and 100M, then auto-negotiation selects 100M as the highest performance mode. If the link partner is capable of half and full-duplex modes, then auto-negotiation selects full-duplex as the highest performance mode.

Once a speed and duplex match has been determined, the link code words are repeated with the acknowledge bit set. Any difference in the main content of the link code words at this time will cause auto-negotiation to re-start. Auto-negotiation will also re-start if all of the required FLP bursts are not received.

Writing the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) bits [8:5] allows software control of the capabilities advertised by the PHY. Writing the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) does not automatically re-start auto-negotiation. The Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x), bit 9 must be set before the new abilities will be advertised. Auto-negotiation can also be disabled via software by clearing bit 12 of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x).

7.2.5.1 PHY Pause Flow Control

The Port 1 & 2 PHYs are capable of generating and receiving pause flow control frames per the IEEE 802.3 specification. The PHYs advertised pause flow control abilities are set via bits 10 (Symmetric Pause) and 11 (Asymmetric Pause) of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x). This allows the PHY to advertise its flow control abilities and auto-negotiate the flow control settings with its link partner. The default values of these bits are determined via configuration straps as defined in Section 14.4.2.5, "Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x)," on page 294.

The pause flow control settings may also be manually set via the manual flow control registers Port 1 Manual Flow Control Register (MANUAL_FC_1) and Port 2 Manual Flow Control Register (MANUAL_FC_2). These registers allow the switch fabric ports flow control settings to be manually set when auto-negotiation is disabled or the Manual Flow Control Select bit 0 is set. The currently enabled duplex and flow control settings can also be monitored via these registers. The flow control values in the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) are not affected by the values of the manual flow control register. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 58 for additional information.

7.2.5.2 Parallel Detection

If the LAN9312 is connected to a device lacking the ability to auto-negotiate (i.e. no FLPs are detected), it is able to determine the speed of the link based on either 100M MLT-3 symbols or 10M Normal Link Pulses. In this case the link is presumed to be half-duplex per the IEEE 802.3 standard. This ability is known as “Parallel Detection.” This feature ensures interoperability with legacy link partners. If a link is formed via parallel detection, then bit 0 in the Port x PHY Auto-Negotiation Expansion Register (PHY_AN_EXP_x) is cleared to indicate that the link partner is not capable of auto-negotiation. If a fault occurs during parallel detection, bit 4 of the Port x PHY Auto-Negotiation Expansion Register (PHY_AN_EXP_x) is set.

The Port x PHY Auto-Negotiation Link Partner Base Page Ability Register (PHY_AN_LP_BASE_ABILITY_x) is used to store the Link Partner Ability information, which is coded in the received FLPs. If the link partner is not auto-negotiation capable, then this register is updated after completion of parallel detection to reflect the speed capability of the link partner.

7.2.5.3 Restarting Auto-Negotiation

Auto-negotiation can be re-started at any time by setting bit 9 of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). Auto-negotiation will also re-start if the link is broken at any time. A broken link is caused by signal loss. This may occur because of a cable break, or because of an interruption in the signal transmitted by the Link Partner. Auto-negotiation resumes in an attempt to determine the new link configuration.

If the management entity re-starts Auto-negotiation by writing to bit 9 of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x), the LAN9312 will respond by stopping all transmission/receiving operations. Once the internal break link time of approximately 1200ms has passed in the Auto-negotiation state-machine, the auto-negotiation will re-start. In this case, the link partner will have also dropped the link due to lack of a received signal, so it too will resume auto-negotiation.

7.2.5.4 Disabling Auto-Negotiation

Auto-negotiation can be disabled by clearing bit 12 of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). The PHY will then force its speed of operation to reflect the speed (bit 13) and duplex (bit 8) of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). The speed and duplex bits in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) should be ignored when auto-negotiation is enabled.

7.2.5.5 Half Vs. Full-Duplex

Half-duplex operation relies on the CSMA/CD (Carrier Sense Multiple Access / Collision Detect) protocol to handle network traffic and collisions. In this mode, the carrier sense signal, CRS, responds to both transmit and receive activity. If data is received while the PHY is transmitting, a collision results.

In full-duplex mode, the PHY is able to transmit and receive data simultaneously. In this mode, CRS responds only to receive activity. The CSMA/CD protocol does not apply and collision detection is disabled.

7.2.6 HP Auto-MDIX

HP Auto-MDIX facilitates the use of CAT-3 (10 BASE-T) or CAT-5 (100 BASE-T) media UTP interconnect cable without consideration of interface wiring scheme. If a user plugs in either a direct connect LAN cable or a cross-over patch cable, as shown in Figure 7.4 (See Note 7.1 on page 83), the PHY is capable of configuring the TXPx/TXNx and RXPx/RXNx twisted pair pins for correct transceiver operation.

The internal logic of the device detects the TX and RX pins of the connecting device. Since the RX and TX line pairs are interchangeable, special PCB design considerations are needed to accommodate the symmetrical magnetics and termination of an Auto-MDIX design.

The Auto-MDIX function can be disabled through bit 15 (AMDIXCTRL) of the Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x). When AMDIXCTRL is cleared, Auto-MDIX can be selected via the auto_mdix_strap_x configuration strap. The MDIX can also be configured manually via the manual_mdix_strap_x if both the AMDIXCTRL bit and the auto_mdix_strap_x configuration strap are low. Refer to Section 3.2, "Pin Descriptions," on page 28 for more information on the configuration straps.

When bit 15 (AMDIXCTRL) of the Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x) is set to 1, the Auto-MDIX capability is determined by bits 13 and 14 of the Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x).

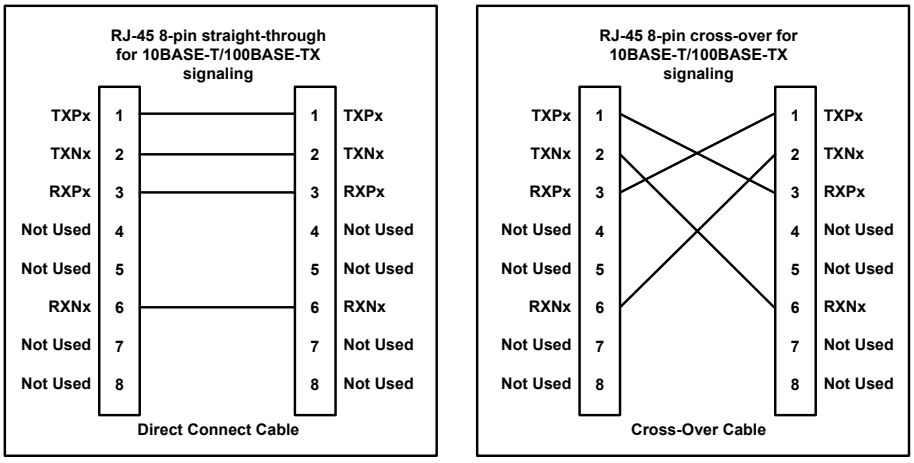


Figure 7.4 Direct Cable Connection vs. Cross-Over Cable Connection

7.2.7 MII MAC Interface

The MII MAC Interface is responsible for the transmission and reception of the Ethernet data to and from the switch fabric MAC. The PHY is connected internally to the switch fabric MAC via standard MII signals per IEEE 802.3.

For a transmission, the switch fabric MAC drives the transmit data onto the internal MII TXD bus and asserts TXEN to indicate valid data. The data is in the form of 4-bit wide data at a rate of 25MHz for 100BASE-TX, or 2.5MHz for 10BASE-T.

For reception, the 4-bit data nibbles are sent to the MII MAC Interface block. These data nibbles are clocked to the controller at a rate of 25MHz for 100BASE-TX, or 2.5MHz for 10BASE-T. RXCLK is the output clock for the internal MII bus. It is recovered from the received data to clock the RXD bus. If there is no received signal, it is derived from the system reference clock.

7.2.8 PHY Management Control

The PHY Management Control block is responsible for the management functions of the PHY, including register access and interrupt generation. A Serial Management Interface (SMI) is used to support registers 0 through 6 as required by the IEEE 802.3 (Clause 22), as well as the vendor specific registers allowed by the specification. The SMI interface consists of the MII Management Data (MDIO) signal and the MII Management Clock (MDC) signal. These signals interface to the Host MAC and allow access to all PHY registers. Refer to Section 14.4.2, "Port 1 & 2 PHY Registers," on page 286 for a list of all supported registers and register descriptions. Non-supported registers will be read as FFFFh.

7.2.8.1 PHY Interrupts

The PHY contains the ability to generate various interrupt events as described in Table 7.3. Reading the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x) shows the source of the interrupt, and clears the interrupt signal. The Port x PHY Interrupt Mask Register (PHY_INTERRUPT_MASK_x) enables or disables each PHY interrupt. The PHY Management Control block aggregates the enabled interrupts status into an internal signal which is sent to the System Interrupt Controller and is reflected via the Interrupt Status Register (INT_STS) bit 26 (PHY_INT1) for the Port 1 PHY, and bit 27 (PHY_INT2) for the Port 2 PHY. For more information on the LAN9312 interrupts, refer to Chapter 5, "System Interrupts," on page 49.

Table 7.3 PHY Interrupt Sources

INTERRUPT SOURCE	PHY_INTERRUPT_MASK_x & PHY_INTERRUPT_SOURCE_x REGISTER BIT #
ENERGYON Activated	7
Auto-Negotiation Complete	6
Remote Fault Detected	5
Link Down (Link Status Negated)	4
Auto-Negotiation LP Acknowledge	3
Parallel Detection Fault	2
Auto-Negotiation Page Received	1

7.2.9 PHY Power-Down Modes

There are two power-down modes for the PHY:

- PHY General Power-Down
- PHY Energy Detect Power-Down

Note: For more information on the various power management features of the LAN9312, refer to Section 4.3, "Power Management," on page 46.

Note: The power-down modes of each PHY (Port 1 PHY and Port 2 PHY) are controlled independently.

Note: The PHY power-down modes do not reload or reset the PHY registers.

7.2.9.1 PHY General Power-Down

This power-down mode is controlled by bit 11 of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). In this mode the entire PHY, except the PHY management control interface, is powered down. The PHY will remain in this power-down state as long as bit 11 is set. When bit 11 is cleared, the PHY powers up and is automatically reset.

7.2.9.2 PHY Energy Detect Power-Down

This power-down mode is enabled by setting bit 13 (EDPWRDOWN) of the Port x PHY Mode Control/Status Register (PHY_MODE_CONTROL_STATUS_x). When in this mode, if no energy is detected on the line, the entire PHY is powered down except for the PHY management control interface, the SQUELCH circuit, and the ENERGYON logic. The ENERGYON logic is used to detect the presence of valid energy from 100BASE-TX, 10BASE-T, or auto-negotiation signals and is responsible for driving the ENERGYON signal (bit 1) of the Port x PHY Mode Control/Status Register (PHY_MODE_CONTROL_STATUS_x).

In this mode, when the ENERGYON signal is cleared, the PHY is powered down and no data is transmitted from the PHY. When energy is received, via link pulses or packets, the ENERGYON signal goes high, and the PHY powers up. The PHY automatically resets itself into its previous state prior to power-down, and asserts the INT7 interrupt (bit 7) of the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x). The first and possibly second packet to activate ENERGYON may be lost.

When bit 13 (EDPWRDOWN) of the Port x PHY Mode Control/Status Register (PHY_MODE_CONTROL_STATUS_x) is low, energy detect power-down is disabled.

The energy detect power down feature is part of the broader power management features of the LAN9312 and can be used to trigger the power management event output pin (PME). This is accomplished by enabling the energy detect power-down feature of the PHY as described above, and setting the corresponding energy detect enable (bit 14 for Port 1 PHY, bit 15 for Port 2 PHY) of the Power Management Control Register (PMT_CTRL). Refer to Section 4.3, "Power Management," on page 46 for additional information.

7.2.10 PHY Resets

In addition to the chip-level hardware reset (nRST) and Power-On Reset (POR), the PHY supports three block specific resets. These are discussed in the following sections. For detailed information on all LAN9312 resets and the reset sequence refer to Section 4.2, "Resets," on page 36.

Note: The DIGITAL_RST bit in the Reset Control Register (RESET_CTL) does not reset the PHYs. Only a hardware reset (nRST) or an EEPROM RELOAD command will automatically reload the configuration strap values into the PHY registers. For all other PHY resets, these values will need to be manually configured via software.

7.2.10.1 PHY Software Reset via RESET_CTL

The PHY can be reset via the Reset Control Register (RESET_CTL). The Port 1 PHY is reset by setting bit 1 (PHY1_RST), and the Port 2 PHY is reset by setting bit 2 (PHY2_RST). These bits are self clearing after approximately 102uS. This reset does not reload the configuration strap values into the PHY registers.

7.2.10.2 PHY Software Reset via PHY_BASIC_CTRL_x

The PHY can also be reset by setting bit 15 (PHY_RST) of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). This bit is self clearing and will return to 0 after the reset is complete. This reset does not reload the configuration strap values into the PHY registers.

7.2.10.3 PHY Power-Down Reset

After the PHY has returned from a power-down state, a reset of the PHY is automatically generated. The PHY power-down modes do not reload or reset the PHY registers. Refer to Section 7.2.9, "PHY Power-Down Modes," on page 94 for additional information.

7.2.11 LEDs

Each PHY provides LED indication signals to the GPIO/LED block of the LAN9312. This allows external LEDs to be used to indicate various PHY related functions such as TX/RX activity, speed, duplex, or link status. Refer to Chapter 13, "GPIO/LED Controller," on page 162 for additional information on the configuration of these signals.

7.2.12 Required Ethernet Magnetics

The magnetics selected for use with the LAN9312 should be an Auto-MDIX style magnetic, which is widely available from several vendors. Please review the SMSC Application note 8.13 “Suggested Magnetics” for the latest qualified and suggested magnetics. A list of vendors and part numbers are provided within the application note.

7.3 Virtual PHY

The Virtual PHY provides a basic MII management interface (MDIO) to the Host MAC per the IEEE 802.3 (clause 22) so that an unmodified driver can be supported as if the Host MAC was attached to a single port PHY. This functionality is designed to allow easy and quick integration of the LAN9312 into designs with minimal driver modifications. The Virtual PHY provides a full bank of registers which comply with the IEEE 802.3 specification. This enables the Virtual PHY to provide various status and control bits similar to those provided by a real PHY. These include the output of speed selection, duplex, loopback, isolate, collision test, and auto-negotiation status. For a list of all Virtual PHY registers and related bit descriptions, refer to Section 14.4.1, "Virtual PHY Registers," on page 286.

7.3.1 Virtual PHY Auto-Negotiation

The purpose of the auto-negotiation function is to automatically configure the Virtual PHY to the optimum link parameters based on the capabilities of its link partner. Because the Virtual PHY has no actual link partner, the auto-negotiation process is emulated with deterministic results.

Auto-negotiation is enabled by setting bit 12 (VPHY_AN) of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) and is restarted by the occurrence of any of the following events:

- Power-On Reset (POR)
- Hardware reset (nRST)
- PHY Software reset (via bit 3 of the Reset Control Register (RESET_CTL), bit 0 of the Power Management Control Register (PMT_CTRL), or bit 15 of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL))
- Setting the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL), bit 9 high (auto-neg restart)
- Digital Reset (via bit 10 of the Reset Control Register (RESET_CTL))
- Issuing an EEPROM Loader RELOAD command (Section 10.2.4, "EEPROM Loader," on page 149)

The emulated auto-negotiation process is much simpler than the real process and can be categorized into three steps:

1. Bit 5 (Auto-Negotiation Complete) is set in the Virtual PHY Basic Status Register (VPHY_BASIC_STATUS).
2. Bit 1 (Page Received) is set in the Virtual PHY Auto-Negotiation Expansion Register (VPHY_AN_EXP).
3. The auto-negotiation result (speed and duplex) is determined and registered.

The auto-negotiation result (speed and duplex) is determined using the Highest Common Denominator (HCD) of the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) and Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY) as specified in the IEEE 802.3 standard. The technology ability bits of these registers are ANDed, and if there are multiple bits in common, the priority is determined as follows:

- 100Mbps Full Duplex (highest priority)
- 100Mbps Half Duplex
- 10Mbps Full Duplex
- 10Mbps Half Duplex (lowest priority)

For example, if the full capabilities of the Virtual PHY are advertised (100Mbps, Full Duplex), and if the link partner is capable of 10Mbps and 100Mbps, then auto-negotiation selects 100Mbps as the highest performance mode. If the link partner is capable of half and full-duplex modes, then auto-negotiation selects full-duplex as the highest performance operation. In the event that there are no bits in common, an emulated Parallel Detection is used.

The Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) defaults to having all four ability bits set. These values can be reconfigured via software. Once the auto-negotiation is complete, any change to the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) will not take affect until the auto-negotiation process is re-run. The emulated link partner always advertises all four abilities (100BASE-X full duplex, 100BASE-X half duplex, 10BASE-T full duplex, and 10BASE-T half duplex) in the Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY). Neither the Virtual PHY or the emulated link partner support next page capability, remote faults, or 100BASE-T4.

If there is at least one common selection between the emulated link partner and the Virtual PHY advertised abilities, then the auto-negotiation succeeds, the Link Partner Auto-Negotiation Able bit 0 of the Virtual PHY Auto-Negotiation Expansion Register (VPHY_AN_EXP) is set, and the technology ability bits in the Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY) are set to indicate the emulated link partners abilities.

Note: For the Virtual PHY, the auto-negotiation register bits (and management of such) are used by the Host MAC. So the perception of local and link partner is reversed. The local device is the Host MAC, while the link partner is the switch fabric. This is consistent with the intention of the Virtual PHY.

7.3.1.1 Parallel Detection

In the event that there are no common bits between the advertised ability and the emulated link partners ability, auto-negotiation fails and emulated parallel detect is used. In this case, the Link Partner Auto-Negotiation Able (bit 0) in the Virtual PHY Auto-Negotiation Expansion Register (VPHY_AN_EXP) will be cleared, and the communication set to 100Mbps half-duplex. Only one of the technology ability bits in the Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY) will be set, indicating the emulated parallel detect result.

7.3.1.2 Disabling Auto-Negotiation

Auto-negotiation can be disabled in the Virtual PHY by clearing bit 12 (VPHY_AN) of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). The Virtual PHY will then force its speed of operation to reflect the speed (bit 13) and duplex (bit 8) of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). The speed and duplex bits in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) should be ignored when auto-negotiation is enabled.

7.3.1.3 Virtual PHY Pause Flow Control

The Virtual PHY supports pause flow control per the IEEE 802.3 specification. The Virtual PHYs advertised pause flow control abilities are set via bits 10 (Symmetric Pause) and 11 (Asymmetric Pause) of the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV). This allows the Virtual PHY to advertise its flow control abilities and auto-negotiate the flow control settings with the emulated link partner. The default values of these bits are as shown in Section 14.2.8.5, "Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV)," on page 252.

The symmetric/asymmetric pause ability of the emulated link partner is based upon the advertised pause flow control abilities of the Virtual PHY in (bits 10 & 11) of the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV). Thus, the emulated link partner always accommodates the asymmetric/symmetric pause ability settings requested by the Virtual PHY, as shown in Table 14.5, “Emulated Link Partner Pause Flow Control Ability Default Values,” on page 255.

The pause flow control settings may also be manually set via the Port 0(Host MAC) Manual Flow Control Register (MANUAL_FC_MII). This register allows the switch fabric port 0 flow control settings to be manually set when auto-negotiation is disabled or the Manual Flow Control Select bit 0 is set. The currently enabled duplex and flow control settings can also be monitored via this register. The flow control values in the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) are not affected by the values of the manual flow control register. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 58 for additional information.

7.3.2 Virtual PHY Resets

In addition to the chip-level hardware reset (nRST) and Power-On Reset (POR), the Virtual PHY supports three block specific resets. These are is discussed in the following sections. For detailed information on all LAN9312 resets, refer to Section 4.2, "Resets," on page 36.

7.3.2.1 Virtual PHY Software Reset via RESET_CTL

The Virtual PHY can be reset via the Reset Control Register (RESET_CTL) by setting bit 3 (VPHY_RST). This bit is self clearing after approximately 102uS.

7.3.2.2 Virtual PHY Software Reset via VPHY_BASIC_CTRL

The Virtual PHY can also be reset by setting bit 15 (VPHY_RST) of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). This bit is self clearing and will return to 0 after the reset is complete.

7.3.2.3 Virtual PHY Software Reset via PMT_CTRL

The Virtual PHY can be reset via the Power Management Control Register (PMT_CTRL) by setting bit 10 (VPHY_RST). This bit is self clearing after approximately 102uS.

Chapter 8 Host Bus Interface (HBI)

8.1 Functional Overview

The Host Bus Interface (HBI) module provides a high-speed asynchronous SRAM-like slave interface that facilitates communication between the LAN9312 and a host system. The HBI allows access to the System CSRs and handles byte swapping based on the dynamic endianess select. The HBI interfaces to the switch fabric via the Host MAC, which contains the TX/RX Data and Status FIFOs, Host MAC registers and power management features. Refer to Chapter 9, "Host MAC," on page 112 for detailed information on the Host MAC.

The following is an overview of the functions provided by the HBI:

Asynchronous 32-bit Host Bus Interface: The HBI provides an asynchronous SRAM-like Host Bus Interface that is compatible with most CPUs.

- **Host data bus endianess control:** The HBI supports dynamic selection of big and little endian host byte ordering based on the END_SEL input pin. This highly flexible interface provides mixed endian access for registers and memory.
- **Direct FIFO access modes:** When the FIFO_SEL input pin is high during host access, all host write operations are to the TX data FIFO and all host read operations are from the RX data FIFOs. This feature facilitates operation with host DMA controllers that do not support FIFO operations.

System CSR's: The HBI allows for configuration and monitoring of the various LAN9312 functions through the System Control and Status Registers (CSRs). These registers are accessible to the host via the Host Bus Interface and allow direct (and indirect) access to all the LAN9312 functions. For a full list of all System CSR's and their descriptions, refer to Section 14.2, "System Control and Status Registers".

Interrupt support: The HBI supports a variety of interrupt sources. Individual interrupts can be monitored and enabled/disabled via registers within the System CSRs for output on the IRQ pin. For more information on interrupts, refer to Chapter 5, "System Interrupts," on page 49.

For a list of all HBI related pins, refer to Table 3.4 on page 30 in Chapter 3, Pin Description and Configuration.

8.2 Host Memory Mapping

The host memory map has two unique modes: normal operation mode, and direct FIFO access mode. During normal operation, the base address decode map is as described in Figure 14.1 on page 166, allowing access to the full range of System Management CSRs and the TX/RX Data and Status FIFOs. This is the default mode of operation. The second mode of operation is the direct FIFO access mode. In direct FIFO access mode, all host write operations are to the TX Data FIFO and all host read operations are from the RX Data FIFO. Refer to Section 14.1.3, "Direct FIFO Access Mode," on page 167 for additional information.

8.3 Host Endianess

The LAN9312 supports big and little endian host byte ordering based upon the END_SEL pin. When END_SEL is low, host access is little endian. When END_SEL is high, host access is big endian. In a typical application, END_SEL is connected to a high-order address line, making endian selection address based. This highly flexible interface provides mixed endian access for registers and memory for both PIO and host DMA access. As an example, PIO transfers to/from the System CSRs can utilize a different byte ordering than host DMA transactions to/from the RX and TX Data FIFOs.

All internal busses are 32-bit with little endian byte ordering. Logic within the host bus interface re-orders bytes based on the state of the endian select signal (END_SEL).

Data path operations for the supported endian configurations are illustrated in Figure 8.1, "Little Endian Byte Ordering" and Figure 8.2, "Big Endian Byte Ordering".

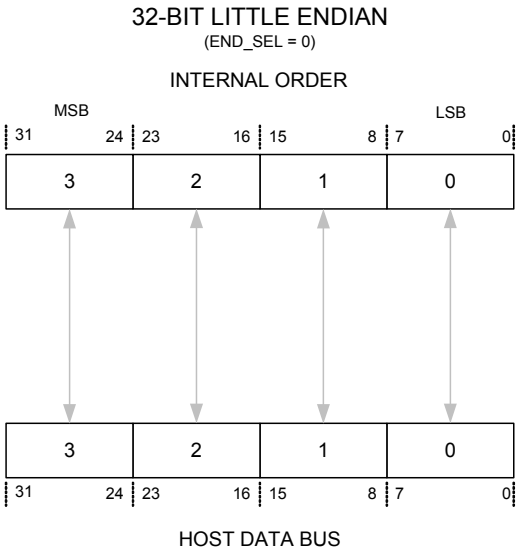


Figure 8.1 Little Endian Byte Ordering

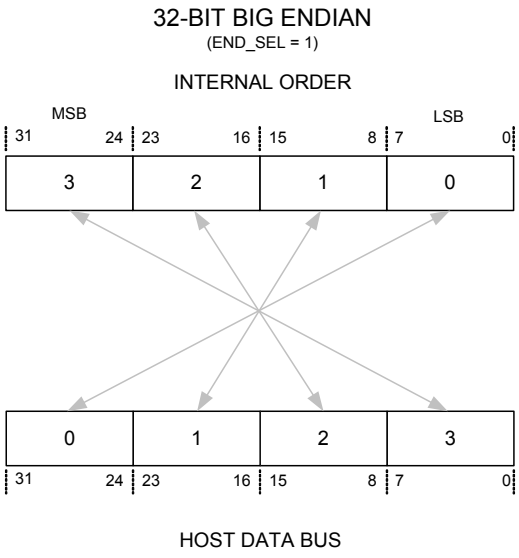


Figure 8.2 Big Endian Byte Ordering

8.4 Host Interface Timing

This section details the characteristics and special restrictions of the various supported host cycles. For detailed timing specifications on supported PIO read/write operations, refer to Section 15.5, "AC Specifications". The LAN9312 supports the following host cycles:

Read Cycles:

- PIO Reads (nCS or nRD controlled)
- PIO Burst Reads (nCS or nRD controlled)
- RX Data FIFO Direct PIO Reads (nCS or nRD controlled)
- RX Data FIFO Direct PIO Burst Reads (nCS or nRD controlled)

Write Cycles:

- PIO Writes (nCS or nWR controlled)
- TX Data FIFO Direct PIO Writes (nCS or nWR controlled)

8.4.1 Special Situations

8.4.1.1 Reset Ending During a Read Cycle

If a reset condition terminates during an active read cycle, the tail end of the read cycle will be ignored by the LAN9312.

8.4.1.2 Writes Following a Reset

Following any reset, writes from the host bus are ignored until after a read cycle is performed.

8.4.2 Special Restrictions on Back-to Back Write-Read Cycles

It is important to note that there are specific restrictions on the timing of back-to-back host write-read operations. These restrictions concern reading the host control registers after *any* write cycle to the LAN9312. In some cases there is a delay between writing to the LAN9312, and the subsequent side effect (change in the control register value). For example, when writing to the TX Data FIFO, it takes up to 135ns for the level indication to change in the TX FIFO Information Register (TX_FIFO_INF).

In order to prevent the host from reading stale data after a write operation, minimum wait periods have been established. These periods are specified in Table 8.1. The host processor is required to wait the specified period of time after any write to the LAN9312 before reading the resource specified in the table. These wait periods are for read operations that immediately follow any write cycle. Note that the required wait period is dependant upon the register being read after the write.

Performing “dummy” reads of the Byte Order Test Register (BYTE_TEST) register is a convenient way to guarantee that the minimum write-to-read timing restriction is met. Table 8.1 shows the number of dummy reads that are required before reading the register indicated. The number of BYTE_TEST reads in this table is based on the minimum timing for T_{cyc} (45ns). For microprocessors with slower busses the number of reads may be reduced as long as the total time is equal to, or greater than the time specified in the table. Note that dummy reads of the BYTE_TEST register are not required as long as the minimum time period is met.

Table 8.1 Read After Write Timing Rules

REGISTER NAME	MINIMUM WAIT TIME FOR READ FOLLOWING ANY WRITE CYCLE (IN NS)	NUMBER OF BYTE_TEST READS (ASSUMING T_{CYC} OF 45NS)
RX Data FIFO	0	0
RX Status FIFO	0	0
RX Status FIFO PEEK	0	0
TX Status FIFO	0	0
TX Status FIFO PEEK	0	0
ID_REV	0	0
IRQ_CFG	135	3
INT_STS	90	2
INT_EN	45	1
BYTE_TEST	0	0
FIFO_INT	45	1
RX_CFG	45	1
TX_CFG	45	1
HW_CFG	45	1
RX_DP_CTRL	45	1
RX_FIFO_INF	0	0
TX_FIFO_INF	135	3
PMT_CTRL	315	7
GPT_CFG	45	1
GPT_CNT	135	3
FREE_RUN	180	4
RX_DROP	0	0
MAC_CSR_CMD	45	1
MAC_CSR_DATA	45	1
AFC_CFG	45	1
1588_CLOCK_HI_RX_CAPTURE_1	0	0
1588_CLOCK_LO_RX_CAPTURE_1	0	0
1588_SEQ_ID_SRC_UUID_HI_RX_CAPTURE_1	0	0
1588_SRC_UUID_LO_RX_CAPTURE_1	0	0
1588_CLOCK_HI_TX_CAPTURE_1	0	0

Table 8.1 Read After Write Timing Rules (continued)

REGISTER NAME	MINIMUM WAIT TIME FOR READ FOLLOWING ANY WRITE CYCLE (IN NS)	NUMBER OF BYTE_TEST READS (ASSUMING T_{CYC} OF 45NS)
1588_CLOCK_LO_TX_CAPTURE_1	0	0
1588_SEQ_ID_SRC_UUID_HI_TX_CAPTURE_1	0	0
1588_SRC_UUID_LO_TX_CAPTURE_1	0	0
1588_CLOCK_HI_RX_CAPTURE_2	0	0
1588_CLOCK_LO_RX_CAPTURE_2	0	0
1588_SEQ_ID_SRC_UUID_HI_RX_CAPTURE_2	0	0
1588_SRC_UUID_LO_RX_CAPTURE_2	0	0
1588_CLOCK_HI_TX_CAPTURE_2	0	0
1588_CLOCK_LO_TX_CAPTURE_2	0	0
1588_SEQ_ID_SRC_UUID_HI_TX_CAPTURE_2	0	0
1588_SRC_UUID_LO_TX_CAPTURE_2	0	0
1588_CLOCK_HI_RX_CAPTURE_MII	0	0
1588_CLOCK_LO_RX_CAPTURE_MII	0	0
1588_SEQ_ID_SRC_UUID_HI_RX_CAPTURE_MII	0	0
1588_SRC_UUID_LO_RX_CAPTURE_MII	0	0
1588_CLOCK_HI_TX_CAPTURE_MII	0	0
1588_CLOCK_LO_TX_CAPTURE_MII	0	0
1588_SEQ_ID_SRC_UUID_HI_TX_CAPTURE_MII	0	0
1588_SRC_UUID_LO_TX_CAPTURE_MII	0	0
1588_CLOCK_HI_CAPTURE_GPIO_8	0	0
1588_CLOCK_LO_CAPTURE_GPIO_8	0	0
1588_CLOCK_HI_CAPTURE_GPIO_9	0	0
1588_CLOCK_LO_CAPTURE_GPIO_9	0	0
1588_CLOCK_HI	45	1
1588_CLOCK_LO	45	1
1588_CLOCK_ADDEND	45	1
1588_CLOCK_TARGET_HI	45	1
1588_CLOCK_TARGET_LO	45	1
1588_CLOCK_TARGET_RELOAD_HI	45	1
1588_CLOCK_TARGET_RELOAD_LO	45	1
1588_AUX_MAC_HI	45	1

Table 8.1 Read After Write Timing Rules (continued)

REGISTER NAME	MINIMUM WAIT TIME FOR READ FOLLOWING ANY WRITE CYCLE (IN NS)	NUMBER OF BYTE_TEST READS (ASSUMING T_{CYC} OF 45NS)
1588_AUX_MAC_LO	45	1
1588_CONFIG	45	1
1588_INT_STS_EN	45	1
MANUAL_FC_1	45	1
MANUAL_FC_2	45	1
MANUAL_FC_MII	45	1
SWITCH_CSR_DATA	45	1
SWITCH_CSR_CMD	45	1
E2P_CMD	45	1
E2P_DATA	45	1
LED_CFG	45	1
VPHY_BASIC_CTRL	45	1
VPHY_BASIC_STATUS	45	1
VPHY_ID_MSB	45	1
VPHY_ID_LSB	45	1
VPHY_AN_ADV	45	1
VPHY_AN_LP_BASE_ABILITY	45	1
VPHY_AN_EXP	45	1
VPHY_SPECIAL_CONTROL_STATUS	45	1
GPIO_CFG	45	1
GPIO_DATA_DIR	45	1
GPIO_INT_STS_EN	45	1
SWITCH_MAC_ADDRH	45	1
SWITCH_MAC_ADDRL	45	1
RESET_CTL	45	1
SWITCH_CSR_DIRECT_DATA	NA	NA

8.4.3 Special Restrictions on Back-to-Back Read Cycles

There are also restrictions on specific back-to-back host read operations. These restrictions concern reading specific registers after reading a resource that has side effects. In many cases there is a delay between reading the LAN9312, and the subsequent indication of the expected change in the control and status register values.

In order to prevent the host from reading stale data on back-to-back reads, minimum wait periods have been established. These periods are specified in Table 8.2. The host processor is required to wait the specified period of time between read operations of specific combinations of resources. The wait period is dependant upon the combination of registers being read.

Performing “dummy” reads of the Byte Order Test Register (BYTE_TEST) register is a convenient way to guarantee that the minimum wait time restriction is met. Table 8.2 below also shows the number of dummy reads that are required for back-to-back read operations. The number of BYTE_TEST reads in this table is based on the minimum timing for T_{cyc} (45ns). For microprocessors with slower busses the number of reads may be reduced as long as the total time is equal to, or greater than the time specified in the table. Dummy reads of the BYTE_TEST register are not required as long as the minimum time period is met.

Table 8.2 Read After Read Timing Rules

AFTER READING...	WAIT FOR THIS MANY NANOSECONDS...	OR PERFORM THIS MANY READS OF BYTE_TEST... (ASSUMING T_{CYC} OF 45NS)	BEFORE READING...
RX Data FIFO	135	3	RX_FIFO_INF
RX Status FIFO	135	3	RX_FIFO_INF
TX Status FIFO	135	3	TX_FIFO_INF
RX_DROP	180	4	RX_DROP
SWITCH_CSR_DATA	45	1	SWITCH_CSR_CMD Note 8.1
VPHY_AN_EXP	45	1	VPHY_AN_EXP

Note 8.1 This timing applies only to the auto-increment and auto-decrement modes of Switch Fabric CSR register access.

8.4.4 PIO Reads

PIO reads can be used to access System CSR's or RX Data and RX/TX Status FIFOs. PIO reads can be performed using Chip Select (nCS) or Read Enable (nRD). A PIO Read cycle begins when both nCS and nRD are asserted. Either or both of these control signals must de-assert between cycles for the period specified in Table 15.8, "PIO Read Cycle Timing Values," on page 447. The cycle ends when either or both nCS and nRD are de-asserted. They may be asserted and de-asserted in any order. Read data is valid as indicated in the functional timing diagram in Figure 8.3.

The endian select signal (END_SEL) has the same timing characteristics as the address lines.

Please refer to Section 15.5.4, "PIO Read Cycle Timing," on page 447 for the AC timing specifications for PIO read operations.

Note: Some registers have restrictions on the timing of back-to-back write-read cycles. Please refer to Section 8.4.2 for information on these restrictions.

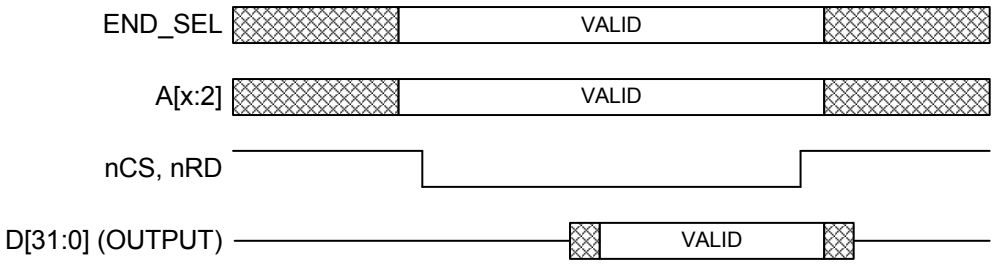


Figure 8.3 Functional Timing for PIO Read Operation

8.4.5 PIO Burst Reads

In this mode, performance is improved by allowing up to 8 DWORD read cycles back-to-back. PIO burst reads can be performed using Chip Select (nCS) or Read Enable (nRD). A PIO Burst Read begins when both nCS and nRD are asserted. Either or both of these control signals must de-assert between bursts for the period specified in Table 15.9, “PIO Burst Read Cycle Timing Values,” on page 448. The burst cycle ends when either or both nCS and nRD are de-asserted. They may be asserted and de-asserted in any order. Read data is valid as indicated in the functional timing diagram in Figure 8.4.

Note: Fresh data is supplied each time A[2] toggles.

The endian select signal (END_SEL) has the same timing characteristics as the upper address lines.

Please refer to Section 15.5.5, "PIO Burst Read Cycle Timing," on page 448 for the AC timing specifications for PIO burst read operations.

Note: PIO burst reads are only supported for the RX Data FIFO. Burst reads from other registers are not supported.

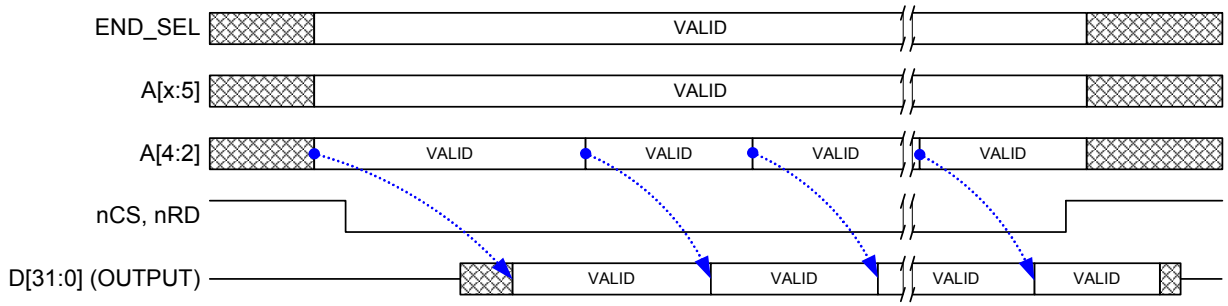


Figure 8.4 Functional Timing for PIO Burst Read Operation

8.4.6 RX Data FIFO Direct PIO Reads

In this mode only A[2] is decoded, and any read of the LAN9312 will read the RX Data FIFO. This mode is enabled when FIFO_SEL is driven high during a read access. This is normally accomplished by connecting the FIFO_SEL signal to a high-order address line. This mode is useful when the host processor must increment its address when accessing the LAN9312.

Timing is identical to a PIO read and the FIFO_SEL and END_SEL signals have the same timing characteristics as the address lines. An RX Data FIFO direct PIO read cycle begins when both nCS and nRD are asserted. Either or both of these control signals must de-assert between cycles for the period specified in Table 15.10, “RX Data FIFO Direct PIO Read Cycle Timing Values,” on page 449. The cycle ends when either or both nCS and nRD are de-asserted. These signals may be asserted and de-asserted in any order. Read data is valid as indicated in the functional timing diagram in Figure 8.5.

Note: A[9:3] are ignored during RX Data FIFO direct PIO reads.

Please refer to Section 15.5.6, "RX Data FIFO Direct PIO Read Cycle Timing," on page 449 for the AC timing specifications for RX Data FIFO direct PIO read operations.

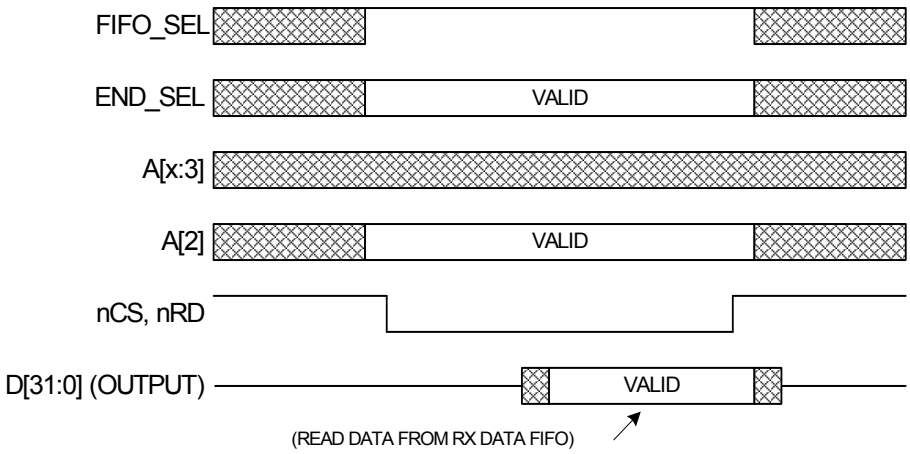


Figure 8.5 Functional Timing for RX Data FIFO Direct PIO Read Operation

8.4.7 RX Data FIFO Direct PIO Burst Reads

In this mode only A[2] is decoded, and any burst read of the LAN9312 will read the RX Data FIFO. This mode is enabled when FIFO_SEL is driven high during a read access. This is normally accomplished by connecting the FIFO_SEL signal to a high-order address line. This mode is useful when the host processor must increment its address when accessing the LAN9312. Timing is identical to a PIO burst read, and the FIFO_SEL and END_SEL signals have the same timing characteristics as the address lines.

In this mode, performance is improved by allowing an unlimited number of back-to-back DWORD read cycles. RX Data FIFO direct PIO burst reads can be performed using chip select (nCS) or read enable (nRD). An RX Data FIFO direct PIO burst read begins when both nCS and nRD are asserted. Either or both of these control signals must de-assert between bursts for the period specified in Table 15.11, “RX Data FIFO Direct PIO Burst Read Cycle Timing Values,” on page 450. The burst cycle ends when either or both nCS and nRD are de-asserted. They may be asserted and de-asserted in any order. Read data is valid as indicated in the functional timing diagram in Figure 8.6.

Note: Fresh data is supplied each time A[2] toggles.

Please refer to Section 15.5.7, "RX Data FIFO Direct PIO Burst Read Cycle Timing," on page 450 for the AC timing specifications for PIO RX Data FIFO direct PIO burst read operations.

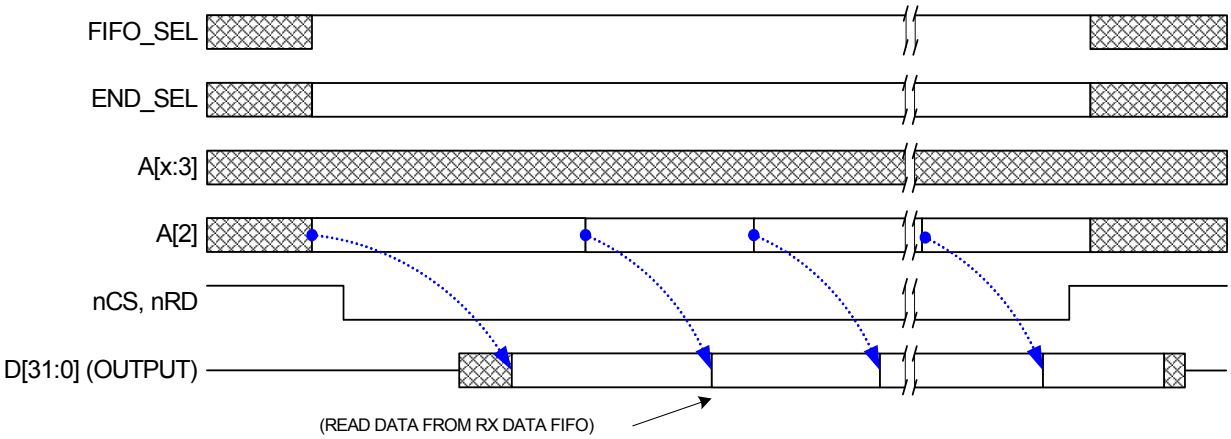


Figure 8.6 Functional Timing for RX Data FIFO Direct PIO Burst Read Operation

8.4.8 PIO Writes

PIO writes are used for all LAN9312 write cycles. PIO writes can be performed using Chip Select (nCS) or Write Enable (nWR). A PIO write cycle begins when both nCS and nWR are asserted. The cycle ends when either or both nCS and nWR are de-asserted. Either or both of these control signals must de-assert between cycles for the period specified in Table 15.12, “PIO Write Cycle Timing Values,” on page 451. They may be asserted and de-asserted in any order. Either or both of these control signals must be de-asserted between cycles for the period specified. The PIO write cycle is illustrated in the functional timing diagram in Figure 8.7.

The END_SEL signal has the same timing characteristics as the address lines.

Please refer to Section 15.5.8, "PIO Write Cycle Timing," on page 451 for the AC timing specifications for PIO write operations.

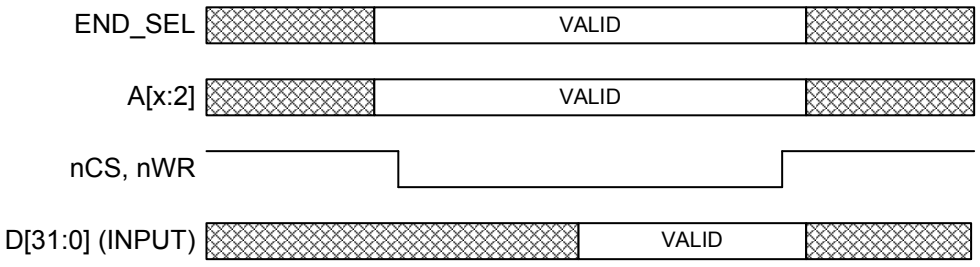


Figure 8.7 Functional Timing for PIO Write Operation

8.4.9 TX Data FIFO Direct PIO Writes

In this mode only A[2] is decoded, and any write to the LAN9312 will write the TX Data FIFO. This mode is enabled when FIFO_SEL is driven high during a write access. This is normally accomplished by connecting the FIFO_SEL signal to a high-order address line. This mode is useful when the host processor must increment its address when accessing the LAN9312.

Timing is identical to a PIO write, and the FIFO_SEL and END_SEL signals have the same timing characteristics as the address lines. A TX Data FIFO direct PIO write cycle begins when both nCS and nWR are asserted. Either or both of these control signals must de-assert between cycles for the period specified in Table 15.13, “TX Data FIFO Direct PIO Write Cycle Timing Values,” on page 452. The cycle ends when either or both nCS and nWR are de-asserted. They may be asserted and de-asserted in any order. The TX Data FIFO direct PIO write cycle is illustrated in the functional timing diagram in Figure 8.8.

Note: A[9:3] are ignored during TX Data FIFO direct PIO writes.

Please refer to Section 15.5.9, "TX Data FIFO Direct PIO Write Cycle Timing," on page 452 for the AC timing specifications for TX Data FIFO direct PIO write operations.

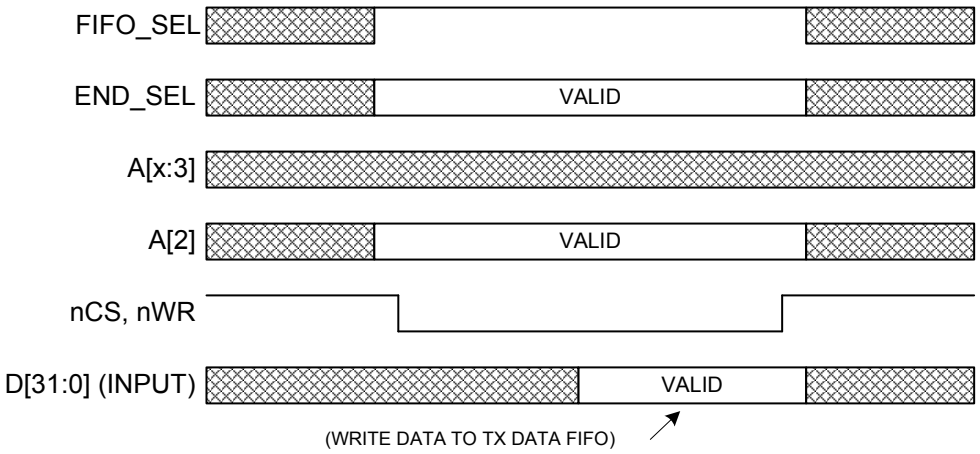


Figure 8.8 Functional Timing for TX Data FIFO Direct PIO Write Operation

8.5 HBI Interrupts

The HBI allows access to all interrupt configuration and status registers within the LAN9312. The LAN9312 implements a multi-tier interrupt hierarchy with the Interrupt Configuration Register (IRQ_CFG), Interrupt Status Register (INT_STS), and Interrupt Enable Register (INT_EN) at the top level. These registers allow for the configuration of which interrupts trigger the IRQ, as well as the IRQ deassertion and polarity properties. Interrupts may be generated from the 1588 Timestamping, Switch Fabric, Port 1 PHY, Port 2 PHY, Host MAC, EEPROM Loader, General Purpose Timer, General Purpose I/O, and Power Management blocks.

For more information of the LAN9312 interrupts, refer to Chapter 5, System Interrupts.

Chapter 9 Host MAC

9.1 Functional Overview

The Host MAC incorporates the essential protocol requirements for operating an Ethernet/IEEE 802.3-compliant node and provides an interface between the Host Bus Interface (HBI) and the Ethernet PHYs and Switch Fabric. On the front end, the Host MAC interfaces to the HBI via 2 sets of FIFO's (TX Data FIFO, TX Status FIFO, RX Data FIFO, RX Status FIFO). An additional bus is used to access the Host MAC CSR's via the Host MAC CSR Interface Command Register (MAC_CSR_CMD) and Host MAC CSR Interface Data Register (MAC_CSR_DATA) system registers.

The receive and transmit FIFO's allow increased packet buffer storage to the Host MAC. The FIFOs are a conduit between the HBI and the Host MAC through which all transmitted and received data and status information is passed. Deep FIFOs allow a high degree of latency tolerance relative to the various transport and OS software stacks reducing and minimizing overrun conditions. Both the Host MAC and the TX/RX FIFOs have separate receive and transmit data paths.

The Host MAC can store up to 250 Ethernet packets utilizing FIFOs, totaling 16KB, with a packet granularity of 4 bytes. This memory is shared by the RX and TX blocks and is configurable in terms of allocation via the Hardware Configuration Register (HW_CFG) register to the ranges described in Section 9.7.3, "FIFO Memory Allocation Configuration". This depth of buffer storage minimizes or eliminates receive overruns.

On the back end, the Host MAC interfaces with the 10/100 Ethernet PHY's (Virtual PHY, Port 1 PHY, Port 2 PHY) via an internal SMI (Serial Management Interface) bus. This allows the Host MAC access to the PHY's internal registers via the Host MAC MII Access Register (HMAC_MII_ACC) and Host MAC MII Data Register (HMAC_MII_DATA). The Host MAC interfaces to the Switch Engine Port 0 via an internal MII (Media Independent Interface) connection allowing for incoming and outgoing Ethernet packet transfers.

The Host MAC can operate at either 100Mbps or 10Mbps in both half-duplex or full-duplex modes. When operating in half-duplex mode, the Host MAC complies fully with Section 4 of ISO/IEC 8802-3 (ANSI/IEEE standard) and ANSI/IEEE 802.3 standards. When operating in full-duplex mode, the Host MAC complies with IEEE 802.3 full-duplex operation standard.

The Host MAC provides programmable enhanced features designed to minimize host supervision, bus utilization, and pre- or post-message processing. These features include the ability to disable retries after a collision, dynamic Frame Check Sequence (FCS) generation on a frame-by-frame basis, automatic pad field insertion and deletion to enforce minimum frame size attributes, and automatic retransmission and detection of collision frames. The Host MAC can sustain transmission or reception of minimally-sized back-to-back packets at full line speed with an interpacket gap (IPG) of 9.6 microseconds for 10 Mbps and 0.96 microseconds for 100 Mbps.

The primary attributes of the Host MAC are:

- Transmit and receive message data encapsulation
- Framing (frame boundary delimitation, frame synchronization)
- Error detection (physical medium transmission errors)
- Media access management
- Medium allocation (collision detection, except in full-duplex operation)
- Contention resolution (collision handling, except in full-duplex operation)
- Flow control during full-duplex mode
- Decoding of control frames (PAUSE command) and disabling the transmitter
- Generation of control frames
- Interface between the Host Bus Interface and the Ethernet PHYs/Switch Fabric.

9.2 Flow Control

The Host MAC supports full-duplex flow control using the pause operation and control frame. Half-duplex flow control using back pressure is also supported. The Host MAC flow control is configured via the memory mapped Host MAC Automatic Flow Control Configuration Register (AFC_CFG) located in the System CSR space and the Host MAC Flow Control Register (HMAC_FLOW) located in the Host MAC CSR space.

Note: The Host MAC controls the flow between the switch fabric and the Host MAC, not the network flow control. The switch fabric handles the network flow control independently.

9.2.1 Full-Duplex Flow Control

In full-duplex mode, flow control is achieved via the pause operation and the transmission of control frames. The pause operation inhibits transmission of data frames for a specified period of time. A pause operation consists of a frame containing the globally assigned multicast address (01-80-C2-00-00-01), the PAUSE opcode, and a parameter indicating the quantum of slot time (512 bit times) to inhibit data transmissions. The PAUSE parameter may range from 0 to 65,535 slot times. The Host MAC logic, upon receiving a frame with the reserved multicast address and PAUSE opcode, inhibits data frame transmissions for the length of time indicated. If a pause request is received while a transmission is in progress, the pause will take effect after the transmission is complete. Control frames are received, processed by the Host MAC, and passed on.

The Host MAC also has the capability of transmitting control frames (pause command) via hardware and software control. The software driver requests the Host MAC to transmit a control frame and gives the value of the PAUSE time to be used in the control frame. The Host MAC function constructs a control frame by setting the appropriate values in the corresponding fields (as defined in the 802.3 specification) and transmits the frame to the internal MII interface. The transmission of the control frame is not affected by the current state of the Pause timer value that may be set due to a recently received control frame.

9.2.2 Half-Duplex Flow Control (Backpressure)

In half-duplex mode, back pressure is used for flow control. Whenever the receive buffer/FIFO becomes full or crosses a certain threshold level, the Host MAC starts sending a jam signal. The Host MAC transmit logic enters a state at the end of current transmission (if any), where it waits for the beginning of a received frame. Once a new frame starts, the Host MAC starts sending the jam signal, which will result in a collision. After sensing the collision, the remote station will back off its transmission. The Host MAC continues sending the jam to make other stations defer transmission. The Host MAC only generates this collision-based back pressure when it receives a new frame, in order to avoid any late collisions.

9.3 Virtual Local Area Network (VLAN) Support

Virtual Local Area Networks (VLANs), as defined within the IEEE 802.3 standard, provide network administrators a means of grouping nodes within a larger network into broadcast domains. To implement a VLAN, four extra bytes are added to the basic Ethernet packet. As shown in Figure 9.1, the four bytes are inserted after the Source Address Field and before the Type/Length field. The first two bytes of the VLAN tag identify the tag, and by convention are set to the value 0x8100. The last two bytes identify the specific VLAN associated with the packet and provide a priority field.

The LAN9312 supports VLAN-tagged packets and provides two Host MAC registers, Host MAC VLAN1 Tag Register (HMAC_VLAN1) and Host MAC VLAN2 Tag Register (HMAC_VLAN2), which are used to identify VLAN-tagged packets. The HMAC_VLAN1 register is used to specify the VLAN1 tag which will increase the legal frame length from 1518 to 1522 bytes. The HMAC_VLAN2 register is used to specify the VLAN2 tag which will increase the legal frame length from 1518 to 1538 bytes. If a packet arrives bearing either of these tags in the two bytes succeeding the Source Address field, the controller will recognize the packet as a VLAN-tagged packet, allowing the packet to be received and processed

by the host software. If both VLAN1 and VLAN2 tag Identifiers are used, each should be unique. If both are set to the same value, VLAN1 is given higher precedence and the maximum legal frame length is set to 1522.

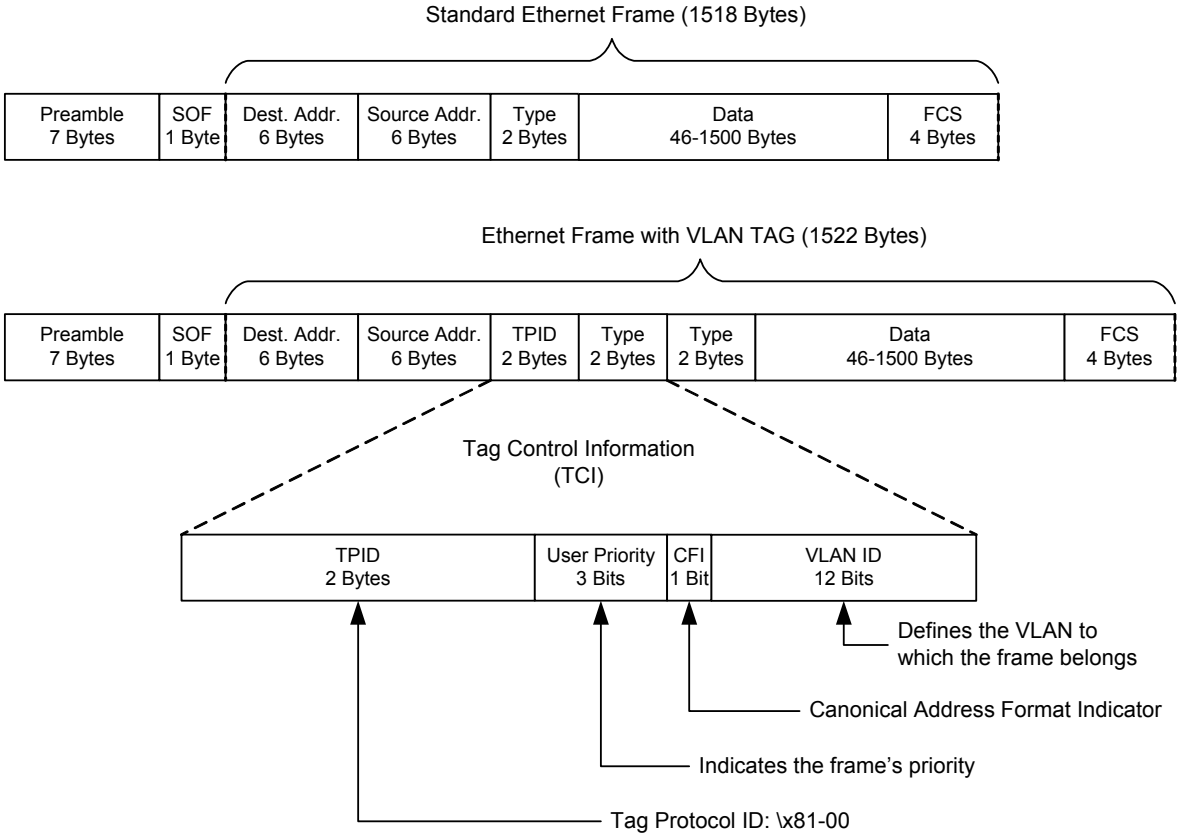


Figure 9.1 VLAN Frame

9.4 Address Filtering

The Ethernet address fields of an Ethernet packet consist of two 6-byte fields: one for the destination address and one for the source address. The first bit of the destination address signifies whether it is a physical address or a multicast address.

The Host MAC address check logic filters the frame based on the Ethernet receive filter mode that has been enabled. The various filter modes of the Host MAC are specified based on the state of the control bits in the Host MAC Control Register (HMAC_CR), as shown in Table 9.1. Please refer to the Section 14.3.1, "Host MAC Control Register (HMAC_CR)," on page 271 for more information on this register.

If the frame fails the filter, the Host MAC does not receive the packet. The host has the option of accepting or ignoring the packet.

Note: This filtering function is performed after any switch fabric filtering functions. The user must ensure the switch filtering is setup properly to allow packets to be passed to the Host MAC for further filtering.

Table 9.1 Address Filtering Modes

MCPAS	PRMS	INVFILT	HO	HPFILT	DESCRIPTION
0	0	0	0	0	MAC address perfect filtering only for all addresses.
0	0	0	0	1	MAC address perfect filtering for physical address and hash filtering for multicast addresses
0	0	0	1	1	Hash Filtering for physical and multicast addresses
0	0	1	0	0	Inverse Filtering
X	1	0	X	X	Promiscuous
1	0	0	0	X	Pass all multicast frames. Frames with physical addresses are perfect-filtered
1	0	0	1	1	Pass all multicast frames. Frames with physical addresses are hash-filtered

9.4.1 Perfect Filtering

This filtering mode passes only incoming frames whose destination address field exactly matches the value programmed into the Host MAC Address High Register (HMAC_ADDRH) and the Host MAC Address Low Register (HMAC_ADDRL). The MAC address is formed by the concatenation of these two registers.

9.4.2 Hash Only Filtering

This type of filtering checks for incoming receive packets (from switch Port 0) with either multicast or physical destination addresses, and executes an imperfect address filtering against the hash table. The hash table is formed by merging the values in the Host MAC Multicast Hash Table High Register (HMAC_HASHH) and the Host MAC Multicast Hash Table Low Register (HMAC_HASHL) to form a 64-bit hash table.

During imperfect hash filtering, the upper 6-bits of the destination address of the incoming frame are used to index the contents of the hash table. The most significant bit of the destination address determines the register to be used (HMAC_HASHH or HMAC_HASHL), while the other five bits determine the bit within the register. A value of 00000 selects Bit 0 of the HMAC_HASHL register and a value of 11111 selects Bit 31 of the HMAC_HASHH register.

9.4.3 Hash Perfect Filtering

In hash perfect filtering, if the received frame is a physical address, the Host MAC packet filter will perfect-filter the incoming frame's destination field with the value programmed into the Host MAC Address High Register (HMAC_ADDRH) and the Host MAC Address Low Register (HMAC_ADDRL). However, if the incoming frame is a multicast frame, the Host MAC packet filter function performs an imperfect address filtering against the hash table.

The imperfect filtering against the hash table is the same imperfect filtering process described in Section 9.4.2, "Hash Only Filtering".

9.4.4 Inverse Filtering

In inverse filtering, the Host MAC packet filter accepts incoming frames (from switch Port 0) with a destination address not matching the perfect address (i.e., the value programmed into the Host MAC Address High Register (HMAC_ADDRH) and the Host MAC Address Low Register (HMAC_ADDRL)) and rejects frames with destination addresses matching the perfect address.

For all filtering modes, when the MCPAS bit of the Host MAC Control Register (HMAC_CR) is set, all multicast frames are accepted. When the PRMS bit is set, all frames are accepted regardless of their destination address. This includes all broadcast frames as well.

9.5 Wake-up Frame Detection

Setting the Wake-Up Frame Enable bit (WUEN) in the Host MAC Wake-up Control and Status Register (HMAC_WUCSR), places the Host MAC in the wake-up frame detection mode. In this mode, normal data reception is disabled, and detection logic within the Host MAC examines received data for the pre-programmed wake-up frame patterns. The Host MAC can be programmed to notify the host of the wake-up frame detection with the assertion of the host interrupt (IRQ) or power management event (PME) signal. Upon detection, the Wake-Up Frame Received bit (WUFR) in the HMAC_WUCSR register is set. When the host clears the WUEN bit, the Host MAC will resume normal receive operation.

Before putting the Host MAC into the wake-up frame detection state, the host must provide the detection logic with a list of sample frames and their corresponding byte masks. This information must be written into the Host MAC Wake-up Frame Filter Register (HMAC_WUFF). The wake-up frame filter is configured through this register using an index mechanism. After power-on reset, hardware reset, or soft reset, the Host MAC loads the first value written to the HMAC_WUFF register to the first DWORD in the wake-up frame filter (filter 0 byte mask). The second value written to this register is loaded to the second DWORD in the wake-up frame filter (filter 1 byte mask) and so on for all eight DWORDs. The wake-up frame filter functionally is described below.

The Host MAC supports four programmable wake-up filters that support many different receive packet patterns. If remote wake-up mode is enabled, the remote wake-up function receives all frames addressed to the Host MAC. It then checks each frame against the enabled filter and recognizes the frame as a remote wake-up frame if it passes the wakeup frame filter register's address filtering and CRC value match.

In order to determine which bytes of the frames should be checked by the CRC module, the Host MAC uses a programmable byte mask and a programmable pattern offset for each of the four supported filters.

The pattern's offset defines the location of the first byte that should be checked in the frame. Since the destination address is checked by the address filtering function, the pattern offset is always greater than 12.

The byte mask is a 31-bit field that specifies whether or not each of the 31 contiguous bytes within the frame, beginning in the pattern offset, should be checked. If bit j in the byte mask is set, the detection logic checks byte offset +j in the frame. In order to load the wake-up frame filter, the host must perform eight writes to the Host MAC Wake-up Frame Filter Register (HMAC_WUFF). Table 9.2 shows the wake-up frame filter register's structure.

Note: The switch fabric must be configured to pass wake-up packets to the Host MAC for this function to operate properly.

Note: When wake-up frame detection is enabled via the WUEN bit of the Host MAC Wake-up Control and Status Register (HMAC_WUCSR), a broadcast wake-up frame will wake-up the device despite the state of the Disable Broadcast Frames (BCAST) bit in the Host MAC Control Register (HMAC_CR).

Table 9.2 Wake-Up Frame Filter Register Structure

Filter 0 Byte Mask							
Filter 1 Byte Mask							
Filter 2 Byte Mask							
Filter 3 Byte Mask							
Reserved	Filter 3 Command	Reserved	Filter 2 Command	Reserved	Filter 1 Command	Reserved	Filter 0 Command
Filter 3 Offset		Filter 2 Offset		Filter 1Offset		Filter 0 Offset	
Filter 1 CRC-16				Filter 0 CRC-16			
Filter 3 CRC-16				Filter 2 CRC-16			

The Filter i Byte Mask defines which incoming frame bytes Filter i will examine to determine whether or not this is a wake-up frame. Table 9.3, describes the byte mask's bit fields.

Table 9.3 Filter i Byte Mask Bit Definitions

FILTER I BYTE MASK DESCRIPTION	
FIELD	**DESCRIPTION**
31	Must be zero (0)
30:0	**Byte Mask:** If bit j of the byte mask is set, the CRC machine processes byte number pattern - (offset + j) of the incoming frame. Otherwise, byte pattern - (offset + j) is ignored.

The Filter i command register controls Filter i operation. Table 9.4 shows the Filter i command register.

Table 9.4 Filter i Command Bit Definitions

FILTER i COMMANDS	
FIELD	**DESCRIPTION**
3	**Address Type:** Defines the destination address type of the pattern. When bit is set, the pattern applies only to multicast frames. When bit is cleared, the pattern applies only to unicast frames.
2:1	**RESERVED**
0	**Enable Filter:** When bit is set, Filter i is enabled, otherwise, Filter i is disabled.

The Filter i Offset register defines the offset in the frame's destination address field from which the frames are examined by Filter i. Table 9.5 describes the Filter i Offset bit fields.

Table 9.5 Filter i Offset Bit Definitions

FILTER i OFFSET DESCRIPTION	
FIELD	**DESCRIPTION**
7:0	**Pattern Offset:** The offset of the first byte in the frame on which CRC is checked for wake-up frame recognition. The minimum value of this field must be 12 since there should be no CRC check for the destination address and the source address fields. The Host MAC checks the first offset byte of the frame for CRC and checks to determine whether the frame is a wake-up frame. Offset 0 is the first byte of the incoming frame's destination address.

The Filter i CRC-16 register contains the CRC-16 result of the frame that should pass Filter i.

Table 9.6 describes the Filter i CRC-16 bit fields.

Table 9.6 Filter i CRC-16 Bit Definitions

FILTER i CRC-16 DESCRIPTION	
FIELD	**DESCRIPTION**
15:0	**Pattern CRC-16:** This field contains the 16-bit CRC value from the pattern and the byte mask programmed to the wake-up filter register function. This value is compared against the CRC calculated on the incoming frame, and a match indicates the reception of a wakeup frame.

9.5.1 Magic Packet Detection

Setting the Magic Packet Enable bit (MPEN) in the Host MAC Wake-up Control and Status Register (HMAC_WUCSR) places the Host MAC in the "Magic Packet" detection mode. In this mode, normal data reception is disabled, and detection logic within the Host MAC examines received data for a Magic Packet. The LAN9312 can be programmed to notify the host of the "Magic Packet" detection with the assertion of the host interrupt (IRQ) or power management event signal (PME). Upon detection, the Magic Packet Received bit (MPR) in the HMAC_WUCSR register is set. When the host clears the MPEN bit, the Host MAC will resume normal receive operation. Please refer to Section 14.3.12, "Host MAC Wake-up Control and Status Register (HMAC_WUCSR)," on page 285 for additional information on this register.

In Magic Packet mode, the Host MAC constantly monitors each frame addressed to the node for a specific Magic Packet pattern. Only packets matching the Host MAC address or broadcast address are checked for the Magic Packet requirements. Once the address requirement has been met, the Host MAC checks the received frame for the pattern 48'hFF_FF_FF_FF_FF_FF after the destination and source address field. The Host MAC then looks in the frame for 16 repetitions of the Host MAC address without any breaks or interruptions. In case of a break in the 16 address repetitions, the Host MAC again scans for the 48'hFF_FF_FF_FF_FF_FF pattern in the incoming frame. The 16 repetitions may be anywhere in the frame but must be preceded by the synchronization stream. The device will also accept a multicast frame, as long as it detects the 16 duplications of the Host MAC address.

For example, if the Host MAC address is 00h 11h 22h 33h 44h 55h, then the MAC scans for the following data sequence in an Ethernet frame:

Destination Address Source Address ……FF FF FF FF FF FF

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

…CRC

Note: The switch fabric must be configured to pass magic packets to the Host MAC for this function to operate properly.

9.6 Host MAC Address

The Host MAC address is configured via the Host MAC Address Low Register (HMAC_ADDRL) and Host MAC Address High Register (HMAC_ADDRH). These registers contain the 48-bit physical address of the Host MAC. The contents of these registers may be loaded directly by the host, or optionally, by the EEPROM Loader from EEPROM at power-on (if a programmed EEPROM is detected). The MAC address value loaded by the EEPROM Loader into the Host MAC address registers (for host packet unicast qualification), is also loaded into the Switch Fabric MAC address registers (for pause packet / flow control): Switch Fabric MAC Address Low Register (SWITCH_MAC_ADDRL) and Switch Fabric MAC Address High Register (SWITCH_MAC_ADDRH). These two sets of registers are loaded simultaneously via the same EEPROM byte addresses.

Table 9.7 below illustrates the byte ordering of the HMAC_ADDRL/SWITCH_MAC_ADDRL and HMAC_ADDRH/SWITCH_MAC_ADDRH registers with respect to the reception of the Ethernet physical address. Also shown is the correlation between the EEPROM addresses and HMAC_ADDRL/SWITCH_MAC_ADDRL and HMAC_ADDRH/SWITCH_MAC_ADDRH registers.

Table 9.7 EEPROM Byte Ordering and Register Correlation

EEPROM Address	Register Locations Written	Order of Reception on Ethernet
01h	HMAC_ADDRL[7:0] SWITCH_MAC_ADDRL[7:0]	1st
02h	HMAC_ADDRL[15:8] SWITCH_MAC_ADDRL[15:8]	2nd
03h	HMAC_ADDRL[23:16] SWITCH_MAC_ADDRL[23:16]	3rd
04h	HMAC_ADDRL[31:24] SWITCH_MAC_ADDRL[31:24]	4th
05h	HMAC_ADDRH[7:0] SWITCH_MAC_ADDRH[7:0]	5th
06h	HMAC_ADDRH[15:8] SWITCH_MAC_ADDRH[15:8]	6th

For example, if the desired Ethernet physical address is 12-34-56-78-9A-BC, the HMAC_ADDRL and HMAC_ADDRH registers would be programmed as shown in Figure 9.2. The values required to automatically load this configuration from the EEPROM are also shown.

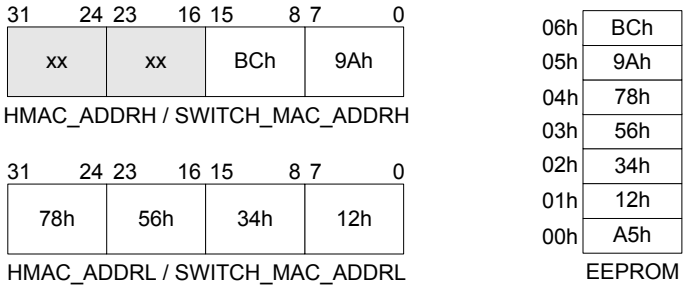


Figure 9.2 Example EEPROM MAC Address Setup

Note: By convention, the right nibble of the left most byte of the Ethernet address (in this example, the 2 of the 12h) is the most significant nibble and is transmitted/received first.

For more information on the EEPROM and EEPROM Loader, refer to Section 10.2, "I2C/Microwire Master EEPROM Controller," on page 137.

9.7 FIFOs

The LAN9312 contains four host-accessible FIFOs (TX Status, RX Status, TX Data, and RX Data) and two internal inaccessible Host MAC TX/RX MIL FIFO's (TX MIL FIFO, RX MIL FIFO).

9.7.1 TX/RX FIFOs

The TX/RX Data and Status FIFOs store the incoming and outgoing address and data information, acting as a conduit between the host bus interface (HBI) and the Host MAC. The sizes of these FIFOs are configurable via the Hardware Configuration Register (HW_CFG) register to the ranges described in Table 9.8. Refer to Section 9.7.3, "FIFO Memory Allocation Configuration" for additional information. The the RX and TX FIFOs related register definitions can be found in section Section 14.2.2, "Host MAC & FIFO's".

The TX and RX Data FIFOs have the base address of 00h and 20h respectively. However, each FIFO is also accessible at seven additional contiguous memory locations, as can be seen in Figure 14.1. The Host may access the TX or RX Data FIFOs at any of these alias port locations, as they all function identically and contain the same data. This alias port addressing is implemented to allow hosts to burst through sequential addresses.

The TX and RX Status FIFOs can each be read from two register locations; the Status FIFO Port, and the Status FIFO PEEK. The TX and RX Status FIFO Ports (48h and 40h respectively) will perform a destructive read, popping the data from the TX or RX Status FIFO. The TX and RX Status FIFO PEEK register locations (4Ch and 44h respectively) allow a non-destructive read of the top (oldest) location of the FIFOs.

Proper use of the The TX/RX Data and Status FIFOs, including the correct data formatting is described in detail in Section 9.8, "TX Data Path Operation," on page 122 and Section 9.9, "RX Data Path Operation," on page 132.

9.7.2 MIL FIFOs

The MAC Interface Layer (MIL), within the Host MAC, contains a 2KB transmit and a 128 Byte receive FIFO which are separate from the TX and RX FIFOs. These MIL FIFOs are not directly accessible from the HBI. The differentiation between the TX/RX FIFOs and the TX/RX MIL FIFOs is that once the transmit or receive packets are in the MIL FIFOs, the host no longer can control or access the TX or RX data. The MIL FIFOs are essentially the working buffers of the Host MAC logic. In the case of

reception, the data must be moved into the RX FIFOs before the host can access the data. For TX operations, the MIL operates in store-and-forward mode and will queue an entire frame before beginning transmission.

As space in the TX MIL FIFO frees, data is moved into it from the TX Data FIFO. Depending on the size of the frames to be transmitted, the Host MAC can hold up to two Ethernet frames. This is in addition to any TX data that may be queued in the TX Data FIFO.

Conversely, as data is received, it is moved from the Host MAC to the RX MIL FIFO, and then into the RX Data FIFO. When the RX Data FIFO fills up, data will continue to collect in the RX MIL FIFO. If the RX MIL FIFO fills up and overruns, subsequent RX frames will be lost until room is made in the RX Data FIFO. For each frame of data that is lost, the Host MAC RX Dropped Frames Counter Register (RX_DROP) is incremented.

RX and TX MIL FIFO levels are not visible to the host processor and operate independent of the TX/RX FIFOs. FIFO levels set for the TX/RX Data and Status FIFOs do not take into consideration the MIL FIFOs.

9.7.3 FIFO Memory Allocation Configuration

TX and RX FIFO space is configurable through the Hardware Configuration Register (HW_CFG). The user must select the FIFO allocation by setting the TX FIFO Size (TX_FIF_SZ) field in the Hardware Configuration Register (HW_CFG). The TX_FIF_SZ field selects the total allocation for the TX data path, including the TX Status FIFO size. The TX Status FIFO size is fixed at 512 Bytes (128 TX Status DWORDs). The TX Status FIFO length is subtracted from the total TX FIFO size with the remainder being the TX Data FIFO Size. The minimum size of the TX FIFOs is 2KB (TX Data and TX Status FIFOs combined). Note that TX Data FIFO space includes both commands and payload data.

RX FIFO Size is the remainder of the unallocated FIFO space (16384 bytes – TX FIFO Size). The RX Status FIFO size is always equal to 1/16 of the RX FIFO size. The RX Status FIFO length is subtracted from the total RX FIFO size with the remainder being the RX Data FIFO Size.

For example, if TX_FIF_SZ = 6 then:

Total TX FIFO Size = 6144 Bytes (6KB)

TX Status FIFO Size = 512 Bytes (Fixed)

TX Data FIFO Size = 6144 – 512 = 5632 Bytes

RX FIFO Size = 16384 – 6144 = 10240 Bytes (10KB)

RX Status FIFO Size = 10240 / 16 = 640 Bytes (160 RX Status DWORDs)

RX Data FIFO Size = 10240 – 640 = 9600 Bytes

Table 9.8 contains an overview of the configurable TX/RX FIFO sizes and defaults. Table 9.9 shows every valid setting for the TX_FIF_SZ field and the resulting FIFO sizes. Note that settings not shown in this table are reserved and should not be used.

Note: The RX Data FIFO is considered full 4 DWORDs before the length that is specified in the HW_CFG register.

Table 9.8 TX/RX FIFO Configurable Sizes

FIFO	SIZE RANGE	DEFAULT
TX Status	512	512
RX Status	128-892	704
TX Data	1536-13824	4608
RX Data	1920-13440	10560

Table 9.9 Valid TX/RX FIFO Allocations

TX_FIF_SZ	TX DATA FIFO SIZE (BYTES)	TX STATUS FIFO SIZE (BYTES)	RX DATA FIFO SIZE (BYTES)	RX STATUS FIFO SIZE (BYTES)
2	1536	512	13440	896
3	2560	512	12480	832
4	3584	512	11520	768
5	4608	512	10560	704
6	5632	512	9600	640
7	6656	512	8640	576
8	7680	512	7680	512
9	8704	512	6720	448
10	9728	512	5760	384
11	10752	512	4800	320
12	11776	512	3840	256
13	12800	512	2880	192
14	13824	512	1920	128

9.8 TX Data Path Operation

Data is queued for transmission by writing it into the TX Data FIFO. Each packet to be transmitted may be divided among multiple buffers. Each buffer starts with a two DWORD TX command (TX command ‘A’ and TX command ‘B’). The TX command instructs the LAN9312 on the handling of the associated buffer. Packet boundaries are delineated using control bits within the TX command.

The host provides a 16-bit Packet Tag field in the TX command. The Packet Tag value is appended to the corresponding TX status DWORD. All Packet Tag fields must have the same value for all buffers in a given packet. If tags differ between buffers in the same packet the TXE error will be asserted. Any value may be chosen for a Packet Tag as long as all tags in the same Packet are identical. Packet Tags also provide a method of synchronization between transmitted packets and their associated status. Software can use unique Packet Tags to assist with validating matching status completions.

Note: The use of Packet Tags is not required by the hardware. This field can be used by the LAN software driver for any application. Packet Tags is only one application example.

The Packet Length field in the TX command specifies the number of bytes in the associated packet. All Packet Length fields must have the same value for all buffers in a given packet. Hardware compares the Packet Length field and the actual amount of data received by the Ethernet controller. If the actual packet length count does not match the Packet Length field as defined in the TX command, the Transmitter Error (TXE) flag is asserted.

The LAN9312 can be programmed to start payload transmission of a buffer on a byte boundary by setting the “Data Start Offset” field in the TX command. The “Data Start Offset” field points to the actual start of the payload data within the first 8 DWORDs of the buffer. Data before the “Data Start Offset” pointer will be ignored. When a packet is split into multiple buffers, each successive buffer may begin on any arbitrary byte.

The LAN9312 can be programmed to strip padding from the end of a transmit packet in the event that the end of the packet does not align with the host burst boundary. This feature is necessary when the LAN9312 is operating in a system that always performs multi-word bursts. In such cases the LAN9312 must guarantee that it can accept data in multiples of the Burst length regardless of the actual packet length. When configured to do so, the LAN9312 will accept extra data at the end of the packet and will remove the extra padding before transmitting the packet. The LAN9312 automatically removes data up to the boundary specified in the Buffer End Alignment field specified in each TX command.

The host can instruct the LAN9312 to issue an interrupt when the buffer has been fully loaded into the TX FIFO contained in the LAN9312 and transmitted. This feature is enabled through the TX command 'Interrupt on Completion' field.

Upon completion of transmission, irrespective of success or failure, the status of the transmission is written to the TX Status FIFO. TX status is available to the host and may be read using PIO operations. An interrupt can be optionally enabled by the host to indicate the availability of a programmable number TX status DWORDS.

Before writing the TX command and payload data to the TX FIFO, the host must check the available TX FIFO space by performing a PIO read of the TX FIFO Information Register (TX_FIFO_INF). The host must ensure that it does not overfill the TX FIFO or the TX Error (TXE) flag will be asserted.

The host proceeds to write the TX command by first writing TX command 'A', then TX command 'B'. After writing the command, the host can then move the payload data into the TX FIFO. TX status DWORDs are stored in the TX Status FIFO to be read by the host at a later time upon completion of the data transmission onto the wire.

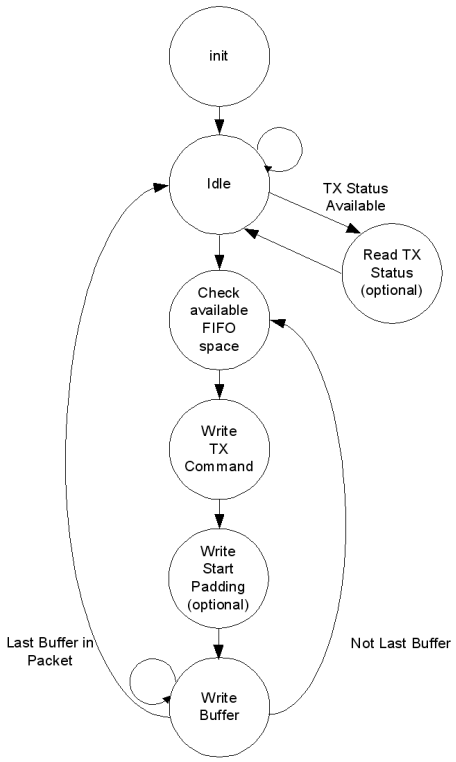


Figure 9.3 Simplified Host TX Flow Diagram

9.8.1 TX Buffer Format

TX buffers exist in the host's memory in a given format. The host writes a TX command word into the TX data buffer before moving the Ethernet packet data. The TX command A and command B are 32-bit values that are used by the LAN9312 in the handling and processing of the associated Ethernet packet data buffer. Buffer alignment, segmentation and other packet processing parameters are included in the command structure. The buffer format is illustrated in Figure 9.4.

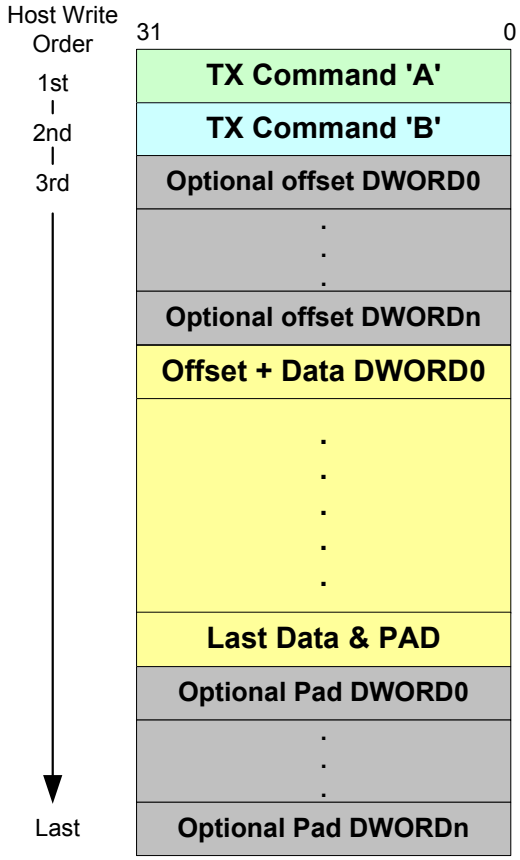


Figure 9.4 TX Buffer Format

Figure 9.4 shows the TX Buffer as it is written into the LAN9312. It should be noted that not all of the data shown in this diagram is actually stored in the TX Data FIFO. This must be taken into account when calculating the actual TX Data FIFO usage. Please refer to Section 9.8.5, "Calculating Actual TX Data FIFO Usage" for a detailed explanation on calculating the actual TX Data FIFO usage.

9.8.2 TX Command Format

The TX command instructs the TX FIFO controller on handling the subsequent buffer. The command precedes the data to be transmitted. The TX command is divided into two, 32-bit words; TX command 'A' and TX command 'B'.

There is a 16-bit Packet Tag in the TX command 'B' command word. Packet Tags may, if host software desires, be unique for each packet (i.e., an incrementing count). The value of the tag will be returned in the TX status word for the associated packet. The Packet tag can be used by host software to uniquely identify each status word as it is returned to the host.

Both TX command ‘A’ and TX command ‘B’ are required for each buffer in a given packet. TX command ‘B’ must be identical for every buffer in a given packet. If the TX command ‘B’ words do not match, the Ethernet controller will assert the Transmitter Error (TXE) flag.

9.8.2.1 TX Command ‘A’

Table 9.10 TX Command 'A' Format

BITS	DESCRIPTION
31	**Interrupt on Completion (IOC).** When set, the TX_IOC bit will be asserted in the Interrupt Status Register (INT_STS) when the current buffer has been fully loaded into the TX FIFO.
30:26	**Reserved.** These bits are reserved. Always write zeros to this field to guarantee future compatibility.
25:24	**Buffer End Alignment.** This field specifies the alignment that must be maintained on the last data transfer of a buffer. The host will add extra DWORDs of data up to the alignment specified in the table below. The LAN9312 will remove the extra DWORDs. This mechanism can be used to maintain cache line alignment on host processors. [25] / [24] / End Alignment 0 / 0 / 4-byte alignment 0 / 1 / 16-byte alignment 1 / 0 / 32-byte alignment 1 / 1 / Reserved
23:21	**Reserved.** These bits are reserved. Always write zeros to this field to guarantee future compatibility
20:16	**Data Start Offset (bytes).** This field specifies the offset of the first byte of TX data. The offset value can be anywhere from 0 bytes to a 31 byte offset.
15:14	**Reserved.** These bits are reserved. Always write zeros to this field to guarantee future compatibility
13	**First Segment (FS).** When set, this bit indicates that the associated buffer is the first segment of the packet.
12	**Last Segment.** When set, this bit indicates that the associated buffer is the last segment of the packet
11	**Reserved.** These bits are reserved. Always write zeros to this field to guarantee future compatibility.
10:0	**Buffer Size (bytes).** This field indicates the number of bytes contained in the buffer following this command. This value, along with the Buffer End Alignment field, is read and checked by the LAN9312 and used to determine how many extra DWORDs were added to the end of the Buffer. A running count is also maintained in the LAN9312 of the cumulative buffer sizes for a given packet. This cumulative value is compared against the Packet Length field in the TX command ‘B’ word and if they do not correlate, the TXE flag is set. **Note:** The buffer size specified does not include the buffer end alignment padding or data start offset added to a buffer.

9.8.2.2 TX Command ‘B’

Table 9.11 TX Command 'B' Format

BITS	DESCRIPTION
31:16	**Packet Tag.** The host should write a unique packet identifier to this field. This identifier is added to the corresponding TX status word and can be used by the host to correlate TX status words with their corresponding packets. **Note:** The use of packet tags is not required by the hardware. This field can be used by the LAN software driver for any application. Packet Tags is one application example.
15:14	**Reserved.** These bits are reserved. Always write zeros to this field to guarantee future compatibility.
13	**Add CRC Disable.** When set, the automatic addition of the CRC is disabled.
12	**Disable Ethernet Frame Padding.** When set, this bit prevents the automatic addition of padding to an Ethernet frame of less than 64 bytes. The CRC field is also added despite the state of the Add CRC Disable field.
11	**Reserved.** These bits are reserved. Always write zeros to this field to guarantee future compatibility.
10:0	**Packet Length (bytes).** This field indicates the total number of bytes in the current packet. This length does not include the offset or padding. If the Packet Length field does not match the actual number of bytes in the packet the Transmitter Error (TXE) flag will be set.

9.8.3 TX Data Format

The TX data section begins at the third DWORD in the TX buffer (after TX command ‘A’ and TX command ‘B’). The location of the first byte of valid buffer data to be transmitted is specified in the “Data Start Offset” field of the TX command ‘A’ word. Table 9.12, "TX DATA Start Offset", shows the correlation between the setting of the LSB’s in the “Data Start Offset” field and the byte location of the first valid data byte. Additionally, transmit buffer data can be offset by up to 7 additional DWORDS as indicated by the upper three MSB’s (5:2) in the “Data Start Offset” field.

Table 9.12 TX DATA Start Offset

Data Start Offset [1:0]:	11	10	01	00
First TX Data Byte:	D[31:24]	D[23:16]	D[15:8]	D[7:0]

TX data is contiguous until the end of the buffer. The buffer may end on a byte boundary. Unused bytes at the end of the packet will not be sent to the Host MAC Interface Layer for transmission.

The Buffer End Alignment field in TX command ‘A’ specifies the alignment that must be maintained for the associated buffer. End alignment may be specified as 4-, 16-, or 32-byte. The host processor is responsible for adding the additional data to the end of the buffer. The hardware will automatically remove this extra data.

9.8.3.1 TX Buffer Fragmentation Rules

Transmit buffers must adhere to the following rules:

- Each buffer can start and end on any arbitrary byte alignment
- The first buffer of any transmit packet can be any length
- Middle buffers (i.e., those with First Segment = Last Segment = 0) must be greater than, or equal to 4 bytes in length
- The final buffer of any transmit packet can be any length

The MIL operates in store-and-forward mode and has specific rules with respect to fragmented packets. The total space consumed in the TX MIL FIFO must be limited to no more than 2KB - 3 DWORDs (2,036 bytes total). Any transmit packet that is so highly fragmented that it takes more space than this must be un-fragmented (by copying to a driver-supplied buffer) before the transmit packet can be sent to the LAN9312.

One approach to determine whether a packet is too fragmented is to calculate the actual amount of space that it will consume, and check it against 2,036 bytes. Another approach is to check the number of buffers against a worst-case limit of 86 (see explanation below).

9.8.3.2 Calculating Worst-Case TX MIL FIFO Usage

The actual space consumed by a buffer in the TX MIL FIFO consists only of any partial DWORD offsets in the first/last DWORD of the buffer, plus all of the whole DWORDs in between. Any whole DWORD offsets and/or alignments are stripped off before the buffer is loaded into the TX Data FIFO, and TX command words are stripped off before the buffer is written to the TX MIL FIFO, so none of those DWORDs count as space consumed. The worst-case overhead for a TX buffer is 6 bytes, which assumes that it started on the high byte of a DWORD and ended on the low byte of a DWORD. A TX packet consisting of 86 such fragments would have an overhead of 516 bytes (6 * 86) which, when added to a 1514-byte max-size transmit packet (1516 bytes, rounded up to the next whole DWORD), would give a total space consumption of 2,032 bytes, leaving 4 bytes to spare; this is the basis for the "86 fragment" rule mentioned above. For more information on the MIL FIFO's refer to Section 9.7.2, "MIL FIFOs," on page 120.

9.8.4 TX Status Format

TX status is passed to the host CPU through a separate FIFO mechanism. A status word is returned for each packet transmitted. Data transmission is suspended if the TX Status FIFO becomes full. Data transmission will resume when the host reads the TX status and there is room in the FIFO for more “TX Status” data.

The host can optionally choose to not read the TX status. The TX status can be ignored by setting the “TX Status Discard Allow Overrun Enable” (TXSAO) bit in the Transmit Configuration Register (TX_CFG). If this option is chosen TX status will not be written to the FIFO. Setting this bit high allows the transmitter to continue operation with a full TX Status FIFO. In this mode the status information is still available in the TX Status FIFO, and TX status interrupts still function. In the case of an overrun, the TXSUSED counter will stay at zero and no further TX status will be written to the TX Status FIFO until the host frees space by reading TX status. If TXSAO is enabled, a TXE error will not be generated if the TX Status FIFO overruns. In this mode the host is responsible for re-synchronizing TX status in the case of an overrun.

Note: Though the Host MAC is communicating locally with the switch fabric MAC, the events described in the TX Status word may still occur.

BITS	DESCRIPTION
31:16	**Packet TAG.** Unique identifier written by the host into the Packet Tag field of the TX command ‘B’ word. This field can be used by the host to correlate TX status words with the associated TX packets.
15	**Error Status (ES).** When set, this bit indicates that the Ethernet controller has reported an error. This bit is the logical OR of bits 11, 10, 9, 8, 2, 1 in this status word.
14:12	**Reserved.** These bits are reserved. Always write zeros to this field to guarantee future compatibility.
11	**Loss of Carrier.** When set, this bit indicates the loss of carrier during transmission.
10	**No Carrier.** When set, this bit indicates that the carrier signal from the transceiver was not present during transmission.

BITS	DESCRIPTION
9	**Late Collision.** When set, indicates that the packet transmission was aborted after the collision window of 64 bytes.
8	**Excessive Collisions.** When set, this bit indicates that the transmission was aborted after 16 collisions while attempting to transmit the current packet.
7	**Reserved.** This bit is reserved. Always write zeros to this field to guarantee future compatibility.
6:3	**Collision Count.** This counter indicates the number of collisions that occurred before the packet was transmitted. It is not valid when excessive collisions (bit 8) is also set.
2	**Excessive Deferral.** If the deferred bit is set in the control register, the setting of the excessive deferral bit indicates that the transmission has ended because of a deferral of over 24288 bit times during transmission.
1	**Reserved.** This bit is reserved. Always write zeros to this field to guarantee future compatibility
0	**Deferred.** When set, this bit indicates that the current packet transmission was deferred.

9.8.5 Calculating Actual TX Data FIFO Usage

The following rules are used to calculate the actual TX Data FIFO space consumed by a TX Packet:

- TX command 'A' is stored in the TX Data FIFO for every TX buffer
- TX command 'B' is written into the TX Data FIFO when the First Segment (FS) bit is set in TX command 'A'
- Any DWORD-long data added as part of the “Data Start Offset” is removed from each buffer before the data is written to the TX Data FIFO. Any data that is less than 1 DWORD is passed to the TX Data FIFO.
- Payload from each buffer within a Packet is written into the TX Data FIFO.
- Any DWORD-long data added as part of the End Padding is removed from each buffer before the data is written to the TX Data FIFO. Any end padding that is less than 1 DWORD is passed to the TX Data FIFO

9.8.6 Transmit Examples

9.8.6.1 TX Example 1

In this example a single, 111-Byte Ethernet packet will be transmitted. This packet is divided into three buffers. The three buffers are as follows:

Buffer 0:

- 7-Byte “Data Start Offset”
- 79-Bytes of payload data
- 16-Byte “Buffer End Alignment”

Buffer 1:

- 0-Byte “Data Start Offset”
- 15-Bytes of payload data
- 16-Byte “Buffer End Alignment”

Buffer 2:

- 10-Byte “Data Start Offset”
- 17-Bytes of payload data
- 16-Byte “Buffer End Alignment”

Figure 9.5 illustrates the TX command structure for this example, and also shows how data is passed to the TX Data FIFO.

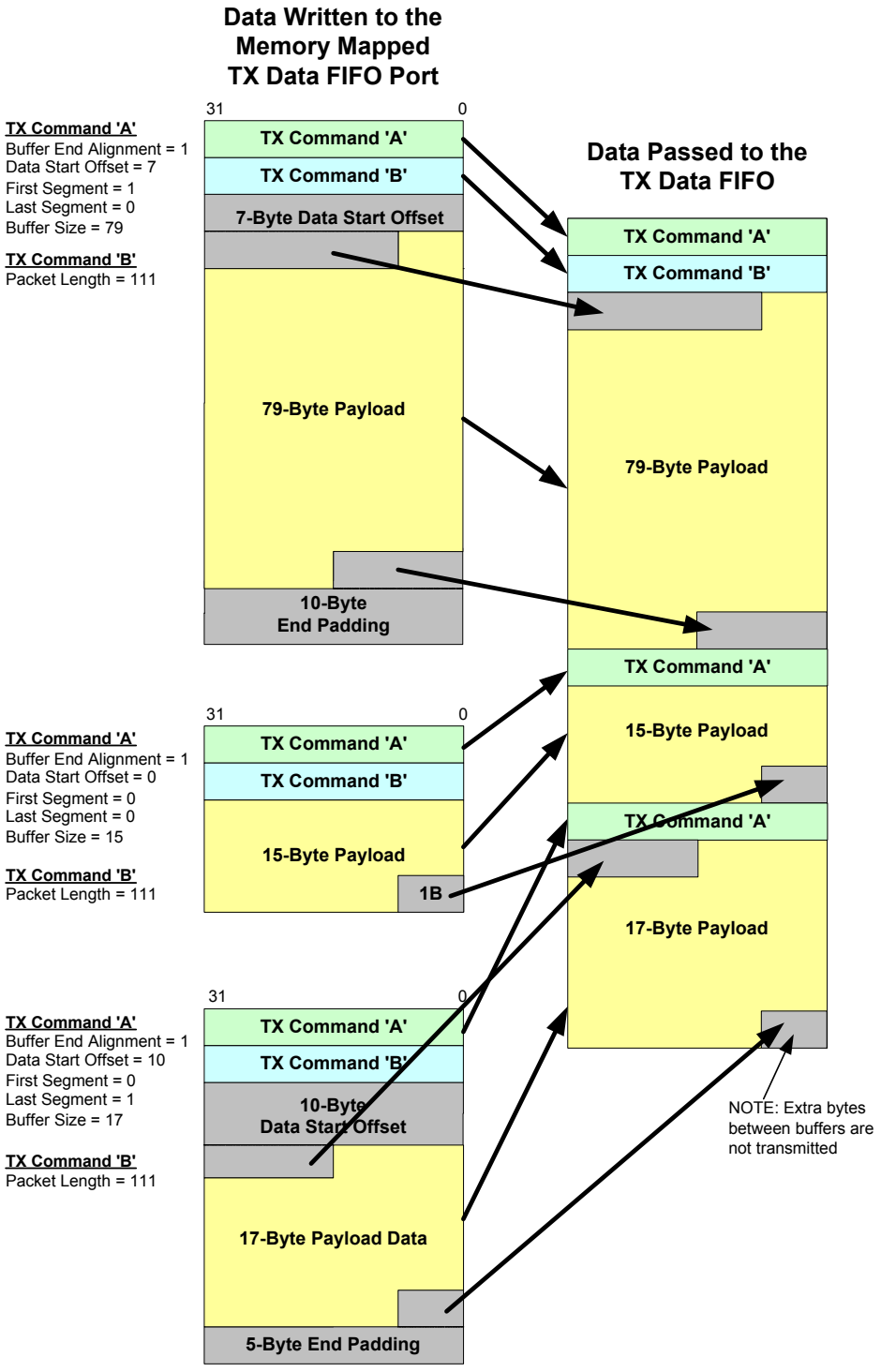


Figure 9.5 TX Example 1

9.8.6.2 TX Example 2

In this example, a single 183-Byte Ethernet packet will be transmitted. This packet is in a single buffer as follows:

- 2-Byte “Data Start Offset”
- 183-Bytes of payload data
- 4-Byte “Buffer End Alignment”

Figure 9.6 illustrates the TX command structure for this example, and also shows how data is passed to the TX Data FIFO. Note that the packet resides in a single TX Buffer, therefore both the FS and LS bits are set in TX command ‘A’.

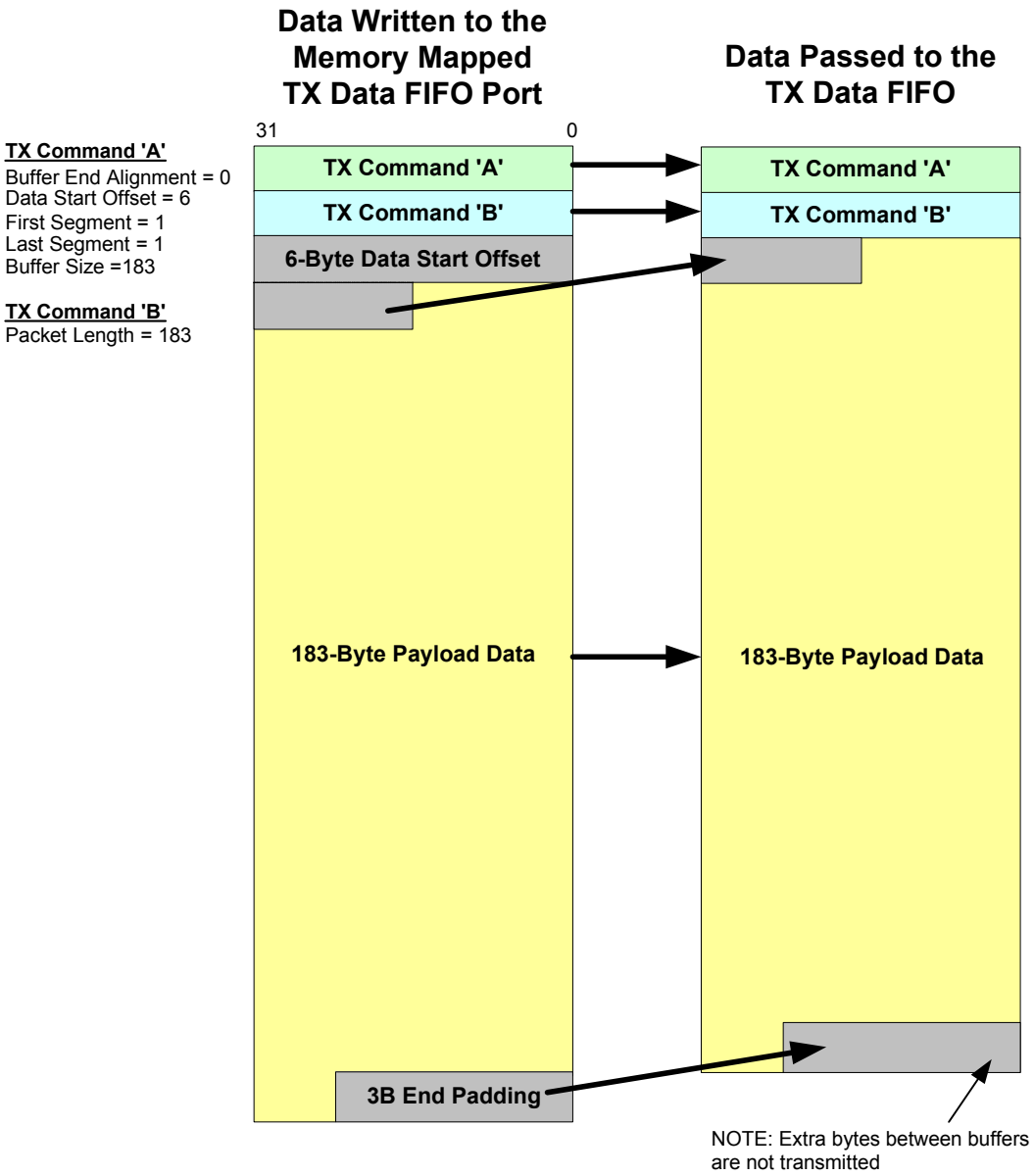


Figure 9.6 TX Example 2

9.8.7 Transmitter Errors

If the Transmitter Error (TXE) flag is asserted for any reason, the transmitter will continue operation. TX Error (TXE) will be asserted under the following conditions:

- If the actual packet length count does not match the Packet Length field as defined in the TX command.
- Both TX command 'A' and TX command 'B' are required for each buffer in a given packet. TX command 'B' must be identical for every buffer in a given packet. If the TX command 'B' words do not match, the Ethernet controller will assert the Transmitter Error (TXE) flag.
- Host overrun of the TX Data FIFO.
- Overrun of the TX Status FIFO (unless TXSAO is enabled)

9.8.8 Stopping and Starting the Transmitter

To halt the transmitter, the host must set the STOP_TX bit in the Transmit Configuration Register (TX_CFG). The transmitter will finish sending the current frame (if there is a frame transmission in progress). When the transmitter has received the TX status for this frame, it will clear the STOP_TX and TX_ON bits, and will pulse the TXSTOP_INT in the Interrupt Status Register (INT_STS).

Once stopped, the host can optionally clear the TX Status and TX Data FIFOs. The host must re-enable the transmitter by setting the TX_ON bit. If the there are frames pending in the TX Data FIFO (i.e., TX Data FIFO was not purged), the transmission will resume with this data.

9.9 RX Data Path Operation

When an Ethernet Packet is received, the Host MAC Interface Layer (MIL) first begins to transfer the RX data. This data is loaded into the RX Data FIFO. The RX Data FIFO pointers are updated as data is written into the FIFO.

The last transfer from the MIL is the RX status word. The LAN9312 implements a separate FIFO for the RX status words. The total available RX data and status queued in the RX FIFO can be read from the RX FIFO Information Register (RX_FIFO_INF). The host may read any number of available RX status words before reading the RX Data FIFO.

The host must use caution when reading the RX data and status. The host must never read more data than what is available in the FIFO's. If this is attempted an underrun condition will occur. If this error occurs, the Ethernet controller will assert the Receiver Error (RXE) interrupt. If an underrun condition occurs, a soft reset is required to regain host synchronization.

A configurable beginning offset is supported in the LAN9312. The RX data Offset field in the Receive Configuration Register (RX_CFG) controls the number of bytes that the beginning of the RX data buffer is shifted. The host can set an offset from 0-31 bytes. The offset may be changed in between RX packets, but it must not be changed during an RX packet read.

The LAN9312 can be programmed to add padding at the end of a receive packet in the event that the end of the packet does not align with the host burst boundary. This feature is necessary when the LAN9312 is operating in a system that always performs multi-DWORD bursts. In such cases the LAN9312 must guarantee that it can transfer data in multiples of the Burst length regardless of the actual packet length. When configured to do so, the LAN9312 will add extra data at the end of the packet to allow the host to perform the necessary number of reads so that the Burst length is not cut short. Once a packet has been padded by the H/W, it is the responsibility of the host to interrogate the packet length field in the RX status and determine how much padding to discard at the end of the packet.

It is possible to read multiple packets out of the RX Data FIFO in one continuous stream. It should be noted that the programmed Offset and Padding will be added to each individual packet in the stream, since packet boundaries are maintained.

9.9.1 RX Slave PIO Operation

Using PIO mode, the host can either implement a polling or interrupt scheme to empty the received packet out of the RX Data FIFO. The host will remain in the idle state until it receives an indication (interrupt or polling) that data is available in the RX Data FIFO. The host will then read the RX Status FIFO to get the packet status, which will contain the packet length and any other status information. The host should perform the proper number of reads, as indicated by the packet length *plus* the start offset *and* the amount of optional padding added to the end of the frame, from the RX Data FIFO. A typical host receive routine using interrupts can be seen in Figure 9.7, while a typical host receive routine using polling can be seen in Figure 9.8.

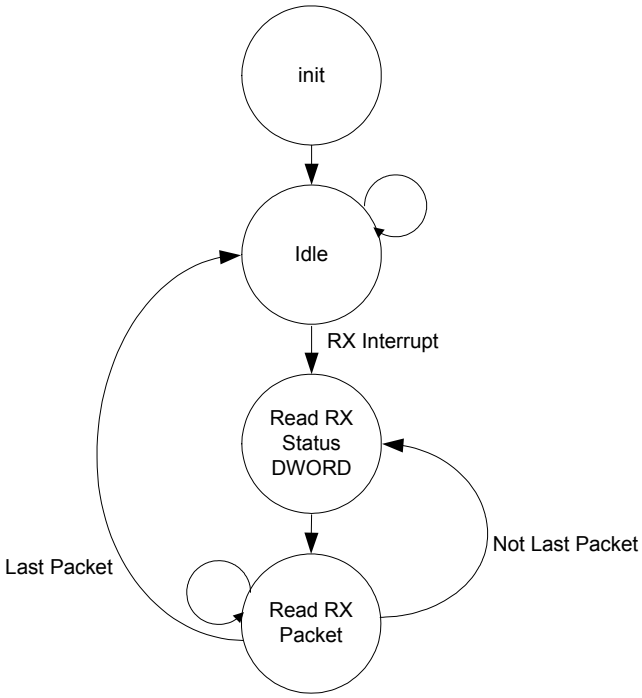


Figure 9.7 Host Receive Routine Using Interrupts

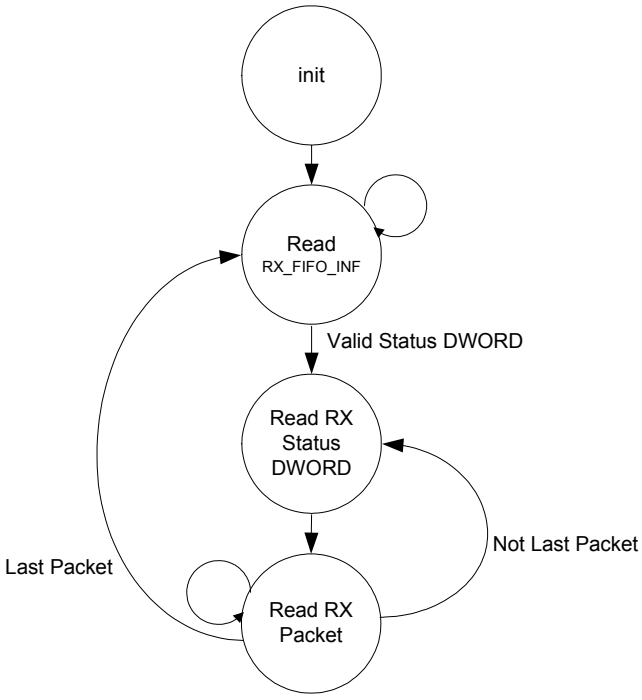


Figure 9.8 Host Receive Routine Using Polling

9.9.1.1 Receive Data FIFO Fast Forward

The RX data path implements an automatic data discard function. Using the RX Data FIFO Fast Forward bit (RX_FFWD) in the Receive Datapath Control Register (RX_DP_CTRL), the host can instruct the LAN9312 to skip the packet at the head of the RX Data FIFO. The RX Data FIFO pointers are automatically incremented to the beginning of the next RX packet.

When performing a fast-forward, there must be at least 4 DWORDs of data in the RX Data FIFO for the packet being discarded. For cases with less than 4 DWORDs, do not use RX_FFWD. In this case data must be read from the RX Data FIFO and discarded using standard PIO read operations.

After initiating a fast-forward operation, do not perform any reads of the RX Data FIFO until the RX_FFWD bit is cleared. Other resources can be accessed during this time (i.e., any registers and/or the other three FIFO's). Also note that the RX_FFWD will only fast-forward the RX Data FIFO, not the RX Status FIFO. After an RX fast-forward operation the RX status must still be read from the RX Status FIFO.

The receiver does not have to be stopped to perform a fast-forward operation.

9.9.1.2 Force Receiver Discard (Receiver Dump)

In addition to the Receive data Fast Forward feature, LAN9312 also implements a receiver "dump" feature. This feature allows the host processor to flush the entire contents of the RX Data and RX Status FIFOs. When activated, the read and write pointers for the RX Data and Status FIFO's will be returned to their reset state. To perform a receiver dump, the LAN9312 receiver must be halted. Once the receiver stop completion is confirmed, the RX_DUMP bit can be set in the Receive Configuration Register (RX_CFG). The RX_DUMP bit is cleared when the dump is complete. For more information on stopping the receiver, please refer to Section 9.9.4, "Stopping and Starting the Receiver". For more information on the RX_DUMP bit, please refer to Section 14.2.2.1, "Receive Configuration Register (RX_CFG)," on page 180.

9.9.2 RX Packet Format

The RX status words can be read from the RX Status FIFO port, while the RX data packets can be read from the RX Data FIFO. RX data packets are formatted in a specific manner before the host can

read them as shown in Figure 9.9. It is assumed that the host has previously read the associated status word from the RX Status FIFO, to ascertain the data size and any error conditions.

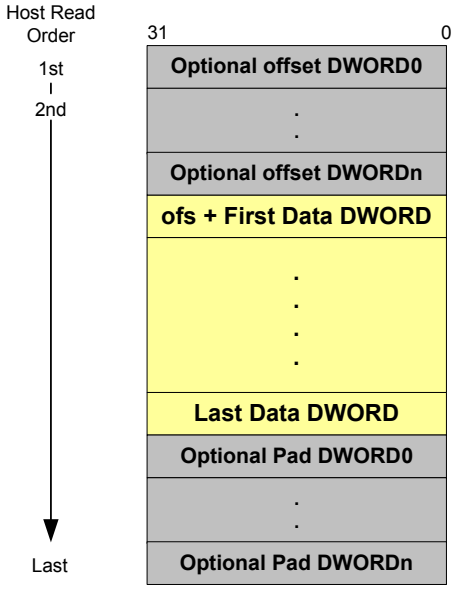


Figure 9.9 RX Packet Format

9.9.3 RX Status Format

Note: Though the Host MAC is communicating locally with the switch fabric MAC, the events described in the RX Status word may still occur.

BITS	DESCRIPTION
31	**Reserved.** This bit is reserved. Reads 0.
30	**Filtering Fail.** When set, this bit indicates that the associated frame failed the address recognizing filtering.
29:16	**Packet Length.** The size, in bytes, of the corresponding received frame.
15	**Error Status (ES).** When set this bit indicates that the Host MAC Interface Layer (MIL) has reported an error. This bit is the Internal logical “or” of bits 11,7,6 and 1.
14	**Reserved.** These bits are reserved. Reads 0.
13	**Broadcast Frame.** When set, this bit indicates that the received frame has a Broadcast address.
12	**Length Error (LE).** When set, this bit indicates that the actual length does not match with the length/type field of the received frame.
11	**Runt Frame.** When set, this bit indicates that frame was prematurely terminated before the collision window (64 bytes). Runt frames are passed on to the host only if the Pass Bad Frames bit (PASSBAD) of the Host MAC Control Register (HMAC_CR) is set.
10	**Multicast Frame.** When set, this bit indicates that the received frame has a Multicast address.
9:8	**Reserved.** These bits are reserved. Reads 0.

BITS	DESCRIPTION
7	**Frame Too Long.** When set, this bit indicates that the frame length exceeds the maximum Ethernet specification of 1518 bytes. This is only a frame too long indication and will not cause the frame reception to be truncated.
6	**Collision Seen.** When set, this bit indicates that the frame has seen a collision after the collision window. This indicates that a late collision has occurred.
5	**Frame Type.** When set, this bit indicates that the frame is an Ethernet-type frame (Length/Type field in the frame is greater than 1500). When reset, it indicates the incoming frame was an 802.3 type frame. This bit is not set for Runt frames less than 14 bytes.
4	**Receive Watchdog time-out.** When set, this bit indicates that the incoming frame is greater than 2048 bytes through 2560 bytes, therefore expiring the Receive Watchdog Timer.
3	**MII Error.** When set, this bit indicates that a receive error was detected during frame reception.
2	**Dribbling Bit.** When set, this bit indicates that the frame contained a non-integer multiple of 8 bits. This error is reported only if the number of dribbling bits in the last byte is at least 3 in the 10 Mbps operating mode. This bit will not be set when the collision seen bit[6] is set. If set and the CRC error bit is [1] reset, then the packet is considered to be valid.
1	**CRC Error.** When set, this bit indicates that a CRC error was detected. This bit is also set when the RX_ER pin is asserted during the reception of a frame even though the CRC may be correct. This bit is not valid if the received frame is a Runt frame, or a late collision was detected or when the Watchdog Time-out occurs.
0	**Reserved.** These bits are reserved. Reads 0

9.9.4 Stopping and Starting the Receiver

To stop the receiver, the host must clear the RXEN bit in the Host MAC Control Register (HMAC_CR). When the receiver is halted, the RXSTOP_INT will be pulsed and reflected in the Interrupt Status Register (INT_STS). Once stopped, the host can optionally clear the RX Status and RX Data FIFOs. The host must re-enable the receiver by setting the RXEN bit.

9.9.5 Receiver Errors

If the Receiver Error (RXE) flag is asserted in the Interrupt Status Register (INT_STS) for any reason, the receiver will continue operation. RX Error (RXE) will be asserted under the following conditions:

- A host underrun of RX Data FIFO
- A host underrun of the RX Status FIFO
- An overrun of the RX Status FIFO

It is the duty of the host to identify and resolve any error conditions.

Chapter 10 Serial Management

10.1 Functional Overview

This chapter details the LAN9312 serial management functionality of the I²C/Microwire EEPROM Controller and the supporting EEPROM Loader.

The I²C/Microwire EEPROM controller is an I²C/Microwire master module which interfaces an optional external EEPROM with the system register bus and the EEPROM Loader. Multiple types (I²C/Microwire) and sizes of external EEPROMs are supported. Configuration of the EEPROM type and size are accomplished via the eeprom_type_strap and eeprom_size_strap[1:0] configuration straps respectively. Various commands are supported for each EEPROM type, allowing for the storage and retrieval of static data. The I²C interface conforms to the Philips *I²C-Bus Specification*.

The EEPROM Loader provides the automatic loading of configuration settings from the EEPROM into the LAN9312 at reset. The EEPROM Loader module interfaces to the EEPROM Controller, Ethernet PHYs, and the system CSRs.

10.2 I²C/Microwire Master EEPROM Controller

Based on the configuration strap eeprom_type_strap, the I²C/Microwire EEPROM controller supports either Microwire or I²C compatible EEPROMs. The I²C/Microwire serial management pins functionality and characteristics differ dependant on the selected EEPROM type as summarized in Table 10.1.

Table 10.1 I²C/Microwire Master Serial Management Pins Characteristics

EEPROM TYPE/MODE	EE_SDA/EEDI PIN	EEDO PIN	EECS PIN	EE_SCL/EECLK PIN
I²C Master EEPROM Mode eeprom_type_strap = 1	**EE_SDA** Input enabled (to I²C master) Open-drain output (from I²C master) Pull-down disabled	**NOT USED** Input enabled (used for straps) Output enabled (driven low)	**NOT USED** Input enabled (used for straps) Output enabled (driven low)	**EE_SCL** Input enabled (to I²C master and used for straps) Open-drain output (from I²C master)
Microwire Master EEPROM Mode eeprom_type_strap = 0	**EEDI** Input enabled (to Microwire master) Output disabled Pull-down enabled	**EEDO** Input enabled (used for straps) Output enabled (from Microwire master)	**EECS** Input enabled (used for straps) Output enabled (from Microwire master)	**EECLK** Input enabled (used for straps) Output enabled (from Microwire master)

Note: When the EEPROM Loader is running, it has exclusive use of the I²C/Microwire EEPROM controller. Refer to Section 10.2.4, "EEPROM Loader" for more information.

10.2.1 EEPROM Controller Operation

I^2C and Microwire master EEPROM operations are performed using the EEPROM Command Register (E2P_CMD) and EEPROM Data Register (E2P_DATA).

In Microwire EEPROM mode, the following operations are supported:

- ERASE (Erase Location)
- ERAL (Erase All)
- EWDS (Erase/Write Disable)
- EWEN (Erase/Write Enable)
- READ (Read Location)
- WRITE (Write Location)
- WRAL (Write All)
- RELOAD (EEPROM Loader Reload - See Section 10.2.4, "EEPROM Loader")

Note: In I^2C EEPROM mode, only a sub-set of the above commands (READ, WRITE, and RELOAD) are supported.

Note: The EEPROM Loader uses the READ command only.

The supported commands of each mode are detailed in Section 14.2.4.1, "EEPROM Command Register (E2P_CMD)," on page 197. Details specific to each EEPROM controller mode (I^2C and Microwire) are explained in Section 10.2.2, "I2C EEPROM" and Section 10.2.3, "Microwire EEPROM" respectively.

When issuing a WRITE, or WRAL command, the desired data must first be written into the EEPROM Data Register (E2P_DATA). The WRITE or WRAL command may then be issued by setting the EPC_COMMAND field of the EEPROM Command Register (E2P_CMD) to the desired command value. If the operation is a WRITE, the EPC_ADDRESS field in the EEPROM Command Register (E2P_CMD) must also be set to the desired location. The command is executed when the EPC_BUSY bit of the EEPROM Command Register (E2P_CMD) is set. The completion of the operation is indicated when the EPC_BUSY bit is cleared.

When issuing a READ command, the EPC_COMMAND and EPC_ADDRESS fields of the EEPROM Command Register (E2P_CMD) must be configured with the desired command value and the read address, respectively. The READ command is executed by setting the EPC_BUSY bit of the EEPROM Command Register (E2P_CMD). The completion of the operation is indicated when the EPC_BUSY bit is cleared, at which time the data from the EEPROM may be read from the EEPROM Data Register (E2P_DATA).

Other EEPROM operations (EWDS, EWEN, ERASE, ERAL, RELOAD) are performed by writing the appropriate command into the EPC_COMMAND field of the EEPROM Command Register (E2P_CMD). The command is executed by setting the EPC_BUSY bit of the EEPROM Command Register (E2P_CMD). In all cases, the software must wait for the EPC_BUSY bit to clear before modifying the EEPROM Command Register (E2P_CMD).

Note: The EEPROM device powers-up in the erase/write disabled state. To modify the contents of the EEPROM, the EWEN command must first be issued.

If an operation is attempted and the EEPROM device does not respond within 30mS, the LAN9312 will time-out, and the EPC_TIMEOUT bit of the EEPROM Command Register (E2P_CMD) will be set.

Figure 10.1 illustrates the process required to perform an EEPROM read or write operation.

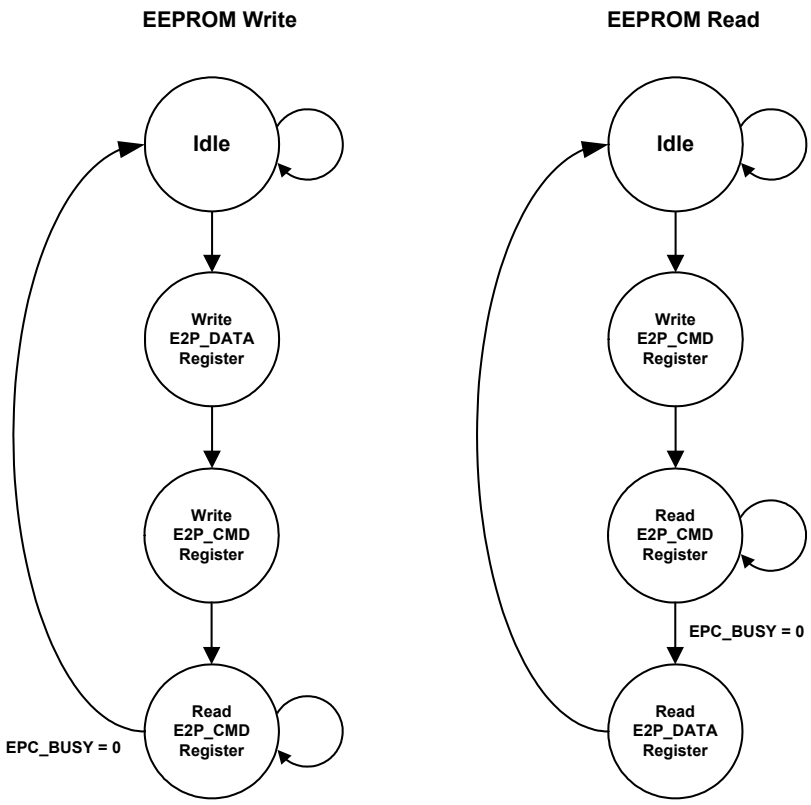


Figure 10.1 EEPROM Access Flow Diagram

10.2.2 I²C EEPROM

The I²C master implements a low level serial interface (start and stop condition generation, data bit transmission and reception, acknowledge generation and reception) for connection to I²C EEPROMs, and consists of a data wire (EE_SDA) and a serial clock (EE_SCL). The serial clock is driven by the master, while the data wire is bi-directional. Both signals are open-drain and require external pull-up resistors.

The serial clock is also used as an input as it can be held low by the slave device in order to wait-state the data cycle. Once the slave has data available or is ready to receive, it will release the clock. Assuming the masters clock low time is also expired, the clock will rise and the cycle will continue. In the event that the slave device holds the clock low for more than 30mS, the current command sequence is aborted and the EPC_TIMEOUT bit in the EEPROM Command Register (E2P_CMD) is set. Both the clock and data signals have Schmitt trigger inputs and digital input filters. The digital filters reject pulses that are less than 100nS.

Note: Since the I²C master is designed to access EEPROM only, multi-master arbitration is not supported.

Based on the configuration strap eeprom_size_strap, various sized I²C EEPROMs are supported. The varying size ranges are supported by additional bits in the address field (EPC_ADDRESS) of the EEPROM Command Register (E2P_CMD). Within each size range, the largest EEPROM uses all the address bits, while the smaller EEPROMs treat the upper address bits as don't cares. The EEPROM

controller drives all the address bits as requested regardless of the actual size of the EEPROM. The supported size ranges for I²C operation are shown in Table 10.2.

Table 10.2 I²C EEPROM Size Ranges

eeprom_size_strap[0]	# OF ADDRESS BYTES	EEPROM SIZE	EEPROM TYPES
0	1 (Note 10.1)	16 x 8 through 2048 x 8	24xx00, 24xx01, 24xx02, 24xx04, 24xx08, 24xx16
1	2	4096 x 8 through 65536 x 8	24xx32, 24xx64, 24xx128, 24xx256, 24xx512

Note 10.1 Bits in the control byte are used as the upper address bits.

The I²C master interface runs at the standard-mode rate of 100KHz and is fully compliant with the Philips *I²C-Bus Specification*. Refer to the he Philips *I²C-Bus Specification* for detailed timing information.

10.2.2.1 I²C Protocol Overview

I²C is a bi-directional 2-wire data protocol. A device that sends data is defined as a transmitter and a device that receives data is defined as a receiver. The bus is controlled by a master which generates the EE_SCL clock, controls bus access, and generates the start and stop conditions. Either the master or slave may operate as a transmitter or receiver as determined by the master.

The following bus states exist:

- **Idle:** Both EE_SDA and EE_SCL are high when the bus is idle.
- **Start & Stop Conditions:** A start condition is defined as a high to low transition on the EE_ SDA line while EE_ SCL is high. A stop condition is defined as a low to high transition on the EE_SDA line while EE_SCL is high. The bus is considered to be busy following a start condition and is considered free 4.7uS/1.3uS (for 100KHz and 400KHz operation, respectively) following a stop condition. The bus stays busy following a repeated start condition (instead of a stop condition). Starts and repeated starts are otherwise functionally equivalent.
- **Data Valid:** Data is valid, following the start condition, when EE_SDA is stable while EE_SCL is high. Data can only be changed while the clock is low. There is one valid bit per clock pulse. Every byte must be 8 bits long and is transmitted msb first.
- **Acknowledge:** Each byte of data is followed by an acknowledge bit. The master generates a ninth clock pulse for the acknowledge bit. The transmitter releases EE_SDA (high). The receiver drives EE_SDA low so that it remains valid during the high period of the clock, taking into account the setup and hold times. The receiver may be the master or the slave depending on the direction of the data. Typically the receiver acknowledges each byte. If the master is the receiver, it does not generate an acknowledge on the last byte of a transfer. This informs the slave to not drive the next byte of data so that the master may generate a stop or repeated start condition.

Figure 10.2 displays the various bus states of a typical I2C cycle.

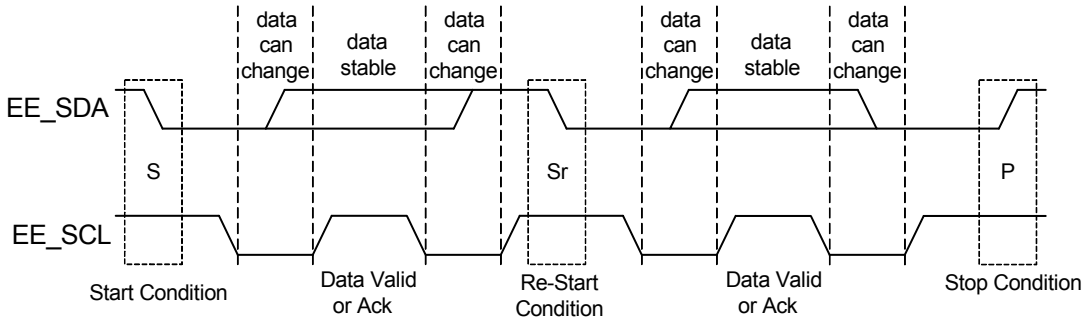


Figure 10.2 I2C Cycle

10.2.2.2 I2C EEPROM Device Addressing

The I2C EEPROM is addressed for a read or write operation by first sending a control byte followed by the address byte or bytes. The control byte is preceded by a start condition. The control byte and address byte(s) are each acknowledged by the EEPROM slave. If the EEPROM slave fails to send an acknowledge, then the sequence is aborted and the EPC_TIMEOUT bit of the EEPROM Command Register (E2P_CMD) is set.

The control byte consists of a 4-bit control code, 3-bits of chip/block select and one direction bit. The control code is 1010b. For single byte addressing EEPROMs, the chip/block select bits are used for address bits 10, 9, and 8. For double byte addressing EEPROMs, the chip/block select bits are set low. The direction bit is set low to indicate the address is being written.

Figure 10.3 illustrates typical I2C EEPROM addressing bit order for single and double byte addressing.

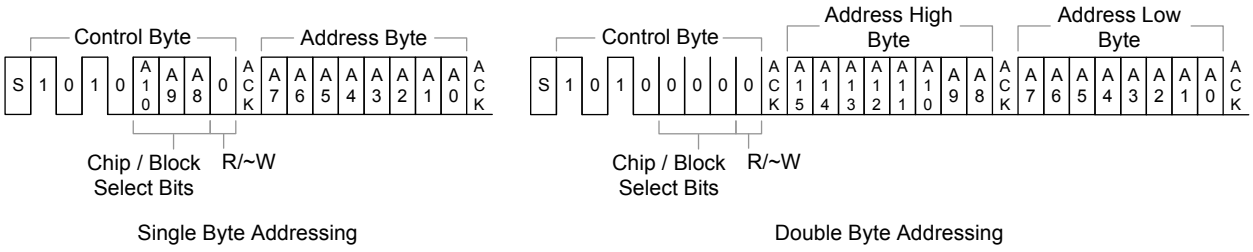


Figure 10.3 I2C EEPROM Addressing

10.2.2.3 I2C EEPROM Byte Read

Following the device addressing, a data byte may be read from the EEPROM by outputting a start condition and control byte with a control code of 1010b, chip/block select bits as described in Section 10.2.2.2, and the R/~W bit high. The EEPROM will respond with an acknowledge, followed by 8-bits of data. If the EEPROM slave fails to send an acknowledge, then the sequence is aborted and the EPC_TIMEOUT bit in the EEPROM Command Register (E2P_CMD) is set. The I2C master then sends a no-acknowledge, followed by a stop condition.

Figure 10.4 illustrates typical I2C EEPROM byte read for single and double byte addressing.

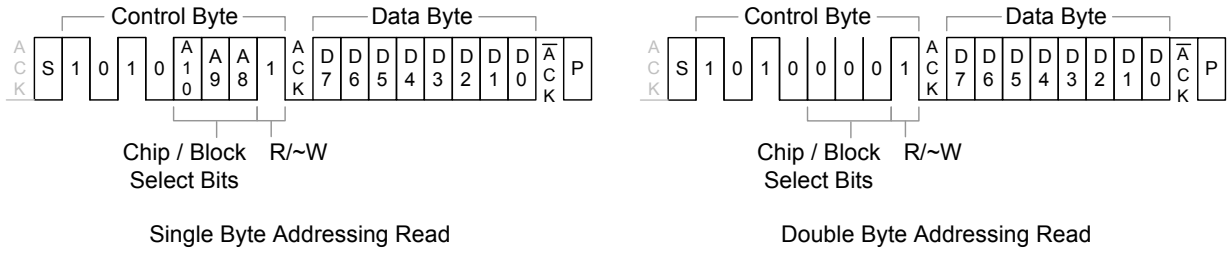


Figure 10.4 I2C EEPROM Byte Read

For a register level description of a read operation, refer to Section 10.2.1, "EEPROM Controller Operation," on page 138.

10.2.2.4 I2C EEPROM Sequential Byte Reads

Following the device addressing, data bytes may be read sequentially from the EEPROM by outputting a start condition and control byte with a control code of 1010b, chip/block select bits as described in Section 10.2.2.2, and the R/~W bit high. The EEPROM will respond with an acknowledge, followed by 8-bits of data. If the EEPROM slave fails to send an acknowledge, then the sequence is aborted and the EPC_TIMEOUT bit in the EEPROM Command Register (E2P_CMD) is set. The I2C master then sends an acknowledge, and the EEPROM responds with the next 8-bits of data. This continues until the last desired byte is read, at which point the I2C master sends a no-acknowledge, followed by a stop condition.

Figure 10.4 illustrates typical I2C EEPROM sequential byte reads for single and double byte addressing.

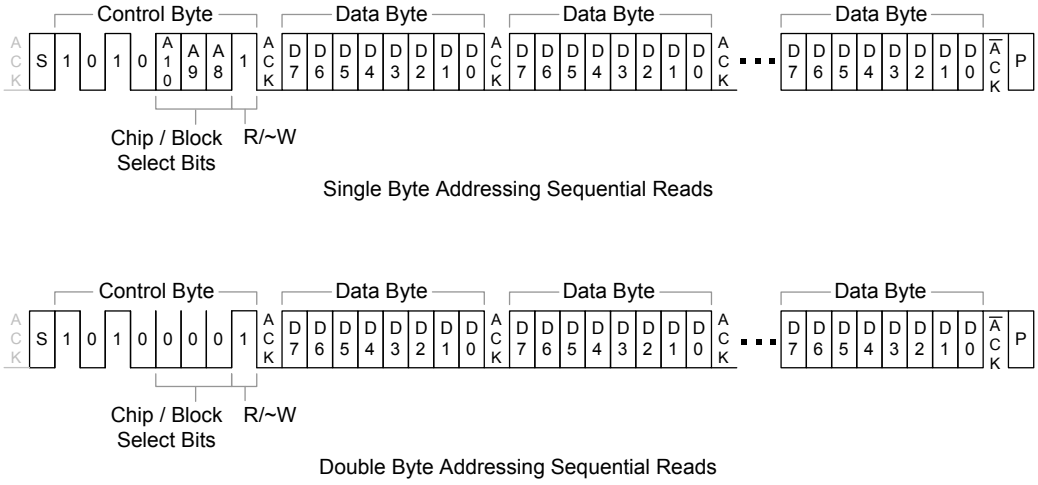


Figure 10.5 I2C EEPROM Sequential Byte Reads

Sequential reads are used by the EEPROM Loader. Refer to Section 10.2.4, "EEPROM Loader" for additional information.

For a register level description of a read operation, refer to Section 10.2.1, "EEPROM Controller Operation," on page 138.

10.2.2.5 I²C EEPROM Byte Writes

Following the device addressing, a data byte may be written to the EEPROM by outputting the data after receiving the acknowledge from the EEPROM. The data byte is acknowledged by the EEPROM slave and the I²C master finishes the write cycle with a stop condition. If the EEPROM slave fails to send an acknowledge, then the sequence is aborted and the EPC_TIMEOUT bit in the EEPROM Command Register (E2P_CMD) is set.

Following the data byte write cycle, the I²C master will poll the EEPROM to determine when the byte write is finished. A start condition is sent followed by a control byte with a control code of 1010b, chip/block select bits low, and the R/~W bit low. If the EEPROM is finished with the byte write, it will respond with an acknowledge. Otherwise, it will respond with a no-acknowledge and the I²C master will repeat the poll. If the acknowledge does not occur within 30mS, a time-out occurs. Once the I²C master receives the acknowledge, it concludes by sending a start condition, followed by a stop condition, which will place the EEPROM into standby.

Figure 10.4 illustrates typical I²C EEPROM byte write.

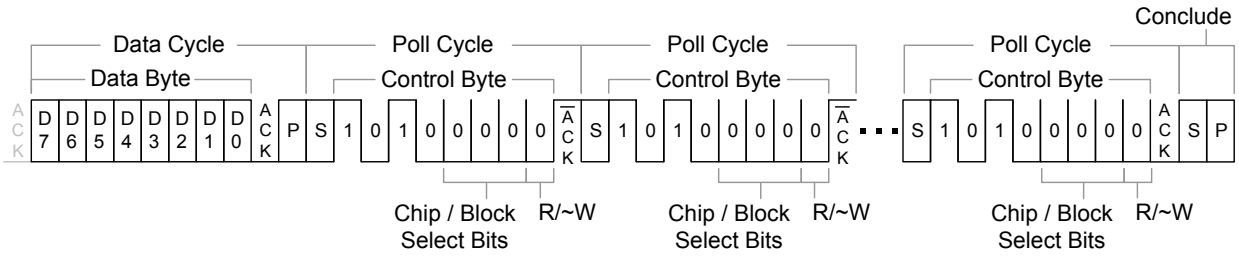


Figure 10.6 I²C EEPROM Byte Write

For a register level description of a write operation, refer to Section 10.2.1, "EEPROM Controller Operation," on page 138.

10.2.3 Microwire EEPROM

Based on the configuration strap eeprom_type_strap, various sized Microwire EEPROMs are supported. The varying size ranges are supported by additional bits in the address field (EPC_ADDRESS) of the EEPROM Command Register (E2P_CMD). Within each size range, the largest EEPROM uses all the address bits, while the smaller EEPROMs treat the upper address bits as don't cares. The EEPROM controller drives all the address bits as requested regardless of the actual size of the EEPROM. The supported size ranges for Microwire operation are shown in Table 10.3.

Table 10.3 Microwire EEPROM Size Ranges

eeprom_size_strap[1:0]	# OF ADDRESS BITS	EEPROM SIZE	EEPROM TYPES
00	7	128 x 8	93xx46A
01	9	256 x 8 and 512 x 8	93xx56A, 93xx66A
10	11	1024 x 8 and 2048 x 8	93xx76A, 93xx86A
11	RESERVED		

Refer to Section 15.5.10, "Microwire Timing," on page 453 for detailed Microwire timing information.

10.2.3.1 Microwire Master Commands

Table 10.4, Table 10.5, and Table 10.6 detail the Microwire command set, including the number of clock cycles required, for 7, 9, and 11 address bits respectively. These commands are detailed in the following sections as well as in Section 14.2.4.1, "EEPROM Command Register (E2P_CMD)," on page 197.

Table 10.4 Microwire Command Set for 7 Address Bits

INST	START BIT	OPCODE	ADDRESS	DATA TO EEPROM	DATA FROM EEPROM	# OF CLOCKS
ERASE	1	11	A6 A5 A4 A3 A2 A1 A0	-	(RDY/~BSY)	10
ERAL	1	00	1 0 X X X X X	-	(RDY/~BSY)	10
EWDS	1	00	0 0 X X X X X	-	Hi-Z	10
EWEN	1	00	1 1 X X X X X	-	Hi-Z	10
READ	1	10	A6 A5 A4 A3 A2 A1 A0	-	D7 - D0	18
WRITE	1	01	A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/~BSY)	18
WRAL	1	00	0 1 X X X X X	D7 - D0	(RDY/~BSY)	18

Table 10.5 Microwire Command Set for 9 Address Bits

INST	START BIT	OPCODE	ADDRESS	DATA TO EEPROM	DATA FROM EEPROM	# OF CLOCKS
ERASE	1	11	A8 A7 A6 A5 A4 A3 A2 A1 A0	-	(RDY/~BSY)	12
ERAL	1	00	1 0 X X X X X X X	-	(RDY/~BSY)	12

Table 10.5 Microwire Command Set for 9 Address Bits (continued)

INST	START BIT	OPCODE	ADDRESS	DATA TO EEPROM	DATA FROM EEPROM	# OF CLOCKS
EWDS	1	00	0 0 X X X X X X X	-	Hi-Z	12
EWEN	1	00	1 1 X X X X X X X	-	Hi-Z	12
READ	1	10	A8 A7 A6 A5 A4 A3 A2 A1 A0	-	D7 - D0	20
WRITE	1	01	A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/~BSY)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/~BSY)	20

Table 10.6 Microwire Command Set for 11 Address Bits

INST	START BIT	OPCODE	ADDRESS	DATA TO EEPROM	DATA FROM EEPROM	# OF CLOCKS
ERASE	1	11	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	-	(RDY/~BSY)	14
ERAL	1	00	1 0 X X X X X X X X X	-	(RDY/~BSY)	14
EWDS	1	00	0 0 X X X X X X X X X	-	Hi-Z	14
EWEN	1	00	1 1 X X X X X X X X X	-	Hi-Z	14
READ	1	10	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	-	D7 - D0	22
WRITE	1	01	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/~BSY)	22
WRAL	1	00	0 1 X X X X X X X X X	D7 - D0	(RDY/~BSY)	22

10.2.3.2 ERASE (Erase Location)

If erase/write operations are enabled in the EEPROM, this command will erase the location selected by the EPC_ADDRESS field of the EEPROM Command Register (E2P_CMD). The EPC_TIMEOUT bit is set if the EEPROM does not respond within 30mS.

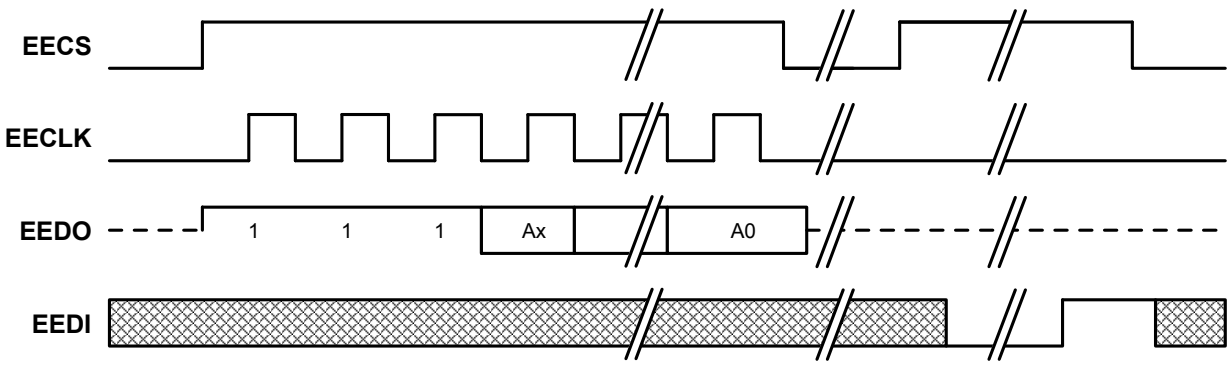


Figure 10.7 EEPROM ERASE Cycle

10.2.3.3 ERAL (Erase All)

If erase/write operations are enabled in the EEPROM, this command will initiate a bulk erase of the entire EEPROM. The EPC_TIMEOUT bit of the EEPROM Command Register (E2P_CMD) is set if the EEPROM does not respond within 30mS.

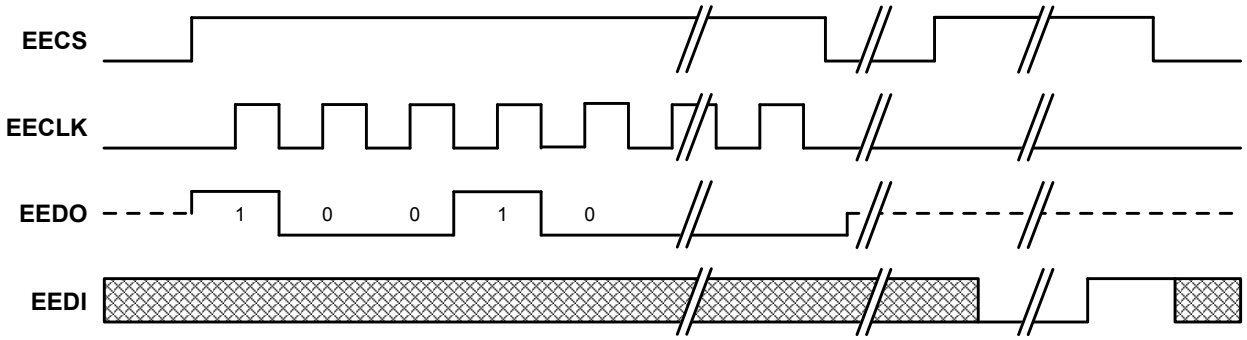


Figure 10.8 EEPROM ERAL Cycle

10.2.3.4 EWDS (Erase/Write Disable)

After this command is issued, the EEPROM will ignore erase and write commands. To re-enable erase/write operations, the EWEN command must be issued.

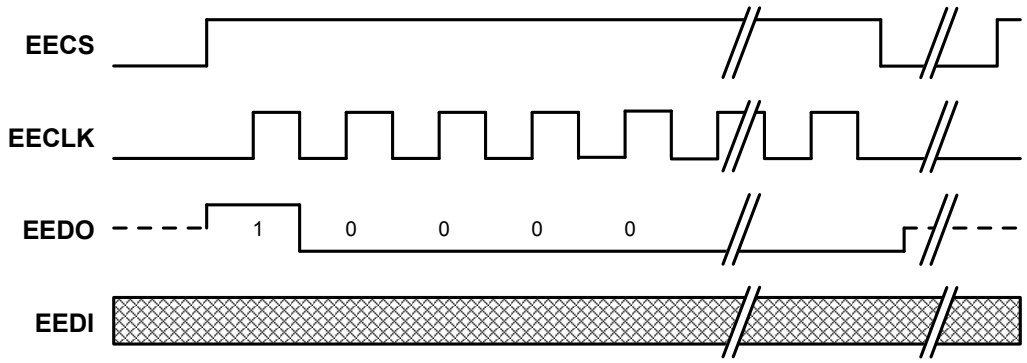


Figure 10.9 EEPROM EWDS Cycle

10.2.3.5 EWEN (Erase/Write Enable)

This command enables the EEPROM for erase and write operations. The EEPROM will allow erase and write operations until the EWDS command is sent, or until power is cycled.

Note: The EEPROM will power-up in the erase/write disabled state. Any erase or write operations will fail until an EWEN command is issued.

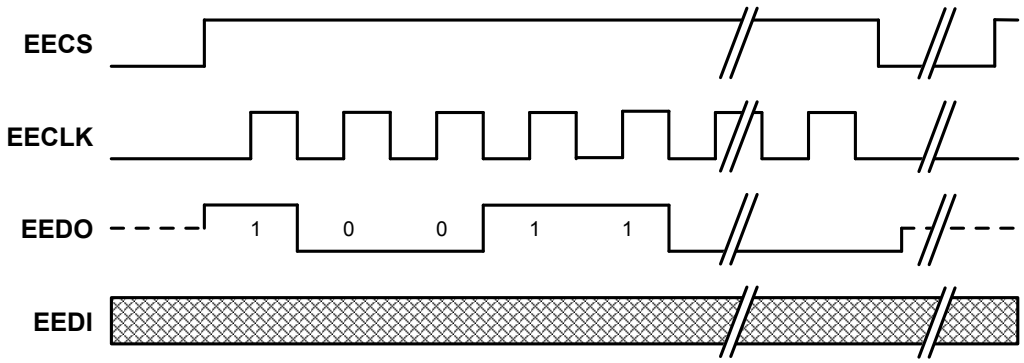


Figure 10.10 EEPROM EWEN Cycle

10.2.3.6 READ (Read Location)

This command will cause a read of the EEPROM location pointed to by the EPC_ADDRESS field of the EEPROM Command Register (E2P_CMD). The result of the read is available in the EEPROM Data Register (E2P_DATA).

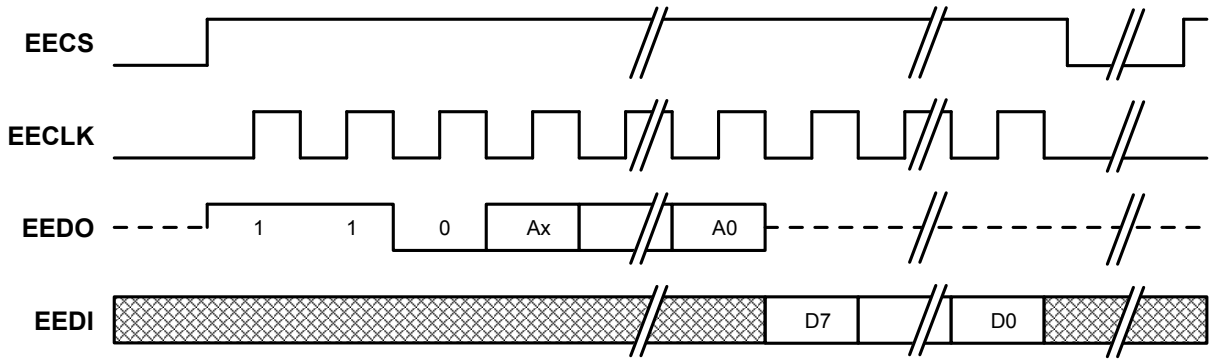


Figure 10.11 EEPROM READ Cycle

10.2.3.7 WRITE (Write Location)

If erase/write operations are enabled in the EEPROM, this command will cause the contents of the EEPROM Data Register (E2P_DATA) to be written to the EEPROM location pointed to by the EPC_ADDRESS field of the EEPROM Command Register (E2P_CMD). The EPC_TIMEOUT bit of the EEPROM Command Register (E2P_CMD) is set if the EEPROM does not respond within 30mS.

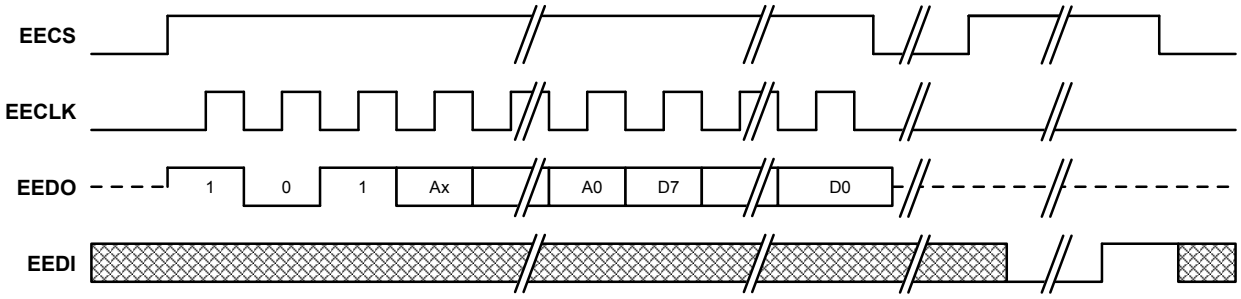


Figure 10.12 EEPROM WRITE Cycle

10.2.3.8 WRAL (Write All)

If erase/write operations are enabled in the EEPROM, this command will cause the contents of the EEPROM Data Register (E2P_DATA) to be written to every EEPROM memory location. The EPC_TIMEOUT bit of the EEPROM Command Register (E2P_CMD) is set if the EEPROM does not respond within 30mS.

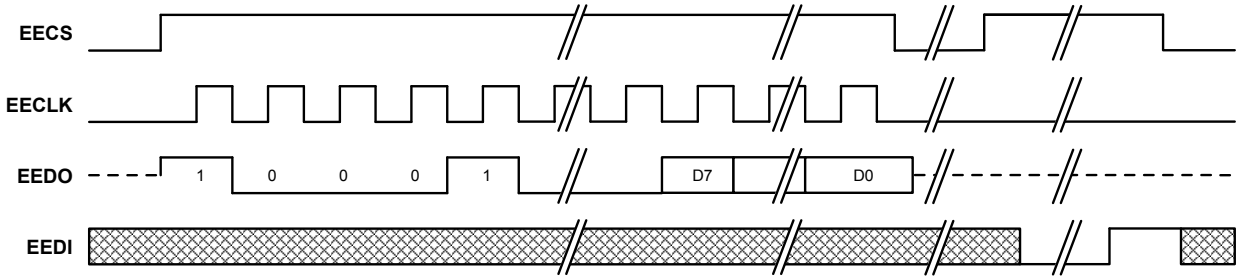


Figure 10.13 EEPROM WRAL Cycle

10.2.4 EEPROM Loader

The EEPROM Loader interfaces to the I^2C/Microwire EEPROM controller, the PHYs, and to the system CSRs (via the Register Access MUX). Only system CSRs at addresses 100h and above are accessible to the EEPROM Loader (with the addition of the PHY Management Interface Data Register (PMI_DATA) and PHY Management Interface Access Register (PMI_ACCESS) at addresses A4 and A8 respectively).

The EEPROM Loader runs upon a pin reset (nRST), power-on reset (POR), digital reset (DIGITAL_RST bit in the Reset Control Register (RESET_CTL)), or upon the issuance of a RELOAD command via the EEPROM Command Register (E2P_CMD). A soft reset will run the EEPROM Loader, but only the MAC address is loaded into the Host MAC. Refer to Section 4.2, "Resets," on page 36 for additional information on the LAN9312 resets.

The EEPROM contents must be loaded in a specific format for use with the EEPROM Loader. An overview of the EEPROM content format is shown in Table 10.7. Each section of EEPROM contents is discussed in detail in the following sections.

Table 10.7 EEPROM Contents Format Overview

EEPROM ADDRESS	DESCRIPTION	VALUE
0	EEPROM Valid Flag	A5h
1	MAC Address Low Word [7:0]	1st Byte on the Network
2	MAC Address Low Word [15:8]	2nd Byte on the Network
3	MAC Address Low Word [23:16]	3rd Byte on the Network
4	MAC Address Low Word [31:24]	4th Byte on the Network
5	MAC Address High Word [7:0]	5th Byte on the Network
6	MAC Address High Word [15:8]	6th Byte on the Network
7	Configuration Strap Values Valid Flag	A5h
8 - 11	Configuration Strap Values	See Table 10.8
12	Burst Sequence Valid Flag	A5h
13	Number of Bursts	See Section 10.2.4.5, "Register Data"
14 and above	Burst Data	See Section 10.2.4.5, "Register Data"

10.2.4.1 EEPROM Loader Operation

Upon a pin reset (nRST), power-on reset (POR), digital reset (DIGITAL_RST bit in the Reset Control Register (RESET_CTL)), or upon the issuance of a RELOAD command via the EEPROM Command Register (E2P_CMD), the EPC_BUSY bit in the EEPROM Command Register (E2P_CMD) will be set. While the EEPROM Loader is active, the READY bit of the Hardware Configuration Register (HW_CFG) and Power Management Control Register (PMT_CTRL) is cleared and no writes to the LAN9312 should be attempted. The operational flow of the EEPROM Loader can be seen in Figure 10.14.

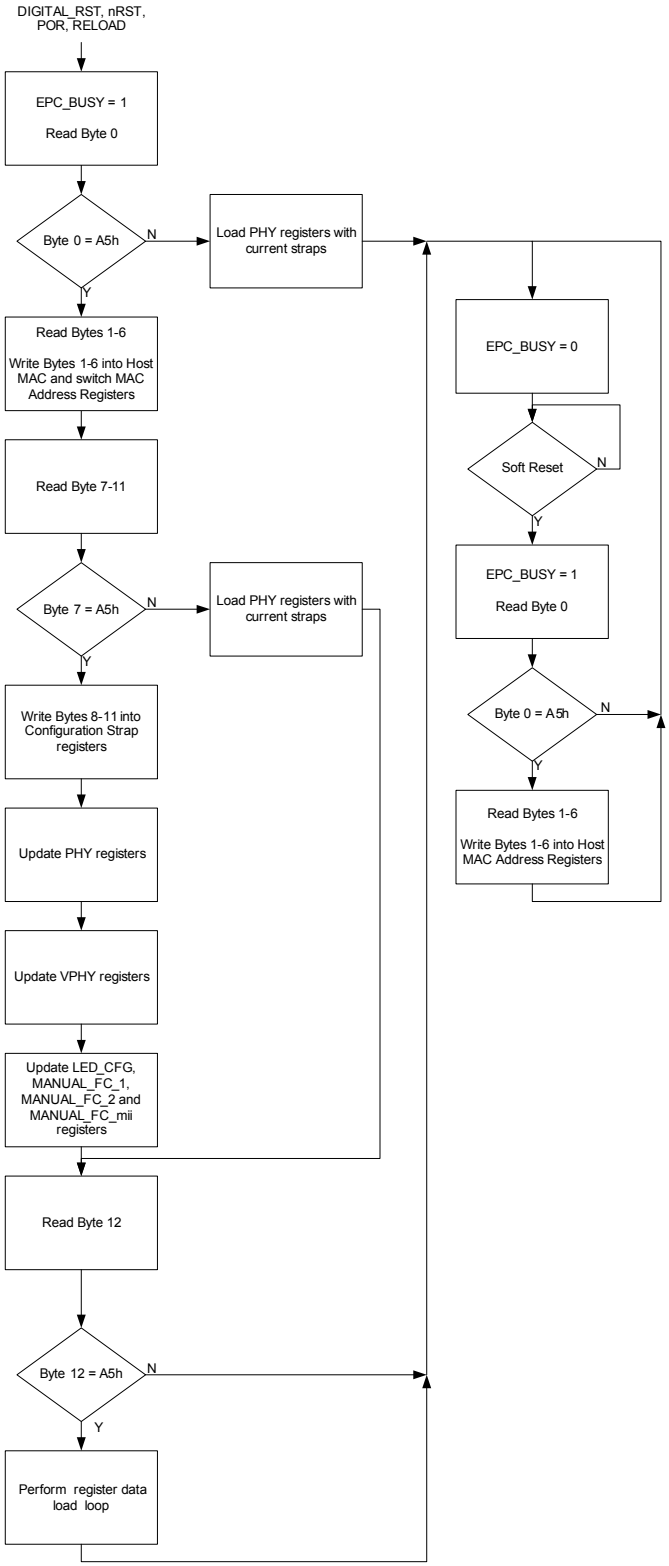


Figure 10.14 EEPROM Loader Flow Diagram

10.2.4.2 EEPROM Valid Flag

Following the release of nRST, POR, DIGITAL_RST, or a RELOAD command, the EEPROM Loader starts by reading the first byte of data from the EEPROM. If the value of A5h is not read from the first byte, the EEPROM Loader will load the current configuration strap values into the PHY registers (see Section 10.2.4.4.1) and then terminate, clearing the EPC_BUSY bit in the EEPROM Command Register (E2P_CMD). Otherwise, the EEPROM Loader will continue reading sequential bytes from the EEPROM.

10.2.4.3 MAC Address

The next six bytes in the EEPROM, after the EEPROM Valid Flag, are written into the Host MAC Address High Register (HMAC_ADDRH) and Host MAC Address Low Register (HMAC_ADDRL), and the Switch Fabric MAC Address High Register (SWITCH_MAC_ADDRH) and Switch Fabric MAC Address Low Register (SWITCH_MAC_ADDRL). The EEPROM bytes are written into the MAC address registers in the order specified in Table 10.7. Refer to Section 9.6, "Host MAC Address," on page 119 for additional information on MAC address loading.

10.2.4.3.1 HOST MAC ADDRESS RELOAD

While the EEPROM Loader is in the wait state, if a Host MAC reset is detected (via the Soft Reset bit in the Hardware Configuration Register (HW_CFG)), the EEPROM Loader will read byte 0. If the byte 0 value is A5h, the EEPROM Loader will read bytes 1 through 6 from the EEPROM and reload the Host MAC Address High Register (HMAC_ADDRH) and Host MAC Address Low Register (HMAC_ADDRL). During this time, the EPC_BUSY bit in the EEPROM Command Register (E2P_CMD) is set.

Note: The switch MAC address registers are not reloaded due to this condition.

10.2.4.4 Soft-Straps

The 7th byte of data to be read from the EEPROM is the Configuration Strap Values Valid Flag. If this byte has a value of A5h, the next 4 bytes of data (8-11) are written into the configuration strap registers per the assignments detailed in Table 10.8. If the flag byte is not A5h, these next 4 bytes are skipped (they are still read to maintain the data burst, but are discarded). However, the current configuration strap values are still loaded into the PHY registers (see Section 10.2.4.4.1). Refer to Section 4.2.4, "Configuration Straps," on page 40 for more information on the LAN9312 configuration straps.

Table 10.8 EEPROM Configuration Bits

BYTE/BIT	7	6	5	4	3	2	1	0
Byte 8	BP_EN_strap_1	FD_FC_strap_1	manual_FC_strap_1	manual_mdix_strap_1	auto_mdix_strap_1	speed_strap_1	duplex_strap_1	autoneg_strap_1
Byte 9	BP_EN_strap_2	FD_FC_strap_2	manual_FC_strap_2	manual_mdix_strap_2	auto_mdix_strap_2	speed_strap_2	duplex_strap_2	autoneg_strap_2
Byte 10	LED_fun_strap[1:0]		BP_EN_strap_mii	FD_FC_strap_mii	manual_FC_strap_mii	speed_strap_mii	duplex_pol_strap_mii	SQE_test_disable_strap_mii
Byte 11	LED_en_strap[7:0]							

10.2.4.4.1 PHY REGISTERS SYNCHRONIZATION

Some PHY register defaults are based on configuration straps. In order to maintain consistency between the updated configuration strap registers and the PHY registers, the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x), Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x), and Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) are written when the EEPROM Loader is run.

The Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) is written with the new defaults as detailed in Section 14.4.2.5, "Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x)," on page 294.

The Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x) is written with the new defaults as detailed in Section 14.4.2.9, "Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x)," on page 301.

The Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) is written with the new defaults as detailed in Section 14.4.2.1, "Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x)," on page 288. Additionally, the Restart Auto-negotiation bit is set in this register. This re-runs the Auto-negotiation using the new default values of the Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) register to determine the new Auto-negotiation results.

Note: Each of these PHY registers is written in its entirety, overwriting any previously changed bits.

10.2.4.4.2 VIRTUAL PHY REGISTERS SYNCHRONIZATION

Some PHY register defaults are based on configuration straps. In order to maintain consistency between the updated configuration strap registers and the Virtual PHY registers, the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV), Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS), and Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) are written when the EEPROM Loader is run.

The Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) is written with the new defaults as detailed in Section 14.2.8.5, "Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV)," on page 252.

The Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS) is written with the new defaults as detailed in Section 14.2.8.8, "Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS)," on page 257.

The Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is written with the new defaults as detailed in Section 14.2.8.1, "Virtual PHY Basic Control Register (VPHY_BASIC_CTRL)," on page 246. Additionally, the Restart Auto-negotiation bit is set in this register. This re-runs the Auto-negotiation using the new default values of the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV) register to determine the new Auto-negotiation results.

Note: Each of these VPHY registers is written in its entirety, overwriting any previously changed bits.

10.2.4.4.3 LED AND MANUAL FLOW CONTROL REGISTER SYNCHRONIZATION

Since the defaults of the LED Configuration Register (LED_CFG), Port 1 Manual Flow Control Register (MANUAL_FC_1), Port 2 Manual Flow Control Register (MANUAL_FC_2), and Port 0(Host MAC) Manual Flow Control Register (MANUAL_FC_MII) are based on configuration straps, the EEPROM Loader reloads these registers with their new default values.

10.2.4.5 Register Data

Optionally following the configuration strap values, the EEPROM data may be formatted to allow access to the LAN9312 parallel, directly writable registers. Access to indirectly accessible registers (e.g. Switch Engine registers, etc.) is achievable with an appropriate sequence of writes (at the cost of EEPROM space).

This data is first preceded with a Burst Sequence Valid Flag (EEPROM byte 12). If this byte has a value of A5h, the data that follows is recognized as a sequence of bursts. Otherwise, the EEPROM Loader is finished, will go into a wait state, and clear the EPC_BUSY bit in the EEPROM Command Register (E2P_CMD). This can optionally generate an interrupt.

The data at EEPROM byte 13 and above should be formatted in a sequence of bursts. The first byte is the total number of bursts. Following this is a series of bursts, each consisting of a starting address, count, and the count x 4 bytes of data. This results in the following formula for formatting register data:

8-bits number_of_bursts

repeat (number_of_bursts)

16-bits {starting_address[9:2] / count[7:0]}

repeat (count)

8-bits data[31:24], 8-bits data[23:16], 8-bits data[15:8], 8-bits data[7:0]

Note: The starting address is a DWORD address. Appending two 0 bits will form the register address.

As an example, the following is a 3 burst sequence, with 1, 2, and 3 DWORDs starting at register addresses 40h, 80h, and C0h respectively:

A5h, (Burst Sequence Valid Flag)

3h, (number_of_bursts)

16{10h, 1h}, (starting_address1 divided by 4 / count1)

11h, 12h, 13h, 14h, (4 x count1 of data)

16{20h, 2h}, (starting_address2 divided by 4 / count2)

21h, 22h, 23h, 24h, 25h, 26h, 27h, 28h, (4 x count2 of data)

16{30h, 3h}, (starting_address3 divided by 4 / count3)

31h, 32h, 33h, 34h, 35h, 36h, 37h, 38h, 39h, 3Ah, 3Bh, 3Ch (4 x count3 of data)

In order to avoid overwriting the Switch CSR register interface or the PHY Management Interface (PMI), the EEPROM Loader waits until the CSR Busy bit of the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) and the MII Busy bit of the PHY Management Interface Access Register (PMI_ACCESS) are cleared before performing any register write.

The EEPROM Loader checks that the EEPROM address space is not exceeded. If so, it will stop and set the EEPROM Loader Address Overflow bit in the EEPROM Command Register (E2P_CMD). The address limit is based on the eeprom_size_strap which specifies a range of sizes. The address limit is set to the largest value of the specified range.

10.2.4.6 EEPROM Loader Finished Wait-State

Once finished with the last burst, the EEPROM Loader will go into a wait-state and the EPC_BUSY bit of the EEPROM Command Register (E2P_CMD) will be cleared.

10.2.4.7 Reset Sequence and EEPROM Loader

In order to allow the EEPROM Loader to change the Port 1/2 PHYs and Virtual PHY strap inputs and maintain consistency with the PHY and Virtual PHY registers, the following sequence is used:

1. After power-up or upon a hardware reset (nRST), the straps are sampled into the LAN9312 as specified in Section 15.5.2, "Reset and Configuration Strap Timing," on page 445.
2. After the PLL is stable, the main chip reset is released and the EEPROM Loader reads the EEPROM and configures (overrides) the strap inputs.
3. The EEPROM Loader writes select Port 1/2 and Virtual PHY registers, as specified in Section 10.2.4.4.1 and Section 10.2.4.4.2, respectively.

Note: Step 3 is also performed in the case of a RELOAD command or digital reset.

Chapter 11 IEEE 1588 Hardware Time Stamp Unit

11.1 Functional Overview

The LAN9312 provides hardware support for the IEEE 1588 Precision Time Protocol (PTP), allowing clock synchronization with remote Ethernet devices, packet time stamping, and time driven event generation. Time stamping is supported on all ports, with an individual IEEE 1588 Time Stamp module connected to each port via the MII bus. Any port may function as a master or a slave clock per the IEEE 1588 specification, and the LAN9312 as a whole may function as a boundary clock.

A 64-bit tunable clock is provided that is used as the time source for all IEEE 1588 time stamp related functions. An IEEE 1588 Clock/Events block provides IEEE 1588 clock comparison based interrupt generation and time stamp related GPIO event generation. Two LAN9312 GPIO pins (GPIO[8:9]) can be used to trigger a time stamp capture when configured as an input, or output a signal from the GPIO based on an IEEE 1588 clock target compare event when configured as an output. Section 11.1.2, "Block Diagram" describes the various IEEE 1588 related blocks and how they interface to other LAN9312 functions.

All features of the IEEE 1588 hardware time stamp unit can be monitored and configured via their respective configuration and status registers. A detailed description of all IEEE 1588 CSRs is included in Section 14.2.5, "IEEE 1588," on page 201.

11.1.1 IEEE 1588

IEEE 1588 specifies a Precision Time Protocol (PTP) used by master and slave clock devices to pass time information in order to achieve clock synchronization. Five network message types are defined:

- Sync
- Delay_Req
- Follow_Up
- Delay_Resp
- Management

Only the first four message types (Sync, Delay_Req, Follow_Up, Delay_Resp) are used for clock synchronization. Using these messages, the protocol software may calculate the offset and network delay between time stamps, adjusting the slave clock frequency as needed. Refer to the IEEE 1588 protocol for message definitions and proper usage.

A PTP domain is segmented into PTP sub-domains, which are then segmented into PTP communication paths. Within each PTP communication path there is a maximum of one master clock, which is the source of time for each slave clock. The determination of which clock is the master and which clock(s) is(are) the slave(s) is not fixed, but determined by the IEEE 1588 protocol. Similarly, each PTP sub-domain may have only one master clock, referred to as the Grand Master Clock.

PTP communication paths are conceptually equivalent to Ethernet collision domains and may contain devices which extend the network. However, unlike Ethernet collision domains, the PTP communication path does not stop at a network switch, bridge, or router. This leads to a loss of precision when the network switch/bridge/router introduces a variable delay. Boundary clocks are defined which conceptually bypass the switch/bridge/router (either physically or via device integration). Essentially, a boundary clock acts as a slave to an upstream master, and as a master to a down stream slave. A boundary clock may contain multiple ports, but a maximum of one slave port is permitted.

For more information on the IEEE 1588 protocol, refer to the National Institute of Standards and Technology IEEE 1588 website:

http://ieee1588.nist.gov/

11.1.2 Block Diagram

The LAN9312 IEEE 1588 implementation is illustrated in Figure 11.1, and consists of the following major function blocks:

- IEEE 1588 Time Stamp
  These three identical blocks provide time stamping functions on all switch fabric ports.
- IEEE 1588 Clock
  This block provides a 64-bit tunable clock that is used as the time source for all IEEE 1588 time stamp related functions.
- IEEE 1588 Clock/Events
  This block provides IEEE 1588 clock comparison-based interrupt generation and time stamp related GPIO event generation.

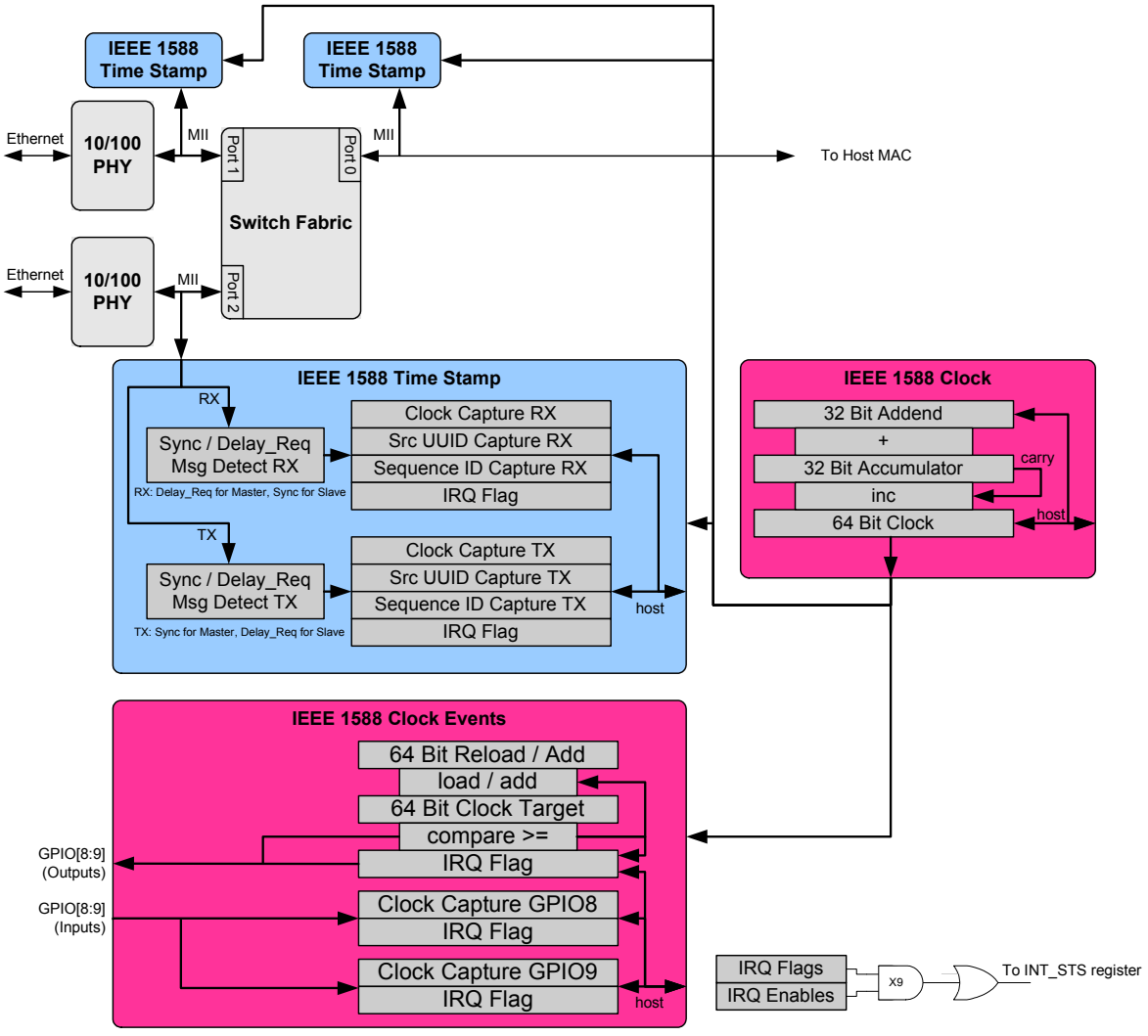


Figure 11.1 IEEE 1588 Block Diagram

11.2 IEEE 1588 Time Stamp

The LAN9312 contains three identical IEEE 1588 Time Stamp blocks as shown in Figure 11.1. These blocks are responsible for capturing the source UUID, sequence ID, and current 64-bit IEEE 1588 clock time upon detection of a Sync or Delay_Req message type on their respective port. The mode of the clock (master or slave) determines which message is detected on receive and transmit. For slave clock operation, Sync messages are detected on receive and Delay_Req messages on transmit. For master clock operation, Delay_Req messages are detected on receive and Sync messages on transmit. Follow_Up, Delay_Resp and Management packet types do not cause capture. Each port may be individually configured as an IEEE 1588 master or slave clock via the master/slave bits (M_nS_1 for Port 1, MnS_2 for Port2, and M_nS_MII for Port 0) in the 1588 Configuration Register (1588_CONFIG). Table 11.1 summarizes the message type detection under slave and master IEEE 1588 clock operation.

Table 11.1 IEEE 1588 Message Type Detection

IEEE 1588 CLOCK MODE	RECEIVE	TRANSMIT
Slave (M_nS_x = 0)	Sync	Delay_Req
Master (M_nS_x = 1)	Delay_Req	Sync

For ports 1 and 2, receive is defined as data *from* the PHY (from the outside world) and transmit is defined as data *to* the PHY. This is consistent with the point-of-view of where the partner clock resides (LAN9312 receives packets from the partner via the PHY, etc.). For the time stamp module connected to the Host MAC (Port 0), the definition of transmit and receive is reversed. Receive is defined as data *from* the switch fabric, while transmit is defined as data *to* the switch fabric. This is consistent with the point-of-view of where the partner clock resides (LAN9312 receives packets from the partner via the switch fabric, etc.).

As defined by IEEE 1588, and shown in Figure 11.2, the message time stamp point is defined as the leading edge of the first data bit following the Start of Frame Delimiter (SFD). However, since the packet contents are not yet known, the time stamp can not yet be loaded into the capture register. Therefore, the time stamp is first stored into a temporary internal holding register at the start of every packet.

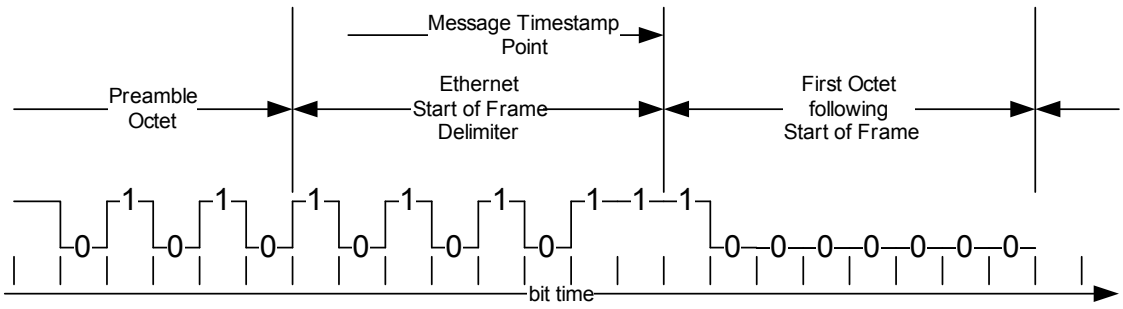


Figure 11.2 IEEE 1588 Message Time Stamp Point

Clock synchronization and hardware processing between the network data and the time stamp capture hardware causes the time stamp point to be slightly delayed. The host software can account for this delay, as it is fairly deterministic. Table 11.2 details the time stamp capture delay as a function of the mode of operation. Refer to Chapter 7, "Ethernet PHYs," on page 82 for details on these modes.

Table 11.2 Time Stamp Capture Delay

MODE OF OPERATION	DELAY (+/- 10 nS)
100 Mbps	30 nS
10 Mbps	120 nS

Once the packet type is matched, according to Table 11.1, and the Frame Check Sequence (FCS) is verified, the following occurs:

- The time stamp is loaded into the corresponding ports' capture registers:
  - –On Reception: Port x 1588 Clock High-DWORD Receive Capture Register (1588_CLOCK_HI_RX_CAPTURE_x) and Port x 1588 Clock Low-DWORD Receive Capture Register (1588_CLOCK_LO_RX_CAPTURE_x)
  - –On Transmission: Port x 1588 Clock High-DWORD Transmit Capture Register (1588_CLOCK_HI_TX_CAPTURE_x) and Port x 1588 Clock Low-DWORD Transmit Capture Register (1588_CLOCK_LO_TX_CAPTURE_x)
- The Sequence ID and Source UUID are loaded into the corresponding ports' registers:
  - –On Reception: Port x 1588 Sequence ID, Source UUID High-WORD Receive Capture Register (1588_SEQ_ID_SRC_UUID_HI_RX_CAPTURE_x) and Port x 1588 Source UUID Low-DWORD Receive Capture Register (1588_SRC_UUID_LO_RX_CAPTURE_x)
  - –On Transmission: Port x 1588 Sequence ID, Source UUID High-WORD Transmit Capture Register (1588_SEQ_ID_SRC_UUID_HI_TX_CAPTURE_x) and Port x 1588 Source UUID Low-DWORD Transmit Capture Register (1588_SRC_UUID_LO_TX_CAPTURE_x)
- The corresponding maskable interrupt flag is set in the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN). (Refer to Section 11.6, "IEEE 1588 Interrupts," on page 160 for information on IEEE 1588 interrupts.)

Note: Packets that do not contain an integral number of octets are not considered valid and do not cause a capture.

11.2.1 Capture Locking

The corresponding ports' clock capture, sequence ID, and source UUID registers can be optionally locked when a capture event occurs, preventing them from being overwritten until the host clears the corresponding interrupt flag in the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN).

This is accomplished by setting the corresponding lock enable bit(s) in the 1588 Configuration Register (1588_CONFIG). Each port has two lock enable control bits within this register, which allow the receive and transmit portions of each port to be locked independently. In addition, a lock enable bit is provided for each time stamp enabled GPIO (LOCK_ENABLE_GPIO_8 and LOCK_ENABLE_GPIO_9) which prevents the corresponding GPIO clock capture registers from being overwritten when the GPIO interrupt in 1588 Interrupt Status and Enable Register (1588_INT_STS_EN) is set. Refer to Section 14.2.5.22, "1588 Configuration Register (1588_CONFIG)," on page 222 for additional information on the capture locking related bits.

11.2.2 PTP Message Detection

In order to provide the most flexibility, loose packet type matching is used by the LAN9312. This assumes that for all packets received with a valid FCS, only the MAC destination address is required to qualify them as a PTP message. For Ethernet, four multicast addresses are specified in the PTP protocol: 224.0.1.129 through 224.0.1.132. These map to Ethernet MAC addresses 01:00:5e:00:01:81 through 01:00:5e:00:01:84. Each of these addresses has one enable bit per port in the 1588 Configuration Register (1588_CONFIG) which enables/disables the corresponding address as a PTP address on the specified port.

In addition to the fixed addresses, a user defined (host programmable) PTP address may be input via the 1588 Auxiliary MAC Address High-WORD Register (1588_AUX_MAC_HI) and 1588 Auxiliary MAC Address Low-DWORD Register (1588_AUX_MAC_LO). The user defined address may be disabled/enabled as a PTP address on each port via the dedicated enable bits in the 1588 Configuration Register (1588_CONFIG). A summary of the supported PTP multicast addresses and corresponding enable bits can be seen in Table 11.3.

Table 11.3 PTP Multicast Addresses

PTP ADDRESS	CORRESPONDING MAC ADDRESS	RELATED ENABLE BITS IN THE 1588_CONFIG REGISTER
224.0.1.129 (Primary)	01:00:5e:00:01:81	MAC_PRI_EN_1 (Port 1) MAC_PRI_EN_2 (Port 2) MAC_PRI_EN_MII (Port 0)
224.0.1.130 (Alternate 1)	01:00:5e:00:01:82	MAC_ALT1_EN_1 (Port 1) MAC_ALT1_EN_2 (Port 2) MAC_ALT1_EN_MII (Port 0)
224.0.1.131 (Alternate 2)	01:00:5e:00:01:83	MAC_ALT2_EN_1 (Port 1) MAC_ALT2_EN_2 (Port 2) MAC_ALT2_EN_MII (Port 0)
224.0.1.132 (Alternate 3)	01:00:5e:00:01:84	MAC_ALT3_EN_1 (Port 1) MAC_ALT3_EN_2 (Port 2) MAC_ALT3_EN_MII (Port 0)
User Defined	User Defined Address (1588_AUX_MAC_HI & 1588_AUX_MAC_LO registers)	MAC_USER_EN_1 (Port 1) MAC_USER_EN_2 (Port 2) MAC_USER_EN_MII (Port 0)

Once a packet is determined to match a PTP destination address, it is further qualified as a Sync or Delay_Req message type. On Ethernet, PTP uses UDP messages. Within the UDP payload is the PTP control byte (offset 32 starting at 0). This byte determines the message type: 0x00 for a Sync message, 0x01 for a Delay_Req message. The UDP payload starts at packet byte offset 42 (from 0) for untagged packets and at byte offset 46 for tagged packets.

Note: Both tagged and untagged packets are supported. Only Ethernet II packet encoding and IPv4 are supported.

Note: For proper routing of the PTP packets, the host must program an entry into the switch engine Address Logic Resolution (ALR) Table. The MAC address should be one of the reserved Multicast addresses in Table 11.3, with Port 0(Host MAC) as a destination.The Static and Valid bits must also be set. Refer to Chapter 6, "Switch Fabric," on page 55 for more information.

11.3 IEEE 1588 Clock

The 64-bit IEEE 1588 clock is the time source for all IEEE 1588 related functions of the LAN9312. It is readable and writable by the host via the 1588 Clock High-DWORD Register (1588_CLOCK_HI) and 1588 Clock Low-DWORD Register (1588_CLOCK_LO).

In order to accurately read this clock, a special procedure must be followed. Since two DWORD reads are required to fully read the 64-bit clock, the possibility exists that as the lower 32-bits roll over, a wrong intermediate value could be read. To prevent this, a snapshot register technique is used. When the 1588_CLOCK_SNAPSHOT bit in the 1588 Command Register (1588_CMD) register is written with "1", the current value of the 1588 clock is saved, allowing it to be properly read.

When writing a new value to the IEEE 1588 clock, two 32-bit write cycles are required (one for each clock register) before the registers are affected. The writes may be in any order. However, caution must be observed when changing the clock value in a live environment as it will disrupt linear time. If the clock must be adjusted during operation of the 1588 protocol, it is preferred to adjust the Addend value, effectively speeding-up or slowing-down the clock until the correct time is achieved.

The 64-bit IEEE 1588 clock consists of the 32-bit 1588 Clock Addend Register (1588_CLOCK_ADDEND) that is added to a 32-bit Accumulator every 100 MHz clock. Upon overflow of the Accumulator, the 64- bit IEEE 1588 clock is incremented. The Addend / Accumulator pair form a high precision frequency divider which can be used to compensate for the inaccuracy of the reference crystal. The nominal frequency of the 64-bit IEEE 1588 clock and the value of the Addend are calculated as follows:

FreqClock = (Addend / 2^{32}) * 100 MHz

Addend = (FreqClock * 2^{32}) / 100 MHz

Typical values for the Addend are shown in Table 11.4. These values should be adjusted based on the accuracy of the IEEE 1588 clock compared to the master clock per the PTP protocol. The adjustment precision column of the table shows the percentage change for the specified IEEE 1588 clock frequency if the Addend was to be incremented or decremented by 1.

Table 11.4 Typical IEEE 1588 Clock Addend Values

IEEE 1588 CLOCK (FreqClock)	1588_CLOCK_ADDEND (Addend)	ADJUSTMENT PRECISION %
33 MHz	547AE147h	$7.1*10^{-8}$
50 MHz	80000000h	$4.7*10^{-8}$
66 MHz	A8F5C28Fh	$3.5*10^{-8}$
75 MHz	C0000000h	$3.1*10^{-8}$
90 MHz	E6666666h	$2.6*10^{-8}$

11.4 IEEE 1588 Clock/Events

The IEEE 1588 Clock/Events block is responsible for generating and controlling all IEEE 1588 clock related events. A 64-bit comparator is included in this block which compares the 64-bit IEEE 1588 clock with a 64-bit Clock Target loaded in the 1588 Clock Target High-DWORD Register (1588_CLOCK_TARGET_HI) and 1588 Clock Target Low-DWORD Register (1588_CLOCK_TARGET_LO).

When the IEEE 1588 clock equals the Clock Target, a clock event occurs which triggers the following:

- The maskable interrupt 1588_TIMER_INT is set in the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN).
- The RELOAD_ADD bit in the 1588 Configuration Register (1588_CONFIG) is checked to determine the new Clock Target behavior:

  –RELOAD_ADD = 1:

  The new Clock Target is loaded from the 64-bit Reload / Add Registers (1588 Clock Target Reload High-DWORD Register (1588_CLOCK_TARGET_RELOAD_HI) and 1588 Clock Target Reload/Add Low-DWORD Register (1588_CLOCK_TARGET_RELOAD_LO)).

  –RELOAD_ADD = 0:

  The Clock Target is incremented by the 1588 Clock Target Reload/Add Low-DWORD Register (1588_CLOCK_TARGET_RELOAD_LO).

Note: Writing the IEEE 1588 clock may cause the interrupt event to occur if the new IEEE 1588 clock value is set equal to the current Clock Target.

The Clock Target reload function (RELOAD_ADD = 1) allows the host to pre-load the next trigger time. The add function (RELOAD_ADD = 0), allows for a repeatable event. When the Clock Target overflows, it will wrap around past 0, as will the 64-bit IEEE 1588 clock. Since the Clock Target and Reload / Add Registers are 64-bits, they require two 32-bit write cycles, one to each half, before the registers are affected. The writes may be in any order.

11.5 IEEE 1588 GPIOs

In addition to time stamping PTP packets, the IEEE 1588 clock value can be saved into a set of clock capture registers based on the GPIO[9:8] inputs. When configured as outputs, GPIO[9:8] can be used to output a signal based on an IEEE 1588 clock target compare event. Refer to Section 13.2.1, "GPIO IEEE 1588 Timestamping," on page 163 for information on using GPIO[9:8] for IEEE 1588 time stamping functions.

11.6 IEEE 1588 Interrupts

The IEEE 1588 hardware time stamp unit provides multiple interrupt conditions. These include time stamp indication on the transmitter and receiver side of each port, individual GPIO[9:8] input time stamp interrupts, and a clock comparison event interrupt. All IEEE 1588 interrupts are located in the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN) and are fully maskable via their respective enable bits. Refer to Section 14.2.5.23, "1588 Interrupt Status and Enable Register (1588_INT_STS_EN)," on page 226 for bit-level definitions of all IEEE 1588 interrupts and enables.

All IEEE 1588 interrupts are ANDed with their individual enables and then ORed, as shown in Figure 11.1, generating the 1588_EVNT bit of the Interrupt Status Register (INT_STS).

When configured as an input, GPIO[9:8] have the added functionality of clearing the Clock Target interrupt bit (1588_TIMER_INT) of the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN) on an active edge. GPIO inputs must be active for greater than 40 nS to be recognized as clear events. For more information on IEEE 1588 GPIO interrupts, refer to Section 13.2.2, "GPIO Interrupts," on page 163.

Refer to Chapter 5, "System Interrupts," on page 49 for additional information on the LAN9312 interrupts.

Chapter 12 General Purpose Timer & Free-Running Clock

This chapter details the LAN9312 General Purpose Timer (GPT) and the Free-Running Clock.

12.1 General Purpose Timer

The LAN9312 provides a 16-bit programmable General Purpose Timer that can be used to generate periodic system interrupts. The resolution of this timer is 100uS.

The GPT loads the General Purpose Timer Count Register (GPT_CNT) with the value in the GPT_LOAD field of the General Purpose Timer Configuration Register (GPT_CFG) when the TIMER_EN bit of the General Purpose Timer Configuration Register (GPT_CFG) is asserted (1). On a chip-level reset, or when the TIMER_EN bit changes from asserted (1) to de-asserted (0), the GPT_LOAD field is initialized to FFFFh. The General Purpose Timer Count Register (GPT_CNT) is also initialized to FFFFh on reset. Software can write a pre-load value into the GPT_LOAD field at any time (e.g. before or after the TIMER_EN bit is asserted).

Once enabled, the GPT counts down until it reaches 0000h, or until a new pre-load value is written to the GPT_LOAD field. At 0000h, the counter wraps around to FFFFh, asserts the GPT interrupt status bit (GPT_INT) in the Interrupt Status Register (INT_STS), asserts the IRQ interrupt (if GPT_INT_EN is set in the Interrupt Status Register (INT_STS)), and continues counting. GPT_INT is a sticky bit. Once this bit is asserted, it can only be cleared by writing a 1 to the bit. Refer to Section 5.2.7, "General Purpose Timer Interrupt," on page 53 for additional information on the GPT interrupt.

12.2 Free-Running Clock

The Free-Running Clock (FRC) is a simple 32-bit up-counter that operates from a fixed 25MHz clock. The current FRC value can be read via the Free Running 25MHz Counter Register (FREE_RUN). On assertion of a chip-level reset, this counter is cleared to zero. On de-assertion of a reset, the counter is incremented once for every 25MHz clock cycle. When the maximum count has been reached, the counter rolls over to zeros. The FRC does not generate interrupts.

Note: The free running counter can take up to 160nS to clear after a reset event.

Chapter 13 GPIO/LED Controller

13.1 Functional Overview

The GPIO/LED Controller provides 12 configurable general purpose input/output pins, GPIO[11:0]. These pins can be individually configured to function as inputs, push-pull outputs, or open drain outputs and each is capable of interrupt generation with configurable polarity. Two of the GPIO pins (GPIO[9:8]) can be used for IEEE 1588 timestamp functions, allowing GPIO driven 1588 time clock capture when configured as an input, or GPIO output generation based on an IEEE 1588 clock target compare event.

In addition, 8 of the GPIO pins can be alternatively configured as LED outputs. These pins, GPIO[7:0] (nP1LED[3:0] and nP2LED[3:0]), may be enabled to drive Ethernet status LEDs for external indication of various attributes of the switch ports.

GPIO and LED functionality is configured via the GPIO/LED System Control and Status Registers (CSRs), accessible through the Host Bus Interface (HBI). These registers are defined in Section 14.2.3, "GPIO/LED," on page 192.

13.2 GPIO Operation

The GPIO controller is comprised of 12 programmable input/output pins. These pins are individually configurable via the GPIO CSRs. On application of a chip-level reset:

- All GPIOs are set as inputs (GPDIR[11:0] cleared in General Purpose I/O Data & Direction Register (GPIO_DATA_DIR))
- All GPIO interrupts are disabled (GPIO[11:0]_INT_EN cleared in General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN)
- All GPIO interrupts are configured to low logic level triggering (GPIO_INT_POL[11:0] cleared in General Purpose I/O Configuration Register (GPIO_CFG))

Note: GPIO[7:0] may be configured as LED outputs by default, dependant on the LED_en_stap[7:0] configuration straps. Refer to Section 13.3, "LED Operation" for additional information.

The direction and buffer type of all 12 GPIOs are configured via the General Purpose I/O Configuration Register (GPIO_CFG) and General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). The direction of each GPIO, input or output, should be configured first via its respective GPIO direction bit (GPDIR[11:0]) in the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). When configured as an output, the output buffer type for each GPIO is selected by the GPIOBUF[11:0] bits in the General Purpose I/O Configuration Register (GPIO_CFG). Push/pull and open-drain output buffers are supported for each GPIO. When functioning as an open-drain driver, the GPIO output pin is driven low when the corresponding data register bit (GPIOD in the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR)) is cleared to 0, and is not driven when set to 1.

When a GPIO is enabled as an output, the value output to the GPIO pin is set via the corresponding GPIOD[11:0] bit in the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). For GPIOs configured as inputs, the corresponding GPIOD[11:0] bit reflects the current state of the GPIO input.

Note: For GPIO[9:8], the pin direction is a function of both the GPDIR[9:8] bits of the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR) and the 1588_GPIO_OE[9:8] bits in the General Purpose I/O Configuration Register (GPIO_CFG).

13.2.1 GPIO IEEE 1588 Timestamping

Two of the GPIO pins, GPIO[9:8], have the option to be used for IEEE 1588 time stamp functions. This allows a time stamp capture to be triggered when the GPIO is configured as an input, or output a signal from the GPIO based on an IEEE 1588 clock target compare event when configured as an output. Refer to Chapter 11, "IEEE 1588 Hardware Time Stamp Unit," on page 154 for additional information on the IEEE 1588 time stamping functions of the LAN9312.

13.2.1.1 IEEE 1588 GPIO Inputs

When the GPIO[9:8] pins are configured as inputs, an active edge will capture the IEEE 1588 clock into the high and low 1588 capture registers (1588_CLOCK_HI_CAPTURE_GPIO_x, and 1588_CLOCK_LO_CAPTURE_GPIO_x where “x” represents the number of the respective 1588 enabled GPIO) and set the corresponding interrupt flags GPIO[9:8]_INT and 1588_GPIO[9:8]_INT in the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN) and 1588 Interrupt Status and Enable Register (1588_INT_STS_EN) respectively. The GPIO[9:8] inputs can also be configured to clear the Clock Target interrupt (1588_TIMER_INT) in the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN) by setting the corresponding GPIO_1588_TIMER_INT_CLEAR_EN[9:8] bit in the General Purpose I/O Configuration Register (GPIO_CFG). GPIO inputs must be active for greater than 40nS to be recognized as capture or interrupt clear events.

13.2.1.2 IEEE 1588 GPIO Outputs

The GPIO[9:8] pins can be configured as IEEE 1588 enabled outputs by setting the corresponding 1588_GPIO_OE[9:8] bits in the General Purpose I/O Configuration Register (GPIO_CFG). These bits override the GPDIR[9:8] bits of the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR) and allow for GPIO output generation based on the IEEE 1588 clock target compare event. Clock target compare events occur when the value loaded into the 1588 Clock Target High-DWORD Register (1588_CLOCK_TARGET_HI) and 1588 Clock Target Low-DWORD Register (1588_CLOCK_TARGET_LO) matches the current IEEE 1588 clock value in the 1588 Clock High-DWORD Register (1588_CLOCK_HI) and 1588 Clock Low-DWORD Register (1588_CLOCK_LO).

Upon detection of a clock target compare event, GPIO[9:8] can be configured to output a 100nS pulse, toggle its output, or reflect the 1588_TIMER_INT bit in the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN) by enabling the GPIO_EVENT_9 or GPIO_EVENT_8 bits of the 1588 Configuration Register (1588_CONFIG). The clock event polarity, which determines whether the IEEE 1588 GPIO output is active high or active low, is controlled via the GPIO_EVENT_POL_9 and GPIO_EVENT_POL_8 bits of the General Purpose I/O Configuration Register (GPIO_CFG).

Note: The 1588_GPIO_OE[9:8] bits do not override the GPIO buffer type bits GPIOBUF[9:8] in the General Purpose I/O Configuration Register (GPIO_CFG).

13.2.2 GPIO Interrupts

Each GPIO of the LAN9312 provides the ability to trigger a unique GPIO interrupt in the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN). Reading the GPIO_INT[11:0] bits of this register provides the current status of the corresponding interrupt, and each interrupt is enabled by setting the corresponding GPIO_INT_EN[11:0] bit. The GPIO/LED Controller aggregates the enabled interrupt values into an internal signal which is sent to the System Interrupt Controller and is reflected via the Interrupt Status Register (INT_STS) bit 12 (GPIO). For more information on the LAN9312 interrupts, refer to Chapter 5, "System Interrupts," on page 49.

13.2.2.1 GPIO Interrupt Polarity

The interrupt polarity can be set for each individual GPIO via the GPIO_INT_POL[11:0] bits in the General Purpose I/O Configuration Register (GPIO_CFG). When set, a high logic level on the GPIO pin will set the corresponding interrupt bit in the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN). When cleared, a low logic level on the GPIO pin will set the corresponding interrupt bit. Because GPIO[9:8] have added IEEE 1588 functionality, the

GPIO_INT_POL[9:8] bits also determine the polarity of the clock events as described in Section 13.2.1.2.

13.2.2.2 IEEE 1588 GPIO Interrupts

In addition to the standard GPIO interrupts in the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN), the IEEE 1588 timestamp enabled GPIO[9:8] pins contain the ability to generate and clear specific IEEE 1588 related interrupts. When GPIO 9 or GPIO 8 are enabled as inputs and an active edge occurs, the IEEE 1588 clock capture is indicated by the 1588_GPIO9_INT and 1588_GPIO8_INT interrupts respectively in the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN). These interrupts are enabled by setting the corresponding 1588_GPIO9_EN and 1588_GPIO8_EN bits in the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN). GPIO inputs must be active for greater than 40nS to be recognized as capture events.

When GPIO 8 and GPIO 9 are enabled, the 1588 Timer Interrupt bit (1588_TIMER_INT) of the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN) can be cleared by an active edge on GPIO[9:8]. A clear is only registered when the GPIO input is active for greater than 40nS.

13.3 LED Operation

Eight pins, GPIO[7:0], are shared with LED functions (nP1LED[3:0] and nP2LED[3:0]). These pins are configured as LED outputs by setting the corresponding LED_EN bit in the LED Configuration Register (LED_CFG). When configured as a LED, the pin is an open-drain, active-low output and the GPIO related input buffer and pull-up are disabled. The LED outputs are always active low. As a result, a low signal on the LED pin equates to the LED “on”, and a high signal equates to the LED “off”.

The functions associated with each LED pin are configurable via the LED_FUN[1:0] bits of the LED Configuration Register (LED_CFG). These bits allow the configuration of each LED pin to indicate various port related functions. These functions are described in Table 13.1 followed by a detailed definition of each indication type.

The default values of the LED_FUN[1:0] and LED_EN[7:0] bits of the LED Configuration Register (LED_CFG) are determined by the LED_fun_strap[1:0] and LED_en_strap[7:0] configuration straps. For more information on the LED Configuration Register (LED_CFG) and its related straps, refer to Section 14.2.3.4, "LED Configuration Register (LED_CFG)," on page 196.

Table 13.1 LED Operation as a Function of LED_CFG[9:8]

	LED_CFG[9:8] (LED_FUN[1:0])			
	00b	**01b**	**10b**	**11b**
nP2LED3 (GPIO7)	RX Port 0	RX Port 0	Activity Port 2	-
nP2LED2 (GPIO6)	Link / Activity Port 2	100Link / Activity Port 2	Link Port 2	-
nP2LED1 (GPIO5)	Full-duplex / Collision Port 2	Full-duplex / Collision Port 2	Full-duplex / Collision Port 2	TXEN Port 2
nP2LED0 (GPIO4)	Speed Port 2	10Link / Activity Port 2	Speed Port 2	RXDV Port 2
nP1LED3 (GPIO3)	TX Port 0	TX Port 0	Activity Port 1	TXEN Port 0
nP1LED2 (GPIO2)	Link / Activity Port 1	100Link / Activity Port 1	Link Port 1	RXDV Port 0

Table 13.1 LED Operation as a Function of LED_CFG[9:8] (continued)

	LED_CFG[9:8] (LED_FUN[1:0])			
nP1LED1 (GPIO1)	Full-duplex / Collision Port 1	Full-duplex / Collision Port 1	Full-duplex / Collision Port 1	TXEN Port 1
nP1LED0 (GPIO0)	Speed Port 1	10Link / Activity Port 1	Speed Port 1	RXDV Port 1

The various LED indication functions shown in Table 13.1 are described below:

- **TX Port 0 -** The signal is pulsed low for 80mS to indicate activity from the switch fabric to the Host MAC. This signal is then driven high for a minimum of 80mS, after which the process will repeat if TX activity is again detected.
- **RX Port 0 -** The signal is pulsed low for 80mS to indicate activity from the Host MAC to the switch fabric. This signal is then driven high for a minimum of 80mS, after which the process will repeat if RX activity is again detected.
- **Link / Activity -** A steady low output indicates that the port has a valid link, while a steady high indicates no link on the port. The signal is pulsed high for 80mS to indicate transmit or receive activity on the port. The signal is then driven low for a minimum of 80mS, after which the process will repeat if RX or TX activity is again detected.
- **Full-duplex / Collision -** A steady low output indicates the port is in full-duplex mode, while a steady high indicates no link on the port. In half-duplex mode, the signal is pulsed low for 80mS to indicate a network collision. The signal is then driven high for a minimum of 80mS, after which the process will repeat if another collision is detected.
- **Speed -** A steady low output indicates the selected speed is 100Mbps. A steady high output indicates the selected speed is 10Mbps. The signal will be held high if the port does not have a valid link.
- **100Link / Activity -** A steady low output indicates the port has a valid link and the speed is 100Mbps. The signal is pulsed high for 80mS to indicate TX or RX activity on the port. The signal is then driven low for a minimum of 80mS, after which the process will repeat if RX or TX activity is again detected. The signal will be held high if the port does not have a valid link.
- **10Link / Activity -** A steady low output indicates the port has a valid link and the speed is 10Mbps. The signal is pulsed high for 80mS to indicate transmit or receive activity on the port. The signal is then driven low for a minimum of 80mS, after which the process will repeat if RX or TX activity is again detected. This signal will be held high if the port does not have a valid link.
- **Activity -** The signal is pulsed low for 80mS to indicate transmit or receive activity. The signal is then driven high for a minimum of 80mS, after which the process will repeat if RX or TX activity is again detected. The signal will be held high if the port does not have a valid link.
- **Link -** A steady low indicates the port has a valid link.
- **TXEN Port 0 -** Non-stretched TXEN signal from the switch fabric to the Host MAC.
- **RXDV Port 0 -** Non-stretched RXDV signal from the Host MAC to the switch fabric.
- **TXEN -** Non-stretched TXEN signal from the switch fabric to the PHY.
- **RXDV -** Non-stretched RXDV signal from the PHY to the switch fabric.

Chapter 14 Register Descriptions

This section describes the various LAN9312 control and status registers (CSR's). These registers are broken into 5 categories. The following sections detail the functionality and accessibility of all the LAN9312 registers within each category:

- Section 14.1, "TX/RX FIFO Ports," on page 167
- Section 14.2, "System Control and Status Registers," on page 168
- Section 14.3, "Host MAC Control and Status Registers," on page 270
- Section 14.4, "Ethernet PHY Control and Status Registers," on page 286
- Section 14.5, "Switch Fabric Control and Status Registers," on page 308

Figure 14.1 contains an overall base register memory map of the LAN9312. This memory map is not drawn to scale, and should be used for general reference only.

Note: Register bit type definitions are provided in Section 1.3, "Register Nomenclature," on page 19.

Note: Not all LAN9312 registers are memory mapped or directly addressable. For details on the accessibility of the various LAN9312 registers, refer the register sub-sections listed above.

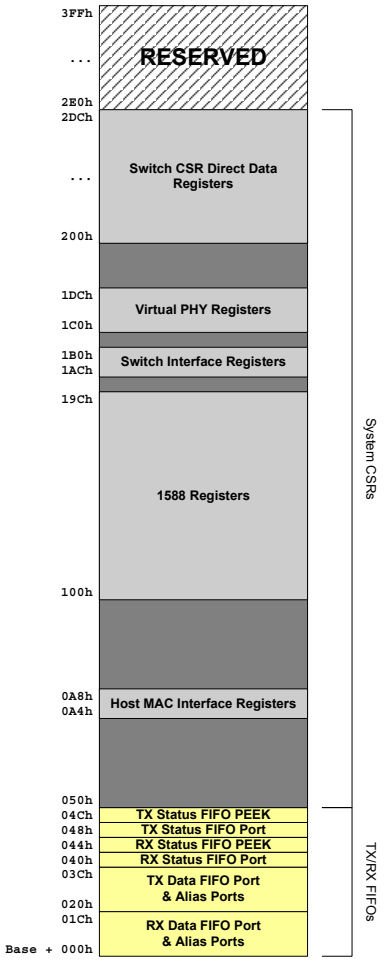


Figure 14.1 LAN9312 Base Register Memory Map

14.1 TX/RX FIFO Ports

The LAN9312 contains four host-accessible FIFO's: TX Status, RX Status, TX Data, and RX Data. These FIFO's store the incoming and outgoing address and data information, acting as a conduit between the host bus interface (HBI) and the Host MAC. The sizes of these FIFO's are configurable via the Hardware Configuration Register (HW_CFG). Refer to Section 9.7.3, "FIFO Memory Allocation Configuration," on page 121 for additional information on FIFO size configuration.

For additional information on the FIFO configuration registers accessible via the Host Bus Interface, refer to their respective register definitions located in section Section 14.2.2, "Host MAC & FIFO's".

14.1.1 TX/RX Data FIFO's

The TX and RX Data FIFO ports have the base address of 020h and 000h respectively. However, each FIFO is also accessible at seven additional contiguous memory locations, as can be seen in Figure 14.1. The Host may access the TX or RX Data FIFO's at any of these alias port locations, as they all function identically and contain the same data. This alias port addressing is implemented to allow hosts to burst through sequential addresses.

14.1.2 TX/RX Status FIFO's

The TX and RX Status FIFO's can each be read from two register locations; the Status FIFO Port, and the Status FIFO PEEK. The TX and RX Status FIFO Ports (048h and 040h respectively) will perform a destructive read, popping the data from the TX or RX Status FIFO. The TX and RX Status FIFO PEEK register locations (04Ch and 044h respectively) allow a non-destructive read of the top (oldest) location of the FIFO's.

14.1.3 Direct FIFO Access Mode

When the FIFO_SEL pin is driven high, the LAN9312 enters the direct FIFO access mode. In this mode, all host write operations are to the TX Data FIFO and all host read operations are from the RX Data FIFO. When FIFO_SEL is asserted, only the A[2] host address signal is decoded. All other address signals are ignored in this mode. When the endianess select pin (END_SEL) is low, the TX/RX Data FIFO's are accessed in little endian mode. When END_SEL is high, the TX/RX Data FIFO's are accessed in big endian mode. The A[2] input is used during Data FIFO direct PIO burst cycles to delimit DWORD accesses. For more information on endianess selection, refer to section Section 8.3, "Host Endianess".

14.2 System Control and Status Registers

The System CSR's are directly addressable memory mapped registers with a base address offset range of 050h to 2DCh. These registers are addressable by the Host via the Host Bus Interface (HBI).

Table 14.1 lists the System CSR's and their corresponding addresses in order. All system CSR's are reset to their default value on the assertion of a chip-level reset.

The System CSR's can be divided into 9 sub-categories. Each of these sub-categories contains the System CSR descriptions of the associated registers. The register descriptions are categorized as follows:

- Section 14.2.1, "Interrupts," on page 172
- Section 14.2.2, "Host MAC & FIFO's," on page 180
- Section 14.2.3, "GPIO/LED," on page 192
- Section 14.2.4, "EEPROM," on page 197
- Section 14.2.5, "IEEE 1588," on page 201
- Section 14.2.6, "Switch Fabric," on page 229
- Section 14.2.7, "PHY Management Interface (PMI)," on page 243
- Section 14.2.8, "Virtual PHY," on page 245
- Section 14.2.9, "Miscellaneous," on page 259

Table 14.1 System Control and Status Registers

ADDRESS OFFSET	SYMBOL	REGISTER NAME
050h	ID_REV	Chip ID and Revision Register, Section 14.2.9.1
054h	IRQ_CFG	Interrupt Configuration Register, Section 14.2.1.1
058h	INT_STS	Interrupt Status Register, Section 14.2.1.2
05Ch	INT_EN	Interrupt Enable Register, Section 14.2.1.3
060h	RESERVED	Reserved for Future Use
064h	BYTE_TEST	Byte Order Test Register, Section 14.2.9.2
068h	FIFO_INT	FIFO Level Interrupts Register, Section 14.2.1.4
06Ch	RX_CFG	Receive Configuration Register, Section 14.2.2.1
070h	TX_CFG	Transmit Configuration Register, Section 14.2.2.2
074h	HW_CFG	Hardware Configuration Register, Section 14.2.9.3
078h	RX_DP_CTRL	RX Datapath Control Register, Section 14.2.2.3
07Ch	RX_FIFO_INF	Receive FIFO Information Register,Section 14.2.2.4
080h	TX_FIFO_INF	Transmit FIFO Information Register, Section 14.2.2.5
084h	PMT_CTRL	Power Management Control Register, Section 14.2.9.4
088h	RESERVED	Reserved for Future Use
08Ch	GPT_CFG	General Purpose Timer Configuration Register, Section 14.2.9.5
090h	GPT_CNT	General Purpose Timer Count Register, Section 14.2.9.6
094h - 098h	RESERVED	Reserved for Future Use

Table 14.1 System Control and Status Registers (continued)

ADDRESS OFFSET	SYMBOL	REGISTER NAME
09Ch	FREE_RUN	Free Running Counter Register, Section 14.2.9.7
0A0h	RX_DROP	Host MAC RX Dropped Frames Counter Register, Section 14.2.2.6
0A4h	MAC_CSR_CMD	Host MAC CSR Interface Command Register, Section 14.2.2.7
0A4h EEPROM Loader Access Only	PMI_DATA	PHY Management Interface Data Register (EEPROM Loader Access Only), Section 14.2.7.1
0A8h	MAC_CSR_DATA	Host MAC CSR Interface Data Register, Section 14.2.2.8
0A8h EEPROM Loader Access Only	PMI_ACCESS	PHY Management Interface Access Register (EEPROM Loader Access Only), Section 14.2.7.2
0ACh	AFC_CFG	Host MAC Automatic Flow Control Configuration Register, Section 14.2.2.9
0B0h - 0FCh	RESERVED	Reserved for Future Use
100h	1588_CLOCK_HI_RX_CAPTURE_1	Port 1 1588 Clock High-DWORD Receive Capture Register, Section 14.2.5.1
104h	1588_CLOCK_LO_RX_CAPTURE_1	Port 1 1588 Clock Low-DWORD Receive Capture Register, Section 14.2.5.2
108h	1588_SEQ_ID_SRC_UUID_HI_RX_CAPTURE_1	Port 1 1588 Sequence ID, Source UUID High-WORD Receive Capture Register, Section 14.2.5.3
10Ch	1588_SRC_UUID_LO_RX_CAPTURE_1	Port 1 1588 Source UUID Low-DWORD Receive Capture Register, Section 14.2.5.4
110h	1588_CLOCK_HI_TX_CAPTURE_1	Port 1 1588 Clock High-DWORD Transmit Capture Register, Section 14.2.5.5
114h	1588_CLOCK_LO_TX_CAPTURE_1	Port 1 1588 Clock Low-DWORD Transmit Capture Register, Section 14.2.5.6
118h	1588_SEQ_ID_SRC_UUID_HI_TX_CAPTURE_1	Port 1 1588 Sequence ID, Source UUID High-WORD Transmit Capture Register, Section 14.2.5.7
11C	1588_SRC_UUID_LO_TX_CAPTURE_1	Port 1 1588 Source UUID Low-DWORD Transmit Capture Register, Section 14.2.5.8
120h	1588_CLOCK_HI_RX_CAPTURE_2	Port 2 1588 Clock High-DWORD Receive Capture Register, Section 14.2.5.1
124h	1588_CLOCK_LO_RX_CAPTURE_2	Port 2 1588 Clock Low-DWORD Receive Capture Register, Section 14.2.5.2
128h	1588_SEQ_ID_SRC_UUID_HI_RX_CAPTURE_2	Port 2 1588 Sequence ID, Source UUID High-WORD Receive Capture Register, Section 14.2.5.3
12Ch	1588_SRC_UUID_LO_RX_CAPTURE_2	Port 2 1588 Source UUID Low-DWORD Receive Capture Register, Section 14.2.5.4
130h	1588_CLOCK_HI_TX_CAPTURE_2	Port 2 1588 Clock High-DWORD Transmit Capture Register, Section 14.2.5.5
134h	1588_CLOCK_LO_TX_CAPTURE_2	Port 2 1588 Clock Low-DWORD Transmit Capture Register, Section 14.2.5.6
138h	1588_SEQ_ID_SRC_UUID_HI_TX_CAPTURE_2	Port 2 1588 Sequence ID, Source UUID High-WORD Transmit Capture Register, Section 14.2.5.7

Table 14.1 System Control and Status Registers (continued)

ADDRESS OFFSET	SYMBOL	REGISTER NAME
13Ch	1588_SRC_UUID_LO_TX_CAPTURE_2	Port 2 1588 Source UUID Low-DWORD Transmit Capture Register, Section 14.2.5.8
140h	1588_CLOCK_HI_RX_CAPTURE_MII	Port 0 1588 Clock High-DWORD Receive Capture Register, Section 14.2.5.1
144h	1588_CLOCK_LO_RX_CAPTURE_MII	Port 0 1588 Clock Low-DWORD Receive Capture Register, Section 14.2.5.2
148h	1588_SEQ_ID_SRC_UUID_HI_RX_CAPTURE_MII	Port 0 1588 Sequence ID, Source UUID High-WORD Receive Capture Register, Section 14.2.5.3
14Ch	1588_SRC_UUID_LO_RX_CAPTURE_MII	Port 0 1588 Source UUID Low-DWORD Receive Capture Register, Section 14.2.5.4
150h	1588_CLOCK_HI_TX_CAPTURE_MII	Port 0 1588 Clock High-DWORD Transmit Capture Register, Section 14.2.5.5
154h	1588_CLOCK_LO_TX_CAPTURE_MII	Port 0 1588 Clock Low-DWORD Transmit Capture Register, Section 14.2.5.6
158h	1588_SEQ_ID_SRC_UUID_HI_TX_CAPTURE_MII	Port 0 1588 Sequence ID, Source UUID High-WORD Transmit Capture Register, Section 14.2.5.7
15Ch	1588_SRC_UUID_LO_TX_CAPTURE_MII	Port 0 1588 Source UUID Low-DWORD Transmit Capture Register, Section 14.2.5.8
160h	1588_CLOCK_HI_CAPTURE_GPIO_8	GPIO 8 1588 Clock High-DWORD Capture Register, Section 14.2.5.9
164h	1588_CLOCK_LO_CAPTURE_GPIO_8	GPIO 8 1588 Clock Low-DWORD Capture Register, Section 14.2.5.10
168h	1588_CLOCK_HI_CAPTURE_GPIO_9	GPIO 9 1588 Clock High-DWORD Capture Register, Section 14.2.5.11
16Ch	1588_CLOCK_LO_CAPTURE_GPIO_9	GPIO 9 1588 Clock Low-DWORD Capture Register, Section 14.2.5.12
170h	1588_CLOCK_HI	1588 Clock High-DWORD Register, Section 14.2.5.13
174h	1588_CLOCK_LO	1588 Clock Low-DWORD Register, Section 14.2.5.14
178h	1588_CLOCK_ADDEND	1588 Clock Addend Register, Section 14.2.5.15
17Ch	1588_CLOCK_TARGET_HI	1588 Clock Target High-DWORD Register, Section 14.2.5.16
180h	1588_CLOCK_TARGET_LO	1588 Clock Target Low-DWORD Register, Section 14.2.5.17
184h	1588_CLOCK_TARGET_RELOAD_HI	1588 Clock Target Reload High-DWORD Register, Section 14.2.5.18
188h	1588_CLOCK_TARGET_RELOAD_LO	1588 Clock Target Reload/Add Low-DWORD Register, Section 14.2.5.19
18Ch	1588_AUX_MAC_HI	1588 Auxiliary MAC Address High-WORD Register, Section 14.2.5.20
190h	1588_AUX_MAC_LO	1588 Auxiliary MAC Address Low-DWORD Register, Section 14.2.5.21
194h	1588_CONFIG	1588 Configuration Register, Section 14.2.5.22
198h	1588_INT_STS_EN	1588 Interrupt Status Enable Register, Section 14.2.5.23
19Ch	1588_CMD	1588 Command Register, Section 14.2.5.24

Table 14.1 System Control and Status Registers (continued)

ADDRESS OFFSET	SYMBOL	REGISTER NAME
1A0h	MANUAL_FC_1	Port 1 Manual Flow Control Register, Section 14.2.6.1
1A4h	MANUAL_FC_2	Port 2 Manual Flow Control Register, Section 14.2.6.2
1A8h	MANUAL_FC_MII	Port 0 Flow Control Register, Section 14.2.6.3
1ACh	SWITCH_CSR_DATA	Switch Fabric CSR Interface Data Register, Section 14.2.6.4
1B0h	SWITCH_CSR_CMD	Switch Fabric CSR Interface Command Register, Section 14.2.6.5
1B4h	E2P_CMD	EEPROM Command Register, Section 14.2.4.1
1B8h	E2P_DATA	EEPROM Data Register, Section 14.2.4.2
1BCh	LED_CFG	LED Configuration Register, Section 14.2.3.4
1C0h	VPHY_BASIC_CTRL	Virtual PHY Basic Control Register, Section 14.2.8.1
1C4h	VPHY_BASIC_STATUS	Virtual PHY Basic Status Register, Section 14.2.8.2
1C8h	VPHY_ID_MSB	Virtual PHY Identification MSB Register, Section 14.2.8.3
1CCh	VPHY_ID_LSB	Virtual PHY Identification LSB Register, Section 14.2.8.4
1D0h	VPHY_AN_ADV	Virtual PHY Auto-Negotiation Advertisement Register, Section 14.2.8.5
1D4h	VPHY_AN_LP_BASE_ABILITY	Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register, Section 14.2.8.6
1D8h	VPHY_AN_EXP	Virtual PHY Auto-Negotiation Expansion Register, Section 14.2.8.7
1DCh	VPHY_SPECIAL_CONTROL_STATUS	Virtual PHY Special Control/Status Register, Section 14.2.8.8
1E0h	GPIO_CFG	General Purpose I/O Configuration Register, Section 14.2.3.1
1E4h	GPIO_DATA_DIR	General Purpose I/O Data & Direction Register, Section 14.2.3.2
1E8h	GPIO_INT_STS_EN	General Purpose I/O Interrupt Status and Enable Register, Section 14.2.3.3
1ECh	RESERVED	Reserved for Future Use
1F0h	SWITCH_MAC_ADDRH	Switch MAC Address High Register, Section 14.2.6.6
1F4h	SWITCH_MAC_ADDRL	Switch MAC Address Low Register, Section 14.2.6.7
1F8h	RESET_CTL	Reset Control Register, Section 14.2.9.8
1FCh	RESERVED	Reserved for Future Use
200h-2DCh	SWITCH_CSR_DIRECT_DATA	Switch Engine CSR Interface Direct Data Register, Section 14.2.6.8
2E0h-3FFh	RESERVED	Reserved for Future Use

14.2.1 Interrupts

This section details the interrupt related System CSR's. These registers control, configure, and monitor the IRQ interrupt output pin and the various LAN9312 interrupt sources. For more information on the LAN9312 interrupts, refer to Chapter 5, "System Interrupts," on page 49.

14.2.1.1 Interrupt Configuration Register (IRQ_CFG)

Offset: 054h Size: 32 bits

This read/write register configures and indicates the state of the IRQ signal.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**Interrupt De-assertion Interval (INT_DEAS)** This field determines the Interrupt Request De-assertion Interval in multiples of 10 microseconds. Setting this field to zero causes the device to disable the INT_DEAS Interval, reset the interval counter and issue any pending interrupts. If a new, non-zero value is written to this field, any subsequent interrupts will obey the new setting. This field does not apply to the PME_INT interrupt.	R/W	00h
23:15	**RESERVED**	RO	-
14	**Interrupt De-assertion Interval Clear (INT_DEAS_CLR)** Writing a 1 to this register clears the de-assertion counter in the Interrupt Controller, thus causing a new de-assertion interval to begin (regardless of whether or not the Interrupt Controller is currently in an active de-assertion interval). **0: Normal operation** **1: Clear de-assertion counter**	R/W SC	0h
13	**Interrupt De-assertion Status (INT_DEAS_STS)** When set, this bit indicates that interrupts are currently in a de-assertion interval, and will not be sent to the IRQ pin. When this bit is clear, interrupts are not currently in a de-assertion interval, and will be sent to the IRQ pin. **0: No interrupts in de-assertion interval** **1: Interrupts in de-assertion interval**	RO SC	0b
12	**Master Interrupt (IRQ_INT)** This read-only bit indicates the state of the internal IRQ line, regardless of the setting of the IRQ_EN bit, or the state of the interrupt de-assertion function. When this bit is set, one of the enabled interrupts is currently active. **0: No enabled interrupts active** **1: One or more enabled interrupts active**	RO	0b
11:9	**RESERVED**	RO	-
8	**IRQ Enable (IRQ_EN)** This bit controls the final interrupt output to the IRQ pin. When clear, the IRQ output is disabled and permanently de-asserted. This bit has no effect on any internal interrupt status bits. **0: Disable output on IRQ pin** **1: Enable output on IRQ pin**	R/W	0b
7:5	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
4	**IRQ Polarity (IRQ_POL)** When cleared, this bit enables the IRQ line to function as an active low output. When set, the IRQ output is active high. When the IRQ is configured as an open-drain output (via the IRQ_TYPE bit), this bit is ignored, and the interrupt is always active low. **0: IRQ active low output** **1: IRQ active high output**	R/W NASR Note 14.1	0b
3:1	**RESERVED**	RO	-
0	**IRQ Buffer Type (IRQ_TYPE)** When this bit is cleared, the IRQ pin functions as an open-drain output for use in a wired-or interrupt configuration. When set, the IRQ is a push-pull driver. **Note:** When configured as an open-drain output, the IRQ_POL bit is ignored and the interrupt output is always active low. **0: IRQ pin open-drain output** **1: IRQ pin push-pull driver**	R/W NASR Note 14.1	0b

Note 14.1 Register bits designated as NASR are not reset when either the SRST bit in the Hardware Configuration Register (HW_CFG) register or the DIGITAL_RST bit in the Reset Control Register (RESET_CTL) is set.

14.2.1.2 Interrupt Status Register (INT_STS)

Offset: 058h Size: 32 bits

This register contains the current status of the generated interrupts. A value of 1 indicates the corresponding interrupt conditions have been met, while a value of 0 indicates the interrupt conditions have not been met. The bits of this register reflect the status of the interrupt source regardless of whether the source has been enabled as an interrupt in the Interrupt Enable Register (INT_EN). Where indicated as R/WC, writing a 1 to the corresponding bits acknowledges and clears the interrupt.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**Software Interrupt (SW_INT)** This interrupt is generated when the SW_INT_EN bit of the Interrupt Enable Register (INT_EN) is set high. Writing a one clears this interrupt.	R/WC	0b
30	**Device Ready (READY)** This interrupt indicates that the LAN9312 is ready to be accessed after a power-up or reset condition.	R/WC	0b
29	**1588 Interrupt Event (1588_EVNT)** This bit indicates an interrupt event from the IEEE 1588 module. This bit should be used in conjunction with the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN) to determine the source of the interrupt event within the 1588 module.	RO	0b
28	**Switch Fabric Interrupt Event (SWITCH_INT)** This bit indicates an interrupt event from the Switch Fabric. This bit should be used in conjunction with the Switch Global Interrupt Pending Register (SW_IPR) to determine the source of the interrupt event within the Switch Fabric.	RO	0b
27	**Port 2 PHY Interrupt Event (PHY_INT2)** This bit indicates an interrupt event from the Port 2 PHY. The source of the interrupt can be determined by polling the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x).	RO	0b
26	**Port 1 PHY Interrupt Event (PHY_INT1)** This bit indicates an interrupt event from the Port 1 PHY. The source of the interrupt can be determined by polling the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x).	RO	0b
25	**TX Stopped (TXSTOP_INT)** This interrupt is issued when STOP_TX bit in Transmit Configuration Register (TX_CFG) is set, and the Host MAC transmitter is halted.	R/WC	0b
24	**RX Stopped (RXSTOP_INT)** This interrupt is issued when the Host MAC receiver is halted.	R/WC	0b
23	**RX Dropped Frame Counter Halfway (RXDFH_INT)** This interrupt is issued when the Host MAC RX Dropped Frames Counter Register (RX_DROP) counts past its halfway point (7FFFFFFFh to 80000000h).	R/WC	0b
22	**RESERVED**	RO	-
21	**TX IOC Interrupt (TX_IOC)** This interrupt is generated when a buffer with the IOC flag set has been fully loaded into the TX Data FIFO.	R/WC	0b
20	**RX DMA Interrupt (RXD_INT)** This interrupt is issued when the amount of data programmed in the RX DMA Count (RX_DMA_CNT) field of the Receive Configuration Register (RX_CFG) has been transferred out of the RX Data FIFO.	R/WC	0b

BITS	DESCRIPTION	TYPE	DEFAULT
19	**GP Timer (GPT_INT)** This interrupt is issued when the General Purpose Timer Count Register (GPT_CNT) wraps past zero to FFFFh.	R/WC	0b
18	**RESERVED**	RO	-
17	**Power Management Interrupt Event (PME_INT)** This interrupt is issued when a Power Management Event is detected as configured in the Power Management Control Register (PMT_CTRL). This interrupt functions independent of the PME signal, and will still function if the PME signal is disabled. Writing a '1' clears this bit regardless of the state of the PME hardware signal. In order to clear this bit, all unmasked bits in the Power Management Control Register (PMT_CTRL) must first be cleared. **Note:** The Interrupt De-assertion interval does not apply to the PME interrupt.	R/WC	0b
16	**TX Status FIFO Overflow (TXSO)** This interrupt is generated when the TX Status FIFO overflows.	R/WC	0b
15	**Receive Watchdog Time-out (RWT)** This interrupt is generated when a packet larger than 2048 bytes has been received by the Host MAC. **Note:** This can occur when the switch engine adds a tag to a non-tagged jumbo packet that is originally larger than 2044 bytes.	R/WC	0b
14	**Receiver Error (RXE)** Indicates that the Host MAC receiver has encountered an error. Please refer to Section 9.9.5, "Receiver Errors," on page 136 for a description of the conditions that will cause an RXE.	R/WC	0b
13	**Transmitter Error (TXE)** When generated, indicates that the Host MAC transmitter has encountered an error. Please refer to Section 9.8.7, "Transmitter Errors," on page 131 for a description of the conditions that will cause a TXE.	R/WC	0b
12	**GPIO Interrupt Event (GPIO)** This bit indicates an interrupt event from the General Purpose I/O. The source of the interrupt can be determined by polling the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN)	RO	0b
11	**RESERVED**	RO	-
10	**TX Data FIFO Overrun Interrupt (TDFO)** This interrupt is generated when the TX Data FIFO is full, and another write is attempted.	R/WC	0b
9	**TX Data FIFO Available Interrupt (TDFA)** This interrupt is generated when the TX Data FIFO available space is greater than the programmed level in the TX Data Available Level field of the FIFO Level Interrupt Register (FIFO_INT).	R/WC	0b
8	**TX Status FIFO Full Interrupt (TSFF)** This interrupt is generated when the TX Status FIFO is full.	R/WC	0b
7	**TX Status FIFO Level Interrupt (TSFL)** This interrupt is generated when the TX Status FIFO reaches the programmed level in the TX Status Level field of the FIFO Level Interrupt Register (FIFO_INT).	R/WC	0b
6	**RX Dropped Frame Interrupt (RXDF_INT)** This interrupt is issued whenever a receive frame is dropped by the Host MAC.	R/WC	0b
5	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
4	**RX Status FIFO Full Interrupt (RSFF)** This interrupt is generated when the RX Status FIFO is full.	R/WC	0b
3	**RX Status FIFO Level Interrupt (RSFL)** This interrupt is generated when the RX Status FIFO reaches the programmed level in the RX Status Level field of the FIFO Level Interrupt Register (FIFO_INT).	R/WC	0b
2:0	**RESERVED**	RO	-

14.2.1.3 Interrupt Enable Register (INT_EN)

Offset: 05Ch Size: 32 bits

This register contains the interrupt enables for the IRQ output pin. Writing 1 to any of the bits enables the corresponding interrupt as a source for IRQ. Bits in the Interrupt Status Register (INT_STS) register will still reflect the status of the interrupt source regardless of whether the source is enabled as an interrupt in this register (with the exception of SW_INT_EN). For descriptions of each interrupt, refer to the Interrupt Status Register (INT_STS) bits, which mimic the layout of this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**Software Interrupt Enable (SW_INT_EN)**	R/W	0b
30	**Device Ready Enable (READY_EN)**	R/W	0b
29	**1588 Interrupt Event Enable (1588_EVNT_EN)**	R/W	0b
28	**Switch Engine Interrupt Event Enable (SWITCH_INT_EN)**	R/W	0b
27	**Port 2 PHY Interrupt Event Enable (PHY_INT2_EN)**	R/W	0b
26	**Port 1 PHY Interrupt Event Enable (PHY_INT1_EN)**	R/W	0b
25	**TX Stopped Interrupt Enable (TXSTOP_INT_EN)**	R/W	0b
24	**RX Stopped Interrupt Enable (RXSTOP_INT_EN)**	R/W	0b
23	**RX Dropped Frame Counter Halfway Interrupt Enable (RXDFH_INT_EN)**	R/W	0b
22	**RESERVED**	RO	-
21	**TX IOC Interrupt Enable (TIOC_INT_EN)**	R/W	0b
20	**RX DMA Interrupt Enable (RXD_INT_EN)**	R/W	0b
19	**GP Timer Interrupt Enable (GPT_INT_EN)**	R/W	0b
18	**RESERVED**	RO	-
17	**Power Management Event Interrupt Enable (PME_INT_EN)**	R/W	0b
16	**TX Status FIFO Overflow Interrupt Enable (TXSO_EN)**	R/W	0b
15	**Receive Watchdog Time-out Interrupt Enable (RWT_INT_EN)**	R/W	0b
14	**Receiver Error Interrupt Enable (RXE_INT_EN)**	R/W	0b
13	**Transmitter Error Interrupt Enable (TXE_INT_EN)**	R/W	0b
12	**GPIO Interrupt Event Enable (GPIO_EN)**	R/W	0b
11	**RESERVED - This bit must be written with 0b for proper operation.**	R/W	0b
10	**TX Data FIFO Overrun Interrupt Enable (TDFO_EN)**	R/W	0b
9	**TX Data FIFO Available Interrupt Enable (TDFA_EN)**	R/W	0b
8	**TX Status FIFO Full Interrupt Enable (TSFF_EN)**	R/W	0b
7	**TX Status FIFO Level Interrupt Enable (TSFL_EN)**	R/W	0b
6	**RX Dropped Frame Interrupt Enable (RXDF_INT_EN)**	R/W	0b

BITS	DESCRIPTION	TYPE	DEFAULT
5	**RESERVED - This bit must be written with 0b for proper operation.**	R/W	0b
4	**RX Status FIFO Full Interrupt Enable (RSFF_EN)**	R/W	0b
3	**RX Status FIFO Level Interrupt Enable (RSFL_EN)**	R/W	0b
2:0	**RESERVED**	RO	-

14.2.1.4 FIFO Level Interrupt Register (FIFO_INT)

Offset: 068h Size: 32 bits

This read/write register configures the limits where the RX/TX Data and Status FIFO's will generate system interrupts.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**TX Data Available Level** The value in this field sets the level, in number of 64 Byte blocks, at which the TX Data FIFO Available Interrupt (TDFA) will be generated. When the TX Data FIFO free space is greater than this value, a TX Data FIFO Available Interrupt (TDFA) will be generated in the Interrupt Status Register (INT_STS).	R/W	48h
23:16	**TX Status Level** The value in this field sets the level, in number of DWORD's, at which the TX Status FIFO Level Interrupt (TSFL) will be generated. When the TX Status FIFO used space is greater than this value, a TX Status FIFO Level Interrupt (TSFL) will be generated in the Interrupt Status Register (INT_STS).	R/W	00h
15:8	**RESERVED - This field must be written with 00h for proper operation.**	R/W	00h
7:0	**RX Status Level** The value in this field sets the level, in number of DWORD's, at which the RX Status FIFO Level Interrupt (RSFL) will be generated. When the RX Status FIFO used space is greater than this value, a RX Status FIFO Level Interrupt (RSFL) will be generated in the Interrupt Status Register (INT_STS).	R/W	00h

14.2.2 Host MAC & FIFO's

This section details the Host MAC and TX/RX FIFO related System CSR's.

These Host Bus Interface accessible registers allow for the configuration of the TX/RX FIFO's, Host MAC and indirect access to the complete set of Host MAC CSR's. The Host MAC CSR's are accessible through the Host Bus Interface via the Host MAC CSR Interface Command Register (MAC_CSR_CMD) and Host MAC CSR Interface Data Register (MAC_CSR_DATA).

Note: For more information on the TX/RX FIFO's, refer to Section 14.1, "TX/RX FIFO Ports".

Note: The full list of Host MAC CSR's are described in Section 14.3, "Host MAC Control and Status Registers," on page 270. For more information on the Host MAC, refer to Chapter 9, "Host MAC," on page 112.

14.2.2.1 Receive Configuration Register (RX_CFG)

Offset: 06Ch Size: 32 bits

This register controls the Host MAC receive engine.

BITS	DESCRIPTION	TYPE	DEFAULT
31:30	**RX End Alignment (RX_EA)** This field specifies the alignment that must be maintained on the last data transfer of a buffer. The LAN9312 will add extra DWORD's of data up to the alignment specified in the table below. The host is responsible for removing these extra DWORD's. This mechanism can be used to maintain cache line alignment on host processors. **Note:** The desired RX End Alignment must be set before reading a packet. The RX End Alignment can be changed between reading receive packets, but must not be changed if the packet is partially read.	R/W	00b
29:28	**RESERVED**	RO	-
27:16	**RX DMA Count (RX_DMA_CNT)** This 12-bit field indicates the amount of data, in DWORD's, to be transferred out of the RX Data FIFO before asserting the RX DMA Interrupt (RXD_INT). After being set, this field is decremented for each DWORD of data that is read from the RX Data FIFO. This field can be overwritten with a new value before it reaches zero.	R/W	000h

BIT VALUES [31:30]	END ALIGNMENT
00	4-Byte Alignment
01	16-Byte Alignment
10	32-Byte Alignment
11	RESERVED

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Force RX Discard (RX_DUMP)** When a 1 is written to this bit, the RX Data and Status FIFO's are cleared of all pending data and the RX data and status pointers are cleared to zero. **Note:** Please refer to Section 9.9.1.2, "Force Receiver Discard (Receiver Dump)," on page 134 for a detailed description regarding the use of RX_DUMP.	WO SC	0b
14:13	**RESERVED**	RO	-
12:8	**RX Data Offset (RXDOFF)** This field controls the offset value, in bytes, that is added to the beginning of an RX data packet. The start of the valid data will be shifted by the number of bytes specified in this field. An offset of 0-31 bytes is a valid number of offset bytes. **Note:** The two LSBs of this field (D[9:8]) must not be modified while the RX is running. The receiver must be halted, and all data purged before these two bits can be modified. The upper three bits (DWORD offset) may be modified while the receiver is running. Modifications to the upper bits will take affect on the next DWORD read.	R/W	00000b
7:0	**RESERVED**	RO	-

14.2.2.2 Transmit Configuration Register (TX_CFG)

Offset: 070h Size: 32 bits

This register controls the Host MAC transmit functions.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15	**Force TX Status Discard (TXS_DUMP)** When a 1 is written to this bit, the TX Status FIFO is cleared of all pending status DWORD's and the TX status pointers are cleared to zero.	WO SC	0b
14	**Force TX Data Discard (TXD_DUMP)** When a 1 is written to this bit, the TX Data FIFO is cleared of all pending data and the TX data pointers are cleared to zero.	WO SC	0b
13:3	**RESERVED**	RO	-
2	**TX Status Allow Overrun (TXSAO)** When this bit is cleared, Host MAC data transmission is suspended if the TX Status FIFO becomes full. Setting this bit high allows the transmitter to continue operation with a full TX Status FIFO. **Note:** This bit does not affect the operation of the TX Status FIFO Full Interrupt (TSFF).	R/W	0b
1	**Transmitter Enable (TX_ON)** When this bit is set, the Host MAC transmitter is enabled. Any data in the TX Data FIFO will be sent. This bit is cleared automatically when the STOP_TX bit is set and the transmitter is halted.	R/W	0b
0	**Stop Transmitter (STOP_TX)** When this bit is set, the Host MAC transmitter will finish the current frame, and will then stop transmitting. When the transmitter has stopped this bit will clear. All writes to this bit are ignored while this bit is high.	R/W SC	0b

14.2.2.3 Receive Datapath Control Register (RX_DP_CTRL)

Offset: 078h Size: 32 bits

This register is used to discard unwanted receive frames.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**RX Data FIFO Fast Forward (RX_FFWD)** Writing a 1 to this bit causes the RX Data FIFO to fast-forward to the start of the next frame. This bit will remain high until the RX Data FIFO fast-forward operation has completed. No reads should be issued to the RX Data FIFO while this bit is high. **Note:** Please refer to section Section 9.9.1.1, "Receive Data FIFO Fast Forward," on page 134 for detailed information regarding the use of RX_FFWD.	R/W SC	0h
30:0	**RESERVED**	RO	-

14.2.2.4 RX FIFO Information Register (RX_FIFO_INF)

Offset: 07Ch Size: 32 bits

This register contains the indication of used space in the RX FIFO's.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:16	**RX Status FIFO Used Space (RXSUSED)** This field indicates the amount of space, in DWORD's, currently used in the RX Status FIFO.	RO	0b
15:0	**RX Data FIFO Used Space (RXDUSED)** This field indicates the amount of space, in bytes, used in the RX Data FIFO. For each receive frame, the field is incremented by the length of the receive data. In cases where the payload does not end on a DWORD boundary, the total will be rounded up to the nearest DWORD.	RO	0b

14.2.2.5 TX FIFO Information Register (TX_FIFO_INF)

Offset: 080h Size: 32 bits

This register contains the indication of free space in the TX Data FIFO and the used space in the TX Status FIFO.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:16	**TX Status FIFO Used Space (TXSUSED)** This field indicates the amount of space, in DWORD's, currently used in the TX Status FIFO.	RO	0b
15:0	**TX Data FIFO Free Space (TXFREE)** This field indicates the amount of space, in bytes, available in the TX Data FIFO. The application should never write more than is available, as indicated by this value.	RO	1200h

14.2.2.6 Host MAC RX Dropped Frames Counter Register (RX_DROP)

Offset: 0A0h Size: 32 bits

This register indicates the number of receive frames that have been dropped by the Host MAC.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Dropped Frame Counter (RX_DFC)** This counter is incremented every time a receive frame is dropped by the Host MAC. RX_DFC is cleared on any read of this register. **Note:** The interrupt RXDFH_INT (bit 23 of the Interrupt Status Register (INT_STS)) can be issued when this counter passes through its halfway point (7FFFFFFFh to 80000000h).	RC	00000000h

14.2.2.7 Host MAC CSR Interface Command Register (MAC_CSR_CMD)

Offset: 0A4h Size: 32 bits

This read-write register is used to control the read and write operations to/from the Host MAC. This register in used in conjunction with the Host MAC CSR Interface Data Register (MAC_CSR_DATA) to indirectly access the Host MAC CSR's.

Note: The full list of Host MAC CSR's are described in Section 14.3, "Host MAC Control and Status Registers," on page 270. For more information on the Host MAC, refer to Chapter 9, "Host MAC," on page 112.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**CSR Busy** When a 1 is written into this bit, the read or write operation is performed to the specified Host MAC CSR. This bit will remain set until the operation is complete. In the case of a read, this indicates that the host can read valid data from the Host MAC CSR Interface Data Register (MAC_CSR_DATA). **Note:** The MAC_CSR_CMD and MAC_CSR_DATA registers must not be modified until this bit is cleared.	R/W SC	0b
30	**R/nW** When set, this bit indicates that the host is requesting a read operation. When clear, the host is performing a write. **0: Host MAC CSR Write Operation** **1: Host MAC CSR Read Operation**	R/W	0b
29:8	**RESERVED**	RO	-
7:0	**CSR Address** The 8-bit value in this field selects which Host MAC CSR will be accessed by the read or write operation. The index of each Host MAC CSR is defined in Section 14.3, "Host MAC Control and Status Registers," on page 270.	R/W	00h

14.2.2.8 Host MAC CSR Interface Data Register (MAC_CSR_DATA)

Offset: 0A8h Size: 32 bits

This read-write register is used in conjunction with the Host MAC CSR Interface Command Register (MAC_CSR_CMD) to indirectly access the Host MAC CSR's.

Note: The full list of Host MAC CSR's are described in Section 14.3, "Host MAC Control and Status Registers," on page 270. For more information on the Host MAC, refer to Chapter 9, "Host MAC," on page 112.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Host MAC CSR Data** This field contains the value read from or written to the Host MAC CSR as specified in the Host MAC CSR Interface Command Register (MAC_CSR_CMD). Upon a read, the value returned depends on the R/nW bit in the MAC_CSR_CMD register. If R/nW is a 1, the data in this register is from the Host MAC. If R/nW is 0, the data is the value that was last written into this register. **Note:** The MAC_CSR_CMD and MAC_CSR_DATA registers must not be modified until the CSR Busy bit is cleared in the MAC_CSR_CMD register.	R/W	00000000h

14.2.2.9 Host MAC Automatic Flow Control Configuration Register (AFC_CFG)

Offset: 0ACh Size: 32 bits

This read/write register configures the mechanism that controls the automatic and software-initiated transmission of pause frames and back pressure from the Host MAC to the switch fabric. This register is used in conjunction with the Host MAC Flow Control Register (HMAC_FLOW) in the Host MAC CSR space. Pause frames and backpressure are sent to the switch fabric to stop it from sending packets to the Host MAC. Network data into the switch fabric is affected only if the switch fabric buffering fills.

Note: The Host MAC will not transmit pause frames or assert back pressure if the transmitter is disabled. This register controls only the Host MAC flow control and not the Switch Engine MAC's flow control.

Refer to section Section 9.2, "Flow Control" for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:16	**Automatic Flow Control High Level (AFC_HI)** This field specifies, in multiples of 64 bytes, the level at which flow control will trigger. When this limit is reached, the chip will apply back pressure or will transmit a pause frame as programmed in bits [3:0] of this register. During full-duplex operation only a single pause frame is transmitted when this level is reached. The pause time transmitted in this frame is programmed in the FCPT field of the Host MAC Flow Control Register (HMAC_FLOW) in the Host MAC CSR space. During half-duplex operation each incoming frame that matches the criteria in bits [3:0] of this register will be jammed for the period set in the BACK_DUR field. **Note:** This level is also used for hard-wired flow control when HW_FC_EN is set in the Port 0(Host MAC) Manual Flow Control Register (MANUAL_FC_MII).	R/W	00h
15:8	**Automatic Flow Control Low Level (AFC_LO)** This field specifies, in multiples of 64 bytes, the level at which a pause frame is transmitted with a pause time setting of zero. When the amount of data in the RX Data FIFO falls below this level the pause frame is transmitted. A pause time value of zero instructs the other transmitting device to immediately resume transmission. The zero time pause frame will only be transmitted if the RX Data FIFO had reached the AFC_HI level and a pause frame was sent. A zero pause time frame is sent whenever automatic flow control in enabled in bits [3:0] of this register. **Note:** When automatic flow control is enabled the AFC_LO setting must always be less than the AFC_HI setting. **Note:** This level is also used for hard-wired flow control when HW_FC_EN is set in the Port 0(Host MAC) Manual Flow Control Register (MANUAL_FC_MII).	R/W	00h
7:4	**Backpressure Duration (BACK_DUR)** When the Host MAC automatically asserts back pressure, it will be asserted for this period of time. In full-duplex mode, this field has no function and is not used. Please refer to Table 14.2, describing Backpressure Duration bit mapping for more information.	R/W	0h

BITS	DESCRIPTION	TYPE	DEFAULT
3	**Flow Control on Multicast Frame (FCMULT)** When this bit is set, the Host MAC will assert back pressure when the AFC level is reached and a multicast frame is received. This field has no function in full-duplex mode. **0: Flow Control on Multicast Frame Disabled** **1: Flow Control on Multicast Frame Enabled**	R/W	0b
2	**Flow Control on Broadcast Frame (FCBRD)** When this bit is set, the Host MAC will assert back pressure when the AFC level is reached and a broadcast frame is received. This field has no function in full-duplex mode. **0: Flow Control on Broadcast Frame Disabled** **1: Flow Control on Broadcast Frame Enabled**	R/W	0b
1	**Flow Control on Address Decode (FCADD)** When this bit is set, the Host MAC will assert back pressure when the AFC level is reached and a frame addressed to the Host MAC is received. This field has no function in full-duplex mode. **0: Flow Control on Address Decode Disabled** **1: Flow Control on Address Decode Enabled**	R/W	0b
0	**Flow Control on Any Frame (FCANY)** When this bit is set, the Host MAC will assert back pressure, or transmit a pause frame when the AFC level is reached and any frame is received. Setting this bit enables full-duplex flow control when the Host MAC is operating in full-duplex mode. When this mode is enabled during half-duplex operation, the Flow Controller does not decode the Host MAC address and will send a JAM upon receipt of a valid preamble (i.e., immediately at the beginning of the next frame after the RX Data FIFO level is reached). When this mode is enabled during full-duplex operation, the Flow Controller will immediately instruct the Host MAC to send a pause frame when the RX Data FIFO level is reached. The MAC will queue the pause frame transmission for the next available window. Setting this bit overrides bits [3:1] of this register.	R/W	0b

Table 14.2 Backpressure Duration Bit Mapping

	BACKPRESSURE DURATION	
[7:4]	**100Mbs Mode**	**10Mbs Mode**
0h	5uS	7.2uS
1h	10uS	12.2uS
2h	15uS	17.2uS
3h	25uS	27.2uS
4h	50uS	52.2uS
5h	100uS	102.2uS
6h	150uS	152.2uS
7h	200uS	202.2uS

Table 14.2 Backpressure Duration Bit Mapping (continued)

	BACKPRESSURE DURATION	
8h	250uS	252.2uS
9h	300uS	302.2uS
Ah	350uS	352.2uS
Bh	400uS	402.2uS
Ch	450uS	452.2uS
Dh	500uS	502.2uS
Eh	550uS	552.2uS
Fh	600uS	602.2uS

14.2.3 GPIO/LED

This section details the General Purpose I/O (GPIO) and LED related System CSR's.

14.2.3.1 General Purpose I/O Configuration Register (GPIO_CFG)

Offset: 1E0h Size: 32 bits

This read/write register configures the GPIO input and output pins. The polarity of the 12 GPIO pins is configured here as well as the IEEE 1588 timestamping and clock compare event output properties of the GPIO[9:8] pins.

BITS	DESCRIPTION	TYPE	DEFAULT
31:30	**RESERVED**	RO	-
29:28	**GPIO 1588 Timer Interrupt Clear Enable 9-8 (GPIO_1588_TIMER_INT_CLEAR_EN[9:8])** These bits enable inputs on GPIO9 and GPIO8 to clear the 1588_TIMER_INT bit of the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN). The polarity of these inputs is determined by GPIO_INT_POL[9:8]. **Note:** The GPIO must be configured as an input for this function to operate. For the clear function, GPIO inputs are edge sensitive and must be active for greater than 40 nS to be recognized.	R/W	00b
27:16	**GPIO Interrupt Polarity 11-0 (GPIO_INT_POL[11:0])** These bits set the interrupt polarity of the 12 GPIO pins. The configured level (high/low) will set the corresponding GPIO_INT bit in the General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN). **0: Sets low logic level trigger on corresponding GPIO pin** **1: Sets high logic level trigger on corresponding GPIO pin** GPIO_INT_POL[9:8] also determines the polarity of the GPIO IEEE 1588 time clock capture events and the GPIO 1588 Timer Interrupt Clear inputs. Refer to Section 13.2, "GPIO Operation," on page 162 for additional information.	R/W	0h
15:14	**1588 GPIO Output Enable 9-8 (1588_GPIO_OE[9:8])** These bits configure GPIO 9 and GPIO 8 to output 1588 clock compare events. **0: Disables the output of 1588 clock compare events** **1: Enables the output of 1588 clock compare events** **Note:** These bits override the direction bits in the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR) register. However, the GPIO buffer type (GPIOBUF[11:0]) in the General Purpose I/O Configuration Register (GPIO_CFG) is not overridden.	R/W	0h
13	**GPIO 9 Clock Event Polarity (GPIO_EVENT_POL_9)** This bit determines if the 1588 clock event output on GPIO 9 is active high or low. **0: 1588 clock event output active low** **1: 1588 clock event output active high**	R/W	1b

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>12</td><td>GPIO 8 Clock Event Polarity (GPIO_EVENT_POL_8)
This bit determines if the 1588 clock event output on GPIO 8 is active high or low.

0: 1588 clock event output active low
1: 1588 clock event output active high</td><td>R/W</td><td>1b</td></tr>
<tr><td>11:0</td><td>GPIO Buffer Type 11-0 (GPIOBUF[11:0])
This field sets the buffer types of the 12 GPIO pins.

0: Corresponding GPIO pin configured as an open-drain driver
1: Corresponding GPIO pin configured as a push/pull driver

As an open-drain driver, the output pin is driven low when the corresponding data register is cleared, and is not driven when the corresponding data register is set.

As an open-drain driver used for 1588 Clock Events, the corresponding GPIO_EVENT_POL_8 and GPIO_EVENT_POL_9 bits determine when the corresponding pin is driven per the following table:

<table>
<tr><th>GPIOx Clock Event Polarity</th><th>1588 Clock Event</th><th>Pin State</th></tr>
<tr><td>0</td><td>no</td><td>not driven</td></tr>
<tr><td>0</td><td>yes</td><td>driven low</td></tr>
<tr><td>1</td><td>no</td><td>driven low</td></tr>
<tr><td>1</td><td>yes</td><td>not driven</td></tr>
</table>
</td><td>R/W</td><td>0h</td></tr>
</table>

14.2.3.2 General Purpose I/O Data & Direction Register (GPIO_DATA_DIR)

Offset: 1E4h Size: 32 bits

This read/write register configures the direction of the 12 GPIO pins and contains the GPIO input and output data bits.

BITS	DESCRIPTION	TYPE	DEFAULT
31:28	**RESERVED**	RO	-
27:16	**GPIO Direction 11-0 (GPIODIR[11:0])** These bits set the input/output direction of the 12 GPIO pins. **0: GPIO pin is configured as an input** **1: GPIO pin is configured as an output**	R/W	0h
15:12	**RESERVED**	RO	-
11:0	**GPIO Data 11-0 (GPIOD[11:0])** When a GPIO pin is enabled as an output, the value written to this field is output on the corresponding GPIO pin. Upon a read, the value returned depends on the current direction of the pin. If the pin is an input, the data reflects the current state of the corresponding GPIO pin. If the pin is an output, the data is the value that was last written into this register. For GPIOs 11-10 and 7-0, the pin direction is determined by the GPDIR bits of this register. For GPIOs 9 and 8, the pin direction is determined by the GPDIR bits and the 1588_GPIO_OE bits in the General Purpose I/O Configuration Register (GPIO_CFG).	R/W	0h

14.2.3.3 General Purpose I/O Interrupt Status and Enable Register (GPIO_INT_STS_EN)

Offset: 1E8h Size: 32 bits

This read/write register contains the GPIO interrupt status bits.

Writing a 1 to any of the interrupt status bits acknowledges and clears the interrupt. If enabled, these interrupt bits are cascaded into bit 12 (GPIO) of the Interrupt Status Register (INT_STS). Writing a 1 to any of the interrupt enable bits will enable the corresponding interrupt as a source. Status bits will still reflect the status of the interrupt source regardless of whether the source is enabled as an interrupt in this register. Bit 12 (GPIO_EN) of the Interrupt Enable Register (INT_EN) must also be set in order for an actual system level interrupt to occur. Refer to Chapter 5, "System Interrupts," on page 49 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:28	**RESERVED**	RO	-
27:16	**GPIO Interrupt Enable[11:0] (GPIO[11:0]_INT_EN)** When set, these bits enable the corresponding GPIO interrupt. **Note:** The GPIO interrupts must also be enabled via bit 12 (GPIO_EN) of the Interrupt Enable Register (INT_EN) in order to cause the interrupt pin (IRQ) to be asserted.	R/W	0h
15:12	**RESERVED**	RO	-
11:0	**GPIO Interrupt[11:0] (GPIO[11:0]_INT)** These signals reflect the interrupt status as generated by the GPIOs. These interrupts are configured through the General Purpose I/O Configuration Register (GPIO_CFG). **Note:** As GPIO interrupts, GPIO inputs are level sensitive and must be active greater than 40 nS to be recognized as interrupt inputs.	R/WC	0h

14.2.3.4 LED Configuration Register (LED_CFG)

Offset: 1BCh Size: 32 bits

This read/write register configures the GPIO[7:0] pins as LED[7:0] pins and sets their functionality.

BITS	DESCRIPTION	TYPE	DEFAULT
31:10	**RESERVED**	RO	-
9:8	**LED Function 1-0 (LED_FUN[1:0])** These bits control the function associated with each LED pin as shown in Table 13.1 of Section 13.3, "LED Operation," on page 164. **Note:** In order for these assignments to be valid, the particular pin must be enabled as an LED output pin via the LED_EN[7:0] bits of this register.	R/W	Note 14.2
7:0	**LED Enable 7-0 (LED_EN[7:0])** This field toggles the functionality of the GPIO[7:0] pins between GPIO and LED. **0: Enables the associated pin as a GPIO signal** **1: Enables the associated pin as a LED output**	R/W	Note 14.3

Note 14.2 The default value of this field is determined by the configuration strap LED_fun_strap[1:0]. Configuration strap values are latched on power-on reset or nRST de-assertion. Some configuration straps can be overridden by values from the EEPROM Loader. Refer to Section 4.2.4, "Configuration Straps," on page 40 for more information.

Note 14.3 The default value of this field is determined by the configuration strap LED_en_strap[7:0]. Configuration strap values are latched on power-on reset or nRST de-assertion. Some configuration straps can be overridden by values from the EEPROM Loader. Refer to Section 4.2.4, "Configuration Straps," on page 40 for more information.

14.2.4 EEPROM

This section details the EEPROM related System CSR's. These registers should only be used if an EEPROM has been connected to the LAN9312. Refer to chapter Section 10.2, "I2C/Microwire Master EEPROM Controller," on page 137 for additional information on the various modes (I^2C and Microwire) of the EEPROM Controller (EPC).

14.2.4.1 EEPROM Command Register (E2P_CMD)

Offset: 1B4h Size: 32 bits

This read/write register is used to control the read and write operations of the serial EEPROM.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**EEPROM Controller Busy (EPC_BUSY)** When a 1 is written into this bit, the operation specified in the EPC_COMMAND field of this register is performed at the specified EEPROM address. This bit will remain set until the selected operation is complete. In the case of a read, this indicates that the Host can read valid data from the EEPROM Data Register (E2P_DATA). The E2P_CMD and E2P_DATA registers should not be modified until this bit is cleared. In the case where a write is attempted and an EEPROM is not present, the EPC_BUSY bit remains set until the EEPROM Controller Timeout (EPC_TIMEOUT) bit is set. At this time the EPC_BUSY bit is cleared. **Note:** EPC_BUSY is set immediately following power-up, or pin reset, or DIGITAL_RST reset. This bit is also set following the settings of the SRST bit in the Hardware Configuration Register (HW_CFG). After the EEPROM Loader has finished loading, the EPC_BUSY bit is cleared. Refer to chapter Section 10.2.4, "EEPROM Loader," on page 149 for more information.	R/W SC	0b

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>30:28</td><td>

EEPROM Controller Command (EPC_COMMAND)
This field is used to issue commands to the EEPROM controller. The EEPROM controller will execute a command when the EPC_BUSY bit is set. A new command must not be issued until the previous command completes. The field is encoded as follows:

<table>
<tr><th>[30]</th><th>[29]</th><th>[28]</th><th>Operation</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>READ</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>EWDS</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>EWEN</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>WRITE</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>WRAL</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>ERASE</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>ERAL</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>RELOAD</td></tr>
</table>

Note: Only the READ, WRITE and RELOAD commands are valid for I^2C mode. If an unsupported command is attempted, the EPC_BUSY bit will be cleared and EPC_TIMEOUT will be set.

The EEPROM operations are defined as follows:

READ (Read Location)
This command will cause a read of the EEPROM location pointed to by the EPC_ADDRESS bit field. The result of the read is available in the EEPROM Data Register (E2P_DATA).

EWDS (Erase/Write Disable)
(Microwire mode only) - When this command is issued, the EEPROM will ignore erase and write commands. To re-enable erase/writes operations, issue the EWEN command.

EWEN (Erase/Write Enable)
(Microwire mode only) - Enables the EEPROM for erase and write operations. The EEPROM will allow erase and write operations until the EWDS command is sent, or until the power is cycled. The Microwire EEPROM device will power-up in the erase/write disabled state. Any erase or write operations will fail until an EWEN command is issued.

WRITE (Write Location)
If erase/write operations are enabled in the EEPROM, this command will cause the contents of the EEPROM Data Register (E2P_DATA) to be written to the EEPROM location selected by the EPC_ADDRESS field. For Microwire, erase/write operations must be enabled in the EEPROM.

WRAL (Write All)
(Microwire mode only) - If erase/write operations are enabled in the EEPROM, this command will cause the contents of the EEPROM Data Register (E2P_DATA) to be written to every EEPROM memory location.

ERASE (Erase Location)
(Microwire mode only) - If erase/write operations are enabled in the EEPROM, this command will erase the location selected by the EPC_ADDRESS field.

ERAL (Erase All)
(Microwire mode only) - If erase/write operations are enabled in the EEPROM, this command will initiate a bulk erase of the entire EEPROM.

RELOAD (EEPROM Loader Reload)
Instructs the EEPROM Loader to reload the device from the EEPROM. If a value of A5h is not found in the first address of the EEPROM, the EEPROM is assumed to be un-programmed and the RELOAD operation will fail. The CFG_LOADED bit indicates a successful load. Following this command, the device will enter the not ready state. The READY bit in the Hardware Configuration Register (HW_CFG) should be polled to determine then the RELOAD is complete.

</td><td>R/W</td><td>000b</td></tr>
<tr><td>27:19</td><td>RESERVED</td><td>RO</td><td>-</td></tr>
</table>

BITS	DESCRIPTION	TYPE	DEFAULT
18	**EEPROM Loader Address Overflow (LOADER_OVERFLOW)** This bit indicates that the EEPROM Loader tried to read past the end of the EEPROM address space. This indicates misconfigured EEPROM data. This bit is cleared when the EEPROM Loader is restarted with a RELOAD command, Soft Reset(SRST), or a Digital Reset(DIGITAL_RST).	RO	0b
17	**EEPROM Controller Timeout (EPC_TIMEOUT)** This bit is set when a timeout occurs, indicating the last operation was unsuccessful. If an EEPROM ERASE, ERAL, WRITE or WRAL operation is performed and no response is received from the EEPROM within 30mS, the EEPROM controller will timeout and return to its idle state. For the I^2C mode, the bit is also set if the EEPROM fails to respond with the appropriate ACKs, if the EEPROM slave device holds the clock low for more than 30ms, or if an unsupported EPC_COMMAND is attempted. This bit is cleared when written high. **Note:** When in Microwire mode, if an EEPROM device is not connected, an internal pull-down on the EEDI pin will keep the EEDI signal low and allow timeouts to occur. If EEDI is pulled high externally, EPC commands will not time out if an EEPROM device is not connected. In this case the EPC_BUSY bit will be cleared as soon as the command sequence is complete. It should also be noted that the ERASE, ERAL, WRITE and WRAL commands are the only EPC commands that will timeout if an EEPROM device is not present *AND* the EEDI signal is pulled low.	R/WC	0b
16	**Configuration Loaded (CFG_LOADED)** When set, this bit indicates that a valid EEPROM was found and the EEPROM Loader completed normally. This bit is set upon a successful load. It is cleared on power-up, pin and DIGITAL_RST resets, Soft Reset(SRST), or at the start of a RELOAD. This bit is cleared when written high.	R/WC	0b
15:0	**EEPROM Controller Address (EPC_ADDRESS)** This field is used by the EEPROM Controller to address a specific memory location in the serial EEPROM. This address must be byte aligned.	R/W	0000h

14.2.4.2 EEPROM Data Register (E2P_DATA)

Offset: 1B8h Size: 32 bits

This read/write register is used in conjunction with the EEPROM Command Register (E2P_CMD) to perform read and write operations with the serial EEPROM.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7:0	**EEPROM Data (EEPROM_DATA)** This field contains the data read from or written to the EEPROM.	R/W	00h

14.2.5 IEEE 1588

This section details the IEEE 1588 timestamp related registers. Each port of the LAN9312 has a 1588 timestamp block with 8 related registers, 4 for transmit capture and 4 for receive capture. These sets of registers are identical in functionality for each port, and thus their register descriptions have been consolidated. In these cases, the register names will be amended with a lowercase “x” in place of the port designation. The wildcard “x” should be replaced with “1”, “2”, or “MII” for the Port 1, Port 2, and Port 0(Host MAC) respectively. A list of all the 1588 related registers can be seen in Table 14.1. For more information on the IEEE 1588, refer to Chapter 11, "IEEE 1588 Hardware Time Stamp Unit," on page 154.

14.2.5.1 Port x 1588 Clock High-DWORD Receive Capture Register (1588_CLOCK_HI_RX_CAPTURE_x)

Offset: Port 1: 100h, Port 2: 120h, Port 0: 140h — Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Timestamp High (TS_HI)** This field contains the high 32-bits of the timestamp taken on the receipt of a 1588 Sync or Delay_Req packet.	RO	00000000h

Note: The selection between Sync or Delay_Req packets is based on the corresponding master/slave bit in the 1588 Configuration Register (1588_CONFIG).

Note: There are multiple instantiations of this register, one for each port of the LAN9312. Refer to Section 14.2.5 for additional information.

Note: For Port 0(Host MAC), receive is defined as data *from* the switch fabric, while transmit is *to* the switch fabric.

14.2.5.2 Port x 1588 Clock Low-DWORD Receive Capture Register (1588_CLOCK_LO_RX_CAPTURE_x)

Offset: Port 1: 104h
Port 2: 124h
Port 0: 144h

Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Timestamp Low (TS_LO)** This field contains the low 32-bits of the timestamp taken on the receipt of a 1588 Sync or Delay_Req packet.	RO	00000000h

Note: The selection between Sync or Delay_Req packets is based on the corresponding master/slave bit in the 1588 Configuration Register (1588_CONFIG).

Note: There are multiple instantiations of this register, one for each port of the LAN9312. Refer to Section 14.2.5 for additional information.

Note: For Port 0(Host MAC), receive is defined as data *from* the switch fabric, while transmit is *to* the switch fabric.

14.2.5.3 Port x 1588 Sequence ID, Source UUID High-WORD Receive Capture Register (1588_SEQ_ID_SRC_UUID_HI_RX_CAPTURE_x)

Offset: Port 1: 108h
Port 2: 128h
Port 0: 148h

Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**Sequence ID (SEQ_ID)** This field contains the Sequence ID from the 1588 Sync or Delay_Req packet.	RO	0000h
15:0	**Source UUID High (SRC_UUID_HI)** This field contains the high 16-bits of the Source UUID from the 1588 Sync or Delay_Req packet.	RO	0000h

Note: The selection between Sync or Delay_Req packets is based on the corresponding master/slave bit in the 1588 Configuration Register (1588_CONFIG).

Note: There are multiple instantiations of this register, one for each port of the LAN9312. Refer to Section 14.2.5 for additional information.

Note: For Port 0(Host MAC), receive is defined as data *from* the switch fabric, while transmit is *to* the switch fabric.

14.2.5.4 Port x 1588 Source UUID Low-DWORD Receive Capture Register (1588_SRC_UUID_LO_RX_CAPTURE_x)

Offset: Port 1: 10Ch
Port 2: 12Ch
Port 0: 14Ch

Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Source UUID Low (SRC_UUID_LO)** This field contains the low 32-bits of the Source UUID from the 1588 Sync or Delay_Req packet.	RO	00000000h

Note: The selection between Sync or Delay_Req packets is based on the corresponding master/slave bit in the 1588 Configuration Register (1588_CONFIG).

Note: There are multiple instantiations of this register, one for each port of the LAN9312. Refer to Section 14.2.5 for additional information.

Note: For Port 0(Host MAC), receive is defined as data *from* the switch fabric, while transmit is *to* the switch fabric.

14.2.5.5 Port x 1588 Clock High-DWORD Transmit Capture Register (1588_CLOCK_HI_TX_CAPTURE_x)

Offset: Port 1: 110h
Port 2: 130h
Port 0: 150h

Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Timestamp High (TS_HI)** This field contains the high 32-bits of the timestamp taken on the transmission of a 1588 Sync or Delay_Req packet.	RO	00000000h

Note: The selection between Sync or Delay_Req packets is based on the corresponding master/slave bit in the 1588 Configuration Register (1588_CONFIG).

Note: There are multiple instantiations of this register, one for each port of the LAN9312. Refer to Section 14.2.5 for additional information.

Note: For Port 0(Host MAC), receive is defined as data *from* the switch fabric, while transmit is *to* the switch fabric.

14.2.5.6 Port x 1588 Clock Low-DWORD Transmit Capture Register (1588_CLOCK_LO_TX_CAPTURE_x)

Offset: Port 1: 114h
Port 2: 134h
Port 0: 154h

Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Timestamp Low (TS_LO)** This field contains the low 32-bits of the timestamp taken on the transmission of a 1588 Sync or Delay_Req packet.	RO	00000000h

Note: The selection between Sync or Delay_Req packets is based on the corresponding master/slave bit in the 1588 Configuration Register (1588_CONFIG).

Note: There are multiple instantiations of this register, one for each port of the LAN9312. Refer to Section 14.2.5 for additional information.

Note: For Port 0(Host MAC), receive is defined as data *from* the switch fabric, while transmit is *to* the switch fabric.

14.2.5.7 Port x 1588 Sequence ID, Source UUID High-WORD Transmit Capture Register (1588_SEQ_ID_SRC_UUID_HI_TX_CAPTURE_x)

Offset: Port 1: 118h
Port 2: 138h
Port 0: 158h

Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**Sequence ID (SEQ_ID)** This field contains the Sequence ID from the 1588 Sync or Delay_Req packet.	RO	0000h
15:0	**Source UUID High (SRC_UUID_HI)** This field contains the high 16-bits of the Source UUID from the 1588 Sync or Delay_Req packet.	RO	0000h

Note: The selection between Sync or Delay_Req packets is based on the corresponding master/slave bit in the 1588 Configuration Register (1588_CONFIG).

Note: There are multiple instantiations of this register, one for each port of the LAN9312. Refer to Section 14.2.5 for additional information.

Note: For Port 0(Host MAC), receive is defined as data *from* the switch fabric, while transmit is *to* the switch fabric.

14.2.5.8 Port x 1588 Source UUID Low-DWORD Transmit Capture Register (1588_SRC_UUID_LO_TX_CAPTURE_x)

Offset: Port 1: 11Ch
Port 2: 13Ch
Port 0: 15Ch

Size: 32 bits

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Source UUID Low (SRC_UUID_TX_LO)** This field contains the low 32-bits of the Source UUID from the 1588 Sync or Delay_Req packet.	RO	00000000h

Note: The selection between Sync or Delay_Req packets is based on the corresponding master/slave bit in the 1588 Configuration Register (1588_CONFIG).

Note: There are multiple instantiations of this register, one for each port of the LAN9312. Refer to Section 14.2.5 for additional information.

Note: For Port 0(Host MAC), receive is defined as data *from* the switch fabric, while transmit is *to* the switch fabric.

14.2.5.9 GPIO 8 1588 Clock High-DWORD Capture Register (1588_CLOCK_HI_CAPTURE_GPIO_8)

Offset: 160h Size: 32 bits

This read only register combined with the GPIO 8 1588 Clock Low-DWORD Capture Register (1588_CLOCK_LO_CAPTURE_GPIO_8) form the 64-bit GPIO 8 timestamp capture.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Timestamp High (TS_HI)** This field contains the high 32-bits of the timestamp upon activation of GPIO 8.	RO	00000000h

14.2.5.10 GPIO 8 1588 Clock Low-DWORD Capture Register (1588_CLOCK_LO_CAPTURE_GPIO_8)

Offset: 164h Size: 32 bits

This read only register combined with the GPIO 8 1588 Clock High-DWORD Capture Register (1588_CLOCK_HI_CAPTURE_GPIO_8) form the 64-bit GPIO 8 timestamp capture.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Timestamp Low (TS_LO)** This field contains the low 32-bits of the timestamp upon activation of GPIO 8.	RO	00000000h

14.2.5.11 GPIO 9 1588 Clock High-DWORD Capture Register (1588_CLOCK_HI_CAPTURE_GPIO_9)

Offset: 168h Size: 32 bits

This read only register combined with the GPIO 9 1588 Clock Low-DWORD Capture Register (1588_CLOCK_LO_CAPTURE_GPIO_9) form the 64-bit GPIO 9 timestamp capture.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Timestamp High (TS_HI)** This field contains the high 32-bits of the timestamp upon activation of GPIO 9.	RO	00000000h

14.2.5.12 GPIO 9 1588 Clock Low-DWORD Capture Register (1588_CLOCK_LO_CAPTURE_GPIO_9)

Offset: 16Ch Size: 32 bits

This read only register combined with the GPIO 9 1588 Clock High-DWORD Capture Register (1588_CLOCK_HI_CAPTURE_GPIO_9) form the 64-bit GPIO 9 timestamp capture.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Timestamp Low (TS_LO)** This field contains the low 32-bits of the timestamp upon activation of GPIO 9.	RO	00000000h

14.2.5.13 1588 Clock High-DWORD Register (1588_CLOCK_HI)

Offset: 170h Size: 32 bits

This read/write register combined with 1588 Clock Low-DWORD Register (1588_CLOCK_LO) form the 64-bit 1588 Clock value. The 1588 Clock value is used for all 1588 timestamping. The 1588 Clock has a base frequency of 100MHz, which can be adjusted via the 1588 Clock Addend Register (1588_CLOCK_ADDEND) accordingly. Refer to Chapter 11, "IEEE 1588 Hardware Time Stamp Unit," on page 154 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Clock High (CLOCK_HI)** This field contains the high 32-bits of the 64-bit 1588 Clock.	R/W	00000000h

Note: Both this register and the 1588 Clock Low-DWORD Register (1588_CLOCK_LO) must be written for either to be affected.

Note: The value read is the saved value of the 1588 Clock when the 1588_CLOCK_SNAPSHOT bit in the 1588 Command Register (1588_CMD) is set.

14.2.5.14 1588 Clock Low-DWORD Register (1588_CLOCK_LO)

Offset: 174h Size: 32 bits

This read/write register combined with 1588 Clock High-DWORD Register (1588_CLOCK_HI) form the 64-bit 1588 Clock value. The 1588 Clock value is used for all 1588 timestamping. The 1588 Clock has a base frequency of 100MHz, which can be adjusted via the 1588 Clock Addend Register (1588_CLOCK_ADDEND) accordingly. Refer to Chapter 11, "IEEE 1588 Hardware Time Stamp Unit," on page 154 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Clock Low (CLOCK_LO)** This field contains the low 32-bits of the 64-bit 1588 Clock.	R/W	00000000h

Note: Both this register and the 1588 Clock High-DWORD Register (1588_CLOCK_HI) must be written for either to be affected.

Note: The value read is the saved value of the 1588 Clock when the 1588_CLOCK_SNAPSHOT bit in the 1588 Command Register (1588_CMD) is set.

14.2.5.15 1588 Clock Addend Register (1588_CLOCK_ADDEND)

Offset: 178h Size: 32 bits

This read/write register is responsible for adjusting the 64-bit 1588 Clock frequency. Refer to Chapter 11, "IEEE 1588 Hardware Time Stamp Unit," on page 154 for details on how to properly use this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Clock Addend (CLOCK_ADDEND)** This 32-bit value is added to the 1588 frequency divisor accumulator every cycle. This allows the base 100MHz frequency of the 64-bit 1588 Clock to be adjusted accordingly.	R/W	00000000h

14.2.5.16 1588 Clock Target High-DWORD Register (1588_CLOCK_TARGET_HI)

Offset: 17Ch Size: 32 bits

This read/write register combined with 1588 Clock Target Low-DWORD Register (1588_CLOCK_TARGET_LO) form the 64-bit 1588 Clock Target value. The 1588 Clock Target value is compared to the current 1588 Clock value and can be used to trigger an interrupt upon at match. Refer to Chapter 11, "IEEE 1588 Hardware Time Stamp Unit," on page 154 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Clock Target High (CLOCK_TARGET_HI)** This field contains the high 32-bits of the 64-bit 1588 Clock Compare value.	R/W	00000000h

Note: Both this register and the 1588 Clock Target Low-DWORD Register (1588_CLOCK_TARGET_LO) must be written for either to be affected.

14.2.5.17 1588 Clock Target Low-DWORD Register (1588_CLOCK_TARGET_LO)

Offset: 180h Size: 32 bits

This read/write register combined with 1588 Clock Target High-DWORD Register (1588_CLOCK_TARGET_HI) form the 64-bit 1588 Clock Target value. The 1588 Clock Target value is compared to the current 1588 Clock value and can be used to trigger an interrupt upon at match. Refer to Chapter 11, "IEEE 1588 Hardware Time Stamp Unit," on page 154 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Clock Target Low (CLOCK_TARGET_LO)** This field contains the low 32-bits of the 64-bit 1588 Clock Compare value.	R/W	00000000h

Note: Both this register and the 1588 Clock Target High-DWORD Register (1588_CLOCK_TARGET_HI) must be written for either to be affected.

14.2.5.18 1588 Clock Target Reload High-DWORD Register (1588_CLOCK_TARGET_RELOAD_HI)

Offset: 184h Size: 32 bits

This read/write register combined with 1588 Clock Target Reload/Add Low-DWORD Register (1588_CLOCK_TARGET_RELOAD_LO) form the 64-bit 1588 Clock Target Reload value. The 1588 Clock Target Reload is the value that is reloaded to the 1588 Clock Compare value when a clock compare event occurs and the Reload/Add (RELOAD_ADD) bit of the 1588 Configuration Register (1588_CONFIG) is set. Refer to Chapter 11, "IEEE 1588 Hardware Time Stamp Unit," on page 154 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Clock Target Reload High (CLOCK_TARGET_RELOAD_HI)** This field contains the high 32-bits of the 64-bit 1588 Clock Target Reload value that is reloaded to the 1588 Clock Compare value.	R/W	00000000h

Note: Both this register and the 1588 Clock Target Reload/Add Low-DWORD Register (1588_CLOCK_TARGET_RELOAD_LO) must be written for either to be affected.

14.2.5.19 1588 Clock Target Reload/Add Low-DWORD Register (1588_CLOCK_TARGET_RELOAD_LO)

Offset: 188h Size: 32 bits

This read/write register combined with 1588 Clock Target Reload High-DWORD Register (1588_CLOCK_TARGET_RELOAD_HI) form the 64-bit 1588 Clock Target Reload value. The 1588 Clock Target Reload is the value that is reloaded or added to the 1588 Clock Compare value when a clock compare event occurs. Whether this value is reloaded or added is determined by the Reload/Add (RELOAD_ADD) bit of the 1588 Configuration Register (1588_CONFIG). Refer to Chapter 11, "IEEE 1588 Hardware Time Stamp Unit," on page 154 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Clock Target Reload Low (CLOCK_TARGET_RELOAD_LO)** This field contains the low 32-bits of the 64-bit 1588 Clock Target Reload value that is reloaded to the 1588 Clock Compare value. Alternatively, these 32-bits are added to the 1588 Clock Compare value when configured accordingly.	R/W	00000000h

Note: Both this register and the 1588 Clock Target Reload High-DWORD Register (1588_CLOCK_TARGET_RELOAD_HI) must be written for either to be affected.

14.2.5.20 1588 Auxiliary MAC Address High-WORD Register (1588_AUX_MAC_HI)

Offset: 18Ch Size: 32 bits

This read/write register combined with the 1588 Auxiliary MAC Address Low-DWORD Register (1588_AUX_MAC_LO) forms the 48-bit Auxiliary (user defined) MAC address. The Auxiliary MAC address can be enabled for each port of the LAN9312 via their respective User Defined MAC Address Enable bit in the 1588 Configuration Register (1588_CONFIG). Refer to Chapter 11, "IEEE 1588 Hardware Time Stamp Unit," on page 154 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**Auxiliary MAC Address High (AUX_MAC_HI)** This field contains the high 16-bits of the Auxiliary MAC address used for PTP packet detection.	R/W	0000h

14.2.5.21 1588 Auxiliary MAC Address Low-DWORD Register (1588_AUX_MAC_LO)

Offset: 190h Size: 32 bits

This read/write register combined with the 1588 Auxiliary MAC Address High-WORD Register (1588_AUX_MAC_HI) forms the 48-bit Auxiliary (user defined) MAC address. The Auxiliary MAC address can be enabled for each port of the LAN9312 via their respective User Defined MAC Address Enable bit in the 1588 Configuration Register (1588_CONFIG). Refer to Chapter 11, "IEEE 1588 Hardware Time Stamp Unit," on page 154 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Auxiliary MAC Address Low (AUX_MAC_LO)** This field contains the low 32-bits of the Auxiliary MAC address used for PTP packet detection.	R/W	00000000h

14.2.5.22 1588 Configuration Register (1588_CONFIG)

Offset: 194h Size: 32 bits

This read/write register is responsible for the configuration of the 1588 timestamps for all ports.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**Master/Slave Port 2 (M_nS_2)** When set, Port 2 is a time clock master and captures timestamps when a Sync packet is transmitted and when a Delay_Req is received. When cleared, Port 2 is a time clock slave and captures timestamps when a Delay_Req packet is transmitted and when a Sync packet is received.	R/W	0b
30	**Primary MAC Address Enable Port 2 (MAC_PRI_EN_2)** This bit enables/disables the primary MAC address on Port 2. **0: Disables primary MAC address on Port 2** **1: Enables MAC address 01:00:5E:00:01:81 as a PTP address on Port 2**	R/W	1b
29	**Alternate MAC Address 1 Enable Port 2 (MAC_ALT1_EN_2)** This bit enables/disables the alternate MAC address 1 on Port 2. **0: Disables alternate MAC address on Port 2** **1: Enables MAC address 01:00:5E:00:01:82 as a PTP address on Port 2**	R/W	0b
28	**Alternate MAC Address 2 Enable Port 2 (MAC_ALT2_EN_2)** This bit enables/disables the alternate MAC address 2 on Port 2. **0: Disables alternate MAC address on Port 2** **1: Enables MAC address 01:00:5E:00:01:83 as a PTP address on Port 2**	R/W	0b
27	**Alternate MAC Address 3 Enable Port 2 (MAC_ALT3_EN_2)** This bit enables/disables the alternate MAC address 3 on Port 2. **0: Disables alternate MAC address on Port 2** **1: Enables MAC address 01:00:5E:00:01:84 as a PTP address on Port 2**	R/W	0b
26	**User Defined MAC Address Enable Port 2 (MAC_USER_EN_2)** This bit enables/disables the auxiliary MAC address on Port 2. The auxiliary address is defined via the 1588_AUX_MAC_HI and 1588_AUX_MAC_LO registers. **0: Disables auxiliary MAC address on Port 2** **1: Enables auxiliary MAC address as a PTP address on Port 2**	R/W	0b
25	**Lock Enable RX Port 2 (LOCK_RX_2)** This bit enables/disables the RX lock. This lock prevents a 1588 capture from overwriting the Clock, UUDI and Sequence ID values if the 1588 RX interrupt for Port 2 is already set due to a previous capture. **0: Disables RX Port 2 Lock** **1: Enables RX Port 2 Lock**	R/W	1b
24	**Lock Enable TX Port 2 (LOCK_TX_2)** This bit enables/disables the TX lock. This lock prevents a 1588 capture from overwriting the Clock, UUDI and Sequence ID values if the 1588 TX interrupt for Port 2 is already set due to a previous capture. **0: Disables TX Port 2 Lock** **1: Enables TX Port 2 Lock**	R/W	1b

BITS	DESCRIPTION	TYPE	DEFAULT
23	**Master/Slave Port 1 (M_nS_1)** When set, Port 1 is a time clock master and captures timestamps when a Sync packet is transmitted and when a Delay_Req is received. When cleared, Port 1 is a time clock slave and captures timestamps when a Delay_Req packet is transmitted and when a Sync packet is received.	R/W	0b
22	**Primary MAC Address Enable Port 1 (MAC_PRI_EN_1)** This bit enables/disables the primary MAC address on Port 1. **0: Disables primary MAC address on Port 1** **1: Enables MAC address 01:00:5E:00:01:81 as a PTP address on Port 1**	R/W	1b
21	**Alternate MAC Address 1 Enable Port 1 (MAC_ALT1_EN_1)** This bit enables/disables the alternate MAC address 1 on Port 1. **0: Disables alternate MAC address on Port 1** **1: Enables MAC address 01:00:5E:00:01:82 as a PTP address on Port 1**	R/W	0b
20	**Alternate MAC Address 2 Enable Port 1 (MAC_ALT2_EN_1)** This bit enables/disables the alternate MAC address 2 on Port 1. **0: Disables alternate MAC address on Port 1** **1: Enables MAC address 01:00:5E:00:01:83 as a PTP address on Port 1**	R/W	0b
19	**Alternate MAC Address 3 Enable Port 1 (MAC_ALT3_EN_1)** This bit enables/disables the alternate MAC address 3 on Port 1. **0: Disables alternate MAC address on Port 1** **1: Enables MAC address 01:00:5E:00:01:84 as a PTP address on Port 1**	R/W	0b
18	**User Defined MAC Address Enable Port 1 (MAC_USER_EN_1)** This bit enables/disables the auxiliary MAC address on Port 1. The auxiliary address is defined via the 1588_AUX_MAC_HI and 1588_AUX_MAC_LO registers. **0: Disables auxiliary MAC address on Port 1** **1: Enables auxiliary MAC address as a PTP address on Port 1**	R/W	0b
17	**Lock Enable RX Port 1 (LOCK_RX_1)** This bit enables/disables the RX lock. This lock prevents a 1588 capture from overwriting the Clock, UUDI and Sequence ID values if the 1588 RX interrupt for Port 1 is ready set due to a previous capture. **0: Disables RX Port 1 Lock** **1: Enables RX Port 1 Lock**	R/W	1b
16	**Lock Enable TX Port 1 (LOCK_TX_1)** This bit enables/disables the TX lock. This lock prevents a 1588 capture from overwriting the Clock, UUDI and Sequence ID values if the 1588 TX interrupt for Port 1 is ready set due to a previous capture. **0: Disables TX Port 1 Lock** **1: Enables TX Port 1 Lock**	R/W	1b
15	**Master/Slave Port 0(Host MAC)(M_nS_MII)** When set, Port 0 is a time clock master and captures timestamps when a Sync packet is transmitted and when a Delay_Req is received. When cleared, Port 0 is a time clock slave and captures timestamps when a Delay_Req packet is transmitted and when a Sync packet is received. **Note:** For Port 0, receive is defined as data *from* the switch fabric, while transmit is defined as data *to* the switch fabric.	R/W	0b
14	**Primary MAC Address Enable Port 0(Host MAC) (MAC_PRI_EN_MII)** This bit enables/disables the primary MAC address on Port 0. **0: Disables primary MAC address on Port 0** **1: Enables MAC address 01:00:5E:00:01:81 as a PTP address on Port 0**	R/W	1b

BITS	DESCRIPTION	TYPE	DEFAULT
13	**Alternate MAC Address 1 Enable Port 0(Host MAC) (MAC_ALT1_EN_MII)** This bit enables/disables the alternate MAC address 1 on Port 0. **0: Disables alternate MAC address on Port 0** **1: Enables MAC address 01:00:5E:00:01:82 as a PTP address on Port 0**	R/W	0b
12	**Alternate MAC Address 2 Enable Port 0(Host MAC) (MAC_ALT2_EN_MII)** This bit enables/disables the alternate MAC address 2 on Port 0. **0: Disables alternate MAC address on Port 0** **1: Enables MAC address 01:00:5E:00:01:83 as a PTP address on Port 0**	R/W	0b
11	**Alternate MAC Address 3 Enable Port 0(Host MAC) (MAC_ALT3_EN_MII)** This bit enables/disables the alternate MAC address 3 on Port 0. **0: Disables alternate MAC address on Port 0** **1: Enables MAC address 01:00:5E:00:01:84 as a PTP address on Port 0**	R/W	0b
10	**User Defined MAC Address Enable Port 0(Host MAC) (MAC_USER_EN_MII)** This bit enables/disables the auxiliary MAC address on Port 0. The auxiliary address is defined via the 1588_AUX_MAC_HI and 1588_AUX_MAC_LO registers. **0: Disables auxiliary MAC address on Port 0** **1: Enables auxiliary MAC address as a PTP address on Port 0**	R/W	0b
9	**Lock Enable RX Port 0(Host MAC) (LOCK_RX_MII)** This bit enables/disables the RX lock. This lock prevents a 1588 capture from overwriting the Clock, UUDI and Sequence ID values if the 1588 RX interrupt for Port 0 is ready set due to a previous capture. **0: Disables RX Port 0 Lock** **1: Enables RX Port 0 Lock** **Note:** For Port 0, receive is defined as data *from* the switch fabric, while transmit is *to* the switch fabric.	R/W	1b
8	**Lock Enable TX Port 0(Host MAC) (LOCK_TX_MII)** This bit enables/disables the TX lock. This lock prevents a 1588 capture from overwriting the Clock, UUDI and Sequence ID values if the 1588 TX interrupt for Port 0 is ready set due to a previous capture. **0: Disables TX Port 0 Lock** **1: Enables TX Port 0 Lock** **Note:** For Port 0, receive is defined as data *from* the switch fabric, while transmit is *to* the switch fabric.	R/W	1b
7	**RESERVED**	RO	-
6	**Lock Enable GPIO 9 (LOCK_GPIO_9)** This bit enables/disables the GPIO 9 lock. This lock prevents a 1588 capture from overwriting the Clock value if the 1588_GPIO9 interrupt in the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN) is already set due to a previous capture. **0: Disables GPIO 9 Lock** **1: Enables GPIO 9 Lock**	R/W	1b

BITS	DESCRIPTION	TYPE	DEFAULT
5	**Lock Enable GPIO 8 (LOCK_GPIO_8)** This bit enables/disables the GPIO 8 lock. This lock prevents a 1588 capture from overwriting the Clock value if the 1588_GPIO8 interrupt in the 1588 Interrupt Status and Enable Register (1588_INT_STS_EN) is already set due to a previous capture. **0: Disables GPIO 8 Lock** **1: Enables GPIO 8 Lock**	R/W	1b
4:3	**GPIO 9 Clock Event Mode (GPIO_EVENT_9)** These bits determine the output on GPIO 9 when a clock target compare event occurs. **00: 100ns pulse output** **01: Toggle output** **10: 1588_TIMER_INT bit value in the 1588_INT_STS_EN register output** **11: RESERVED** **Note:** The 1588_GPIO_OE[9] bit in the General Purpose I/O Configuration Register (GPIO_CFG) must be set in order for the GPIO output to be controlled by the 1588 block. **Note:** The polarity of the pulse or level is set by the GPIO_EVENT_POL_9 bit in the General Purpose I/O Configuration Register (GPIO_CFG). The GPIOBUF[9] bit still determines the GPIO buffer type.	R/W	00b
2:1	**GPIO 8 Clock Event Mode (GPIO_EVENT_8)** These bits determine the output on GPIO 8 when a clock target compare event occurs. **00: 100ns pulse output** **01: Toggle output** **10: 1588_TIMER_INT bit value in the 1588_INT_STS_EN register output** **11: RESERVED** **Note:** The 1588_GPIO_OE[8] bit in the General Purpose I/O Configuration Register (GPIO_CFG) must be set in order for the GPIO output to be controlled by the 1588 block. **Note:** The polarity of the pulse or level is set by the GPIO_EVENT_POL_8 bit in the General Purpose I/O Configuration Register (GPIO_CFG). The GPIOBUF[8] bit still determines the GPIO buffer type.	R/W	00b
0	**Reload/Add (RELOAD_ADD)** This bit determines the course of action when a clock target compare event occurs. When set, the 1588 Clock Target High-DWORD Register (1588_CLOCK_TARGET_HI) and 1588 Clock Target Low-DWORD Register (1588_CLOCK_TARGET_LO) are loaded from the 1588 Clock Target Reload High-DWORD Register (1588_CLOCK_TARGET_RELOAD_HI) and 1588 Clock Target Reload/Add Low-DWORD Register (1588_CLOCK_TARGET_RELOAD_LO) when a clock target compare event occurs. When low, the Clock Target Low and High Registers are incremented by the Clock Target Reload Low Register when a clock target compare event occurs. **0: Reload upon a clock target compare event** **1: Increment upon a clock target compare event**	R/W	0b

14.2.5.23 1588 Interrupt Status and Enable Register (1588_INT_STS_EN)

Offset: 198h Size: 32 bits

This read/write register contains the IEEE 1588 interrupt status and enable bits.

Writing a 1 to any of the interrupt status bits acknowledges and clears the interrupt. If enabled, these interrupt bits are cascaded into bit 29 (1588_EVNT) of the Interrupt Status Register (INT_STS). Writing a 1 to any of the interrupt enable bits will enable the corresponding interrupt as a source. Status bits will still reflect the status of the interrupt source regardless of whether the source is enabled as an interrupt in this register. Bit 29 (1588_EVNT_EN) of the Interrupt Enable Register (INT_EN) must also be set in order for an actual system level interrupt to occur. Refer to Chapter 5, "System Interrupts," on page 49 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:25	**RESERVED**	RO	-
24	**1588 Port 2 RX Interrupt Enable (1588_PORT2_RX_EN)**	R/W	0b
23	**1588 Port 2 TX Interrupt Enable (1588_PORT2_TX_EN)**	R/W	0b
22	**1588 Port 1 RX Interrupt Enable (1588_PORT1_RX_EN)**	R/W	0b
21	**1588 Port 1 TX Interrupt Enable (1588_PORT1_TX_EN)**	R/W	0b
20	**1588 Port 0(Host MAC) RX Interrupt Enable (1588_MII_RX_EN)**	R/W	0b
19	**1588 Port 0(Host MAC) TX Interrupt Enable (1588_MII_TX_EN)**	R/W	0b
18	**GPIO9 1588 Interrupt Enable (1588_GPIO9_EN)**	R/W	0b
17	**GPIO8 1588 Interrupt Enable (1588_GPIO8_EN)**	R/W	0b
16	**1588 Timer Interrupt Enable (1588_TIMER_EN)**	R/W	0b
15:9	**RESERVED**	RO	-
8	**1588 Port 2 RX Interrupt (1588_PORT2_RX_INT)** This interrupt indicates that a packet received by Port 2 matches the configured PTP packet and the 1588 clock was captured.	R/WC	0b
7	**1588 Port 2 TX Interrupt (1588_PORT2_TX_INT)** This interrupt indicates that a packet transmitted by Port 2 matches the configured PTP packet and the 1588 clock was captured.	R/WC	0b
6	**1588 Port 1 RX Interrupt (1588_PORT1_RX_INT)** This interrupt indicates that a packet received by Port 1 matches the configured PTP packet and the 1588 clock was captured.	R/WC	0b
5	**1588 Port 1 TX Interrupt (1588_PORT1_TX_INT)** This interrupt indicates that a packet transmitted by Port 1 matches the configured PTP packet and the 1588 clock was captured.	R/WC	0b
4	**1588 Port 0(Host MAC) RX Interrupt (1588_MII_RX_INT)** This interrupt indicates that a packet from the switch fabric to the Host MAC the matches the configured PTP packet and the 1588 clock was captured. **Note:** For Port 0, receive is defined as data *from* the switch fabric, while transmit is *to* the switch fabric.	R/WC	0b

BITS	DESCRIPTION	TYPE	DEFAULT
3	**1588 Port 0(Host MAC) TX Interrupt (1588_MII_TX_INT)** This interrupt indicates that a packet from the Host MAC to the switch fabric matches the configured PTP packet and the 1588 clock was captured. **Note:** For Port 0, receive is defined as data *from* the switch fabric, while transmit is *to* the switch fabric.	R/WC	0b
2	**1588 GPIO9 Interrupt (1588_GPIO9_INT)** This interrupt indicates that an event on GPIO9 occurred and the 1588 clock was captured. These interrupts are configured through the General Purpose I/O Configuration Register (GPIO_CFG) register. **Note:** As 1588 capture inputs, GPIO inputs are edge sensitive and must be active for greater than 40 nS to be recognized as interrupt inputs.	R/WC	0b
1	**1588 GPIO8 Interrupt (1588_GPIO8_INT)** This interrupt indicates that an event on GPIO8 occurred and the 1588 clock was captured. These interrupts are configured through the General Purpose I/O Configuration Register (GPIO_CFG) register. **Note:** As 1588 capture inputs, GPIO inputs are edge sensitive and must be active for greater than 40 nS to be recognized as interrupt inputs.	R/WC	0b
0	**1588 Timer Interrupt (1588_TIMER_INT)** This interrupt indicates that the 1588 clock equaled or passed the Clock Target value in the 1588 Clock Target High-DWORD Register (1588_CLOCK_TARGET_HI) and 1588 Clock Target Low-DWORD Register (1588_CLOCK_TARGET_LO). **Note:** This bit is also cleared by an active edge on GPIO[9:8] if enabled. For the clear function, GPIO inputs are edge sensitive and must be active for greater than 40 nS to be recognized as a clear input. Refer to Section 13.2, "GPIO Operation," on page 162 for additional information.	R/WC	0b

14.2.5.24 1588 Command Register (1588_CMD)

Offset: 19Ch Size: 32 bits

This register is used to issue 1588 commands. Using the clock snapshot bit allows the host to properly read the current IEEE 1588 clock values from the 1588 Clock High-DWORD Register (1588_CLOCK_HI) and 1588 Clock Low-DWORD Register (1588_CLOCK_LO). Refer to section Section 11.3, "IEEE 1588 Clock," on page 159 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Clock Snapshot (1588_CLOCK_SNAPSHOT)** Setting this bit causes the current 1588 Clock High-DWORD Register (1588_CLOCK_HI) and 1588 Clock Low-DWORD Register (1588_CLOCK_LO) values to be saved so they can be read.	WO SC	0b

14.2.6 Switch Fabric

This section details the memory mapped System CSR's which are related to the Switch Fabric. The flow control of all three ports of the switch fabric can be configured via the memory mapped System CSR's MANUAL_FC_1, MANUAL_FC_2 and MANUAL_FC_MII. The MAC address used by the switch for Pause frames is configured via the SWITCH_MAC_ADDRH and SWITCH_MAC_ADDRL registers. In addition, the SWITCH_CSR_CMD, SWITCH_CSR_DATA and SWITCH_CSR_DIRECT_DATA registers serve as a memory mapped accessible interface to the full range of otherwise inaccessible switch control and status registers. A list of all the switch fabric CSRs can be seen in Table 14.12. For additional information on the switch fabric, including a full explanation on how to use the switch fabric CSR interface registers, refer to Chapter 6, "Switch Fabric," on page 55. For detailed descriptions of the Switch Fabric CSR's that are accessible via these interface registers, refer to section Section 14.5, "Switch Fabric Control and Status Registers".

14.2.6.1 Port 1 Manual Flow Control Register (MANUAL_FC_1)

Offset: 1A0h Size: 32 bits

This read/write register allows for the manual configuration of the switch Port 1 flow control. This register also provides read back of the currently enabled flow control settings, whether set manually or Auto-Negotiated. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 58 for additional information.

Note: The flow control values in the PHY_AN_ADV_1 register (see Section 14.4.2.5, on page 294) within the PHY are not affected by the values of this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31:7	**RESERVED**	RO	-
6	**Port 1 Backpressure Enable (BP_EN_1)** This bit enables/disables the generation of half-duplex backpressure on switch Port 1. **0: Disable backpressure** **1: Enable backpressure**	R/W	Note 14.4
5	**Port 1 Current Duplex (CUR_DUP_1)** This bit indicates the actual duplex setting of switch Port 1. **0: Full-Duplex** **1: Half-Duplex**	RO	Note 14.5
4	**Port 1 Current Receive Flow Control Enable (CUR_RX_FC_1)** This bit indicates the actual receive flow setting of switch Port 1. **0: Flow control receive is currently disabled** **1: Flow control receive is currently enabled**	RO	Note 14.5
3	**Port 1 Current Transmit Flow Control Enable (CUR_TX_FC_1)** This bit indicates the actual transmit flow setting of switch Port 1. **0: Flow control transmit is currently disabled** **1: Flow control transmit is currently enabled**	RO	Note 14.5
2	**Port 1 Full-Duplex Receive Flow Control Enable (RX_FC_1)** When the MANUAL_FC_1 bit is set, or Auto-Negotiation is disabled, this bit enables/disables the detection of full-duplex Pause packets on switch Port 1. **0: Disable flow control receive** **1: Enable flow control receive**	R/W	Note 14.6

BITS	DESCRIPTION	TYPE	DEFAULT
1	**Port 1 Full-Duplex Transmit Flow Control Enable (TX_FC_1)** When the MANUAL_FC_1 bit is set, or Auto-Negotiation is disabled, this bit enables/disables full-duplex Pause packets to be generated on switch Port 1. **0: Disable flow control transmit** **1: Enable flow control transmit**	R/W	Note 14.6
0	**Port 1 Full-Duplex Manual Flow Control Select (MANUAL_FC_1)** This bit toggles flow control selection between manual and auto-negotiation. **0: If auto-negotiation is enabled, the auto-negotiation function determines the flow control of switch Port 1 (RX_FC_1 and TX_FC_1 values ignored). If auto-negotiation is disabled, the RX_FC_1 and TX_FC_1 values are used.** **1: TX_FC_1 and RX_FC_1 bits determine the flow control of switch Port 1 when in full-duplex mode**	R/W	Note 14.7

Note 14.4 The default value of this field is determined by the BP_EN_strap_1 configuration strap. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 40 for more information.

Note 14.5 The default value of this bit is determined by multiple strap settings. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 58 for additional information.

Note 14.6 The default value of this field is determined by the FD_FC_strap_1 configuration strap. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 40 for more information.

Note 14.7 The default value of this field is determined by the manual_FC_strap_1 configuration strap. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 40 for more information.

14.2.6.2 Port 2 Manual Flow Control Register (MANUAL_FC_2)

Offset: 1A4h Size: 32 bits

This read/write register allows for the manual configuration of the switch Port 2 flow control. This register also provides read back of the currently enabled flow control settings, whether set manually or Auto-Negotiated. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 58 for additional information.

Note: The flow control values in the PHY_AN_ADV_2 register (see Section 14.4.2.5, on page 294) within the PHY are not affected by the values of this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31:7	**RESERVED**	RO	-
6	**Port 2 Backpressure Enable (BP_EN_2)** This bit enables/disables the generation of half-duplex backpressure on switch Port 2. **0: Disable backpressure** **1: Enable backpressure**	R/W	Note 14.8
5	**Port 2 Current Duplex (CUR_DUP_2)** This bit indicates the actual duplex setting of switch Port 2. **0: Full-Duplex** **1: Half-Duplex**	RO	Note 14.9
4	**Port 2 Current Receive Flow Control Enable (CUR_RX_FC_2)** This bit indicates the actual receive flow setting of switch Port 2. **0: Flow control receive is currently disabled** **1: Flow control receive is currently enabled**	RO	Note 14.9
3	**Port 2 Current Transmit Flow Control Enable (CUR_TX_FC_2)** This bit indicates the actual transmit flow setting of switch Port 2. **0: Flow control transmit is currently disabled** **1: Flow control transmit is currently enabled**	RO	Note 14.9
2	**Port 2 Full-Duplex Receive Flow Control Enable (RX_FC_2)** When the MANUAL_FC_2 bit is set, or Auto-Negotiation is disabled, this bit enables/disables the detection of full-duplex Pause packets on switch Port 2. **0: Disable flow control receive** **1: Enable flow control receive**	R/W	Note 14.10
1	**Port 2 Full-Duplex Transmit Flow Control Enable (TX_FC_2)** When the MANUAL_FC_2 bit is set, or Auto-Negotiation is disabled, this bit enables/disables full-duplex Pause packets to be generated on switch Port 2. **0: Disable flow control transmit** **1: Enable flow control transmit**	R/W	Note 14.10

BITS	DESCRIPTION	TYPE	DEFAULT
0	**Port 2 Full-Duplex Manual Flow Control Select (MANUAL_FC_2)** This bit toggles flow control selection between manual and auto-negotiation. **0: If auto-negotiation is enabled, the auto-negotiation function determines the flow control of switch Port 2 (RX_FC_2 and TX_FC_2 values ignored). If auto-negotiation is disabled, the RX_FC_2 and TX_FC_2 values are used.** **1: TX_FC_2 and RX_FC_2 bits determine the flow control of switch Port 2 when in full-duplex mode**	R/W	Note 14.11

Note 14.8 The default value of this field is determined by the BP_EN_strap_2 configuration strap. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 40 for more information.

Note 14.9 The default value of this bit is determined by multiple strap settings. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 58 for additional information.

Note 14.10 The default value of this field is determined by the FD_FC_strap_2 configuration strap. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 40 for more information.

Note 14.11 The default value of this field is determined by the manual_FC_strap_2 configuration strap. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 40 for more information.

14.2.6.3 Port 0(Host MAC) Manual Flow Control Register (MANUAL_FC_MII)

Offset: 1A8h Size: 32 bits

This read/write register allows for the manual configuration of the switch Port 0(Host MAC) flow control. This register also provides read back of the currently enabled flow control settings, whether set manually or Auto-Negotiated. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 58 for additional information.

Note: The flow control values in the Section 14.2.8.5, "Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV)," on page 252 are not affected by the values of this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7	**Port 0 Hard-wired Flow Control (HW_FC_MII)** When set to “1”, the Host MACs RX FIFO level is connected to the switch engine’s transmitter and the switch engines RX FIFO level is connected to the Host MACs transmitter. This achieves lower latency flow control. **Note:** All other flow control methods must be disabled when using this feature. (MANUAL_FC_MII should be set, TX_FC_MII, RX_FC_MII, and BP_EN_MII should be cleared. FCANY, FCADD, FCBRD, and FCMULT in the AFC_CFG register should be cleared).	R/W	0b
6	**Port 0 Backpressure Enable (BP_EN_MII)** This bit enables/disables the generation of half-duplex backpressure on switch Port 0. **0: Disable backpressure** **1: Enable backpressure**	R/W	Note 14.12
5	**Port 0 Current Duplex (CUR_DUP_MII)** This bit indicates the actual duplex setting of the switch Port 0. **0: Full-Duplex** **1: Half-Duplex**	RO	Note 14.13
4	**Port 0 Current Receive Flow Control Enable (CUR_RX_FC_MII)** This bit indicates the actual receive flow setting of switch Port 0 **0: Flow control receive is currently disabled** **1: Flow control receive is currently enabled**	RO	Note 14.13
3	**Port 0 Current Transmit Flow Control Enable (CUR_TX_FC_MII)** This bit indicates the actual transmit flow setting of switch Port 0. **0: Flow control transmit is currently disabled** **1: Flow control transmit is currently enabled**	RO	Note 14.13
2	**Port 0 Receive Flow Control Enable (RX_FC_MII)** When the MANUAL_FC_MII bit is set, or Virtual Auto-Negotiation is disabled, this bit enables/disables the detection of full-duplex Pause packets on switch Port 0. **0: Disable flow control receive** **1: Enable flow control receive**	R/W	Note 14.14

BITS	DESCRIPTION	TYPE	DEFAULT
1	**Port 0 Transmit Flow Control Enable (TX_FC_MII)** When the MANUAL_FC_MII bit is set, or Virtual Auto-Negotiation is disabled, this bit enables/disables full-duplex Pause packets to be generated on switch Port 0. **0: Disable flow control transmit** **1: Enable flow control transmit**	R/W	Note 14.14
0	**Port 0 Full-Duplex Manual Flow Control Select (MANUAL_FC_MII)** This bit toggles flow control selection between manual and auto-negotiation. **0: If auto-negotiation is enabled, the auto-negotiation function determines the flow control of switch Port 0 (RX_FC_MII and TX_FC_MII values ignored). If auto-negotiation is disabled, the RX_FC_MII and TX_FC_MII values are used.** **1: TX_FC_MII and RX_FC_MII bits determine the flow control of switch Port 0 when in full-duplex mode**	R/W	Note 14.15

Note 14.12 The default value of this field is determined by the BP_EN_strap_mii configuration strap. The strap value is loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the value, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 40 for more information.

Note 14.13 The default value of this bit is determined by multiple strap settings. The strap values are loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the values, this register is updated with the new values. Refer to Section 6.2.3, "Flow Control Enable Logic," on page 58 for additional information.

Note 14.14 The default value of this field is determined by the FD_FC_strap_mii configuration strap. The strap value is loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the value, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 40 for more information.

Note 14.15 The default value of this field is determined by the manual_FC_strap_mii configuration strap. The strap value is loaded during reset and can be re-written by the EEPROM Loader. Once the EEPROM Loader re-writes the value, this register is updated with the new values. See Section 4.2.4, "Configuration Straps," on page 40 for more information.

14.2.6.4 Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA)

Offset: 1ACh Size: 32 bits

This read/write register is used in conjunction with the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) to perform read and write operations with the Switch Fabric CSR's. Refer to Section 14.5, "Switch Fabric Control and Status Registers," on page 308 for details on the registers indirectly accessible via this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Switch CSR Data (CSR_DATA)** This field contains the value read from or written to the Switch Fabric CSR. The Switch Fabric CSR is selected via the CSR Address (CSR_ADDR[15:0]) bits of the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD). Upon a read, the value returned depends on the R/nW bit in the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD). If R/nW is set, the data is from the switch fabric. If R/nW is cleared, the data is the value that was last written into this register.	R/W	00000000h

14.2.6.5 Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD)

Offset: 1B0h Size: 32 bits

This read/write register is used in conjunction with the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) to control the read and write operations to the various Switch Fabric CSR's. Refer to Section 14.5, "Switch Fabric Control and Status Registers," on page 308 for details on the registers indirectly accessible via this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**CSR Busy (CSR_BUSY)** When a 1 is written to this bit, the read or write operation (as determined by the R_nW bit) is performed to the specified Switch Fabric CSR in CSR Address (CSR_ADDR[15:0]). This bit will remain set until the operation is complete, at which time the bit will clear. In the case of a read, the clearing of this bit indicates to the Host that valid data can be read from the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA). The SWITCH_CSR_CMD and SWITCH_CSR_DATA registers should not be modified until this bit is cleared.	R/W SC	0b
30	**Read/Write (R_nW)** This bit determines whether a read or write operation is performed by the Host to the specified Switch Engine CSR. **0: Write** **1: Read**	R/W	0b
29	**Auto Increment (AUTO_INC)** This bit enables/disables the auto increment feature. When this bit is set, a write to the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) register will automatically set the CSR Busy (CSR_BUSY) bit. Once the write command is finished, the CSR Address (CSR_ADDR[15:0]) will automatically increment. When this bit is set, a read from the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) will automatically increment the CSR Address (CSR_ADDR[15:0]) and set the CSR Busy (CSR_BUSY) bit. This bit should be cleared by software before the last read from the SWITCH_CSR_DATA register. **0: Disable Auto Increment** **1: Enable Auto Increment** **Note:** This bit has precedence over the Auto Decrement (AUTO_DEC) bit	R/W	0b
28	**Auto Decrement (AUTO_DEC)** This bit enables/disables the auto decrement feature. When this bit is set, a write to the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) will automatically set the CSR Busy (CSR_BUSY) bit. Once the write command is finished, the CSR Address (CSR_ADDR[15:0]) will automatically decrement. When this bit is set, a read from the Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) will automatically decrement the CSR Address (CSR_ADDR[15:0]) and set the CSR Busy (CSR_BUSY) bit. This bit should be cleared by software before the last read from the SWITCH_CSR_DATA register. **0: Disable Auto Decrement** **1: Enable Auto Decrement**	R/W	0b
27:20	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
19:16	**CSR Byte Enable (CSR_BE[3:0])** This field is a 4-bit byte enable used for selection of valid bytes during write operations. Bytes which are not selected will not be written to the corresponding Switch Engine CSR. CSR_BE[3] corresponds to register data bits [31:24] CSR_BE[2] corresponds to register data bits [23:16] CSR_BE[1] corresponds to register data bits [15:8] CSR_BE[0] corresponds to register data bits [7:0] Typically all four byte enables should be set for auto increment and auto decrement operations.	R/W	0h
15:0	**CSR Address (CSR_ADDR[15:0])** This field selects the 16-bit address of the Switch Fabric CSR that will be accessed with a read or write operation. Refer to Table 14.12, “Indirectly Accessible Switch Control and Status Registers,” on page 308 for a list of Switch Fabric CSR addresses.	R/W	00h

14.2.6.6 Switch Fabric MAC Address High Register (SWITCH_MAC_ADDRH)

Offset: 1F0h Size: 32 bits

This register contains the upper 16-bits of the MAC address used by the switch for Pause frames. This register is used in conjunction with Switch Fabric MAC Address Low Register (SWITCH_MAC_ADDRL). The contents of this register are optionally loaded from the EEPROM at power-on through the EEPROM Loader if a programmed EEPROM is detected. The least significant byte of this register (bits [7:0]) is loaded from address 05h of the EEPROM. The second byte (bits [15:8]) is loaded from address 06h of the EEPROM. These EEPROM values are also loaded into the Host MAC Address High Register (HMAC_ADDRH). The Host can update the contents of this field after the initialization process has completed.

Refer to Section 9.6, "Host MAC Address," on page 119 for details on how the EEPROM Loader loads this register. Section 10.2.4, "EEPROM Loader," on page 149 contains additional details on using the EEPROM Loader.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**Physical Address[47:32]** This field contains the upper 16-bits (47:32) of the physical address of the Switch Fabric MACs.	R/W	FFFFh

14.2.6.7 Switch Fabric MAC Address Low Register (SWITCH_MAC_ADDRL)

Offset: 1F4h Size: 32 bits

This register contains the lower 32-bits of the MAC address used by the switch for Pause frames. This register is used in conjunction with Switch Fabric MAC Address High Register (SWITCH_MAC_ADDRH). The contents of this register are optionally loaded from the EEPROM at power-on through the EEPROM Loader if a programmed EEPROM is detected. The least significant byte of this register (bits [7:0]) is loaded from address 01h of the EEPROM. The most significant byte (bits [31:24]) is loaded from address 04h of the EEPROM. These EEPROM values are also loaded into the Host MAC Address Low Register (HMAC_ADDRL). The Host can update the contents of this field after the initialization process has completed.

Refer to Section 9.6, "Host MAC Address," on page 119 for details on how the EEPROM Loader loads this register. Refer to Section 10.2.4, "EEPROM Loader," on page 149 for information on using the EEPROM Loader.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Physical Address[31:0]** This field contains the lower 32-bits (31:0) of the physical address of the Switch Fabric MACs.	R/W	FF0F8000h

14.2.6.8 Switch Fabric CSR Interface Direct Data Register (SWITCH_CSR_DIRECT_DATA)

Offset: 200h - 2DCh Size: 32 bits

This write-only register set is used to perform directly addressed write operations to the Switch Fabric CSR's. Using this set of registers, writes can be directly addressed to select Switch Fabric registers, as specified in Table 14.3.

Writes within the Switch Fabric CSR Interface Direct Data Register (SWITCH_CSR_DIRECT_DATA) address range automatically set the appropriate address, set the four byte enable bits, clear the R/nW bit and set the Busy bit in the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD). The completion of the write cycle is indicated when the Busy bit is cleared. The address that is set in the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) is mapped via Table 14.3. For more information on this method of writing to the Switch Fabric CSR's, refer to Section 6.2.3, "Flow Control Enable Logic," on page 58.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Switch CSR Data (CSR_DATA)** This field contains the value to be written to the corresponding Switch Fabric register.	WO	00000000h

Note: This set of registers is for write operations only. Reads can be performed via the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD) and Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA) registers only.

Table 14.3 Switch Fabric CSR to SWITCH_CSR_DIRECT_DATA Address Range Map

REGISTER NAME	SWITCH FABRIC CSR REGISTER #	SWITCH_CSR_DIRECT_DATA ADDRESS
General Switch CSRs		
SW_RESET	0001h	200h
SW_IMR	0004h	204h
Switch Port 0 CSRs		
MAC_RX_CFG_MII	0401h	208h
MAC_TX_CFG_MII	0440h	20Ch
MAC_TX_FC_SETTINGS_MII	0441h	210h
MAC_IMR_MII	0480h	214h
Switch Port 1 CSRs		
MAC_RX_CFG_1	0801h	218h
MAC_TX_CFG_1	0840h	21Ch
MAC_TX_FC_SETTINGS_1	0841h	220h
MAC_IMR_1	0880h	224h
Switch Port 2 CSRs		
MAC_RX_CFG_2	0C01h	228h

Table 14.3 Switch Fabric CSR to SWITCH_CSR_DIRECT_DATA Address Range Map (continued)

REGISTER NAME	SWITCH FABRIC CSR REGISTER #	SWITCH_CSR_DIRECT_DATA ADDRESS
MAC_TX_CFG_2	0C40h	22Ch
MAC_TX_FC_SETTINGS_2	0C41h	230h
MAC_IMR_2	0C80h	234h
Switch Engine CSRs		
SWE_ALR_CMD	1800h	238h
SWE_ALR_WR_DAT_0	1801h	23Ch
SWE_ALR_WR_DAT_1	1802h	240h
SWE_ALR_CFG	1809h	244h
SWE_VLAN_CMD	180Bh	248h
SWE_VLAN_WR_DATA	180Ch	24Ch
SWE_DIFFSERV_TBL_CMD	1811h	250h
SWE_DIFFSERV_TBL_WR_DATA	1812h	254h
SWE_GLB_INGRESS_CFG	1840h	258h
SWE_PORT_INGRESS_CFG	1841h	25Ch
SWE_ADMT_ONLY_VLAN	1842h	260h
SWE_PORT_STATE	1843h	264h
SWE_PRI_TO_QUE	1845h	268h
SWE_PORT_MIRROR	1846h	26Ch
SWE_INGRESS_PORT_TYP	1847h	270h
SWE_BCST_THROT	1848h	274h
SWE_ADMT_N_MEMBER	1849h	278h
SWE_INGRESS_RATE_CFG	184Ah	27Ch
SWE_INGRESS_RATE_CMD	184Bh	280h
SWE_INGRESS_RATE_WR_DATA	184Dh	284h
SWE_INGRESS_REGEN_TBL_MII	1855h	288h
SWE_INGRESS_REGEN_TBL_1	1856h	28Ch
SWE_INGRESS_REGEN_TBL_2	1857h	290h
SWE_IMR	1880h	294h
Buffer Manager (BM) CSRs		
BM_CFG	1C00h	298h
BM_DROP_LVL	1C01h	29Ch
BM_FC_PAUSE_LVL	1C02h	2A0h

Table 14.3 Switch Fabric CSR to SWITCH_CSR_DIRECT_DATA Address Range Map (continued)

REGISTER NAME	SWITCH FABRIC CSR REGISTER #	SWITCH_CSR_DIRECT_DATA ADDRESS
BM_FC_RESUME_LVL	1C03h	2A4h
BM_BCST_LVL	1C04h	2A8h
BM_RNDM_DSCRD_TBL_CMD	1C09h	2ACh
BM_RNDM_DSCRD_TBL_WDATA	1C0Ah	2B0h
BM_EGRSS_PORT_TYPE	1C0Ch	2B4h
BM_EGRSS_RATE_00_01	1C0Dh	2B8h
BM_EGRSS_RATE_02_03	1C0Eh	2BCh
BM_EGRSS_RATE_10_11	1C0Fh	2C0h
BM_EGRSS_RATE_12_13	1C10h	2C4h
BM_EGRSS_RATE_20_21	1C11h	2C8h
BM_EGRSS_RATE_22_23	1C12h	2CCh
BM_VLAN_MII	1C13h	2D0h
BM_VLAN_1	1C14h	2D4h
BM_VLAN_2	1C15h	2D8h
BM_IMR	1C20h	2DCh

14.2.7 PHY Management Interface (PMI)

The PMI registers are used (by the EEPROM Loader only) to indirectly access the PHY registers. Refer to Section 14.4, "Ethernet PHY Control and Status Registers," on page 286 for additional information on the PHY registers.

Note: These registers are only accessible by the EEPROM Loader and *NOT* by the Host bus. Refer to Section 10.2.4, "EEPROM Loader," on page 149 for additional information.

14.2.7.1 PHY Management Interface Data Register (PMI_DATA)

Offset:	0A4h EEPROM Loader Access Only	Size:	32 bits

This register is used in conjunction with the PHY Management Interface Access Register (PMI_ACCESS) to perform write operations to the PHYs.

Note: This register is only accessible by the EEPROM Loader and *NOT* by the Host bus. Refer to Section 10.2.4, "EEPROM Loader," on page 149 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**MII Data** This field contains the value written to the PHYs. For a write operation, this register should be first written with the desired data.	WO	00000000h

14.2.7.2 PHY Management Interface Access Register (PMI_ACCESS)

Offset: 0A8h EEPROM Loader Access Only

Size: 32 bits

This register is used to control the management cycles to the PHYs. A PHY access is initiated when this register is written. This register is used in conjunction with the PHY Management Interface Data Register (PMI_DATA) to perform write operations to the PHYs.

Note: This register is only accessible by the EEPROM Loader and *NOT* by the Host bus. Refer to Section 10.2.4, "EEPROM Loader," on page 149 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:11	**PHY Address (PHY_ADDR)** These bits select the PHY device being accessed. Refer to Section 7.1.1, "PHY Addressing," on page 82 for information on PHY address assignments.	WO	00000b
10:6	**MII Register Index (MIIRINDA)** These bits select the desired MII register in the PHY. Refer to Section 14.4, "Ethernet PHY Control and Status Registers," on page 286 for detailed descriptions on all PHY registers.	WO	00000b
5:2	**RESERVED**	RO	-
1	**RESERVED** **Note:** This bit must always be written with a value of 1.	WO	0b
0	**RESERVED**	RO	0b

14.2.8 Virtual PHY

This section details the Virtual PHY System CSR's. These registers provide status and control information similar to that of a real PHY while maintaining IEEE 802.3 compatibility. The Virtual PHY registers are addressable via the memory map, as described in Table 14.1, as well as serially via the MII management protocol (IEEE 802.3 clause 22). When accessed serially, these registers are accessed indirectly through the Host MAC MII Access Register (HMAC_MII_ACC) and Host MAC MII Data Register (HMAC_MII_DATA) via the MII serial management protocol specified in IEEE 802.3 clause 22. When being accessed serially, the Virtual PHY will respond when the PHY address equals the address assigned by the phy_addr_sel_strap configuration strap, as defined in Section 7.1.1, "PHY Addressing," on page 82. A list of all Virtual PHY register indexes for serial access can be seen in Table 14.4. For more information on the Virtual PHY access modes, refer to section Section 14.4. For Virtual PHY functionality and operation information, see Section 7.3, "Virtual PHY," on page 96.

Note: All Virtual PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set. All functionality and bit definitions comply with these standards. The IEEE 802.3 specified register index (in decimal) is included under the LAN9312 memory mapped offset of each Virtual PHY register as a reference. For additional information, refer to the IEEE 802.3 Specification.

Note: When serially accessed, the Virtual PHY registers are only 16-bits wide, as is standard for MII management of PHY's.

Table 14.4 Virtual PHY MII Serially Adressable Register Index

INDEX #	SYMBOL	REGISTER NAME
0	VPHY_BASIC_CTRL	Virtual PHY Basic Control Register, Section 14.2.8.1
1	VPHY_BASIC_STATUS	Virtual PHY Basic Status Register, Section 14.2.8.2
2	VPHY_ID_MSB	Virtual PHY Identification MSB Register, Section 14.2.8.3
3	VPHY_ID_LSB	Virtual PHY Identification LSB Register, Section 14.2.8.4
4	VPHY_AN_ADV	Virtual PHY Auto-Negotiation Advertisement Register, Section 14.2.8.5
5	VPHY_AN_LP_BASE_ABILITY	Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register, Section 14.2.8.6
6	VPHY_AN_EXP	Virtual PHY Auto-Negotiation Expansion Register, Section 14.2.8.7
31	VPHY_SPEC_CTRL_STATUS	Virtual PHY Special Control/Status Register, Section 14.2.8.8

14.2.8.1 Virtual PHY Basic Control Register (VPHY_BASIC_CTRL)

Offset: 1C0h Size: 32 bits
Index (decimal): 0

This read/write register is used to configure the Virtual PHY.

Note: This register is re-written in its entirety by the EEPROM Loader following the release or reset or a RELOAD command. Refer to Section 10.2.4, "EEPROM Loader," on page 149 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 14.16)	RO	-
15	**Reset (VPHY_RST)** When set, this bit resets all the Virtual PHY registers to their default state. This bit is self clearing. **0: Normal Operation** **1: Reset**	R/W SC	0b
14	**Loopback (VPHY_LOOPBACK)** This bit enables/disables the loopback mode. When enabled, transmissions from the Host MAC are not sent to the switch fabric. Instead, they are looped back onto the receive path. **0: Loopback mode disabled (normal operation)** **1: Loopback mode enabled**	R/W	0b
13	**Speed Select LSB (VPHY_SPEED_SEL_LSB)** This bit is used to set the speed of the Virtual PHY when the Auto-Negotiation (VPHY_AN) bit is disabled. **0: 10 Mbps** **1: 100 Mbps**	R/W	0b
12	**Auto-Negotiation (VPHY_AN)** This bit enables/disables Auto-Negotiation. When enabled, the Speed Select LSB (VPHY_SPEED_SEL_LSB) and Duplex Mode (VPHY_DUPLEX) bits are overridden. **0: Auto-Negotiation disabled** **1: Auto-Negotiation enabled**	R/W	1b
11	**Power Down (VPHY_PWR_DWN)** This bit is not used by the Virtual PHY and has no effect.	R/W	0b
10	**Isolate (VPHY_ISO)** This bit is not used by the Virtual PHY and has no effect.	R/W	0b
9	**Restart Auto-Negotiation (VPHY_RST_AN)** When set, this bit updates the emulated Auto-Negotiation results. **0: Normal operation** **1: Auto-Negotiation restarted**	R/W SC	0b
8	**Duplex Mode (VPHY_DUPLEX)** This bit is used to set the duplex when the Auto-Negotiation (VPHY_AN) bit is disabled. **0: Half Duplex** **1: Full Duplex**	R/W	0b

BITS	DESCRIPTION	TYPE	DEFAULT
7	**Collision Test (VPHY_COL_TEST)** This bit enables/disables the collision test mode. When set, the collision signal to the Host MAC is active during transmission from the Host MAC. **Note:** It is recommended that this bit be used only when in loopback mode. **0: Collision test mode disabled** **1: Collision test mode enabled**	R/W	0b
6	**Speed Select MSB (VPHY_SPEED_SEL_MSB)** This bit is not used by the Virtual PHY and has no effect. The value returned is always 0.	RO	0b
5:0	**RESERVED**	RO	-

Note 14.16 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

14.2.8.2 Virtual PHY Basic Status Register (VPHY_BASIC_STATUS)

Offset: 1C4h Size: 32 bits
Index (decimal): 1

This register is used to monitor the status of the Virtual PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 14.17)	RO	-
15	**100BASE-T4** This bit displays the status of 100BASE-T4 compatibility. **0: PHY not able to perform 100BASE-T4** **1: PHY able to perform 100BASE-T4**	RO	0b Note 14.18
14	**100BASE-X Full Duplex** This bit displays the status of 100BASE-X full duplex compatibility. **0: PHY not able to perform 100BASE-X full duplex** **1: PHY able to perform 100BASE-X full duplex**	RO	1b
13	**100BASE-X Half Duplex** This bit displays the status of 100BASE-X half duplex compatibility. **0: PHY not able to perform 100BASE-X half duplex** **1: PHY able to perform 100BASE-X half duplex**	RO	1b
12	**10BASE-T Full Duplex** This bit displays the status of 10BASE-T full duplex compatibility. **0: PHY not able to perform 10BASE-T full duplex** **1: PHY able to perform 10BASE-T full duplex**	RO	1b
11	**10BASE-T Half Duplex** This bit displays the status of 10BASE-T half duplex compatibility. **0: PHY not able to perform 10BASE-T half duplex** **1: PHY able to perform 10BASE-T half duplex**	RO	1b
10	**100BASE-T2 Full Duplex** This bit displays the status of 100BASE-T2 full duplex compatibility. **0: PHY not able to perform 100BASE-T2 full duplex** **1: PHY able to perform 100BASE-T2 full duplex**	RO	0b Note 14.18
9	**100BASE-T2 Half Duplex** This bit displays the status of 100BASE-T2 half duplex compatibility. **0: PHY not able to perform 100BASE-T2 half duplex** **1: PHY able to perform 100BASE-T2 half duplex**	RO	0b Note 14.18
8	**Extended Status** This bit displays whether extended status information is in register 15 (per IEEE 802.3 clause 22.2.4). **0: No extended status information in Register 15** **1: Extended status information in Register 15**	RO	0b Note 14.19
7	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
6	**MF Preamble Suppression** This bit indicates whether the Virtual PHY accepts management frames with the preamble suppressed. **0: Management frames with preamble suppressed not accepted** **1: Management frames with preamble suppressed accepted**	RO	0b
5	**Auto-Negotiation Complete** This bit indicates the status of the Auto-Negotiation process. **0: Auto-Negotiation process not completed** **1: Auto-Negotiation process completed**	RO	1b Note 14.20
4	**Remote Fault** This bit indicates if a remote fault condition has been detected. **0: No remote fault condition detected** **1: Remote fault condition detected**	RO	0b Note 14.21
3	**Auto-Negotiation Ability** This bit indicates the status of the Virtual PHY's auto-negotiation. **0: Virtual PHY is unable to perform auto-negotiation** **1: Virtual PHY is able to perform auto-negotiation**	RO	1b
2	**Link Status** This bit indicates the status of the link. **0: Link is down** **1: Link is up**	RO	1b Note 14.21
1	**Jabber Detect** This bit indicates the status of the jabber condition. **0: No jabber condition detected** **1: Jabber condition detected**	RO	0b Note 14.21
0	**Extended Capability** This bit indicates whether extended register capability is supported. **0: Basic register set capabilities only** **1: Extended register set capabilities**	RO	1b Note 14.22

Note 14.17 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 14.18 The Virtual PHY supports 100BASE-X (half and full duplex) and 10BASE-T (half and full duplex) only. All other modes will always return as 0 (unable to perform).

Note 14.19 The Virtual PHY does not support Register 15 or 1000 Mb/s operation. Thus this bit is always returned as 0.

Note 14.20 The Auto-Negotiation Complete bit is first cleared on a reset, but set shortly after (when the Auto-Negotiation process is run). Refer to Section 7.3.1, "Virtual PHY Auto-Negotiation," on page 96 for additional details.

Note 14.21 The Virtual PHY never has remote faults, its link is always up, and does not detect jabber.

Note 14.22 The VIrtual PHY supports basic and some extended register capability. The Virtual PHY supports Registers 0-6 (per the IEEE 802.3 specification).

14.2.8.3 Virtual PHY Identification MSB Register (VPHY_ID_MSB)

Offset: 1C8h Size: 32 bits
Index (decimal): 2

This read/write register contains the MSB of the Virtual PHY Organizationally Unique Identifier (OUI). The LSB of the Virtual PHY OUI is contained in the Virtual PHY Identification LSB Register (VPHY_ID_LSB).

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 14.23)	RO	-
15:0	**PHY ID** This field contains the MSB of the Virtual PHY OUI (Note 14.24).	R/W	0000h

Note 14.23 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 14.24 IEEE allows a value of zero in each of the 32-bits of the PHY Identifier.

14.2.8.4 Virtual PHY Identification LSB Register (VPHY_ID_LSB)

Offset: 1CCh Size: 32 bits
Index (decimal): 3

This read/write register contains the LSB of the Virtual PHY Organizationally Unique Identifier (OUI). The MSB of the Virtual PHY OUI is contained in the Virtual PHY Identification MSB Register (VPHY_ID_MSB).

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 14.25)	RO	-
15:10	**PHY ID** This field contains the lower 6-bits of the Virtual PHY OUI (Note 14.26).	R/W	000000b
9:4	**Model Number** This field contains the 6-bit manufacturer's model number of the Virtual PHY (Note 14.26).	R/W	000000b
3:0	**Revision Number** This field contain the 4-bit manufacturer's revision number of the Virtual PHY (Note 14.26).	R/W	0000b

Note 14.25 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 14.26 IEEE allows a value of zero in each of the 32-bits of the PHY Identifier.

14.2.8.5 Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV)

Offset: 1D0h Size: 32 bits
Index (decimal): 4

This read/write register contains the advertised ability of the Virtual PHY and is used in the Auto-Negotiation process with the link partner.

Note: This register is re-written in its entirety by the EEPROM Loader following the release or reset or a RELOAD command. Refer to Section 10.2.4, "EEPROM Loader," on page 149 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 14.27)	RO	-
15	**Next Page** This bit determines the advertised next page capability and is always 0. **0: Virtual PHY does not advertise next page capability** **1: Virtual PHY advertises next page capability**	RO	0b Note 14.28
14	**RESERVED**	RO	-
13	**Remote Fault** This bit is not used since there is no physical link partner.	RO	0b Note 14.29
12	**RESERVED**	RO	-
11	**Asymmetric Pause** This bit determines the advertised asymmetric pause capability. **0: No Asymmetric PAUSE toward link partner advertised** **1: Asymmetric PAUSE toward link partner advertised**	R/W	0b
10	**Pause** This bit determines the advertised symmetric pause capability. **0: No Symmetric PAUSE toward link partner advertised** **1: Symmetric PAUSE toward link partner advertised**	R/W	Note 14.30
9	**100BASE-T4** This bit determines the advertised 100BASE-T4 capability and is always 0. **0: 100BASE-T4 ability not advertised** **1: 100BASE-T4 ability advertised**	RO	0b Note 14.31
8	**100BASE-X Full Duplex** This bit determines the advertised 100BASE-X full duplex capability. **0: 100BASE-X full duplex ability not advertised** **1: 100BASE-X full duplex ability advertised**	R/W	1b
7	**100BASE-X Half Duplex** This bit determines the advertised 100BASE-X half duplex capability. **0: 100BASE-X half duplex ability not advertised** **1: 100BASE-X half duplex ability advertised**	R/W	1b

BITS	DESCRIPTION	TYPE	DEFAULT
6	**10BASE-T Full Duplex** This bit determines the advertised 10BASE-T full duplex capability. **0: 10BASE-T full duplex ability not advertised** **1: 10BASE-T full duplex ability advertised**	R/W	1b
5	**10BASE-T Half Duplex** This bit determines the advertised 10BASE-T half duplex capability. **0: 10BASE-T half duplex ability not advertised** **1: 10BASE-T half duplex ability advertised**	R/W	1b
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. **00001: IEEE 802.3**	R/W	00001b Note 14.32

Note 14.27 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 14.28 The Virtual PHY does not support next page capability. This bit value will always be 0.

Note 14.29 The Remote Fault bit is not useful since there is no actual link partner to send a fault to.

Note 14.30 The Pause bit defaults to 1 if the manual_FC_strap_mii strap is low, and 0 if the manual_FC_strap_mii strap is high. Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 40.

Note 14.31 Virtual 100BASE-T4 is not supported.

Note 14.32 The Virtual PHY supports only IEEE 802.3. Only a value of 00001b should be used in this field.

14.2.8.6 Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY)

Offset: 1D4h Size: 32 bits
Index (decimal): 5

This read-only register contains the advertised ability of the link partner's PHY and is used in the Auto-Negotiation process with the Virtual PHY. Because the Virtual PHY does not physically connect to an actual link partner, the values in this register are emulated as described below.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 14.33)	RO	-
15	**Next Page** This bit indicates the emulated link partner PHY next page capability and is always 0. **0: Link partner PHY does not advertise next page capability** **1: Link partner PHY advertises next page capability**	RO	0b Note 14.34
14	**Acknowledge** This bit indicates whether the link code word has been received from the partner and is always 1. **0: Link code word not yet received from partner** **1: Link code word received from partner**	RO	1b Note 14.34
13	**Remote Fault** Since there is no physical link partner, this bit is not used and is always returned as 0.	RO	0b Note 14.34
12	**RESERVED**	RO	-
11	**Asymmetric Pause** This bit indicates the emulated link partner PHY asymmetric pause capability. **0: No Asymmetric PAUSE toward link partner** **1: Asymmetric PAUSE toward link partner**	RO	Note 14.35
10	**Pause** This bit indicates the emulated link partner PHY symmetric pause capability. **0: No Symmetric PAUSE toward link partner** **1: Symmetric PAUSE toward link partner**	RO	Note 14.35
9	**100BASE-T4** This bit indicates the emulated link partner PHY 100BASE-T4 capability. This bit is always 0. **0: 100BASE-T4 ability not supported** **1: 100BASE-T4 ability supported**	RO	0b Note 14.34
8	**100BASE-X Full Duplex** This bit indicates the emulated link partner PHY 100BASE-X full duplex capability. **0: 100BASE-X full duplex ability not supported** **1: 100BASE-X full duplex ability supported**	RO	Note 14.36

BITS	DESCRIPTION	TYPE	DEFAULT
7	**100BASE-X Half Duplex** This bit indicates the emulated link partner PHY 100BASE-X half duplex capability. **0: 100BASE-X half duplex ability not supported** **1: 100BASE-X half duplex ability supported**	RO	Note 14.36
6	**10BASE-T Full Duplex** This bit indicates the emulated link partner PHY 10BASE-T full duplex capability. **0: 10BASE-T full duplex ability not supported** **1: 10BASE-T full duplex ability supported**	RO	Note 14.36
5	**10BASE-T Half Duplex** This bit indicates the emulated link partner PHY 10BASE-T half duplex capability. **0: 10BASE-T half duplex ability not supported** **1: 10BASE-T half duplex ability supported**	RO	Note 14.36
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. **00001: IEEE 802.3**	RO	00001b

Note 14.33 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 14.34 The emulated link partner does not support next page, always instantly sends its link code word, never sends a fault, and does not support 100BASE-T4.

Note 14.35 The emulated link partner's asymmetric/symmetric pause ability is based upon the values of the Asymmetric Pause and Pause bits of the Virtual PHY Auto-Negotiation Advertisement Register (VPHY_AN_ADV). Thus the emulated link partner always accommodates the request of the Virtual PHY, as shown in Table 14.5. See Section 7.3.1, "Virtual PHY Auto-Negotiation," on page 96 for additional information.

Table 14.5 Emulated Link Partner Pause Flow Control Ability Default Values

	VPHY Symmetric Pause (register 4.10)	VPHY Asymmetric Pause (register 4.11)	Link Partner Symmetric Pause (register 5.10)	Link Partner Asymmetric Pause (register 5.11)
No Flow Control Enabled	0	0	0	0
Symmetric Pause	1	0	1	0
Asymmetric Pause Towards Switch	0	1	1	1
Asymmetric Pause Towards MAC	1	1	0	1

Note 14.36 The emulated link partner always has the following capabilities: 100BASE-X full duplex, 100BASE-X half duplex, 10BASE-T full duplex, and 10BASE-T half duplex. For more information on the Virtual PHY auto-negotiation, see Section 7.3.1, "Virtual PHY Auto-Negotiation," on page 96.

14.2.8.7 Virtual PHY Auto-Negotiation Expansion Register (VPHY_AN_EXP)

Offset: 1D8h Size: 32 bits
Index (decimal): 6

This register is used in the Auto-Negotiation process.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 14.37)	RO	-
15:5	**RESERVED**	RO	-
4	**Parallel Detection Fault** This bit indicates whether a Parallel Detection Fault has been detected. This bit is always 0. **0: A fault hasn't been detected via the Parallel Detection function** **1: A fault has been detected via the Parallel Detection function**	RO	0b Note 14.38
3	**Link Partner Next Page Able** This bit indicates whether the link partner has next page ability. This bit is always 0. **0: Link partner does not contain next page capability** **1: Link partner contains next page capability**	RO	0b Note 14.39
2	**Local Device Next Page Able** This bit indicates whether the local device has next page ability. This bit is always 0. **0: Local device does not contain next page capability** **1: Local device contains next page capability**	RO	0b Note 14.39
1	**Page Received** This bit indicates the reception of a new page. **0: A new page has not been received** **1: A new page has been received**	RO/LH	1b Note 14.40
0	**Link Partner Auto-Negotiation Able** This bit indicates the Auto-negotiation ability of the link partner. **0: Link partner is not Auto-Negotiation able** **1: Link partner is Auto-Negotiation able**	RO	1b Note 14.41

Note 14.37 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 14.38 Since the Virtual PHY link partner is emulated, there is never a Parallel Detection Fault and this bit is always 0.

Note 14.39 Next page ability is not supported by the Virtual PHY or emulated link partner.

Note 14.40 The page received bit is clear when read. It is first cleared on reset, but set shortly thereafter when the Auto-Negotiation process is run.

Note 14.41 The emulated link partner will show Auto-Negotiation able unless Auto-Negotiation fails (no common bits between the advertised ability and the link partner ability).

14.2.8.8 Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS)

Offset: 1DCh Size: 32 bits
Index (decimal): 31

This read/write register contains a current link speed/duplex indicator and SQE control.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED** (See Note 14.42)	RO	-
15	**RESERVED**	RO	-
14	**Switch Looopback MII** When set, transmissions from the switch fabric Port 0(Host MAC) are not sent to the Host MAC. Instead, they are looped back into the switch engine. From the MAC viewpoint, this is effectively a FAR LOOPBACK. If loopback is enabled during half-duplex operation, then the Enable Receive Own Transmit bit in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x) must be set for this port. Otherwise, the switch fabric will ignore receive activity when transmitting in half-duplex mode. This mode works even if the Isolate bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is set.	R/W	0b
13:8	**RESERVED**	RO	-
7	**Switch Collision Test MII** When set, the collision signal to the switch fabric Port 0(Host MAC) is active during transmission from the switch engine. It is recommended that this bit be used only when using loopback mode.	R/W	0b
6:5	**RESERVED**	RO	-
4:2	**Current Speed/Duplex Indication** This field indicates the current speed and duplex of the Virtual PHY link.	RO	Note 14.43
1	**RESERVED**	RO	-
0	**SQEOFF** This bit enables/disables the Signal Quality Error (Heartbeat) test. **0: SQE test enabled** **1: SQE test disabled**	R/W NASR Note 14.44	Note 14.45

[4]	[3]	[2]	Speed	Duplex
0	0	0	RESERVED	
0	0	1	10Mbps	half-duplex
0	1	0	100Mbps	half-duplex
0	1	1	RESERVED	
1	0	0	RESERVED	
1	0	1	10Mbps	full-duplex
1	1	0	100Mbps	full-duplex
1	1	1	RESERVED	

Note 14.42 The reserved bits 31-16 are used to pad the register to 32-bits so that each register is on a DWORD boundary. When accessed serially (through the MII management protocol), the register is 16-bits wide.

Note 14.43 The default value of this field is the result of the Auto-Negotiation process if the Auto-Negotiation (VPHY_AN) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is set. Otherwise, this field reflects the Speed Select LSB (VPHY_SPEED_SEL_LSB) and Duplex Mode (VPHY_DUPLEX) bit settings of the VPHY_BASIC_CTRL register. Refer to Section 7.3.1, "Virtual PHY Auto-Negotiation," on page 96 for information on the Auto-Negotiation determination process of the Virtual PHY.

Note 14.44 Register bits designated as NASR are reset when the Virtual PHY Reset is generated via the Reset Control Register (RESET_CTL) or Power Management Control Register (PMT_CTRL). The NASR designation is only applicable when the Reset (VPHY_RST) bit of the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) is set.

Note 14.45 The default value of this field is determined via the SQE_test_disable_strap_mii configuration strap. Refer to Section 4.2.4, "Configuration Straps," on page 40 for additional information.

14.2.9 Miscellaneous

This section details the remainder of the System CSR's. These registers allow for monitoring and configuration of various LAN9312 functions such as the Chip ID/revision, byte order testing, power management, hardware configuration, general purpose timer, and free running counter.

14.2.9.1 Chip ID and Revision (ID_REV)

Offset: 050h Size: 32 bits

This read-only register contains the ID and Revision fields for the LAN9312.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**Chip ID** This field indicates the chip ID.	RO	9312h
15:0	**Chip Revision** This field indicates the design revision.	RO	Note 14.46

Note 14.46 Default value is dependent on device revision.

14.2.9.2 Byte Order Test Register (BYTE_TEST)

Offset: 064h Size: 32 bits

This read-only register can be used to determine the byte ordering of the current configuration. Byte ordering is a function of the host data bus width and endianess. Refer to Section 8.3, "Host Endianess," on page 99 for additional information on byte ordering.

Note: This register can be read while the LAN9312 is in the reset or not ready states.

The BYTE_TEST register can optionally be used as a dummy read register when assuring minimum write-to-read or read-to-read timing. Refer to Section 8.4.2, "Special Restrictions on Back-to Back Write-Read Cycles," on page 101 and Section 8.4.3, "Special Restrictions on Back-to-Back Read Cycles," on page 105 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Byte Test (BYTE_TEST)** This field reflects the current byte ordering	RO	87654321h

14.2.9.3 Hardware Configuration Register (HW_CFG)

Offset: 074h Size: 32 bits

This register allows the configuration of various hardware features including TX/RX FIFO sizes, Host MAC transmit threshold properties, and software reset. A detailed explanation of the allowable settings for FIFO memory allocation can be found in Section 9.7.3, "FIFO Memory Allocation Configuration," on page 121.

Note: This register can be polled while the LAN9312 is in the reset or not ready state (READY bit is cleared).

BITS	DESCRIPTION	TYPE	DEFAULT
31:28	**RESERVED**	RO	-
27	**Device Ready (READY)** When set, this bit indicates that the LAN9312 is ready to be accessed. Upon power-up, nRST reset, soft reset, or digital reset, the host processor may interrogate this field as an indication that the LAN9312 has stabilized and is fully active. This bit can cause an interrupt if enabled. **Note:** With the exception of the HW_CFG, PMT_CTRL, BYTE_TEST, and RESET_CTL registers, read access to any internal resources is forbidden while the READY bit is cleared. Writes to any address are invalid until this bit is set. **Note:** This bit is identical to bit 0 of the Power Management Control Register (PMT_CTRL).	RO	0b
26	**AMDIX_EN Strap State Port 2** This bit reflects the state of the auto_mdix_strap_2 strap that connects to the PHY. The strap value is loaded with the level of the auto_mdix_strap_2 during reset and can be re-written by the EEPROM Loader. The strap value can be overridden by bit 15 and 13 of the Port 2 PHY Special Control/Status Indication Register (Section 14.4.2.10).	RO	Note 14.47
25	**AMDIX_EN Strap State Port 1** This bit reflects the state of the auto_mdix_strap_1 strap that connects to the PHY. The strap value is loaded with the level of the auto_mdix_strap_1 during reset and can be re-written by the EEPROM Loader. The strap value can be overridden by bit 15 and 13 of the Port 1 PHY Special Control/Status Indication Register (Section 14.4.2.10).	RO	Note 14.48
24:22	**RESERVED**	RO	-
21	**RESERVED - This bit must be written with 0b for proper operation.**	R/W	0b
20	**Must Be One (MBO).** This bit must be set to ‘1’ for normal device operation.	R/W	0b

BITS	DESCRIPTION	TYPE	DEFAULT
19:16	**TX FIFO Size (TX_FIF_SZ)** This field sets the size of the TX FIFOs in 1KB values to a maximum of 14KB. The TX Status FIFO consumes 512 bytes of the space allocated by TX_FIF_SIZ, and the TX Data FIFO consumes the remaining space specified by TX_FIF_SZ. The minimum size of the TX FIFOs is 2KB (TX Data FIFO and Status FIFO combined). The TX Data FIFO is used for both TX data and TX commands. The RX Status and Data FIFOs consume the remaining space, which is equal to 16KB minus TX_FIF_SIZ. See section Section 9.7.3, "FIFO Memory Allocation Configuration," on page 121 for more information.	R/W	5h
15:14	**RESERVED**	RO	-
13:12	**RESERVED - This field must be written with 00b for proper operation.**	R/W	00b
11:1	**RESERVED**	RO	-
0	**Soft Reset (SRST)** Writing 1 generates a software initiated reset to the Host Bus Interface, the Host MAC, and System CSR's below address 100h. The System CSR's are all reset except for any NASR bits. Soft reset also clears any TX or RX errors in the Host MAC transmitter and receiver (TXE/RXE). This bit is self-clearing. In order to reset all values, the Reset Control Register (RESET_CTL) must be used. **Note:** This bit will read high during assertion of DIGITAL_RST in the Reset Control Register (RESET_CTL). The LAN9312 must always be read at least once after power-up or reset to ensure that write operations function correctly.	R/W SC	0b

Note 14.47 The default value of this field is determined by the configuration strap auto_mdix_strap_2. See Section 4.2.4, "Configuration Straps," on page 40 for more information.

Note 14.48 The default value of this field is determined by the configuration strap auto_mdix_strap_1. See Section 4.2.4, "Configuration Straps," on page 40 for more information.

14.2.9.4 Power Management Control Register (PMT_CTRL)

Offset: 084h Size: 32 bits

This read-write register controls the power management features and the PME pin of the LAN9312. The ready state of the LAN9312 can be determined via the Device Ready (READY) bit of this register. Refer to Section 4.3, "Power Management," on page 46 for additional information.

Note: This register is one of only four registers (the others are HW_CFG, BYTE_TEST, and RESET_CTL) which can be polled while the LAN9312 is in the reset or not ready state (READY bit is cleared).

BITS	DESCRIPTION	TYPE	DEFAULT
31:18	**RESERVED**	RO	-
17	**Energy-Detect Status Port 2 (ED_STS2)** This bit indicates an energy detect event occurred on the Port 2 PHY. In order to clear this bit, it is required that the event in the PHY be cleared as well. The event sources are described in Section 4.3, "Power Management," on page 46.	R/WC	0b
16	**Energy-Detect Status Port 1 (ED_STS1)** This bit indicates an energy detect event occurred on the Port 1 PHY. In order to clear this bit, it is required that the event in the PHY be cleared as well. The event sources are described in Section 4.3, "Power Management," on page 46.	R/WC	0b
15	**Energy-Detect Enable Port 2 (ED_EN2)** When set, the PME signal (if enabled via the PME_EN bit) will be asserted in accordance with the PME_IND bit upon an energy-detect event from Port 2. When set, the PME_INT bit in the Interrupt Status Register (INT_STS) will also be asserted upon an energy-detect event from Port 2, regardless of the setting of the PME_EN bit. **Note:** The EDPWRDOWN bit of the Port x PHY Mode Control/Status Register (PHY_MODE_CONTROL_STATUS_x) of the Port 2 PHY must also be set to enable the energy detect feature.	R/W	0b
14	**Energy-Detect Enable Port 1 (ED_EN1)** When set, the PME signal (if enabled via the PME_EN bit) will be asserted in accordance with the PME_IND bit upon an energy-detect event from Port 1. When set, the PME_INT bit in the Interrupt Status Register (INT_STS) will also be asserted upon an energy-detect event from Port 1, regardless of the setting of the PME_EN bit. **Note:** The EDPWRDOWN bit in the Port x PHY Mode Control/Status Register (PHY_MODE_CONTROL_STATUS_x) of the Port 1 PHY must also be set to enable the energy detect feature.	R/W	0b
13:11	**RESERVED**	RO	-
10	**Virtual PHY Reset (VPHY_RST)** Writing a 1 to this bit resets the Virtual PHY. When the Virtual PHY is released from reset, this bit is automatically cleared. All writes to this bit are ignored while this bit is high.	R/W SC	0b
9	**Wake-On-LAN Enable (WOL_EN)** When set, the PME signal (if enabled via the PME_EN bit) will be asserted in accordance with the PME_IND bit upon a WOL event. When set, the PME_INT bit in the Interrupt Status Register (INT_STS) will also be asserted upon a WOL event, regardless of the setting of the PME_EN bit.	R/W	0b

BITS	DESCRIPTION	TYPE	DEFAULT
8:7	**RESERVED**	RO	-
6	**PME Buffer Type (PME_TYPE)** When this bit is cleared, the PME pin functions as an open-drain buffer for use in a wired-or configuration. When set, the PME pin is a push-pull driver. **Note:** When PME is configured as an open-drain output, the PME_POL field of this register is ignored and the output is always active low. **0: PME pin open-drain output** **1: PME pin push-pull driver**	R/W NASR	0b
5	**Wake On LAN Status (WOL_STS)** This bit indicates that a wake-up frame or magic packet was detected by the Host MAC. In order to clear this bit, it is required that the event in the Host MAC be cleared as well. The event sources are described in Section 4.3, "Power Management," on page 46.	R/WC	0b
4	**RESERVED**	RO	-
3	**PME Indication (PME_IND)** The PME signal can be configured as a pulsed output or a static signal, which is asserted upon detection of a wake-up event. When set, the PME signal will pulse active for 50mS upon detection of a wake-up event. When cleared, the PME signal is driven continuously upon detection of a wake-up event. **0: PME 50mS pulse on detection of event** **1: PME driven continuously on detection of event** The PME signal can be deactivated by clearing the WOL_STS bit or by clearing the appropriate enable.	R/W	0b
2	**PME Polarity (PME_POL)** This bit controls the polarity of the PME signal. When set, the PME output is an active high signal. When cleared, it is active low. **Note:** When PME is configured as an open-drain output, this field is ignored and the output is always active low. **0: PME active low** **1: PME active high**	R/W NASR	0b
1	**PME Enable (PME_EN)** When set, this bit enables the external PME signal pin. When cleared, the external PME signal is disabled. **Note:** This bit does not affect the PME_INT interrupt bit of the Interrupt Status Register (INT_STS). **0: PME pin disabled** **1: PME pin enabled**	R/W	0b

BITS	DESCRIPTION	TYPE	DEFAULT
0	**Device Ready (READY)** When set, this bit indicates that the LAN9312 is ready to be accessed. Upon power-up, nRST reset, soft reset, or digital reset, the host processor may interrogate this field as an indication that the LAN9312 has stabilized and is fully active. This bit can cause an interrupt if enabled. **Note:** With the exception of the HW_CFG, PMT_CTRL, BYTE_TEST, and RESET_CTL registers, read access to any internal resources is forbidden while the READY bit is cleared. Writes to any address are invalid until this bit is set. **Note:** This bit is identical to bit 27 of the Hardware Configuration Register (HW_CFG).	RO	0b

14.2.9.5 General Purpose Timer Configuration Register (GPT_CFG)

Offset: 08Ch Size: 32 bits

This read/write register configures the LAN9312 General Purpose Timer (GPT). The GPT can be configured to generate host interrupts at the interval defined in this register. The current value of the GPT can be monitored via the General Purpose Timer Count Register (GPT_CNT). Refer to Section 12.1, "General Purpose Timer," on page 161 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:30	**RESERVED**	RO	-
29	**General Purpose Timer Enable (TIMER_EN)** This bit enables the GPT. When set, the GPT enters the run state. When cleared, the GPT is halted. On the 1 to 0 transition of this bit, the GPT_LOAD field of this register will be preset to FFFFh. **0: GPT Disabled** **1: GPT Enabled**	R/W	0b
28:16	**RESERVED**	RO	-
15:0	**General Purpose TImer Pre-Load (GPT_LOAD)** This value is pre-loaded into the GPT. This is the starting value of the GPT. The timer will begin decrementing from this value when enabled.	R/W	FFFFh

14.2.9.6 General Purpose Timer Count Register (GPT_CNT)

Offset: 090h Size: 32 bits

This read-only register reflects the current general purpose timer (GPT) value. The register should be used in conjunction with the General Purpose Timer Configuration Register (GPT_CFG) to configure and monitor the GPT. Refer to Section 12.1, "General Purpose Timer," on page 161 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**General Purpose Timer Current Count (GPT_CNT)** This 16-bit field represents the current value of the GPT.	RO	FFFFh

14.2.9.7 Free Running 25MHz Counter Register (FREE_RUN)

Offset: 09Ch Size: 32 bits

This read-only register reflects the current value of the free-running 25MHz counter. Refer to Section 12.2, "Free-Running Clock," on page 161 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Free Running Counter (FR_CNT)** This field reflects the current value of the free-running 32-bit counter. At reset, the counter starts at zero and is incremented by one every 25MHz cycle. When the maximum count has been reached, the counter will rollover to zero and continue counting. **Note:** The free running counter can take up to 160nS to clear after a reset event.	RO	00000000h

14.2.9.8 Reset Control Register (RESET_CTL)

Offset: 1F8h Size: 32 bits

This register contains software controlled resets.

Note: This register can be read while the LAN9312 is in the reset or not ready states.

BITS	DESCRIPTION	TYPE	DEFAULT
31:4	**RESERVED**	RO	-
3	**Virtual PHY Reset (VPHY_RST)** Setting this bit resets the Virtual PHY. When the Virtual PHY is released from reset, this bit is automatically cleared. All writes to this bit are ignored while this bit is set. **Note:** This bit is not accessible via the EEPROM Loader.	R/W SC	0b
2	**Port 2 PHY Reset (PHY2_RST)** Setting this bit resets the Port 2 PHY. The internal logic automatically holds the PHY reset for a minimum of 102uS. When the Port 2 PHY is released from reset, this bit is automatically cleared. All writes to this bit are ignored while this bit is set. **Note:** This bit is not accessible via the EEPROM Loader.	R/W SC	0b
1	**Port 1 PHY Reset (PHY1_RST)** Setting this bit resets the Port 1 PHY. The internal logic automatically holds the PHY reset for a minimum of 102uS. When the Port 1 PHY is released from reset, this bit is automatically cleared. All writes to this bit are ignored while this bit is set. **Note:** This bit is not accessible via the EEPROM Loader.	R/W SC	0b
0	**Digital Reset (DIGITAL_RST)** Setting this bit resets the complete chip except the PLL, Virtual PHY, Port 1 PHY, and Port 2 PHY. The EEPROM Loader will automatically reload the configuration following this reset, but will not reset the Virtual PHY, Port 1 PHY, or Port 2 PHY. If desired, the above PHY resets can be issued once the device is configured. All system CSRs are reset except for any NASR type bits. Any in progress EEPROM commands (including RELOAD) are terminated. When the chip is released from reset, this bit is automatically cleared. This bit should be polled to determine when the reset is complete. All writes to this bit are ignored while this bit is set. **Note:** The LAN9312must always be read at least once after power-up or reset to ensure that write operations function properly. **Note:** This bit is not accessible via the EEPROM Loader.	R/W SC	0b

14.3 Host MAC Control and Status Registers

This section details the Host MAC System CSR's. These registers are located in the Host MAC and are accessed indirectly via the HBI system CSR's. Table 14.6 lists Host MAC registers that are accessible through the indexing method using the Host MAC CSR Interface Command Register (MAC_CSR_CMD) and Host MAC CSR Interface Data Register (MAC_CSR_DATA).

The Host MAC registers allow configuration of the various Host MAC parameters including the Host MAC address, flow control, multicast hash table, and wake-up configuration. The Host MAC CSR's also provide serial access to the PHYs via the registers HMAC_MII_ACC and HMAC_MII_DATA. These registers allow access to the 10/100 Ethernet PHY registers and the switch engine (via Port 0).

Table 14.6 Host MAC Adressable Registers

INDEX #	SYMBOL	REGISTER NAME
00h	RESERVED	Reserved for Future Use
01h	HMAC_CR	Host MAC Control Register, Section 14.3.1
02h	HMAC_ADDRH	Host MAC Address High Register, Section 14.3.2
03h	HMAC_ADDRL	Host MAC Address Low Register, Section 14.3.3
04h	HMAC_HASHH	Host MAC Multicast Hash Table High Register, Section 14.3.4
05h	HMAC_HASHL	Host MAC Multicast Hash Table Low Register, Section 14.3.5
06h	HMAC_MII_ACC	Host MAC MII Access Register, Section 14.3.6
07h	HMAC_MII_DATA	Host MAC MII Data Register, Section 14.3.7
08h	HMAC_FLOW	Host MAC Flow Control Register, Section 14.3.8
09h	HMAC_VLAN1	Host MAC VLAN1 Tag Register, Section 14.3.9
0Ah	HMAC_VLAN2	Host MAC VLAN2 Tag Register, Section 14.3.10
0Bh	HMAC_WUFF	Host MAC Wake-up Frame Filter Register, Section 14.3.11
0Ch	HMAC_WUCSR	Host MAC Wake-up Control and Status Register, Section 14.3.12
0Dh-FFh	RESERVED	Reserved for Future Use

14.3.1 Host MAC Control Register (HMAC_CR)

Offset: 1h Size: 32 bits

This read/write register establishes the RX and TX operation modes and controls for address filtering and packet filtering. Refer to Chapter 9, "Host MAC," on page 112 for additional information.

Bits 19-15, 13, and 11 determine if the Host MAC accepts the packets from the switch fabric. The switch fabric address table and configuration determine which packets get sent to the Host MAC.

BITS	DESCRIPTION	TYPE	DEFAULT
31	**Receive All Mode (RXALL)** When set, all incoming packets will be received and passed on to the address filtering function for processing of the selected filtering mode on the received frame. Address filtering then occurs and is reported in Receive Status. When cleared, only frames that pass Destination Address filtering will be sent to the application.	R/W	0b
30:24	**RESERVED**	RO	-
23	**Disable Receive Own (RCVOWN)** When set, the Host MAC disables the reception of frames when TXEN (bit 3) is asserted. The Host MAC blocks the transmitted frame on the receive path. When cleared, the Host MAC receives all packets, including those transmitted by the Host MAC. This bit should be cleared when the Full Duplex Mode bit is set.	R/W	0b
22	**RESERVED**	RO	-
21	**Loopback operation Mode (LOOPBK)** Selects the loop back operation modes for the Host MAC. This field is only valid for full duplex mode. In internal loopback mode, the TX frame is received by the internal MII interface, and sent back to the Host MAC without being sent to the switch fabric. **0: Normal Operation. Loopback disabled.** **1: Loopback enabled** **Note:** When enabling or disabling the loopback mode it can take up to 10µs for the mode change to occur. The transmitter and receiver must be stopped and disabled when modifying the LOOPBK bit. The transmitter or receiver should not be enabled within10µs of modifying the LOOPBK bit.	R/W	0b
20	**Full Duplex Mode (FDPX)** When set, the Host MAC operates in Full-Duplex mode, in which it can transmit and receive simultaneously.	R/W	0b
19	**Pass All Multicast (MCPAS)** When set, indicates that all incoming frames with a Multicast destination address (first bit in the destination address field is 1) are received. Incoming frames with physical address (Individual Address/Unicast) destinations are filtered and received only if the address matches the Host MAC Address.	R/W	0b
18	**Promiscuous Mode (PRMS)** When set, indicates that any incoming frame is received regardless of its destination address.	R/W	1b
17	**Inverse filtering (INVFILT)** When set, the address check function operates in inverse filtering mode. This is valid only during Perfect filtering mode. Refer to Section 9.4.4, "Inverse Filtering," on page 116 for additional information.	R/W	0b

BITS	DESCRIPTION	TYPE	DEFAULT
16	**Pass Bad Frames (PASSBAD)** When set, all incoming frames that passed address filtering are received, including runt frames and collided frames. Refer to Section 9.4, "Address Filtering," on page 114 for additional information.	R/W	0b
15	**Hash Only Filtering mode (HO)** When set, the address check Function operates in the Imperfect address filtering mode for both physical and multicast addresses. Refer to Section 9.4.2, "Hash Only Filtering," on page 115 for additional information.	R/W	0b
14	**RESERVED**	RO	-
13	**Hash/Perfect Filtering Mode (HPFILT)** When cleared (0), the LAN9312 will implement a perfect address filter on incoming frames according the address specified in the Host MAC address registers (Host MAC Address High Register (HMAC_ADDRH) and Host MAC Address Low Register (HMAC_ADDRL)). When set (1), the address check function performs imperfect address filtering of multicast incoming frames according to the hash table specified in the multicast hash table register. If the Hash Only Filtering mode (HO) bit 15 is set, then the physical (IA) addresses are also imperfect filtered. If the Hash Only Filtering mode (HO) bit is cleared, then the IA addresses are perfect address filtered according to the MAC Address register Refer to Section 9.4.3, "Hash Perfect Filtering," on page 115 for additional information.	R/W	0b
12	**RESERVED**	RO	-
11	**Disable Broadcast Frames (BCAST)** When set, disables the reception of broadcast frames. When cleared, forwards all broadcast frames to the application. **Note:** When wake-up frame detection is enabled via the WUEN bit of the Host MAC Wake-up Control and Status Register (HMAC_WUCSR), a broadcast wake-up frame will wake-up the device despite the state of this bit.	R/W	0b
10	**Disable Retry (DISRTY)** When set, the Host MAC attempts only one transmission. When a collision is seen on the bus, the Host MAC ignores the current frame and goes to the next frame and a retry error is reported in the Transmit status. When reset, the Host MAC attempts 16 transmissions before signaling a retry error.	R/W	0b
9	**RESERVED**	RO	-
8	**Automatic Pad Stripping (PADSTR)** When set, the Host MAC strips the pad field on all incoming frames, if the length field is less than 46 bytes. The FCS field is also stripped, since it is computed at the transmitting station based on the data and pad field characters, and is invalid for a received frame that has had the pad characters stripped. Receive frames with a 46-byte or greater length field are passed to the application unmodified (FCS is not stripped). When cleared, the Host MAC passes all incoming frames to the host unmodified.	R/W	0b

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>7:6</td><td>BackOff Limit (BOLMT)
The BOLMT bits allow the user to set the back-off limit in a relaxed or aggressive mode. According to IEEE 802.3, the Host MAC has to wait for a random number [r] of slot-times(see note) after it detects a collision, where:
(eq.1)0 < r < ₂K
The exponent K is dependent on how many times the current frame to be transmitted has been retried, as follows:
(eq.2)K = min (n, 10) where n is the current number of retries.
If a frame has been retried three times, then K = 3 and r= 8 slot-times maximum. If it has been retried 12 times, then K = 10, and r = 1024 slot-times maximum.
An LFSR (linear feedback shift register) 20-bit counter emulates a 20 bit random number generator, from which r is obtained. Once a collision is detected, the number of the current retry of the current frame is used to obtain K (eq.2). This value of K translates into the number of bits to use from the LFSR counter. If the value of K is 3, the Host MAC takes the value in the first three bits of the LFSR counter and uses it to count down to zero on every slot-time. This effectively causes the Host MAC to wait eight slot-times. To give the user more flexibility, the BOLMT value forces the number of bits to be used from the LFSR counter to a predetermined value as in the table below.
<table>
<tr><th>BOLMT Value</th><th># Bits Used from LFSR Counter</th></tr>
<tr><td>00b</td><td>10</td></tr>
<tr><td>01b</td><td>8</td></tr>
<tr><td>10b</td><td>4</td></tr>
<tr><td>11b</td><td>1</td></tr>
</table>
Thus, if the value of K = 10, the Host MAC will look at the BOLMT if it is 00b, then use the lower ten bits of the LFSR counter for the wait countdown. If the BOLMT is 10b, then it will only use the value in the first four bits for the wait countdown, etc.
Note: Slot-time = 512 bit times. (See IEEE 802.3 Spec., sections 4.2.3.25 and 4.4.2.1)</td><td>R/W</td><td>0b</td></tr>
<tr><td>5</td><td>Deferral Check (DFCHK)
When set, enables the deferral check in the Host MAC. The Host MAC will abort the transmission attempt if it has deferred for more than 24,288 bit times. Deferral starts when the transmitter is ready to transmit, but is prevented from doing so because the CRS is active. Deferral time is not cumulative. If the transmitter defers for 10,000 bit times, then transmits, collides, backs off, and then has to defer again after completion of back-off, the deferral timer resets to 0 and restarts. When this bit is cleared, the deferral check is disabled in the Host MAC and the Host MAC defers indefinitely.</td><td>R/W</td><td>0b</td></tr>
<tr><td>4</td><td>RESERVED</td><td>RO</td><td>-</td></tr>
<tr><td>3</td><td>Transmitter enable (TXEN)
When set, the Host MAC’s transmitter is enabled and it will transmit frames from the buffer.
When cleared, the Host MAC’s transmitter is disabled and will not transmit any frames.</td><td>R/W</td><td>0b</td></tr>
<tr><td>2</td><td>Receiver Enable (RXEN)
When set, the Host MAC’s receiver is enabled and will receive frames.
When cleared, the MAC’s receiver is disabled and will not receive any frames.</td><td>R/W</td><td>0b</td></tr>
<tr><td>1:0</td><td>RESERVED</td><td>RO</td><td>-</td></tr>
</table>

14.3.2 Host MAC Address High Register (HMAC_ADDRH)

Offset: 2h Size: 32 bits

This read/write register contains the upper 16-bits of the physical address of the Host MAC. The contents of this register are optionally loaded from the EEPROM at power-on through the EEPROM Loader if a programmed EEPROM is detected. The least significant byte of this register (bits [7:0]) is loaded from address 05h of the EEPROM. The second byte (bits [15:8]) is loaded from address 06h of the EEPROM. Section 9.6, "Host MAC Address," on page 119 details the byte ordering of the HMAC_ADDRL and HMAC_ADDRH registers with respect to the reception of the Ethernet physical address. Please refer to Section 10.2, "I2C/Microwire Master EEPROM Controller," on page 137 for more information on the EEPROM Loader.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**Physical Address [47:32]** This field contains the upper 16-bits (47:32) of the Physical Address of the Host MAC. The content of this field is undefined until loaded from the EEPROM at power-on. The host can update the contents of this field after the initialization process has completed.	R/W	FFFFh

14.3.3 Host MAC Address Low Register (HMAC_ADDRL)

Offset: 3h Size: 32 bits

This read/write register contains the lower 32-bits of the physical address of the Host MAC. The contents of this register are optionally loaded from the EEPROM at power-on through the EEPROM Loader if a programmed EEPROM is detected. The least significant byte of this register (bits [7:0]) is loaded from address 01h of the EEPROM. The most significant byte of this register is loaded from address 04h of the EEPROM. Section 9.6, "Host MAC Address," on page 119 details the byte ordering of the HMAC_ADDRL and HMAC_ADDRH registers with respect to the reception of the Ethernet physical address. Please refer to Section 10.2, "I2C/Microwire Master EEPROM Controller," on page 137 for more information on the EEPROM Loader.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Physical Address [31:0]** This field contains the lower 32-bits (31:0) of the Physical Address of the Host MAC. The content of this field is undefined until loaded from the EEPROM at power-on. The host can update the contents of this field after the initialization process has completed.	R/W	FFFFFFFFh

14.3.4 Host MAC Multicast Hash Table High Register (HMAC_HASHH)

Offset: 4h Size: 32 bits

The 64-bit Multicast table is used for group address filtering. For hash filtering, the contents of the destination address in the incoming frame is used to index the contents of the Hash table. The most significant bit determines the register to be used (Hi/Low), while the other five bits determine the bit within the register. A value of 00000 selects Bit 0 of the Multicast Hash Table Lo register and a value of 11111 selects the Bit 31 of the Multicast Hash Table Hi register.

If the corresponding bit is 1, then the multicast frame is accepted. Otherwise, it is rejected. If the “Pass All Multicast” (MCPAS) bit of the Host MAC Control Register (HMAC_CR) is set, then all multicast frames are accepted regardless of the multicast hash values.

The Multicast Hash Table High register contains the higher 32 bits of the hash table and the Multicast Hash Table Low register contains the lower 32 bits of the hash table. Refer to Section 9.4, "Address Filtering," on page 114 for more information on address filtering.

This table determines if the Host MAC accepts the packets from the switch fabric. The switch fabric address table and configuration determine the packets that get sent to the Host MAC.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Upper 32-bits of the 64-bit Hash Table**	R/W	00000000h

14.3.5 Host MAC Multicast Hash Table Low Register (HMAC_HASHL)

Offset: 5h Size: 32 bits

This read/write register defines the lower 32-bits of the Multicast Hash Table. Please refer to the Host MAC Multicast Hash Table High Register (HMAC_HASHH) and Section 9.4, "Address Filtering" for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Lower 32-bits of the 64-bit Hash Table**	R/W	00000000h

14.3.6 Host MAC MII Access Register (HMAC_MII_ACC)

Offset: 6h Size: 32 bits

This read/write register is used in conjunction with the Host MAC MII Data Register (HMAC_MII_DATA) to access the internal PHY registers. Refer to Section 14.4, "Ethernet PHY Control and Status Registers" for a list of accessible PHY registers and PHY address information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:11	**PHY Address (PHY_ADDR)** This field must be loaded with the PHY address that the MII access is intended for. A list default PHY addresses can be seen in Table 7.1. Refer to Section 7.1.1, "PHY Addressing," on page 82 for additional information on PHY addressing.	R/W	00000b
10:6	**MII Register Index (MIIRINDA)** These bits select the desired MII register in the PHY.	R/W	00000b
5:2	**RESERVED**	RO	-
1	**MII Write (MIIWnR)** Setting this bit tells the PHY that this will be a write operation using the Host MAC MII Data Register (HMAC_MII_DATA). If this bit is cleared, a read operation will occur, packing the data in the Host MAC MII Data Register (HMAC_MII_DATA).	R/W	0b
0	**MII Busy (MIIBZY)** This bit must be polled to determine when the MII register access is complete. This bit must read a logical 0 before writing to this register or the Host MAC MII Data Register (HMAC_MII_DATA). The LAN driver software must set this bit in order for the LAN9312 to read or write any of the MII PHY registers. During a MII register access, this bit will be set, signifying a read or write access is in progress. The MII data register must be kept valid until the Host MAC clears this bit during a PHY write operation. The MII data register is invalid until the Host MAC has cleared this bit during a PHY read operation.	RO SC	0b

14.3.7 Host MAC MII Data Register (HMAC_MII_DATA)

Offset: 7h Size: 32 bits

This read/write register is used in conjunction with the Host MAC MII Access Register (HMAC_MII_ACC) to access the internal PHY registers. This register contains either the data to be written to the PHY register specified in the HMAC_MII_ACC Register, or the read data from the PHY register whose index is specified in the HMAC_MII_ACC Register.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**MII Data** This field contains the 16-bit value read from the PHY read operation or the 16-bit data value to be written to the PHY before an MII write operation.	R/W	0000h

14.3.8 Host MAC Flow Control Register (HMAC_FLOW)

Offset: 8h Size: 32 bits

This read/write register controls the generation and reception of the Control (Pause command) frames by the Host MAC's flow control block. The control frame fields are selected as specified in the 802.3 Specification and the Pause-Time value from this register is used in the "Pause Time" field of the control frame. In full-duplex mode the FCBSY bit is set until the control frame is completely transferred. In half-duplex mode FCBSY is set while back pressure is being asserted. The host has to make sure that the FCBSY bit is cleared before writing the register. The Pass Control Frame bit (FCPASS) does not affect the sending of the frames, including Control Frames, to the host. The Flow Control Enable (FCEN) bit enables the receive portion of the Flow Control block.

This register is used in conjunction with the Host MAC Automatic Flow Control Configuration Register (AFC_CFG) in the System CSR's to configure flow control. Software flow control is initiated using the AFC_CFG register.

Note: The Host MAC will not transmit pause frames or assert back pressure if the transmitter is disabled.

Note: For the Host MAC, flow control/backpressure is to/from the switch fabric, not the external network.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**Pause Time (FCPT)** This field indicates the value to be used in the PAUSE TIME field in the control frame. This field must be initialized before full-duplex automatic flow control is enabled.	R/W	0000h
15:3	**RESERVED**	RO	-
2	**Pass Control Frames (FCPASS)** When set, the Host MAC sets the packet filter bit in the receive packet status to indicate to the application that a valid pause frame has been received. The application must accept or discard a received frame based on the packet filter control bit. The Host MAC receives, decodes and performs the Pause function when a valid Pause frame is received in Full-Duplex mode and when flow control is enabled (FCE bit set). When this bit is cleared, the Host MAC resets the Packet Filter bit in the Receive packet status. The Host MAC always passes the data of all frames it receives (including flow control frames) to the application. Frames that do not pass address filtering, as well as frames with errors, are passed to the application. The application must discard or retain the received frame's data based on the received frame's STATUS field. Filtering modes (promiscuous mode, for example) take precedence over the FCPASS bit.	R/W	0b
1	**Flow Control Enable (FCEN)** When set, enables the Host MAC flow control function. The Host MAC decodes all incoming frames for control frames; if it receives a valid control frame (PAUSE command), it disables the transmitter for a specified time (Decoded pause time x slot time). When this bit is cleared, the Host MAC flow control function is disabled; the MAC does not decode frames for control frames. **Note:** Flow Control is applicable when the Host MAC is set in full duplex mode. In half-duplex mode, this bit enables the backpressure function to control the flow of received frames to the Host MAC.	R/W	0b

BITS	DESCRIPTION	TYPE	DEFAULT
0	**Flow Control Busy (FCBSY)** In full-duplex mode, this bit should read logical 0 before writing to the Host MAC Flow Control (HMAC_FLOW) register. To initiate a PAUSE control frame, the bit must be set. During a transfer of control frame, this bit continues to be set, signifying that a frame transmission is in progress. After the PAUSE control frame's transmission is complete, the Host MAC resets the bit to 0. **Backpressure Enable (BkPresEn)** In half-duplex mode, this signal functions as a backpressure enable and is set high whenever backpressure is transmitted. **Notes:** ■ When writing this register, the FCBSY bit must always be zero. ■ Applications must always write a zero to this bit	R/W	0b

14.3.9 Host MAC VLAN1 Tag Register (HMAC_VLAN1)

Offset: 9h Size: 32 bits

This read/write register contains the VLAN tag field to identify VLAN1 frames. When a VLAN1 frame is detected, the legal frame length is increased from 1518 bytes to 1522 bytes. Refer to Section 9.3, "Virtual Local Area Network (VLAN) Support," on page 113 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**VLAN1 Tag Identifier (VTI1)** This field contains the VLAN Tag used to identify VLAN1 frames. This field is compared with the 13th and 14th bytes of the incoming frames for VLAN1 frame detection. **Note:** If used, this register is typically set to the standard VLAN value of 8100h.	R/W	FFFFh

14.3.10 Host MAC VLAN2 Tag Register (HMAC_VLAN2)

Offset: Ah Size: 32 bits

This read/write register contains the VLAN tag field to identify VLAN2 frames. When a VLAN2 frame is detected, the legal frame length is increased from 1518 bytes to 1538 bytes. Refer to Section 9.3, "Virtual Local Area Network (VLAN) Support," on page 113 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**VLAN2 Tag Identifier (VTI2)** This field contains the VLAN Tag used to identify VLAN2 frames. This field is compared with the 13th and 14th bytes of the incoming frames for VLAN2 frame detection. **Note:** If used, this register is typically set to the standard VLAN value of 8100h. If both VLAN1 and VLAN2 Tag Identifiers are used, they should be unique. If both are set to the same value, VLAN1 is given higher precedence and the maximum legal frame length is set to 1522.	R/W	FFFFh

14.3.11 Host MAC Wake-up Frame Filter Register (HMAC_WUFF)

Offset: Bh Size: 32 bits

This write-only register is used to configure the wake-up frame filter. Refer to Section 9.5, "Wake-up Frame Detection," on page 116 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Wake-Up Frame Filter (WFF)** The Wake-up frame filter is configured through this register using an indexing mechanism. After power-on reset, digital reset, or soft reset, the Host MAC loads the first value written to this location to the first DWORD in the Wake-up frame filter (filter 0 byte mask). The second value written to this location is loaded to the second DWORD in the wake-up frame filter (filter 1 byte mask) and so on. Once all eight DWORD's have been written, the internal pointer will once again point to the first entry and the filter entries can be modified in the same manner. **Note:** This is a write-only register.	WO	-

14.3.12 Host MAC Wake-up Control and Status Register (HMAC_WUCSR)

Offset: Ch Size: 32 bits

This read/write register contains data and control settings pertaining to the Host MAC's remote wake-up status and capabilities. It is used in conjunction with the Host MAC Wake-up Frame Filter Register (HMAC_WUFF) to fully configure the wake-up frame filter. Refer to Section 9.5, "Wake-up Frame Detection," on page 116 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:10	**RESERVED**	RO	-
9	**Global Unicast Enable (GUE)** When set, the Host MAC wakes up from power-saving mode on receipt of a global unicast frame. This is accomplished by enabling global unicasts as a wakeup frame qualifier. A global unicast frame has the MAC Address [0] bits set to 0.	R/W	0b
8:7	**RESERVED**	RO	-
6	**Remote Wake-Up Frame Received (WUFR)** The Host MAC sets this bit upon receiving a valid Remote Wake-up frame.	R/WC	0b
5	**Magic Packet Received (MPR)** The Host MAC sets this bit upon receiving a valid Magic Packet	R/WC	0b
4-3	**RESERVED**	RO	-
2	**Wake-Up Frame enabled (WUEN)** When set, Remote Wake-Up mode is enabled and the Host MAC is capable of detecting wake-up frames as programmed in the Host MAC Wake-up Frame Filter Register (HMAC_WUFF).	R/W	0b
1	**Magic Packet Enable (MPEN)** When set, Magic Packet Wake-up mode is enabled.	R/W	0b
0	**RESERVED**	RO	-

14.4 Ethernet PHY Control and Status Registers

This section details the various LAN9312 Ethernet PHY control and status registers. The LAN9312 contains three PHY's: Port 1 PHY, Port 2 PHY and a Virtual PHY. All PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set. All functionality and bit definitions comply with these standards. The IEEE 802.3 specified register index (in decimal) is included with each register definition, allowing for addressing of these registers via the MII serial management protocol. For additional information on the MII management protocol, refer to the IEEE 802.3 Specification.

Each individual PHY is assigned a unique PHY address as detailed in Section 7.1.1, "PHY Addressing," on page 82.

14.4.1 Virtual PHY Registers

The Virtual PHY provides a basic MII management interface for communication with the Host MAC for connection to the Host as if it was attached to a single port PHY. The Virtual PHY registers differ from the Port 1 & 2 PHY registers in that they are addressable via the memory map, as described in Table 14.1, as well as serially. These modes of access are described in Section 14.2.8, "Virtual PHY," on page 245.

Because the Virtual PHY registers are also memory mapped, their definitions have been included in the System Control and Status Registers Section 14.2.8, "Virtual PHY," on page 245. A list of the Virtual PHY MII addressable registers and their corresponding register index numbers is also included in Table 14.4.

Note: When serially accessed, the Virtual PHY registers are only 16-bits wide, as is standard for MII management of PHY's.

14.4.2 Port 1 & 2 PHY Registers

The Port 1 and Port 2 PHY's are comparable in functionality and have an identical set of non-memory mapped registers. The Port 1 and Port 2 PHY registers are not memory mapped. These registers are indirectly accessed through the Host MAC MII Access Register (HMAC_MII_ACC) and Host MAC MII Data Register (HMAC_MII_DATA) registers in the Host MAC via the MII serial management protocol specified in IEEE 802.3 clause 22. Because the Port 1 & 2 PHY registers are functionally identical, their register descriptions have been consolidated. A lowercase "x" has been appended to the end of each PHY register name in this section, where "x" should be replaced with "1" or "2" for the Port 1 PHY or the Port 2 PHY registers respectively. A list of the Port 1 & 2 PHY MII addressable registers and their corresponding register index numbers is included in Table 14.7. Each individual PHY is assigned a unique PHY address as detailed in Section 7.1.1, "PHY Addressing," on page 82.

Table 14.7 Port 1 & 2 PHY MII Serially Adressable Registers

INDEX #	SYMBOL	REGISTER NAME
0	PHY_BASIC_CONTROL_x	Port x PHY Basic Control Register, Section 14.4.2.1
1	PHY_BASIC_STATUS_x	Port x PHY Basic Status Register, Section 14.4.2.2
2	PHY_ID_MSB_x	Port x PHY Identification MSB Register, Section 14.4.2.3
3	PHY_ID_LSB_x	Port x PHY Identification LSB Register, Section 14.4.2.4
4	PHY_AN_ADV_x	Port x PHY Auto-Negotiation Advertisement Register, Section 14.4.2.5
5	PHY_AN_LP_BASE_ABILITY_x	Port x PHY Auto-Negotiation Link Partner Base Page Ability Register, Section 14.4.2.6
6	PHY_AN_EXP_x	Port x PHY Auto-Negotiation Expansion Register, Section 14.4.2.7

Table 14.7 Port 1 & 2 PHY MII Serially Adressable Registers (continued)

INDEX #	SYMBOL	REGISTER NAME
17	PHY_MODE_CONTROL_STATUS_x	Port x PHY Mode Control/Status Register, Section 14.4.2.8
18	PHY_SPECIAL_MODES_x	Port x PHY Special Modes Register, Section 14.4.2.9
27	PHY_SPECIAL_CONTROL_STAT_IND_x	Port x PHY Special Control/Status Indication Register, Section 14.4.2.10
29	PHY_INTERRUPT_SOURCE_x	Port x PHY Interrupt Source Flags Register, Section 14.4.2.11
30	PHY_INTERRUPT_MASK_x	Port x PHY Interrupt Mask Register, Section 14.4.2.12
31	PHY_SPECIAL_CONTROL_STATUS_x	Port x PHY Special Control/Status Register, Section 14.4.2.13

14.4.2.1 Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x)

Index (decimal): 0 Size: 16 bits

This read/write register is used to configure the Port x PHY.

Note: This register is re-written in its entirety by the EEPROM Loader following the release of reset or a RELOAD command. Refer to Section 10.2.4, "EEPROM Loader," on page 149 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Reset (PHY_RST)** When set, this bit resets all the Port x PHY registers to their default state, except those marked as NASR type. This bit is self clearing. **0: Normal operation** **1: Reset**	R/W SC	0b
14	**Loopback (PHY_LOOPBACK)** This bit enables/disables the loopback mode. When enabled, transmissions from the switch fabric are not sent to network. Instead, they are looped back into the switch fabric. **Note:** If loopback is enabled during half-duplex operation, then the Enable Receive Own Transmit bit in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x) must be set for the specified port. Otherwise, the switch fabric will ignore receive activity when transmitting in half-duplex mode. **0: Loopback mode disabled (normal operation)** **1: Loopback mode enabled**	R/W	0b
13	**Speed Select LSB (PHY_SPEED_SEL_LSB)** This bit is used to set the speed of the Port x PHY when the Auto-Negotiation (PHY_AN) bit is disabled. **0: 10 Mbps** **1: 100 Mbps**	R/W	Note 14.49
12	**Auto-Negotiation (PHY_AN)** This bit enables/disables Auto-Negotiation. When enabled, the Speed Select LSB (PHY_SPEED_SEL_LSB) and Duplex Mode (PHY_DUPLEX) bits are overridden. **0: Auto-Negotiation disabled** **1: Auto-Negotiation enabled**	R/W	Note 14.50
11	**Power Down (PHY_PWR_DWN)** This bit controls the power down mode of the Port x PHY. After this bit is cleared the PHY may auto-negotiate with it's partner station. This process can take up to a few seconds to complete. Once Auto-Negotiation is complete, bit 5 (Auto-Negotiation Complete) of the Port x PHY Basic Status Register (PHY_BASIC_STATUS_x) will be set. **Note:** The PHY_AN bit of this register must be cleared before setting this bit. **0: Normal operation** **1: General power down mode**	R/W	0b
10	**RESERVED**	RO	-

BITS	DESCRIPTION	TYPE	DEFAULT
9	**Restart Auto-Negotiation (PHY_RST_AN)** When set, this bit restarts the Auto-Negotiation process. **0: Normal operation** **1: Auto-Negotiation restarted**	R/W SC	0b
8	**Duplex Mode (PHY_DUPLEX)** This bit is used to set the duplex when the Auto-Negotiation (PHY_AN) bit is disabled. **0: Half Duplex** **1: Full Duplex**	R/W	Note 14.51
7	**Collision Test Mode (PHY_COL_TEST)** This bit enables/disables the collision test mode of the Port x PHY. When set, the collision signal is active during transmission. It is recommended that this feature be used only in loopback mode. **0: Collision test mode disabled** **1: Collision test mode enabled**	R/W	0b
6:0	**RESERVED**	RO	-

Note 14.49 The default value of this bit is determined by the logical OR of the Auto-Negotiation strap (autoneg_strap_1 for Port 1 PHY, autoneg_strap_2 for Port 2 PHY) and the speed select strap (speed_strap_1 for Port 1 PHY, speed_strap_2 for Port 2 PHY). Essentially, if the Auto-Negotiation strap is set, the default value is 1, otherwise the default is determined by the value of the speed select strap. Refer to Section 4.2.4, "Configuration Straps," on page 40 for more information.

Note 14.50 The default value of this bit is determined by the value of the Auto-Negotiation strap (autoneg_strap_1 for Port 1 PHY, autoneg_strap_2 for Port 2 PHY). Refer to Section 4.2.4, "Configuration Straps," on page 40 for more information.

Note 14.51 The default value of this bit is determined by the logical AND of the negation of the Auto-Negotiation strap (autoneg_strap_1 for Port 1 PHY, autoneg_strap_2 for Port 2 PHY) and the duplex select strap (duplex_strap_1 for Port 1 PHY, duplex_strap_2 for Port 2 PHY). Essentially, if the Auto-Negotiation strap is set, the default value is 0, otherwise the default is determined by the value of the duplex select strap. Refer to Section 4.2.4, "Configuration Straps," on page 40 for more information.

14.4.2.2 Port x PHY Basic Status Register (PHY_BASIC_STATUS_x)

Index (decimal): 1 Size: 16 bits

This register is used to monitor the status of the Port x PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
15	**100BASE-T4** This bit displays the status of 100BASE-T4 compatibility. **0: PHY not able to perform 100BASE-T4** **1: PHY able to perform 100BASE-T4**	RO	0b Note 14.52
14	**100BASE-X Full Duplex** This bit displays the status of 100BASE-X full duplex compatibility. **0: PHY not able to perform 100BASE-X full duplex** **1: PHY able to perform 100BASE-X full duplex**	RO	1b
13	**100BASE-X Half Duplex** This bit displays the status of 100BASE-X half duplex compatibility. **0: PHY not able to perform 100BASE-X half duplex** **1: PHY able to perform 100BASE-X half duplex**	RO	1b
12	**10BASE-T Full Duplex** This bit displays the status of 10BASE-T full duplex compatibility. **0: PHY not able to perform 10BASE-T full duplex** **1: PHY able to perform 10BASE-T full duplex**	RO	1b
11	**10BASE-T Half Duplex** This bit displays the status of 10BASE-T half duplex compatibility. **0: PHY not able to perform 10BASE-T half duplex** **1: PHY able to perform 10BASE-T half duplex**	RO	1b
10	**100BASE-T2 Full Duplex** This bit displays the status of 100BASE-T2 full duplex compatibility. **0: PHY not able to perform 100BASE-T2 full duplex** **1: PHY able to perform 100BASE-T2 full duplex**	RO	0b Note 14.52
9	**100BASE-T2 Half Duplex** This bit displays the status of 100BASE-T2 half duplex compatibility. **0: PHY not able to perform 100BASE-T2 half duplex** **1: PHY able to perform 100BASE-T2 half duplex**	RO	0b Note 14.52
8:6	**RESERVED**	RO	-
5	**Auto-Negotiation Complete** This bit indicates the status of the Auto-Negotiation process. **0: Auto-Negotiation process not completed** **1: Auto-Negotiation process completed**	RO	0b
4	**Remote Fault** This bit indicates if a remote fault condition has been detected. **0: No remote fault condition detected** **1: Remote fault condition detected**	RO/LH	0b

BITS	DESCRIPTION	TYPE	DEFAULT
3	**Auto-Negotiation Ability** This bit indicates the status of the PHY's auto-negotiation. **0: PHY is unable to perform auto-negotiation** **1: PHY is able to perform auto-negotiation**	RO	1b
2	**Link Status** This bit indicates the status of the link. **0: Link is down** **1: Link is up**	RO/LL	0b
1	**Jabber Detect** This bit indicates the status of the jabber condition. **0: No jabber condition detected** **1: Jabber condition detected**	RO/LH	0b
0	**Extended Capability** This bit indicates whether extended register capability is supported. **0: Basic register set capabilities only** **1: Extended register set capabilities**	RO	1b

Note 14.52 The PHY supports 100BASE-TX (half and full duplex) and 10BASE-T (half and full duplex) only. All other modes will always return as 0 (unable to perform).

14.4.2.3 Port x PHY Identification MSB Register (PHY_ID_MSB_x)

Index (decimal): 2 Size: 16 bits

This read/write register contains the MSB of the Organizationally Unique Identifier (OUI) for the Port x PHY. The LSB of the PHY OUI is contained in the Port x PHY Identification LSB Register (PHY_ID_LSB_x).

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**PHY ID** This field is assigned to the 3rd through 18th bits of the OUI, respectively (OUI = 00800Fh).	R/W	0007h

14.4.2.4 Port x PHY Identification LSB Register (PHY_ID_LSB_x)

Index (decimal): 3 Size: 16 bits

This read/write register contains the LSB of the Organizationally Unique Identifier (OUI) for the Port x PHY. The MSB of the PHY OUI is contained in the Port x PHY Identification MSB Register (PHY_ID_MSB_x).

BITS	DESCRIPTION	TYPE	DEFAULT
15:10	**PHY ID** This field is assigned to the 19th through 24th bits of the PHY OUI, respectively. (OUI = 00800Fh).	R/W	110000b
9:4	**Model Number** This field contains the 6-bit manufacturer's model number of the PHY.	R/W	001101b
3:0	**Revision Number** This field contain the 4-bit manufacturer's revision number of the PHY.	R/W	0001b

14.4.2.5 Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x)

Index (decimal): 4 Size: 16 bits

This read/write register contains the advertised ability of the Port x PHY and is used in the Auto-Negotiation process with the link partner.

Note: This register is re-written by the EEPROM Loader following the release of reset or a RELOAD command. Refer to Section 10.2.4, "EEPROM Loader," on page 149 for additional information.

BITS	DESCRIPTION	TYPE	DEFAULT
15:14	**RESERVED**	RO	-
13	**Remote Fault** This bit determines if remote fault indication will be advertised to the link partner. **0: Remote fault indication not advertised** **1: Remote fault indication advertised**	R/W	0b
12	**RESERVED** **Note:** This bit should be written as 0.	R/W	0b
11	**Asymmetric Pause** This bit determines the advertised asymmetric pause capability. **0: No Asymmetric PAUSE toward link partner advertised** **1: Asymmetric PAUSE toward link partner advertised**	R/W	0b Note 14.53
10	**Symmetric Pause** This bit determines the advertised symmetric pause capability. **0: No Symmetric PAUSE toward link partner advertised** **1: Symmetric PAUSE toward link partner advertised**	R/W	Note 14.53 Note 14.54
9	**RESERVED**	RO	-
8	**100BASE-X Full Duplex** This bit determines the advertised 100BASE-X full duplex capability. **0: 100BASE-X full duplex ability not advertised** **1: 100BASE-X full duplex ability advertised**	R/W	1b
7	**100BASE-X Half Duplex** This bit determines the advertised 100BASE-X half duplex capability. **0: 100BASE-X half duplex ability not advertised** **1: 100BASE-X half duplex ability advertised**	R/W	1b
6	**10BASE-T Full Duplex** This bit determines the advertised 10BASE-T full duplex capability. **0: 10BASE-T full duplex ability not advertised** **1: 10BASE-T full duplex ability advertised**	R/W	Note 14.55 Table 14.8

BITS	DESCRIPTION	TYPE	DEFAULT
5	**10BASE-T Half Duplex** This bit determines the advertised 10BASE-T half duplex capability. **0: 10BASE-T half duplex ability not advertised** **1: 10BASE-T half duplex ability advertised**	R/W	Note 14.56 Table 14.9
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. **00001: IEEE 802.3**	R/W	00001b

Note 14.53 The Pause and Asymmetric Pause bits are loaded into the PHY registers by the EEPROM Loader.

Note 14.54 The default value of this bit is determined by the Manual Flow Control Enable Strap (manual_FC_strap_x). When the Manual Flow Control Enable Strap is 0, this bit defaults to 1 (symmetric pause advertised). When the Manual Flow Control Enable Strap is 1, this bit defaults to 0 (symmetric pause not advertised). Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 40. Refer to Section 4.2.4, "Configuration Straps," on page 40 for configuration strap definitions.

Note 14.55 The default value of this bit is determined by the logical OR of the Auto-Negotiation strap (autoneg_strap_x) with the logical AND of the negated speed select strap (speed_strap_x) and (duplex_strap_x). Table 14.8 defines the default behavior of this bit. Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 40. Refer to Section 4.2.4, "Configuration Straps," on page 40 for configuration strap definitions.

Table 14.8 10BASE-T Full Duplex Advertisement Default Value

autoneg_strap_x	speed_strap_x	duplex_strap_x	Default 10BASE-T Full Duplex (Bit 6) Value
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Note 14.56 The default value of this bit is determined by the logical OR of the Auto-Negotiation strap (autoneg_strap_x) and the negated speed strap (speed_strap_x). Table 14.9 defines the default behavior of this bit. Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 40. Refer to Section 4.2.4, "Configuration Straps," on page 40 for configuration strap definitions.

Table 14.9 10BASE-T Half Duplex Advertisement Bit Default Value

autoneg_strap_x	speed_strap_x	Default 10BASE-T Half Duplex (Bit 5) Value
0	0	1
0	1	0
1	0	1
1	1	1

14.4.2.6 Port x PHY Auto-Negotiation Link Partner Base Page Ability Register (PHY_AN_LP_BASE_ABILITY_x)

Index (decimal): 5 Size: 16 bits

This read-only register contains the advertised ability of the link partner's PHY and is used in the Auto-Negotiation process between the link partner and the Port x PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Next Page** This bit indicates the link partner PHY page capability. **0: Link partner PHY does not advertise next page capability** **1: Link partner PHY advertises next page capability**	RO	0b
14	**Acknowledge** This bit indicates whether the link code word has been received from the partner. **0: Link code word not yet received from partner** **1: Link code word received from partner**	RO	0b
13	**Remote Fault** This bit indicates whether a remote fault has been detected. **0: No remote fault** **1: Remote fault detected**	RO	0b
12	**RESERVED**	RO	-
11	**Asymmetric Pause** This bit indicates the link partner PHY asymmetric pause capability. **0: No Asymmetric PAUSE toward link partner** **1: Asymmetric PAUSE toward link partner**	RO	0b
10	**Pause** This bit indicates the link partner PHY symmetric pause capability. **0: No Symmetric PAUSE toward link partner** **1: Symmetric PAUSE toward link partner**	RO	0b
9	**100BASE-T4** This bit indicates the link partner PHY 100BASE-T4 capability. **0: 100BASE-T4 ability not supported** **1: 100BASE-T4 ability supported**	RO	0b
8	**100BASE-X Full Duplex** This bit indicates the link partner PHY 100BASE-X full duplex capability. **0: 100BASE-X full duplex ability not supported** **1: 100BASE-X full duplex ability supported**	RO	0b
7	**100BASE-X Half Duplex** This bit indicates the link partner PHY 100BASE-X half duplex capability. **0: 100BASE-X half duplex ability not supported** **1: 100BASE-X half duplex ability supported**	RO	0b

BITS	DESCRIPTION	TYPE	DEFAULT
6	**10BASE-T Full Duplex** This bit indicates the link partner PHY 10BASE-T full duplex capability. **0: 10BASE-T full duplex ability not supported** **1: 10BASE-T full duplex ability supported**	RO	0b
5	**10BASE-T Half Duplex** This bit indicates the link partner PHY 10BASE-T half duplex capability. **0: 10BASE-T half duplex ability not supported** **1: 10BASE-T half duplex ability supported**	RO	0b
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. **00001: IEEE 802.3**	RO	00001b Note 14.57

Note 14.57 The Port 1 & 2 PHY's support only IEEE 802.3.

14.4.2.7 Port x PHY Auto-Negotiation Expansion Register (PHY_AN_EXP_x)

Index (decimal): 6 Size: 16 bits

This read/write register is used in the Auto-Negotiation process between the link partner and the Port x PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
15:5	**RESERVED**	RO	-
4	**Parallel Detection Fault** This bit indicates whether a Parallel Detection Fault has been detected. **0: A fault hasn't been detected via the Parallel Detection function** **1: A fault has been detected via the Parallel Detection function**	RO/LH	0b
3	**Link Partner Next Page Able** This bit indicates whether the link partner has next page ability. **0: Link partner does not contain next page capability** **1: Link partner contains next page capability**	RO	0b
2	**Local Device Next Page Able** This bit indicates whether the local device has next page ability. **0: Local device does not contain next page capability** **1: Local device contains next page capability**	RO	0b
1	**Page Received** This bit indicates the reception of a new page. **0: A new page has not been received** **1: A new page has been received**	RO/LH	0b
0	**Link Partner Auto-Negotiation Able** This bit indicates the Auto-negotiation ability of the link partner. **0: Link partner is not Auto-Negotiation able** **1: Link partner is Auto-Negotiation able**	RO	0b

14.4.2.8 Port x PHY Mode Control/Status Register (PHY_MODE_CONTROL_STATUS_x)

Index (decimal): 17 Size: 16 bits

This read/write register is used to control and monitor various Port x PHY configuration options.

BITS	DESCRIPTION	TYPE	DEFAULT
15:14	**RESERVED**	RO	-
13	**Energy Detect Power-Down (EDPWRDOWN)** This bit controls the Energy Detect Power-Down mode. **0: Energy Detect Power-Down is disabled** **1: Energy Detect Power-Down is enabled**	R/W	0b
12:2	**RESERVED**	RO	-
1	**Energy On (ENERGYON)** This bit indicates whether energy is detected on the line. It is cleared if no valid energy is detected within 256ms. This bit is unaffected by a software reset and is reset to 1 by a hardware reset. **0: No valid energy detected on the line** **1: Energy detected on the line**	RO	1b
0	**RESERVED**	R/W	0b

14.4.2.9 Port x PHY Special Modes Register (PHY_SPECIAL_MODES_x)

Index (decimal): 18 Size: 16 bits

This read/write register is used to control the special modes of the Port x PHY.

Note: This register is re-written by the EEPROM Loader following the release of reset or a RELOAD command. Refer to Section 10.2.4, "EEPROM Loader," on page 149 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
15:8	**RESERVED**	RO	-
7:5	**PHY Mode (MODE[2:0])** This field controls the PHY mode of operation. Refer to Table 14.10 for a definition of each mode.	R/W NASR Note 14.58	Note 14.59
4:0	**PHY Address (PHYADD)** The PHY Address field determines the MMI address to which the PHY will respond and is also used for initialization of the cipher (scrambler) key. Each PHY must have a unique address. Refer to Section 7.1.1, "PHY Addressing," on page 82 for additional information. **Note:** No check is performed to ensure that this address is unique from the other PHY addresses (Port 1 PHY, Port 2 PHY, and Virtual PHY).	R/W NASR Note 14.58	Note 14.60

Note 14.58 Register bits designated as NASR are reset when the Port x PHY Reset is generated via the Reset Control Register (RESET_CTL). The NASR designation is only applicable when the Reset (PHY_RST) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) is set.

Note 14.59 The default value of this field is determined by a combination of the configuration straps autoneg_strap_x, speed_strap_x, and duplex_strap_x. If the autoneg_strap_x is 1, then the default MODE[2:0] value is 111b. Else, the default value of this field is determined by the remaining straps. MODE[2]=0, MODE[1]=(speed_strap_1 for Port 1 PHY, speed_strap_2 for Port 2 PHY), and MODE[0]=(duplex_strap_1 for Port 1 PHY, duplex_strap_2 for Port 2 PHY). Configuration strap values are latched upon the de-assertion of a chip-level reset as described in Section 4.2.4, "Configuration Straps," on page 40. Refer to Section 4.2.4, "Configuration Straps," on page 40 for configuration strap definitions.

Note 14.60 The default value of this field is determined by the phy_addr_sel_strap configuration strap. Refer to Section 7.1.1, "PHY Addressing," on page 82 for additional information.

Table 14.10 MODE[2:0] Definitions

MODE[2:0]	MODE DEFINITIONS	AFFECTED REGISTER BIT VALUES	
		PHY_BASIC_CONTROL_x	PHY_AN_ADV_x
		[13,12,10,8]	[8,7,6,5]
000	10BASE-T Half Duplex. Auto-negotiation disabled.	0000	N/A
001	10BASE-T Full Duplex. Auto-negotiation disabled.	0001	N/A
010	100BASE-TX Half Duplex. Auto-negotiation disabled. CRS is active during Transmit & Receive.	1000	N/A

Table 14.10 MODE[2:0] Definitions (continued)

MODE[2:0]	MODE DEFINITIONS	AFFECTED REGISTER BIT VALUES	
		PHY_BASIC_CONTROL_x	PHY_AN_ADV_x
		[13,12,10,8]	[8,7,6,5]
011	100BASE-TX Full Duplex. Auto-negotiation disabled. CRS is active during Receive.	1001	N/A
100	100BASE-TX Half Duplex is advertised. Auto-negotiation enabled. CRS is active during Transmit & Receive.	1100	0100
101	Repeater mode. Auto-negotiation enabled. 100BASE-TX Half Duplex is advertised. CRS is active during Receive.	1100	0100
110	Power Down mode. In this mode the PHY wake-up in Power-Down mode.	N/A	N/A
111	All capable. Auto-negotiation enabled.	X10X	1111

14.4.2.10 Port x PHY Special Control/Status Indication Register (PHY_SPECIAL_CONTROL_STAT_IND_x)

Index (decimal): 27 Size: 16 bits

This read/write register is used to control various options of the Port x PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Auto-MDIX Control (AMDIXCTRL)** This bit is responsible for determining the source of Auto-MDIX control for Port x. When set, the Manual MDIX and Auto MDIX straps (manual_mdix_strap_1/auto_mdix_strap_1 for Port 1 PHY, manual_mdix_strap_2/auto_mdix_strap_2 for Port 2 PHY) are overridden, and Auto-MDIX functions are controlled using bit 14 (AMDIXEN) and bit 13 (AMDIXSTATE) of this register. When cleared, Auto-MDIX functionality is controlled by the Manual MDIX and Auto MDIX straps by default. Refer to Section 4.2.4, "Configuration Straps," on page 40 for configuration strap definitions. **0: Port x Auto-MDIX determined by strap inputs** **1: Port x Auto-MDIX determined by bits 14 and 13**	R/W NASR Note 14.61	0b
14	**Auto-MDIX Enable (AMDIXEN)** When bit 15 (AMDIXCTRL) of this register is set, this bit is used in conjunction with bit 13 (Auto-MDIX State) to control the Port x Auto-MDIX functionality as shown in Table 14.11.	R/W NASR Note 14.61	0b
13	**Auto-MDIX State (AMDIXSTATE)** When bit 15 (AMDIXCTRL) of this register is set, this bit is used in conjunction with bit 14 (Auto-MDIX Enable) to control the Port x Auto-MDIX functionality as shown in Table 14.11.	R/W NASR Note 14.61	0b
12	**RESERVED**	RO	-
11	**SQE Test Disable (SQEOFF)** This bit controls the disabling of the SQE test (Heartbeat). SQE test is enabled by default. **0: SQE test enabled** **1: SQE test disabled**	R/W NASR Note 14.61	0b
10	**Receive PLL Lock Control (VCOOFF_LP)** This bit controls the locking of the receive PLL. Setting this bit to 1 forces the receive PLL 10M to lock on the reference clock at all times. When in this mode, 10M data packets cannot be received. **0: Receive PLL 10M can lock on reference or line as needed (normal operation)** **1: Receive PLL 10M locked onto reference clock at all times**	R/W NASR Note 14.61	0b
9:5	**RESERVED**	RO	-
4	**10Base-T Polarity State (XPOL)** This bit shows the polarity state of the 10Base-T. **0: Normal Polarity** **1: Reversed Polarity**	RO	0b
3:0	**RESERVED**	RO	-

Note 14.61 Register bits designated as NASR are reset when the Port x PHY Reset is generated via the Reset Control Register (RESET_CTL). The NASR designation is only applicable when the Reset (PHY_RST) bit of the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) is set.

Table 14.11 Auto-MDIX Enable and Auto-MDIX State Bit Functionality

Auto-MDIX Enable (Bit 14)	Auto-MDIX State (Bit 13)	MODE
0	0	Manual mode, no crossover
0	1	Manual mode, crossover
1	0	Auto-MDIX mode
1	1	RESERVED (do not use this state)

14.4.2.11 Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x)

Index (decimal): 29 Size: 16 bits

This read-only register is used to determine to source of various Port x PHY interrupts. All interrupt source bits in this register are read-only and latch high upon detection of the corresponding interrupt (if enabled). A read of this register clears the interrupts. These interrupts are enabled or masked via the Port x PHY Interrupt Mask Register (PHY_INTERRUPT_MASK_x).

BITS	DESCRIPTION	TYPE	DEFAULT
15:8	**RESERVED**	RO	-
7	**INT7** This interrupt source bit indicates when the ENERGYON bit of the Port x PHY Mode Control/Status Register (PHY_MODE_CONTROL_STATUS_x) has been set. **0: Not source of interrupt** **1: ENERGYON generated**	RO/LH	0b
6	**INT6** This interrupt source bit indicates Auto-Negotiation is complete. **0: Not source of interrupt** **1: Auto-Negotiation complete**	RO/LH	0b
5	**INT5** This interrupt source bit indicates a remote fault has been detected. **0: Not source of interrupt** **1: Remote fault detected**	RO/LH	0b
4	**INT4** This interrupt source bit indicates a Link Down (link status negated). **0: Not source of interrupt** **1: Link Down (link status negated)**	RO/LH	0b
3	**INT3** This interrupt source bit indicates an Auto-Negotiation LP acknowledge. **0: Not source of interrupt** **1: Auto-Negotiation LP acknowledge**	RO/LH	0b
2	**INT2** This interrupt source bit indicates a Parallel Detection fault. **0: Not source of interrupt** **1: Parallel Detection fault**	RO/LH	0b
1	**INT1** This interrupt source bit indicates an Auto-Negotiation page received. **0: Not source of interrupt** **1: Auto-Negotiation page received**	RO/LH	0b
0	**RESERVED**	RO	-

14.4.2.12 Port x PHY Interrupt Mask Register (PHY_INTERRUPT_MASK_x)

Index (decimal): 30 Size: 16 bits

This read/write register is used to enable or mask the various Port x PHY interrupts and is used in conjunction with the Port x PHY Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x).

BITS	DESCRIPTION	TYPE	DEFAULT
15:8	**RESERVED**	RO	-
7	**INT7_MASK** This interrupt mask bit enables/masks the ENERGYON interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
6	**INT6_MASK** This interrupt mask bit enables/masks the Auto-Negotiation interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
5	**INT5_MASK** This interrupt mask bit enables/masks the remote fault interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
4	**INT4_MASK** This interrupt mask bit enables/masks the Link Down (link status negated) interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
3	**INT3_MASK** This interrupt mask bit enables/masks the Auto-Negotiation LP acknowledge interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
2	**INT2_MASK** This interrupt mask bit enables/masks the Parallel Detection fault interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
1	**INT1_MASK** This interrupt mask bit enables/masks the Auto-Negotiation page received interrupt. **0: Interrupt source is masked** **1: Interrupt source is enabled**	R/W	0b
0	**RESERVED**	RO	-

14.4.2.13 Port x PHY Special Control/Status Register (PHY_SPECIAL_CONTROL_STATUS_x)

Index (decimal): 31 Size: 16 bits

This read/write register is used to control and monitor various options of the Port x PHY.

BITS	DESCRIPTION	TYPE	DEFAULT
15:13	**RESERVED**	RO	-
12	**Autodone** This bit indicates the status of the Auto-Negotiation on the Port x PHY. **0: Auto-Negotiation is not completed, is disabled, or is not active** **1: Auto-Negotiation is completed**	RO	0b
11:5	**RESERVED - Write as 0000010b, ignore on read**	R/W	0000010b
4:2	**Speed Indication** This field indicates the current Port x PHY speed configuration. STATE / DESCRIPTION 000 RESERVED 001 10BASE-T Half-duplex 010 100BASE-TX Half-duplex 011 RESERVED 100 RESERVED 101 10BASE-T Full-duplex 110 100BASE-TX Full-duplex 111 RESERVED	RO	000b
1:0	**RESERVED**	R/W	0b

14.5 Switch Fabric Control and Status Registers

This section details the various LAN9312 switch control and status registers that reside within the switch fabric. The switch control and status registers allow configuration of each individual switch port, the switch engine, and buffer manager. Switch fabric related interrupts and resets are also controlled and monitored via the switch CSRs.

The switch CSRs are not memory mapped. All switch CSRs are accessed indirectly via the Switch Fabric CSR Interface Command Register (SWITCH_CSR_CMD), Switch Fabric CSR Interface Data Register (SWITCH_CSR_DATA), and Switch Fabric CSR Interface Direct Data Register (SWITCH_CSR_DIRECT_DATA) in the system CSR memory mapped address space. All accesses to the switch CSRs must be performed through these registers. Refer to Section 14.2.6, "Switch Fabric" for additional information.

Note: The flow control settings of the switch ports are configured via the Switch Fabric registers: Port 1 Manual Flow Control Register (MANUAL_FC_1), Port 2 Manual Flow Control Register (MANUAL_FC_2), and Port 0(Host MAC) Manual Flow Control Register (MANUAL_FC_MII) located in the system CSR address space.

Table 14.12 lists the Switch CSRs and their corresponding addresses in order. The switch fabric registers can be categorized into the following sub-sections:

- Section 14.5.1, "General Switch CSRs," on page 319
- Section 14.5.2, "Switch Port 0, Port 1, and Port 2 CSRs," on page 323
- Section 14.5.3, "Switch Engine CSRs," on page 367
- Section 14.5.4, "Buffer Manager CSRs," on page 412

Table 14.12 Indirectly Accessible Switch Control and Status Registers

REGISTER #	SYMBOL	REGISTER NAME
General Switch CSRs		
0000h	SW_DEV_ID	Switch Device ID Register, Section 14.5.1.1
0001h	SW_RESET	Switch Reset Register, Section 14.5.1.2
0002h-0003h	RESERVED	Reserved for Future Use
0004h	SW_IMR	Switch Global Interrupt Mask Register, Section 14.5.1.3
0005h	SW_IPR	Switch Global Interrupt Pending Register, Section 14.5.1.4
0006h-03FFh	RESERVED	Reserved for Future Use
Switch Port 0 CSRs		
0400h	MAC_VER_ID_MII	Port 0 MAC Version ID Register, Section 14.5.2.1
0401h	MAC_RX_CFG_MII	Port 0 MAC Receive Configuration Register, Section 14.5.2.2
0402h-040Fh	RESERVED	Reserved for Future Use
0410h	MAC_RX_UNDSZE_CNT_MII	Port 0 MAC Receive Undersize Count Register, Section 14.5.2.3
0411h	MAC_RX_64_CNT_MII	Port 0 MAC Receive 64 Byte Count Register, Section 14.5.2.4
0412h	MAC_RX_65_TO_127_CNT_MII	Port 0 MAC Receive 65 to 127 Byte Count Register, Section 14.5.2.5
0413h	MAC_RX_128_TO_255_CNT_MII	Port 0 MAC Receive 128 to 255 Byte Count Register, Section 14.5.2.6

Table 14.12 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0414h	MAC_RX_256_TO_511_CNT_MII	Port 0 MAC Receive 256 to 511 Byte Count Register, Section 14.5.2.7
0415h	MAC_RX_512_TO_1023_CNT_MII	Port 0 MAC Receive 512 to 1023 Byte Count Register, Section 14.5.2.8
0416h	MAC_RX_1024_TO_MAX_CNT_MII	Port 0 MAC Receive 1024 to Max Byte Count Register, Section 14.5.2.9
0417h	MAC_RX_OVRSZE_CNT_MII	Port 0 MAC Receive Oversize Count Register, Section 14.5.2.10
0418h	MAC_RX_PKTOK_CNT_MII	Port 0 MAC Receive OK Count Register, Section 14.5.2.11
0419h	MAC_RX_CRCERR_CNT_MII	Port 0 MAC Receive CRC Error Count Register, Section 14.5.2.12
041Ah	MAC_RX_MULCST_CNT_MII	Port 0 MAC Receive Multicast Count Register, Section 14.5.2.13
041Bh	MAC_RX_BRDCST_CNT_MII	Port 0 MAC Receive Broadcast Count Register, Section 14.5.2.14
041Ch	MAC_RX_PAUSE_CNT_MII	Port 0 MAC Receive Pause Frame Count Register, Section 14.5.2.15
041Dh	MAC_RX_FRAG_CNT_MII	Port 0 MAC Receive Fragment Error Count Register, Section 14.5.2.16
041Eh	MAC_RX_JABB_CNT_MII	Port 0 MAC Receive Jabber Error Count Register, Section 14.5.2.17
041Fh	MAC_RX_ALIGN_CNT_MII	Port 0 MAC Receive Alignment Error Count Register, Section 14.5.2.18
0420h	MAC_RX_PKTLEN_CNT_MII	Port 0 MAC Receive Packet Length Count Register, Section 14.5.2.19
0421h	MAC_RX_GOODPKTLEN_CNT_MII	Port 0 MAC Receive Good Packet Length Count Register, Section 14.5.2.20
0422h	MAC_RX_SYMBL_CNT_MII	Port 0 MAC Receive Symbol Error Count Register, Section 14.5.2.21
0423h	MAC_RX_CTLFRM_CNT_MII	Port 0 MAC Receive Control Frame Count Register, Section 14.5.2.22
0424h-043Fh	RESERVED	Reserved for Future Use
0440h	MAC_TX_CFG_MII	Port 0 MAC Transmit Configuration Register, Section 14.5.2.23
0441h	MAC_TX_FC_SETTINGS_MII	Port 0 MAC Transmit Flow Control Settings Register, Section 14.5.2.24
0442h-0450h	RESERVED	Reserved for Future Use
0451h	MAC_TX_DEFER_CNT_MII	Port 0 MAC Transmit Deferred Count Register, Section 14.5.2.25
0452h	MAC_TX_PAUSE_CNT_MII	Port 0 MAC Transmit Pause Count Register, Section 14.5.2.26
0453h	MAC_TX_PKTOK_CNT_MII	Port 0 MAC Transmit OK Count Register, Section 14.5.2.27
0454h	MAC_TX_64_CNT_MII	Port 0 MAC Transmit 64 Byte Count Register, Section 14.5.2.28

Table 14.12 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0455h	MAC_TX_65_TO_127_CNT_MII	Port 0 MAC Transmit 65 to 127 Byte Count Register, Section 14.5.2.29
0456h	MAC_TX_128_TO_255_CNT_MII	Port 0 MAC Transmit 128 to 255 Byte Count Register, Section 14.5.2.30
0457h	MAC_TX_256_TO_511_CNT_MII	Port 0 MAC Transmit 256 to 511 Byte Count Register, Section 14.5.2.31
0458h	MAC_TX_512_TO_1023_CNT_MII	Port 0 MAC Transmit 512 to 1023 Byte Count Register, Section 14.5.2.32
0459h	MAC_TX_1024_TO_MAX_CNT_MII	Port 0 MAC Transmit 1024 to Max Byte Count Register, Section 14.5.2.33
045Ah	MAC_TX_UNDSZE_CNT_MII	Port 0 MAC Transmit Undersize Count Register, Section 14.5.2.34
045Bh	RESERVED	Reserved for Future Use
045Ch	MAC_TX_PKTLEN_CNT_MII	Port 0 MAC Transmit Packet Length Count Register, Section 14.5.2.35
045Dh	MAC_TX_BRDCST_CNT_MII	Port 0 MAC Transmit Broadcast Count Register, Section 14.5.2.36
045Eh	MAC_TX_MULCST_CNT_MII	Port 0 MAC Transmit Multicast Count Register, Section 14.5.2.37
045Fh	MAC_TX_LATECOL_MII	Port 0 MAC Transmit Late Collision Count Register, Section 14.5.2.38
0460h	MAC_TX_EXCOL_CNT_MII	Port 0 MAC Transmit Excessive Collision Count Register, Section 14.5.2.39
0461h	MAC_TX_SNGLECOL_CNT_MII	Port 0 MAC Transmit Single Collision Count Register, Section 14.5.2.40
0462h	MAC_TX_MULTICOL_CNT_MII	Port 0 MAC Transmit Multiple Collision Count Register, Section 14.5.2.41
0463h	MAC_TX_TOTALCOL_CNT_MII	Port 0 MAC Transmit Total Collision Count Register, Section 14.5.2.42
0464-047Fh	RESERVED	Reserved for Future Use
0480h	MAC_IMR_MII	Port 0 MAC Interrupt Mask Register, Section 14.5.2.43
0481h	MAC_IPR_MII	Port 0 MAC Interrupt Pending Register, Section 14.5.2.44
0482h-07FFh	RESERVED	Reserved for Future Use
Switch Port 1 CSRs		
0800h	MAC_VER_ID_1	Port 1 MAC Version ID Register, Section 14.5.2.1
0801h	MAC_RX_CFG_1	Port 1 MAC Receive Configuration Register, Section 14.5.2.2
0802h-080Fh	RESERVED	Reserved for Future Use
0810h	MAC_RX_UNDSZE_CNT_1	Port 1 MAC Receive Undersize Count Register, Section 14.5.2.3
0811h	MAC_RX_64_CNT_1	Port 1 MAC Receive 64 Byte Count Register, Section 14.5.2.4

Table 14.12 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0812h	MAC_RX_65_TO_127_CNT_1	Port 1 MAC Receive 65 to 127 Byte Count Register, Section 14.5.2.5
0813h	MAC_RX_128_TO_255_CNT_1	Port 1 MAC Receive 128 to 255 Byte Count Register, Section 14.5.2.6
0814h	MAC_RX_256_TO_511_CNT_1	Port 1 MAC Receive 256 to 511 Byte Count Register, Section 14.5.2.7
0815h	MAC_RX_512_TO_1023_CNT_1	Port 1 MAC Receive 512 to 1023 Byte Count Register, Section 14.5.2.8
0816h	MAC_RX_1024_TO_MAX_CNT_1	Port 1 MAC Receive 1024 to Max Byte Count Register, Section 14.5.2.9
0817h	MAC_RX_OVRSZE_CNT_1	Port 1 MAC Receive Oversize Count Register, Section 14.5.2.10
0818h	MAC_RX_PKTOK_CNT_1	Port 1 MAC Receive OK Count Register, Section 14.5.2.11
0819h	MAC_RX_CRCERR_CNT_1	Port 1 MAC Receive CRC Error Count Register, Section 14.5.2.12
081Ah	MAC_RX_MULCST_CNT_1	Port 1 MAC Receive Multicast Count Register, Section 14.5.2.13
081Bh	MAC_RX_BRDCST_CNT_1	Port 1 MAC Receive Broadcast Count Register, Section 14.5.2.14
081Ch	MAC_RX_PAUSE_CNT_1	Port 1 MAC Receive Pause Frame Count Register, Section 14.5.2.15
081Dh	MAC_RX_FRAG_CNT_1	Port 1 MAC Receive Fragment Error Count Register, Section 14.5.2.16
081Eh	MAC_RX_JABB_CNT_1	Port 1 MAC Receive Jabber Error Count Register, Section 14.5.2.17
081Fh	MAC_RX_ALIGN_CNT_1	Port 1 MAC Receive Alignment Error Count Register, Section 14.5.2.18
0820h	MAC_RX_PKTLEN_CNT_1	Port 1 MAC Receive Packet Length Count Register, Section 14.5.2.19
0821h	MAC_RX_GOODPKTLEN_CNT_1	Port 1 MAC Receive Good Packet Length Count Register, Section 14.5.2.20
0822h	MAC_RX_SYMBL_CNT_1	Port 1 MAC Receive Symbol Error Count Register, Section 14.5.2.21
0823h	MAC_RX_CTLFRM_CNT_1	Port 1 MAC Receive Control Frame Count Register, Section 14.5.2.22
0824h-083Fh	RESERVED	Reserved for Future Use
0840h	MAC_TX_CFG_1	Port 1 MAC Transmit Configuration Register, Section 14.5.2.23
0841h	MAC_TX_FC_SETTINGS_1	Port 1 MAC Transmit Flow Control Settings Register, Section 14.5.2.24
0842h-0850h	RESERVED	Reserved for Future Use
0851h	MAC_TX_DEFER_CNT_1	Port 1 MAC Transmit Deferred Count Register, Section 14.5.2.25

Table 14.12 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0852h	MAC_TX_PAUSE_CNT_1	Port 1 MAC Transmit Pause Count Register, Section 14.5.2.26
0853h	MAC_TX_PKTOK_CNT_1	Port 1 MAC Transmit OK Count Register, Section 14.5.2.27
0854h	MAC_RX_64_CNT_1	Port 1 MAC Transmit 64 Byte Count Register, Section 14.5.2.28
0855h	MAC_TX_65_TO_127_CNT_1	Port 1 MAC Transmit 65 to 127 Byte Count Register, Section 14.5.2.29
0856h	MAC_TX_128_TO_255_CNT_1	Port 1 MAC Transmit 128 to 255 Byte Count Register, Section 14.5.2.30
0857h	MAC_TX_256_TO_511_CNT_1	Port 1 MAC Transmit 256 to 511 Byte Count Register, Section 14.5.2.31
0858h	MAC_TX_512_TO_1023_CNT_1	Port 1 MAC Transmit 512 to 1023 Byte Count Register, Section 14.5.2.32
0859h	MAC_TX_1024_TO_MAX_CNT_1	Port 1 MAC Transmit 1024 to Max Byte Count Register, Section 14.5.2.33
085Ah	MAC_TX_UNDSZE_CNT_1	Port 1 MAC Transmit Undersize Count Register, Section 14.5.2.34
085Bh	RESERVED	Reserved for Future Use
085Ch	MAC_TX_PKTLEN_CNT_1	Port 1 MAC Transmit Packet Length Count Register, Section 14.5.2.35
085Dh	MAC_TX_BRDCST_CNT_1	Port 1 MAC Transmit Broadcast Count Register, Section 14.5.2.36
085Eh	MAC_TX_MULCST_CNT_1	Port 1 MAC Transmit Multicast Count Register, Section 14.5.2.37
085Fh	MAC_TX_LATECOL_1	Port 1 MAC Transmit Late Collision Count Register, Section 14.5.2.38
0860h	MAC_TX_EXCOL_CNT_1	Port 1 MAC Transmit Excessive Collision Count Register, Section 14.5.2.39
0861h	MAC_TX_SNGLECOL_CNT_1	Port 1 MAC Transmit Single Collision Count Register, Section 14.5.2.40
0862h	MAC_TX_MULTICOL_CNT_1	Port 1 MAC Transmit Multiple Collision Count Register, Section 14.5.2.41
0863h	MAC_TX_TOTALCOL_CNT_1	Port 1 MAC Transmit Total Collision Count Register, Section 14.5.2.42
0864-087Fh	RESERVED	Reserved for Future Use
0880h	MAC_IMR_1	Port 1 MAC Interrupt Mask Register, Section 14.5.2.43
0881h	MAC_IPR_1	Port 1 MAC Interrupt Pending Register, Section 14.5.2.44
0882h-0BFFh	RESERVED	Reserved for Future Use
Switch Port 2 CSRs		
0C00h	MAC_VER_ID_2	Port 2 MAC Version ID Register, Section 14.5.2.1
0C01h	MAC_RX_CFG_2	Port 2 MAC Receive Configuration Register, Section 14.5.2.2

Table 14.12 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0C02h-0C0Fh	RESERVED	Reserved for Future Use
0C10h	MAC_RX_UNDSZE_CNT_2	Port 2 MAC Receive Undersize Count Register, Section 14.5.2.3
0C11h	MAC_RX_64_CNT_2	Port 2 MAC Receive 64 Byte Count Register, Section 14.5.2.4
0C12h	MAC_RX_65_TO_127_CNT_2	Port 2 MAC Receive 65 to 127 Byte Count Register, Section 14.5.2.5
0C13h	MAC_RX_128_TO_255_CNT_2	Port 2 MAC Receive 128 to 255 Byte Count Register, Section 14.5.2.6
0C14h	MAC_RX_256_TO_511_CNT_2	Port 2 MAC Receive 256 to 511 Byte Count Register, Section 14.5.2.7
0C15h	MAC_RX_512_TO_1023_CNT_2	Port 2 MAC Receive 512 to 1023 Byte Count Register, Section 14.5.2.8
0C16h	MAC_RX_1024_TO_MAX_CNT_2	Port 2 MAC Receive 1024 to Max Byte Count Register, Section 14.5.2.9
0C17h	MAC_RX_OVRSZE_CNT_2	Port 2 MAC Receive Oversize Count Register, Section 14.5.2.10
0C18h	MAC_RX_PKTOK_CNT_2	Port 2 MAC Receive OK Count Register, Section 14.5.2.11
0C19h	MAC_RX_CRCERR_CNT_2	Port 2 MAC Receive CRC Error Count Register, Section 14.5.2.12
0C1Ah	MAC_RX_MULCST_CNT_2	Port 2 MAC Receive Multicast Count Register, Section 14.5.2.13
0C1Bh	MAC_RX_BRDCST_CNT_2	Port 2 MAC Receive Broadcast Count Register, Section 14.5.2.14
0C1Ch	MAC_RX_PAUSE_CNT_2	Port 2 MAC Receive Pause Frame Count Register, Section 14.5.2.15
0C1Dh	MAC_RX_FRAG_CNT_2	Port 2 MAC Receive Fragment Error Count Register, Section 14.5.2.16
0C1Eh	MAC_RX_JABB_CNT_2	Port 2 MAC Receive Jabber Error Count Register, Section 14.5.2.17
0C1Fh	MAC_RX_ALIGN_CNT_2	Port 2 MAC Receive Alignment Error Count Register, Section 14.5.2.18
0C20h	MAC_RX_PKTLEN_CNT_2	Port 2 MAC Receive Packet Length Count Register, Section 14.5.2.19
0C21h	MAC_RX_GOODPKTLEN_CNT_2	Port 2 MAC Receive Good Packet Length Count Register, Section 14.5.2.20
0C22h	MAC_RX_SYMBL_CNT_2	Port 2 MAC Receive Symbol Error Count Register, Section 14.5.2.21
0C23h	MAC_RX_CTLFRM_CNT_2	Port 2 MAC Receive Control Frame Count Register, Section 14.5.2.22
0C24h-0C3Fh	RESERVED	Reserved for Future Use
0C40h	MAC_TX_CFG_2	Port 2 MAC Transmit Configuration Register, Section 14.5.2.23

Table 14.12 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0C41h	MAC_TX_FC_SETTINGS_2	Port 2 MAC Transmit Flow Control Settings Register, Section 14.5.2.24
0C42h-0C50h	RESERVED	Reserved for Future Use
0C51h	MAC_TX_DEFER_CNT_2	Port 2 MAC Transmit Deferred Count Register, Section 14.5.2.25
0C52h	MAC_TX_PAUSE_CNT_2	Port 2 MAC Transmit Pause Count Register, Section 14.5.2.26
0C53h	MAC_TX_PKTOK_CNT_2	Port 2 MAC Transmit OK Count Register, Section 14.5.2.27
0C54h	MAC_RX_64_CNT_2	Port 2 MAC Transmit 64 Byte Count Register, Section 14.5.2.28
0C55h	MAC_TX_65_TO_127_CNT_2	Port 2 MAC Transmit 65 to 127 Byte Count Register, Section 14.5.2.29
0C56h	MAC_TX_128_TO_255_CNT_2	Port 2 MAC Transmit 128 to 255 Byte Count Register, Section 14.5.2.30
0C57h	MAC_TX_256_TO_511_CNT_2	Port 2 MAC Transmit 256 to 511 Byte Count Register, Section 14.5.2.31
0C58h	MAC_TX_512_TO_1023_CNT_2	Port 2 MAC Transmit 512 to 1023 Byte Count Register, Section 14.5.2.32
0C59h	MAC_TX_1024_TO_MAX_CNT_2	Port 2 MAC Transmit 1024 to Max Byte Count Register, Section 14.5.2.33
0C5Ah	MAC_TX_UNDSZE_CNT_2	Port 2 MAC Transmit Undersize Count Register, Section 14.5.2.34
0C5Bh	RESERVED	Reserved for Future Use
0C5Ch	MAC_TX_PKTLEN_CNT_2	Port 2 MAC Transmit Packet Length Count Register, Section 14.5.2.35
0C5Dh	MAC_TX_BRDCST_CNT_2	Port 2 MAC Transmit Broadcast Count Register, Section 14.5.2.36
0C5Eh	MAC_TX_MULCST_CNT_2	Port 2 MAC Transmit Multicast Count Register, Section 14.5.2.37
0C5Fh	MAC_TX_LATECOL_2	Port 2 MAC Transmit Late Collision Count Register, Section 14.5.2.38
0C60h	MAC_TX_EXCOL_CNT_2	Port 2 MAC Transmit Excessive Collision Count Register, Section 14.5.2.39
0C61h	MAC_TX_SNGLECOL_CNT_2	Port 2 MAC Transmit Single Collision Count Register, Section 14.5.2.40
0C62h	MAC_TX_MULTICOL_CNT_2	Port 2 MAC Transmit Multiple Collision Count Register, Section 14.5.2.41
0C63h	MAC_TX_TOTALCOL_CNT_2	Port 2 MAC Transmit Total Collision Count Register, Section 14.5.2.42
0C64-0C7Fh	RESERVED	Reserved for Future Use
0C80h	MAC_IMR_2	Port 2 MAC Interrupt Mask Register, Section 14.5.2.43
0C81h	MAC_IPR_2	Port 2 MAC Interrupt Pending Register, Section 14.5.2.44

Table 14.12 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
0C82h-17FFh	RESERVED	Reserved for Future Use
Switch Engine CSRs		
1800h	SWE_ALR_CMD	Switch Engine ALR Command Register, Section 14.5.3.1
1801h	SWE_ALR_WR_DAT_0	Switch Engine ALR Write Data 0 Register, Section 14.5.3.2
1802h	SWE_ALR_WR_DAT_1	Switch Engine ALR Write Data 1 Register, Section 14.5.3.3
1803h-1804h	RESERVED	Reserved for Future Use
1805h	SWE_ALR_RD_DAT_0	Switch Engine ALR Read Data 0 Register, Section 14.5.3.4
1806h	SWE_ALR_RD_DAT_1	Switch Engine ALR Read Data 1 Register, Section 14.5.3.5
1807h	RESERVED	Reserved for Future Use
1808h	SWE_ALR_CMD_STS	Switch Engine ALR Command Status Register, Section 14.5.3.6
1809h	SWE_ALR_CFG	Switch Engine ALR Configuration Register, Section 14.5.3.7
180Ah	RESERVED	Reserved for Future Use
180Bh	SWE_VLAN_CMD	Switch Engine VLAN Command Register, Section 14.5.3.8
180Ch	SWE_VLAN_WR_DATA	Switch Engine VLAN Write Data Register, Section 14.5.3.9
180Dh	RESERVED	Reserved for Future Use
180Eh	SWE_VLAN_RD_DATA	Switch Engine VLAN Read Data Register, Section 14.5.3.10
180Fh	RESERVED	Reserved for Future Use
1810h	SWE_VLAN_CMD_STS	Switch Engine VLAN Command Status Register, Section 14.5.3.11
1811h	SWE_DIFFSERV_TBL_CMD	Switch Engine DIFSERV Table Command Register, Section 14.5.3.12
1812h	SWE_DIFFSERV_TBL_WR_DATA	Switch Engine DIFFSERV Table Write Data Register, Section 14.5.3.13
1813h	SWE_DIFFSERV_TBL_RD_DATA	Switch Engine DIFFSERV Table Read Data Register, Section 14.5.3.14
1814h	SWE_DIFFSERV_TBL_CMD_STS	Switch Engine DIFFSERV Table Command Status Register, Section 14.5.3.15
1815h-183Fh	RESERVED	Reserved for Future Use
1840h	SWE_GLB_INGRESS_CFG	Switch Engine Global Ingress Configuration Register, Section 14.5.3.16
1841h	SWE_PORT_INGRESS_CFG	Switch Engine Port Ingress Configuration Register, Section 14.5.3.17
1842h	SWE_ADMT_ONLY_VLAN	Switch Engine Admit Only VLAN Register, Section 14.5.3.18
1843h	SWE_PORT_STATE	Switch Engine Port State Register, Section 14.5.3.19
1844h	RESERVED	Reserved for Future Use
1845h	SWE_PRI_TO_QUE	Switch Engine Priority to Queue Register, Section 14.5.3.20

Table 14.12 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
1846h	SWE_PORT_MIRROR	Switch Engine Port Mirroring Register, Section 14.5.3.21
1847h	SWE_INGRESS_PORT_TYP	Switch Engine Ingress Port Type Register, Section 14.5.3.22
1848h	SWE_BCST_THROT	Switch Engine Broadcast Throttling Register, Section 14.5.3.23
1849h	SWE_ADMT_N_MEMBER	Switch Engine Admit Non Member Register, Section 14.5.3.24
184Ah	SWE_INGRESS_RATE_CFG	Switch Engine Ingress Rate Configuration Register, Section 14.5.3.25
184Bh	SWE_INGRESS_RATE_CMD	Switch Engine Ingress Rate Command Register, Section 14.5.3.26
184Ch	SWE_INGRESS_RATE_CMD_STS	Switch Engine Ingress Rate Command Status Register, Section 14.5.3.27
184Dh	SWE_INGRESS_RATE_WR_DATA	Switch Engine Ingress Rate Write Data Register, Section 14.5.3.28
184Eh	SWE_INGRESS_RATE_RD_DATA	Switch Engine Ingress Rate Read Data Register, Section 14.5.3.29
184Fh	RESERVED	Reserved for Future Use
1850h	SWE_FILTERED_CNT_MII	Switch Engine Port 0 Ingress Filtered Count Register, Section 14.5.3.30
1851h	SWE_FILTERED_CNT_1	Switch Engine Port 1 Ingress Filtered Count Register, Section 14.5.3.31
1852h	SWE_FILTERED_CNT_2	Switch Engine Port 2 Ingress Filtered Count Register, Section 14.5.3.32
1853h-1854h	RESERVED	Reserved for Future Use
1855h	SWE_INGRESS_REGEN_TBL_MII	Switch Engine Port 0 Ingress VLAN Priority Regeneration Register, Section 14.5.3.33
1856h	SWE_INGRESS_REGEN_TBL_1	Switch Engine Port 1 Ingress VLAN Priority Regeneration Register, Section 14.5.3.34
1857h	SWE_INGRESS_REGEN_TBL_2	Switch Engine Port 2 Ingress VLAN Priority Regeneration Register, Section 14.5.3.35
1858h	SWE_LRN_DISCRD_CNT_MII	Switch Engine Port 0 Learn Discard Count Register, Section 14.5.3.36
1859h	SWE_LRN_DISCRD_CNT_1	Switch Engine Port 1 Learn Discard Count Register, Section 14.5.3.37
185Ah	SWE_LRN_DISCRD_CNT_2	Switch Engine Port 2 Learn Discard Count Register, Section 14.5.3.38
185Bh-187Fh	RESERVED	Reserved for Future Use
1880h	SWE_IMR	Switch Engine Interrupt Mask Register, Section 14.5.3.39
1881h	SWE_IPR	Switch Engine Interrupt Pending Register, Section 14.5.3.40
1882h-1BFFh	RESERVED	Reserved for Future Use
Buffer Manager (BM) CSRs		

Table 14.12 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
1C00h	BM_CFG	Buffer Manager Configuration Register, Section 14.5.4.1
1C01h	BM_DROP_LVL	Buffer Manager Drop Level Register, Section 14.5.4.2
1C02h	BM_FC_PAUSE_LVL	Buffer Manager Flow Control Pause Level Register, Section 14.5.4.3
1C03h	BM_FC_RESUME_LVL	Buffer Manager Flow Control Resume Level Register, Section 14.5.4.4
1C04h	BM_BCST_LVL	Buffer Manager Broadcast Buffer Level Register, Section 14.5.4.5
1C05h	BM_DRP_CNT_SRC_MII	Buffer Manager Port 0 Drop Count Register, Section 14.5.4.6
1C06h	BM_DRP_CNT_SRC_1	Buffer Manager Port 1 Drop Count Register, Section 14.5.4.7
1C07h	BM_DRP_CNT_SRC_2	Buffer Manager Port 2 Drop Count Register, Section 14.5.4.8
1C08h	BM_RST_STS	Buffer Manager Reset Status Register, Section 14.5.4.9
1C09h	BM_RNDM_DSCRD_TBL_CMD	Buffer Manager Random Discard Table Command Register, Section 14.5.4.10
1C0Ah	BM_RNDM_DSCRD_TBL_WDATA	Buffer Manager Random Discard Table Write Data Register, Section 14.5.4.11
1C0Bh	BM_RNDM_DSCRD_TBL_RDATA	Buffer Manager Random Discard Table Read Data Register, Section 14.5.4.12
1C0Ch	BM_EGRSS_PORT_TYPE	Buffer Manager Egress Port Type Register, Section 14.5.4.13
1C0Dh	BM_EGRSS_RATE_00_01	Buffer Manager Port 0 Egress Rate Priority Queue 0/1 Register, Section 14.5.4.14
1C0Eh	BM_EGRSS_RATE_02_03	Buffer Manager Port 0 Egress Rate Priority Queue 2/3 Register, Section 14.5.4.15
1C0Fh	BM_EGRSS_RATE_10_11	Buffer Manager Port 1 Egress Rate Priority Queue 0/1 Register, Section 14.5.4.16
1C10h	BM_EGRSS_RATE_12_13	Buffer Manager Port 1 Egress Rate Priority Queue 2/3 Register, Section 14.5.4.17
1C11h	BM_EGRSS_RATE_20_21	Buffer Manager Port 2 Egress Rate Priority Queue 0/1 Register, Section 14.5.4.18
1C12h	BM_EGRSS_RATE_22_23	Buffer Manager Port 2 Egress Rate Priority Queue 2/3 Register, Section 14.5.4.19
1C13h	BM_VLAN_MII	Buffer Manager Port 0 Default VLAN ID and Priority Register, Section 14.5.4.20
1C14h	BM_VLAN_1	Buffer Manager Port 1 Default VLAN ID and Priority Register, Section 14.5.4.21
1C15h	BM_VLAN_2	Buffer Manager Port 2 Default VLAN ID and Priority Register, Section 14.5.4.22
1C16h	BM_RATE_DRP_CNT_SRC_MII	Buffer Manager Port 0 Ingress Rate Drop Count Register, Section 14.5.4.23
1C17h	BM_RATE_DRP_CNT_SRC_1	Buffer Manager Port 1 Ingress Rate Drop Count Register, Section 14.5.4.24

Table 14.12 Indirectly Accessible Switch Control and Status Registers (continued)

REGISTER #	SYMBOL	REGISTER NAME
1C18h	BM_RATE_DRP_CNT_SRC_2	Buffer Manager Port 2 Ingress Rate Drop Count Register, Section 14.5.4.25
1C19h-1C1Fh	RESERVED	Reserved for Future Use
1C20h	BM_IMR	Buffer Manager Interrupt Mask Register, Section 14.5.4.26
1C21h	BM_IPR	Buffer Manager Interrupt Pending Register, Section 14.5.4.27
1C22h-FFFFh	RESERVED	Reserved for Future Use

14.5.1 General Switch CSRs

This section details the general switch fabric CSRs. These registers control the main reset and interrupt functions of the switch fabric. A list of the general switch CSRs and their corresponding register numbers is included in Table 14.12.

14.5.1.1 Switch Device ID Register (SW_DEV_ID)

Register #: 0000h Size: 32 bits

This read-only register contains switch device ID information, including the device type, chip version and revision codes.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:16	**Device Type Code (DEVICE_TYPE)**	RO	03h
15:8	**Chip Version Code (CHIP_VERSION)**	RO	04h
7:0	**Revision Code (REVISION)**	RO	07h

14.5.1.2 Switch Reset Register (SW_RESET)

Register #: 0001h Size: 32 bits

This register contains the switch fabric global reset. Refer to Section 4.2, "Resets," on page 36 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Switch Fabric Reset (SW_RESET)** This bit is the global switch fabric reset. All switch fabric blocks are affected. This bit must be manually cleared.	WO	0b

14.5.1.3 Switch Global Interrupt Mask Register (SW_IMR)

Register #: 0004h Size: 32 bits

This read/write register contains the global interrupt mask for the switch fabric interrupts. All switch related interrupts in the Switch Global Interrupt Pending Register (SW_IPR) may be masked via this register. An interrupt is masked by setting the corresponding bit of this register. Clearing a bit will unmask the interrupt. When an unmasked switch fabric interrupt is generated in the Switch Global Interrupt Pending Register (SW_IPR), the interrupt will trigger the SWITCH_INT bit in the Interrupt Status Register (INT_STS). Refer to Chapter 5, "System Interrupts," on page 49 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:9	**RESERVED**	RO	-
8:7	**RESERVED** **Note:** These bits must be written as 11b	R/W	11b
6	**Buffer Manager Interrupt Mask (BM)** When set, prevents the generation of switch fabric interrupts due to the Buffer Manager via the Buffer Manager Interrupt Pending Register (BM_IPR). The status bits in the SW_IPR register are not affected.	R/W	1b
5	**Switch Engine Interrupt Mask (SWE)** When set, prevents the generation of switch fabric interrupts due to the Switch Engine via the Switch Engine Interrupt Pending Register (SWE_IPR). The status bits in the SW_IPR register are not affected.	R/W	1b
4:3	**RESERVED** **Note:** These bits must be written as 11b	R/W	11b
2	**Port 2 MAC Interrupt Mask (MAC_2)** When set, prevents the generation of switch fabric interrupts due to the Port 2 MAC via the MAC_IPR_2 register (see Section 14.5.2.44, on page 366). The status bits in the SW_IPR register are not affected.	R/W	1b
1	**Port 1 MAC Interrupt Mask (MAC_1)** When set, prevents the generation of switch fabric interrupts due to the Port 1 MAC via the MAC_IPR_1 register (see Section 14.5.2.44, on page 366). The status bits in the SW_IPR register are not affected.	R/W	1b
0	**Port 0 MAC Interrupt Mask (MAC_MII)** When set, prevents the generation of switch fabric interrupts due to the Port 0 MAC via the MAC_IPR_MII register (see Section 14.5.2.44, on page 366). The status bits in the SW_IPR register are not affected.	R/W	1b

14.5.1.4 Switch Global Interrupt Pending Register (SW_IPR)

Register #: 0005h Size: 32 bits

This read-only register contains the pending global interrupts for the switch fabric. A set bit indicates an unmasked bit in the corresponding switch fabric sub-system has been triggered. All switch related interrupts in this register may be masked via the Switch Global Interrupt Mask Register (SW_IMR) register. When an unmasked switch fabric interrupt is generated in this register, the interrupt will trigger the SWITCH_INT bit in the Interrupt Status Register (INT_STS). Refer to Chapter 5, "System Interrupts," on page 49 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:7	**RESERVED**	RO	-
6	**Buffer Manager Interrupt (BM)** Set when any unmasked bit in the Buffer Manager Interrupt Pending Register (BM_IPR) is triggered. This bit is cleared upon a read.	RC	0b
5	**Switch Engine Interrupt (SWE)** Set when any unmasked bit in the Switch Engine Interrupt Pending Register (SWE_IPR) is triggered. This bit is cleared upon a read.	RC	0b
4:3	**RESERVED**	RO	-
2	**Port 2 MAC Interrupt (MAC_2)** Set when any unmasked bit in the MAC_IPR_2 register (see Section 14.5.2.44, on page 366) is triggered. This bit is cleared upon a read.	RC	0b
1	**Port 1 MAC Interrupt (MAC_1)** Set when any unmasked bit in the MAC_IPR_1 register (see Section 14.5.2.44, on page 366) is triggered. This bit is cleared upon a read.	RC	0b
0	**Port 0 MAC Interrupt (MAC_MII)** Set when any unmasked bit in the MAC_IPR_MII register (see Section 14.5.2.44, on page 366) is triggered. This bit is cleared upon a read.	RC	0b

14.5.2 Switch Port 0, Port 1, and Port 2 CSRs

This section details the switch Port 0(Host MAC), Port 1, and Port 2 CSRs. Each port provides a functionally identical set of registers which allow for the configuration of port settings, interrupts, and the monitoring of the various packet counters.

Because the Port 0, Port 1, and Port 2 CSRs are functionally identical, their register descriptions have been consolidated. A lowercase “x” has been appended to the end of each switch port register name in this section, where “x” should be replaced with “MII”, “1”, or “2” for the Port 0, Port 1, or Port 2 registers respectively. A list of the Switch Port 0, Port 1, and Port 2 registers and their corresponding register numbers is included in Table 14.12.

14.5.2.1 Port x MAC Version ID Register (MAC_VER_ID_x)

Register #: Port0: 0400h
Port1: 0800h
Port2: 0C00h

Size: 32 bits

This read-only register contains switch device ID information, including the device type, chip version and revision codes.

BITS	DESCRIPTION	TYPE	DEFAULT
31:12	**RESERVED**	RO	-
11:8	**Device Type Code (DEVICE_TYPE)**	RO	5h
7:4	**Chip Version Code (CHIP_VERSION)**	RO	8h
3:0	**Revision Code (REVISION)**	RO	3h

14.5.2.2 Port x MAC Receive Configuration Register (MAC_RX_CFG_x)

Register #: Port0: 0401h Size: 32 bits
Port1: 0801h
Port2: 0C01h

This read/write register configures the packet type passing parameters of the port.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7	**RESERVED** **Note:** This bit must always be written as 0.	R/W	0b
6	**RESERVED**	RO	-
5	**Enable Receive Own Transmit** When set, the switch port will receive its own transmission if it is looped back from the PHY. Normally, this function is only used in Half Duplex PHY loopback.	R/W	0b
4	**RESERVED**	RO	-
3	**Jumbo2K** When set, the maximum packet size accepted is 2048 bytes. Statistics boundaries are also adjusted.	R/W	0b
2	**RESERVED**	RO	-
1	**Reject MAC Types** When set, MAC control frames (packets with a type field of 8808h) are filtered. When cleared, MAC Control frames, other than MAC Control Pause frames, are sent to the forwarding process. MAC Control Pause frames are always consumed by the switch.	R/W	1b
0	**RX Enable** When set, the receive port is enabled. When cleared, the receive port is disabled.	R/W	1b

14.5.2.3 Port x MAC Receive Undersize Count Register (MAC_RX_UNDSZE_CNT_x)

Register #: Port0: 0410h
Port1: 0810h
Port2: 0C10h

Size: 32 bits

This register provides a counter of undersized packets received by the port. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Undersize** Count of packets that have less than 64 byte and a valid FCS. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 115 hours.	RC	00000000h

14.5.2.4 Port x MAC Receive 64 Byte Count Register (MAC_RX_64_CNT_x)

Register #: Port0: 0411h
Port1: 0811h
Port2: 0C11h

Size: 32 bits

This register provides a counter of 64 byte packets received by the port. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX 64 Bytes** Count of packets (including bad packets) that have exactly 64 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: A bad packet is defined as a packet that has an FCS or Symbol error. For this counter, a packet that is not an integral number of bytes is rounded down to the nearest byte.

14.5.2.5 Port x MAC Receive 65 to 127 Byte Count Register (MAC_RX_65_TO_127_CNT_x)

Register #: Port0: 0412h
Port1: 0812h
Port2: 0C12h

Size: 32 bits

This register provides a counter of received packets between the size of 65 to 127 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX 65 to 127 Bytes** Count of packets (including bad packets) that have between 65 and 127 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 487 hours.	RC	00000000h

Note: A bad packet is defined as a packet that has an FCS or Symbol error. For this counter, a packet that is not an integral number of bytes is rounded down to the nearest byte.

14.5.2.6 Port x MAC Receive 128 to 255 Byte Count Register (MAC_RX_128_TO_255_CNT_x)

Register #: Port0: 0413h
Port1: 0813h
Port2: 0C13h

Size: 32 bits

This register provides a counter of received packets between the size of 128 to 255 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX 128 to 255 Bytes** Count of packets (including bad packets) that have between 128 and 255 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 848 hours.	RC	00000000h

Note: A bad packet is defined as a packet that has an FCS or Symbol error. For this counter, a packet that is not an integral number of bytes is rounded down to the nearest byte.

14.5.2.7 Port x MAC Receive 256 to 511 Byte Count Register (MAC_RX_256_TO_511_CNT_x)

Register #: Port0: 0414h
Port1: 0814h
Port2: 0C14h

Size: 32 bits

This register provides a counter of received packets between the size of 256 to 511 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX 256 to 511 Bytes** Count of packets (including bad packets) that have between 256 and 511 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 1581 hours.	RC	00000000h

Note: A bad packet is defined as a packet that has an FCS or Symbol error. For this counter, a packet that is not an integral number of bytes is rounded down to the nearest byte.

14.5.2.8 Port x MAC Receive 512 to 1023 Byte Count Register (MAC_RX_512_TO_1023_CNT_x)

Register #: Port0: 0415h
Port1: 0815h
Port2: 0C15h

Size: 32 bits

This register provides a counter of received packets between the size of 512 to 1023 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX 512 to 1023 Bytes** Count of packets (including bad packets) that have between 512 and 1023 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 3047 hours.	RC	00000000h

Note: A bad packet is defined as a packet that has an FCS or Symbol error. For this counter, a packet that is not an integral number of bytes is rounded down to the nearest byte.

14.5.2.9 Port x MAC Receive 1024 to Max Byte Count Register (MAC_RX_1024_TO_MAX_CNT_x)

Register #: Port0: 0416h
Port1: 0816h
Port2: 0C16h

Size: 32 bits

This register provides a counter of received packets between the size of 1024 to the maximum allowable number bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX 1024 to Max Bytes** Count of packets (including bad packets) that have between 1024 and the maximum allowable number of bytes. The max number of bytes is 1518 for untagged packets and 1522 for tagged packets. If Jumbo2K (bit 3) is set in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x), the max number of bytes is 2048. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 5979 hours.	RC	00000000h

Note: A bad packet is defined as a packet that has an FCS or Symbol error. For this counter, a packet with the maximum number of bytes that is not an integral number of bytes (e.g. a 1518 1/2 byte packet) is counted.

14.5.2.10 Port x MAC Receive Oversize Count Register (MAC_RX_OVRSZE_CNT_x)

Register #: Port0: 0417h
Port1: 0817h
Port2: 0C17h

Size: 32 bits

This register provides a counter of received packets with a size greater than the maximum byte size. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Oversize** Count of packets that have more than the maximum allowable number of bytes and a valid FCS. The max number of bytes is 1518 for untagged packets and 1522 for tagged packets. If Jumbo2K (bit 3) is set in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x), the max number of bytes is 2048. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 8813 hours.	RC	00000000h

Note: For this counter, a packet with the maximum number of bytes that is not an integral number of bytes (e.g. a 1518 1/2 byte packet) is not considered oversize.

14.5.2.11 Port x MAC Receive OK Count Register (MAC_RX_PKTOK_CNT_x)

Register #: Port0: 0418h
Port1: 0818h
Port2: 0C18h

Size: 32 bits

This register provides a counter of received packets that are or proper length and are free of errors. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX OK** Count of packets that are of proper length and are free of errors. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: A bad packet is one that has a FCS or Symbol error.

14.5.2.12 Port x MAC Receive CRC Error Count Register (MAC_RX_CRCERR_CNT_x)

Register #: Port0: 0419h
Port1: 0819h
Port2: 0C19h

Size: 32 bits

This register provides a counter of received packets that with CRC errors. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX CRC** Count of packets that have between 64 and the maximum allowable number of bytes and have a bad FCS, but do not have an extra nibble. The max number of bytes is 1518 for untagged packets and 1522 for tagged packets. If Jumbo2K (bit 3) is set in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x), the max number of bytes is 2048. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 137 hours.	RC	00000000h

14.5.2.13 Port x MAC Receive Multicast Count Register (MAC_RX_MULCST_CNT_x)

Register #: Port0: 041Ah Port1: 081Ah Port2: 0C1Ah Size: 32 bits

This register provides a counter of valid received packets with a multicast destination address. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Multicast** Count of good packets (proper length and free of errors), including MAC control frames, that have a multicast destination address (not including broadcasts). **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: A bad packet is one that has a FCS or Symbol error.

14.5.2.14 Port x MAC Receive Broadcast Count Register (MAC_RX_BRDCST_CNT_x)

Register #: Port0: 041Bh
Port1: 081Bh
Port2: 0C1Bh

Size: 32 bits

This register provides a counter of valid received packets with a broadcast destination address. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Broadcast** Count of valid packets (proper length and free of errors) that have a broadcast destination address. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: A bad packet is one that has a FCS or Symbol error.

14.5.2.15 Port x MAC Receive Pause Frame Count Register (MAC_RX_PAUSE_CNT_x)

Register #: Port0: 041Ch
Port1: 081Ch
Port2: 0C1Ch

Size: 32 bits

This register provides a counter of valid received pause frame packets. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Pause Frame** Count of valid packets (proper length and free of errors) that have a type field of 8808h and an op-code of 0001(Pause). **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: A bad packet is one that has a FCS or Symbol error.

14.5.2.16 Port x MAC Receive Fragment Error Count Register (MAC_RX_FRAG_CNT_x)

Register #: Port0: 041Dh
Port1: 081Dh
Port2: 0C1Dh

Size: 32 bits

This register provides a counter of received packets of less than 64 bytes and a FCS error. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Fragment** Count of packets that have less than 64 bytes and a FCS error. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 115 hours.	RC	00000000h

14.5.2.17 Port x MAC Receive Jabber Error Count Register (MAC_RX_JABB_CNT_x)

Register #: Port0: 041Eh
Port1: 081Eh
Port2: 0C1Eh

Size: 32 bits

This register provides a counter of received packets with greater than the maximum allowable number of bytes and a FCS error. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Jabber** Count of packets that have more than the maximum allowable number of bytes and a FCS error. The max number of bytes is 1518 for untagged packets and 1522 for tagged packets. If Jumbo2K (bit 3) is set in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x), the max number of bytes is 2048. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 8813 hours.	RC	00000000h

Note: For this counter, a packet with the maximum number of bytes that is not an integral number of bytes (e.g. a 1518 1/2 byte packet) and contains a FCS error is not considered jabber and is not counted here.

14.5.2.18 Port x MAC Receive Alignment Error Count Register (MAC_RX_ALIGN_CNT_x)

Register #: Port0: 041Fh
Port1: 081Fh
Port2: 0C1Fh

Size: 32 bits

This register provides a counter of received packets with 64 bytes to the maximum allowable, and a FCS error. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Alignment** Count of packets that have between 64 bytes and the maximum allowable number of bytes and are not byte aligned and have a bad FCS. The max number of bytes is 1518 for untagged packets and 1522 for tagged packets. If Jumbo2K (bit 3) is set in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x), the max number of bytes is 2048. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: For this counter, a packet with the maximum number of bytes that is not an integral number of bytes (e.g. a 1518 1/2 byte packet) and a FCS error is considered an alignment error and is counted.

14.5.2.19 Port x MAC Receive Packet Length Count Register (MAC_RX_PKTLEN_CNT_x)

Register #: Port0: 0420h
Port1: 0820h
Port2: 0C20h

Size: 32 bits

This register provides a counter of total bytes received. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Bytes** Count of total bytes received (including bad packets). **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 5.8 hours.	RC	00000000h

Note: If necessary, for oversized packets, the packet is either truncated at 1518 bytes (untagged, Jumbo2K=0), 1522 bytes (tagged, Jumbo2K=0), or 2048 bytes (Jumbo2K=1). If this occurs, the byte count recorded is 1518, 1522, or 2048, respectively. The Jumbo2K bit is located in the Port x MAC Receive Configuration Register (MAC_RX_CFG_x).

Note: A bad packet is one that has an FCS or Symbol error. For this counter, a packet that is not an integral number of bytes (e.g. a 1518 1/2 byte packet) is rounded down to the nearest byte.

14.5.2.20 Port x MAC Receive Good Packet Length Count Register (MAC_RX_GOODPKTLEN_CNT_x)

Register #: Port0: 0421h
Port1: 0821h
Port2: 0C21h

Size: 32 bits

This register provides a counter of total bytes received in good packets. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Good Bytes** Count of total bytes received in good packets (proper length and free of errors). **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 5.8 hours.	RC	00000000h

Note: A bad packet is one that has an FCS or Symbol error.

14.5.2.21 Port x MAC Receive Symbol Error Count Register (MAC_RX_SYMBOL_CNT_x)

Register #: Port0: 0422h
Port1: 0822h
Port2: 0C22h

Size: 32 bits

This register provides a counter of received packets with a symbol error. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Symbol** Count of packets that had a receive symbol error. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 115 hours.	RC	00000000h

14.5.2.22 Port x MAC Receive Control Frame Count Register (MAC_RX_CTLFRM_CNT_x)

Register #: Port0: 0423h
Port1: 0823h
Port2: 0C23h

Size: 32 bits

This register provides a counter of good packets with a type field of 8808h. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RX Control Frame** Count of good packets (proper length and free of errors) that have a type field of 8808h. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

Note: A bad packet is one that has an FCS or Symbol error.

14.5.2.23 Port x MAC Transmit Configuration Register (MAC_TX_CFG_x)

Register #: Port0: 0440h
Port1: 0840h
Port2: 0C40h

Size: 32 bits

This read/write register configures the transmit packet parameters of the port.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7	**MAC Counter Test** When set, TX and RX counters that normally clear to 0 when read, will be set to 7FFF_FFFCh when read with the exception of the Port x MAC Receive Packet Length Count Register (MAC_RX_PKTLEN_CNT_x), Port x MAC Transmit Packet Length Count Register (MAC_TX_PKTLEN_CNT_x), and Port x MAC Receive Good Packet Length Count Register (MAC_RX_GOODPKTLEN_CNT_x) counters which will be set to 7FFF_FF80h.	R/W	0b
6:2	**IFG Config** These bits control the transmit inter-frame gap. IFG bit times = (IFG Config *4) + 12 **Note:** IFG Config values less than 15 are unsupported.	R/W	10101b
1	**TX Pad Enable** When set, packets shorter than 64 bytes are padded with zeros if needed and a FCS is appended. Packets that are 60 bytes or less will become 64 bytes. Packets that are 61, 62, and 63 bytes will become 65, 66, and 67 bytes respectively.	R/W	1b
0	**TX Enable** When set, the transmit port is enabled. When cleared, the transmit port is disabled.	R/W	1b

14.5.2.24 Port x MAC Transmit Flow Control Settings Register (MAC_TX_FC_SETTINGS_x)

Register #: Port0: 0441h
Port1: 0841h
Port2: 0C41h

Size: 32 bits

This read/write register configures the flow control settings of the port.

BITS	DESCRIPTION	TYPE	DEFAULT
31:18	**RESERVED**	RO	-
17:16	**Backoff Reset RX/TX** Half duplex-only. Determines when the truncated binary exponential backoff attempts counter is reset. **00 = Reset on successful transmission (IEEE standard)** **01 = Reset on successful reception** **1X = Reset on either successful transmission or reception**	R/W	00b
15:0	**Pause Time Value** The value that is inserted into the transmitted pause packet when the switch wants to “XOFF” its link partner.	R/W	FFFFh

14.5.2.25 Port x MAC Transmit Deferred Count Register (MAC_TX_DEFER_CNT_x)

Register #: Port0: 0451h
Port1: 0851h
Port2: 0C51h

Size: 32 bits

This register provides a counter deferred packets. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Deferred** Count of packets that were available for transmission but were deferred on the first transmit attempt due to network traffic (either on receive or prior transmission). This counter is not incremented on collisions. This counter is incremented only in half-duplex operation. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.2.26 Port x MAC Transmit Pause Count Register (MAC_TX_PAUSE_CNT_x)

Register #: Port0: 0452h
Port1: 0852h
Port2: 0C52h

Size: 32 bits

This register provides a counter of transmitted pause packets. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Pause** Count of pause packets transmitted. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.2.27 Port x MAC Transmit OK Count Register (MAC_TX_PKTOK_CNT_x)

Register #: Port0: 0453h
Port1: 0853h
Port2: 0C53h

Size: 32 bits

This register provides a counter of successful transmissions. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX OK** Count of successful transmissions. Undersize packets are not included in this count. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.2.28 Port x MAC Transmit 64 Byte Count Register (MAC_TX_64_CNT_x)

Register #: Port0: 0454h
Port1: 0854h
Port2: 0C54h

Size: 32 bits

This register provides a counter of 64 byte packets transmitted by the port. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX 64 Bytes** Count of packets that have exactly 64 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.2.29 Port x MAC Transmit 65 to 127 Byte Count Register (MAC_TX_65_TO_127_CNT_x)

Register #: Port0: 0455h
Port1: 0855h
Port2: 0C55h

Size: 32 bits

This register provides a counter of transmitted packets between the size of 65 to 127 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX 65 to 127 Bytes** Count of packets that have between 65 and 127 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 487 hours.	RC	00000000h

14.5.2.30 Port x MAC Transmit 128 to 255 Byte Count Register (MAC_TX_128_TO_255_CNT_x)

Register #: Port0: 0456h
Port1: 0856h
Port2: 0C56h

Size: 32 bits

This register provides a counter of transmitted packets between the size of 128 to 255 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX 128 to 255 Bytes** Count of packets that have between 128 and 255 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 848 hours.	RC	00000000h

14.5.2.31 Port x MAC Transmit 256 to 511 Byte Count Register (MAC_TX_256_TO_511_CNT_x)

Register #: Port0: 0457h
Port1: 0857h
Port2: 0C57h

Size: 32 bits

This register provides a counter of transmitted packets between the size of 256 to 511 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX 256 to 511 Bytes** Count of packets that have between 256 and 511 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 1581 hours.	RC	00000000h

14.5.2.32 Port x MAC Transmit 512 to 1023 Byte Count Register (MAC_TX_512_TO_1023_CNT_x)

Register #: Port0: 0458h
Port1: 0858h
Port2: 0C58h

Size: 32 bits

This register provides a counter of transmitted packets between the size of 512 to 1023 bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX 512 to 1023 Bytes** Count of packets that have between 512 and 1023 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 3047 hours.	RC	00000000h

14.5.2.33 Port x MAC Transmit 1024 to Max Byte Count Register (MAC_TX_1024_TO_MAX_CNT_x)

Register #: Port0: 0459h
Port1: 0859h
Port2: 0C59h

Size: 32 bits

This register provides a counter of transmitted packets between the size of 1024 to the maximum allowable number bytes. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX 1024 to Max Bytes** Count of packets that have more than 1024 bytes. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 5979 hours.	RC	00000000h

14.5.2.34 Port x MAC Transmit Undersize Count Register (MAC_TX_UNDSZE_CNT_x)

Register #: Port0: 045Ah Port1: 085Ah Port2: 0C5Ah

Size: 32 bits

This register provides a counter of undersized packets transmitted by the port. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Undersize** Count of packets that have less than 64 bytes. **Note:** This condition could occur when TX padding is disabled and a tag is removed. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 458 hours.	RC	00000000h

14.5.2.35 Port x MAC Transmit Packet Length Count Register (MAC_TX_PKTLEN_CNT_x)

Register #: Port0: 045Ch
Port1: 085Ch
Port2: 0C5Ch

Size: 32 bits

This register provides a counter of total bytes transmitted. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Bytes** Count of total bytes transmitted (does not include bytes from collisions, but does include bytes from Pause packets). **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 5.8 hours.	RC	00000000h

14.5.2.36 Port x MAC Transmit Broadcast Count Register (MAC_TX_BRDCST_CNT_x)

Register #: Port0: 045Dh
Port1: 085Dh
Port2: 0C5Dh

Size: 32 bits

This register provides a counter of transmitted broadcast packets. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Broadcast** Count of broadcast packets transmitted. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.2.37 Port x MAC Transmit Multicast Count Register (MAC_TX_MULCST_CNT_x)

Register #: Port0: 045Eh Size: 32 bits
Port1: 085Eh
Port2: 0C5Eh

This register provides a counter of transmitted multicast packets. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Multicast** Count of multicast packets transmitted including MAC Control Pause frames. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.2.38 Port x MAC Transmit Late Collision Count Register (MAC_TX_LATECOL_CNT_x)

Register #: Port0: 045Fh
Port1: 085Fh
Port2: 0C5Fh

Size: 32 bits

This register provides a counter of transmitted packets which experienced a late collision. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Late Collision** Count of transmitted packets that experienced a late collision. This counter is incremented only in half-duplex operation. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.2.39 Port x MAC Transmit Excessive Collision Count Register (MAC_TX_EXCCOL_CNT_x)

Register #: Port0: 0460h
Port1: 0860h
Port2: 0C60h

Size: 32 bits

This register provides a counter of transmitted packets which experienced 16 collisions. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Excessive Collision** Count of transmitted packets that experienced 16 collisions. This counter is incremented only in half-duplex operation. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 1466 hours.	RC	00000000h

14.5.2.40 Port x MAC Transmit Single Collision Count Register (MAC_TX_SNGLECOL_CNT_x)

Register #: Port0: 0461h
Port1: 0861h
Port2: 0C61h

Size: 32 bits

This register provides a counter of transmitted packets which experienced exactly 1 collision. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Excessive Collision** Count of transmitted packets that experienced exactly 1 collision. This counter is incremented only in half-duplex operation. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 573 hours.	RC	00000000h

14.5.2.41 Port x MAC Transmit Multiple Collision Count Register (MAC_TX_MULTICOL_CNT_x)

Register #: Port0: 0462h
Port1: 0862h
Port2: 0C62h

Size: 32 bits

This register provides a counter of transmitted packets which experienced between 2 and 15 collisions. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Excessive Collision** Count of transmitted packets that experienced between 2 and 15 collisions. This counter is incremented only in half-duplex operation. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 664 hours.	RC	00000000h

14.5.2.42 Port x MAC Transmit Total Collision Count Register (MAC_TX_TOTALCOL_CNT_x)

Register #: Port0: 0463h
Port1: 0863h
Port2: 0C63h

Size: 32 bits

This register provides a counter of total collisions including late collisions. The counter is cleared upon being read.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**TX Total Collision** Total count of collisions including late collisions. This counter is incremented only in half-duplex operation. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 92 hours.	RC	00000000h

14.5.2.43 Port x MAC Interrupt Mask Register (MAC_IMR_x)

Register #: Port0: 0480h
Port1: 0880h
Port2: 0C80h

Size: 32 bits

This register contains the Port x interrupt mask. Port x related interrupts in the Port x MAC Interrupt Pending Register (MAC_IPR_x) may be masked via this register. An interrupt is masked by setting the corresponding bit of this register. Clearing a bit will unmask the interrupt. Refer to Chapter 5, "System Interrupts," on page 49 for more information.

Note: There are no possible Port x interrupt conditions available. This register exists for future use, and should be configured as indicated for future compatibility.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7:0	**RESERVED** **Note:** These bits must be written as 11h	R/W	11h

14.5.2.44 Port x MAC Interrupt Pending Register (MAC_IPR_x)

Register #: Port0: 0481h
Port1: 0881h
Port2: 0C81h

Size: 32 bits

This read-only register contains the pending Port x interrupts. A set bit indicates an interrupt has been triggered. All interrupts in this register may be masked via the Port x MAC Interrupt Pending Register (MAC_IPR_x) register. Refer to Chapter 5, "System Interrupts," on page 49 for more information.

Note: There are no possible Port x interrupt conditions available. This register exists for future use.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**RESERVED**	RO	-

14.5.3 Switch Engine CSRs

This section details the switch engine related CSRs. These registers allow configuration and monitoring of the various switch engine components including the ALR, VLAN, Port VID, and DIFFSERV tables. A list of the general switch CSRs and their corresponding register numbers is included in Table 14.12.

14.5.3.1 Switch Engine ALR Command Register (SWE_ALR_CMD)

Register #: 1800h Size: 32 bits

This register is used to manually read and write MAC addresses from/into the ALR table.

For a read access, the Switch Engine ALR Read Data 0 Register (SWE_ALR_RD_DAT_0) and Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1) should be read following the setting of bit 1(Get First Entry) or bit 0(Get Next Entry) of this register.

For write access, the Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0) and Switch Engine ALR Write Data 1 Register (SWE_ALR_WR_DAT_1) registers should first be written with the MAC address, followed by the setting of bit 2(Make Entry) of this register. The Make Pending bit in the Switch Engine ALR Command Status Register (SWE_ALR_CMD_STS) register indicates when the command is finished.

Refer to Chapter 6, "Switch Fabric," on page 55 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2	**Make Entry** When set, the contents of ALR_WR_DAT_0 and ALR_WR_DAT_1 are written into the ALR table. The ALR logic determines the location where the entry is written. This command can also be used to change or delete a previously written or automatically learned entry. This bit has no affect when written low. This bit must be cleared once the ALR Make command is completed, which can be determined by the ALR Status bit in the Switch Engine ALR Command Status Register (SWE_ALR_CMD_STS) register.	R/W	0b
1	**Get First Entry** When set, the ALR read pointer is reset to the beginning of the ALR table and the ALR table is searched for the first valid entry, which is loaded into the ALR_RD_DAT_0 and ALR_RD_DAT_1 registers. The bit has no affect when written low. This bit must be cleared after it is set.	R/W	0b
0	**Get Next Entry** When set, the next valid entry in the ALR MAC address table is loaded into the ALR_RD_DAT_0 and ALR_RD_DAT_1 registers. This bit has no affect when written low. This bit must be cleared after it is set.	R/W	0b

14.5.3.2 Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0)

Register #: 1801h Size: 32 bits

This register is used in conjunction with the Switch Engine ALR Write Data 1 Register (SWE_ALR_WR_DAT_1) and contains the first 32 bits of ALR data to be manually written via the Make Entry command in the Switch Engine ALR Command Register (SWE_ALR_CMD).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**MAC Address** This field contains the first 32 bits of the ALR entry that will be written into the ALR table. These bits correspond to the first 32 bits of the MAC address. Bit 0 holds the LSB of the first byte (the multicast bit).	R/W	00000000h

14.5.3.3 Switch Engine ALR Write Data 1 Register (SWE_ALR_WR_DAT_1)

Register #: 1802h Size: 32 bits

This register is used in conjunction with the Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0) and contains the last 32 bits of ALR data to be manually written via the Make Entry command in the Switch Engine ALR Command Register (SWE_ALR_CMD).

BITS	DESCRIPTION	TYPE	DEFAULT
31:25	**RESERVED**	RO	-
24	**Valid** When set, this bit makes the entry valid. It can be cleared to invalidate a previous entry that contained the specified MAC address.	R/W	0b
23	**Age/Override** This bit is used by the aging and forwarding processes. If the Static bit of this register is cleared, this bit should be set so that the entry will age in the normal amount of time. If the Static bit is set, this bit is used as a port state override bit. When set, packets received with a destination address that matches the MAC address in the SWE_ALR_WR_DAT_1 and SWE_ALR_WR_DAT_0 registers will be forwarded regardless of the port state of the ingress or egress port(s). This is typically used to allow the reception of BPDU packets in the non-forwarding state.	R/W	0b
22	**Static** When this bit is set, this entry will not be removed by the aging process and/or be changed by the learning process. When this bit is cleared, this entry will be automatically removed after 5 to 10 minutes of inactivity. Inactivity is defined as no packets being received with a source address that matches this MAC address. **Note:** This bit is normally set when adding manual entries. It must be cleared when removing an entry (clearing the Valid bit).	R/W	0b
21	**Filter** When set, packets with a destination address that matches this MAC address will be filtered.	R/W	0b
20:19	**Priority** These bits specify the priority that is used for packets with a destination address that matches this MAC address. This priority is only used if the Static bit of this register is set, and the DA Highest Priority (bit 5) in the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG) is set.	R/W	00b

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>18:16</td><td>Port
These bits indicate the port(s) associated with this MAC address. When bit 18 is cleared, a single port is selected. When bit 18 is set, multiple ports are selected.

<table><tr><th>VALUE</th><th>ASSOCIATED PORT(S)</th></tr><tr><td>000</td><td>Port 0(Host MAC)</td></tr><tr><td>001</td><td>Port 1</td></tr><tr><td>010</td><td>Port 2</td></tr><tr><td>011</td><td>RESERVED</td></tr><tr><td>100</td><td>Port 0(Host MAC) and Port 1</td></tr><tr><td>101</td><td>Port 0(Host MAC) and Port 2</td></tr><tr><td>110</td><td>Port 1 and Port 2</td></tr><tr><td>111</td><td>Port 0(Host MAC), Port 1, and Port 2</td></tr></table></td><td>R/W</td><td>000b</td></tr>
<tr><td>15:0</td><td>MAC Address
These field contains the last 16 bits of the ALR entry that will be written into the ALR table. They correspond to the last 16 bits of the MAC address. Bit 15 holds the MSB of the last byte (the last bit on the wire). The first 32 bits of the MAC address are located in the Switch Engine ALR Write Data 0 Register (SWE_ALR_WR_DAT_0).</td><td>R/W</td><td>0000h</td></tr>
</table>

14.5.3.4 Switch Engine ALR Read Data 0 Register (SWE_ALR_RD_DAT_0)

Register #: 1805h Size: 32 bits

This register is used in conjunction with the Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1) to read the ALR table. It contains the first 32 bits of the ALR entry and is loaded via the Get First Entry or Get Next Entry commands in the Switch Engine ALR Command Register (SWE_ALR_CMD). This register is only valid when either of the Valid or End of Table bits in the Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1) are set.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**MAC Address** This field contains the first 32 bits of the ALR entry. These bits correspond to the first 32 bits of the MAC address. Bit 0 holds the LSB of the first byte (the multicast bit).	RO	00000000h

14.5.3.5 Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1)

Register #: 1806h Size: 32 bits

This register is used in conjunction with the Switch Engine ALR Read Data 0 Register (SWE_ALR_RD_DAT_0) to read the ALR table. It contains the last 32 bits of the ALR entry and is loaded via the Get First Entry or Get Next Entry commands in the Switch Engine ALR Command Register (SWE_ALR_CMD). This register is only valid when either of the Valid or End of Table bits are set.

BITS	DESCRIPTION	TYPE	DEFAULT
31:25	**RESERVED**	RO	-
24	**Valid** This bit is cleared when the Get First Entry or Get Next Entry bits of the Switch Engine ALR Command Register (SWE_ALR_CMD) are written. This bit is set when a valid entry is found in the ALR table. This bit stays cleared when the top of the ALR table is reached without finding an entry.	RO	0b
23	**End of Table** This bit indicates that the end of the ALR table has been reached and further Get Next Entry commands are not required. **Note:** The Valid bit may or may not be set when the end of the table is reached.	RO	0b
22	**Static** Indicates that this entry will not be removed by the aging process. When this bit is cleared, this entry will be automatically removed after 5 to 10 minutes of inactivity. Inactivity is defined as no packets being received with a source address that matches this MAC address.	RO	0b
21	**Filter** When set, indicates that packets with a destination address that matches this MAC address will be filtered.	RO	0b
20:19	**Priority** These bits indicate the priority that is used for packets with a destination address that matches this MAC address. This priority is only used if the Static bit of this register is set, and the DA Highest Priority (bit 5) in the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG) register is set.	RO	00b

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>18:16</td><td>Port
These bits indicate the port(s) associated with this MAC address. When bit 18 is cleared, a single port is selected. When bit 18 is set, multiple ports are selected.

<table><tr><th>VALUE</th><th>ASSOCIATED PORT(S)</th></tr><tr><td>000</td><td>Port 0(Host MAC)</td></tr><tr><td>001</td><td>Port 1</td></tr><tr><td>010</td><td>Port 2</td></tr><tr><td>011</td><td>RESERVED</td></tr><tr><td>100</td><td>Port 0(Host MAC) and Port 1</td></tr><tr><td>101</td><td>Port 0(Host MAC) and Port 2</td></tr><tr><td>110</td><td>Port 1 and Port 2</td></tr><tr><td>111</td><td>Port 0(Host MAC), Port 1, and Port 2</td></tr></table></td><td>RO</td><td>000b</td></tr>
<tr><td>15:0</td><td>MAC Address
These field contains the last 16 bits of the ALR entry. They correspond to the last 16 bits of the MAC address. Bit 15 holds the MSB of the last byte (the last bit on the wire). The first 32 bits of the MAC address are located in the Switch Engine ALR Read Data 0 Register (SWE_ALR_RD_DAT_0).</td><td>RO</td><td>0000h</td></tr>
</table>

14.5.3.6 Switch Engine ALR Command Status Register (SWE_ALR_CMD_STS)

Register #: 1808h Size: 32 bits

This register indicates the current ALR command status.

BITS	DESCRIPTION	TYPE	DEFAULT
31:2	**RESERVED**	RO	-
1	**ALR Init Done** When set, indicates that the ALR table has finished being initialized by the reset process. The initialization is performed upon any reset that resets the switch fabric. The initialization takes approximately 20uS. During this time, any received packet will be dropped. Software should monitor this bit before writing any of the ALR tables or registers.	RO SS	Note 14.62
0	**Make Pending** When set, indicates that the Make Entry command is taking place. This bit is cleared once the Make Entry command has finished.	RO SC	0b

Note 14.62 The default value of this bit is 0 immediately following any switch fabric reset and then self-sets to 1 once the ALR table is initialized.

14.5.3.7 Switch Engine ALR Configuration Register (SWE_ALR_CFG)

Register #: 1809h Size: 32 bits

This register controls the ALR aging timer duration.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**ALR Age Test** When set, this bit decreases the aging timer from 5 minutes to 50mS.	R/W	0b

14.5.3.8 Switch Engine VLAN Command Register (SWE_VLAN_CMD)

Register #: 180Bh Size: 32 bits

This register is used to read and write the VLAN or Port VID tables. A write to this address performs the specified access.

For a read access, the Operation Pending bit in the Switch Engine VLAN Command Status Register (SWE_VLAN_CMD_STS) indicates when the command is finished. The Switch Engine VLAN Read Data Register (SWE_VLAN_RD_DATA) can then be read.

For a write access, the Switch Engine VLAN Write Data Register (SWE_VLAN_WR_DATA) register should be written first. The Operation Pending bit in the Switch Engine VLAN Command Status Register (SWE_VLAN_CMD_STS) indicates when the command is finished.

BITS	DESCRIPTION	TYPE	DEFAULT
31:6	**RESERVED**	RO	-
5	**VLAN RnW** This bit specifies a read(1) or a write(0) command.	R/W	0b
4	**PVIDnVLAN** When set, this bit selects the Port VID table. When cleared, this bit selects the VLAN table.	R/W	0b
3:0	**VLAN/Port** This field specifies the VLAN(0-15) or port(0-2) to be read or written. **Note:** Values outside of the valid range may cause unexpected results.	R/W	0h

14.5.3.9 Switch Engine VLAN Write Data Register (SWE_VLAN_WR_DATA)

Register #: 180Ch Size: 32 bits

This register is used write the VLAN or Port VID tables.

BITS	DESCRIPTION	TYPE	DEFAULT
31:18	**RESERVED**	RO	-
17:0	**Port Default VID and Priority** When the port VID table is selected (PVIDnVLAN=1 of the Switch Engine VLAN Command Register (SWE_VLAN_CMD)), bits 11:0 of this field specify the default VID for the port and bits 14:12 specify the default priority. All other bits of this field are reserved. These bits are used when a packet is received without a VLAN tag or with a NULL VLAN ID. By default, the VID and priority for all three ports is 0. **Note:** Values of 0 and FFFh should not be used since they are special VLAN IDs per the IEEE 802.3Q specification. **VLAN Data** When the VLAN table is selected (PVIDnVLAN=0 of the Switch Engine VLAN Command Register (SWE_VLAN_CMD)), the bits form the VLAN table entry as follows:	R/W	0b

BITS	DESCRIPTION	DEFAULT
17	**Member Port 2** Indicates the configuration of Port 2 for this VLAN entry. **1 = Member** - Packets with a VID that matches this entry are allowed on ingress. The port is a member of the broadcast domain on egress. **0 = Not a Member** - Packets with a VID that matches this entry are filtered on ingress unless the Admit Non Member bit in the Switch Engine Admit Non Member Register (SWE_ADMT_N_MEMBER) is set for this port. The port is not a member of the broadcast domain on egress.	0b
16	**Un-Tag Port 2** When this bit is set, packets received on Port 2 with a VID that matches this entry will have their tag removed when re-transmitted by egress ports that are designated as Hybrid ports via the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE).	0b
15	**Member Port 1** See description for Member Port 2.	0b
14	**Un-Tag Port 1** See description for Un-Tag Port 2.	0b
13	**Member Port 0 (Host MAC)** See description for Member Port 2.	0b
12	**Un-Tag Port 0 (Host MAC)** See description for Un-Tag Port 2.	0b
11:0	**VID** These bits specify the VLAN ID associated with this VLAN entry. To disable a VLAN entry, a value of 0 should be used. **Note:** A value of 0 is considered a NULL VLAN and should not normally be used other than to disable a VLAN entry. **Note:** A value of 3FFh is considered reserved by IEEE 802.1Q and should not be used.	000h

14.5.3.10 Switch Engine VLAN Read Data Register (SWE_VLAN_RD_DATA)

Register #: 180Eh Size: 32 bits

This register is used to read the VLAN or Port VID tables.

BITS	DESCRIPTION	TYPE	DEFAULT
31:18	**RESERVED**	RO	-
17:0	**Port Default VID and Priority** When the port VID table is selected (PVIDnVLAN=1 of the Switch Engine VLAN Command Register (SWE_VLAN_CMD)), bits 11:0 of this field specify the default VID for the port and bits 14:12 specify the default priority. All other bits of this field are reserved. These bits are used when a packet is received without a VLAN tag or with a NULL VLAN ID. By default, the VID and priority for all three ports is 0. **VLAN Data** When the VLAN table is selected (PVIDnVLAN=0 of the Switch Engine VLAN Command Register (SWE_VLAN_CMD)), the bits form the VLAN table entry as follows:	RO	00000h

BITS	DESCRIPTION	DEFAULT
17	**Member Port 2** Indicates the configuration of Port 2 for this VLAN entry. **1 = Member** - Packets with a VID that matches this entry are allowed on ingress. The port is a member of the broadcast domain on egress. **0 = Not a Member** - Packets with a VID that matches this entry are filtered on ingress unless the Admit Non Member bit in the Switch Engine Admit Non Member Register (SWE_ADMT_N_MEMBER) is set for this port. The port is not a member of the broadcast domain on egress.	0b
16	**Un-Tag Port 2** When this bit is set, packets received on Port 2 with a VID that matches this entry will have their tag removed when re-transmitted by egress ports that are designated as Hybrid ports via the Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE).	0b
15	**Member Port 1** See description for Member Port 2.	0b
14	**Un-Tag Port 1** See description for Un-Tag Port 2.	0b
13	**Member Port 0 (Host MAC)** See description for Member Port 2.	0b
12	**Un-Tag Port 0 (Host MAC)** See description for Un-Tag Port 2.	0b
11:0	**VID** These bits specify the VLAN ID associated with this VLAN entry.	000h

14.5.3.11 Switch Engine VLAN Command Status Register (SWE_VLAN_CMD_STS)

Register #: 1810h Size: 32 bits

This register indicates the current VLAN command status.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Operation Pending** When set, this bit indicates that the read or write command is taking place. This bit is cleared once the command has finished.	RO SC	0b

14.5.3.12 Switch Engine DIFFSERV Table Command Register (SWE_DIFFSERV_TBL_CFG)

Register #: 1811h Size: 32 bits

This register is used to read and write the DIFFSERV table. A write to this address performs the specified access. This table is used to map the received IP ToS/CS to a priority.

For a read access, the Operation Pending bit in the Switch Engine DIFFSERV Table Command Status Register (SWE_DIFFSERV_TBL_CMD_STS) indicates when the command is finished. The Switch Engine DIFFSERV Table Read Data Register (SWE_DIFFSERV_TBL_RD_DATA) can then be read.

For a write access, the Switch Engine DIFFSERV Table Write Data Register (SWE_DIFFSERV_TBL_WR_DATA) register should be written first. The Operation Pending bit in the Switch Engine DIFFSERV Table Command Status Register (SWE_DIFFSERV_TBL_CMD_STS) indicates when the command is finished.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7	**DIFFSERV Table RnW** This bit specifies a read(1) or a write(0) command.	R/W	0b
6	**RESERVED**	RO	-
5:0	**DIFFSERV Table Index** This field specifies the ToS/CS entry that is accessed.	R/W	0h

14.5.3.13 Switch Engine DIFFSERV Table Write Data Register (SWE_DIFFSERV_TBL_WR_DATA)

Register #: 1812h Size: 32 bits

This register is used to write the DIFFSERV table. The DIFFSERV table is not initialized upon reset on power-up. If DIFFSERV is enabled, the full table should be initialized by the host.

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2:0	**DIFFSERV Priority** These bits specify the assigned receive priority for IP packets with a ToS/CS field that matches this index.	R/W	000b

14.5.3.14 Switch Engine DIFFSERV Table Read Data Register (SWE_DIFFSERV_TBL_RD_DATA)

Register #: 1813h Size: 32 bits

This register is used to read the DIFFSERV table.

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2:0	**DIFFSERV Priority** These bits specify the assigned receive priority for IP packets with a ToS/CS field that matches this index.	RO	000b

14.5.3.15 Switch Engine DIFFSERV Table Command Status Register (SWE_DIFFSERV_TBL_CMD_STS)

Register #: 1814h Size: 32 bits

This register indicates the current DIFFSERV command status.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Operation Pending** When set, this bit indicates that the read or write command is taking place. This bit is cleared once the command has finished.	RO SC	0b

14.5.3.16 Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG)

Register #: 1840h Size: 32 bits

This register is used to configure the global ingress rules.

BITS	DESCRIPTION	TYPE	DEFAULT
31:14	**RESERVED**	RO	-
13	**Allow Monitorin Echo** When set, monitored packets are allowed to be echoed back to the source port. When cleared, monitored packets, like other packets, are never sent back to the source port. This bit is useful when the monitoring port wishes to receive it's own IGMP packets.	R/W	0b
12:10	**IGMP Monitoring Port** This field is the port bit map where IPv4 IGMP packets are sent.	R/W	0b
9	**Use IP** When set, the IPv4 TOS or IPv6 SC field is enabled as a transmit priority queue choice.	R/W	0b
8	**RESERVED**	R/W	0b
7	**Enable IGMP Monitoring** When set, IPv4 IGMP packets are monitored and sent to the IGMP monitoring port.	R/W	0b
6	**SWE Counter Test** When this bit is set the Switch Engine counters that normally clear to 0 when read will be set to 7FFF_FFFCh when read.	R/W	0b
5	**DA Highest Priority** When this bit is set and the Static bit in the ALR table for the destination MAC address is set, the transmit priority queue that is selected is taken from the ALR Priority bits (see the Switch Engine ALR Read Data 1 Register (SWE_ALR_RD_DAT_1)).	R/W	0b
4	**Filter Multicast** When this bit is set, packets with a multicast destination address are filtered if the address is not found in the ALR table. Broadcasts are not included in this filter.	R/W	0b
3	**Drop Unknown** When this bit is set, packets with a unicast destination address are filtered if the address is not found in the ALR table.	R/W	0b
2	**Use Precedence** When the priority is taken from an IPV4 packet (enabled via the Use IP bit), this bit selects between precedence bits in the TOS octet or the DIFFSERV table. When set, IPv4 packets will use the precedence bits in the TOS octet to select the transmit priority queue. When cleared, IPv4 packets will use the DIFFSERV table to select the transmit priority queue.	R/W	1b

BITS	DESCRIPTION	TYPE	DEFAULT
1	**VL Higher Priority** When this bit is set and VLANs are enabled, the priority from the VLAN tag has higher priority than the IP TOS/SC field.	R/W	1b
0	**VLAN Enable** When set, VLAN ingress rules are enabled. This also enables the VLAN to be used as the transmit priority queue selection.	R/W	0b

14.5.3.17 Switch Engine Port Ingress Configuration Register (SWE_PORT_INGRSS_CFG)

Register #: 1841h Size: 32 bits

This register is used to configure the per port ingress rules.

BITS	DESCRIPTION	TYPE	DEFAULT
31:6	**RESERVED**	RO	-
5:3	**Enable Learning on Ingress** When set, source addresses are learned when a packet is received on the corresponding port and the corresponding Port State in the Switch Engine Port State Register (SWE_PORT_STATE) is set to forwarding or learning. There is one enable bit per ingress port. Bits 5,4,3 correspond to switch ports 2,1,0 respectively.	R/W	111b
2:0	**Enable Membership Checking** When set, VLAN membership is checked when a packet is received on the corresponding port. The packet will be filtered if the ingress port is not a member of the VLAN (unless the Admit Non Member bit is set for the port in the Switch Engine Admit Non Member Register (SWE_ADMT_N_MEMBER)) For destination addresses that are found in the ALR table, the packet will be filtered if the egress port is not a member of the VLAN (for destination addresses that are not found in the ALR table only the ingress port is checked for membership). The VLAN Enable bit in the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG) needs to be set for these bits to have an affect. There is one enable bit per ingress port. Bits 2,1,0 correspond to switch ports 2,1,0 respectively.	R/W	000b

14.5.3.18 Switch Engine Admit Only VLAN Register (SWE_ADMT_ONLY_VLAN)

Register #: 1842h Size: 32 bits

This register is used to configure the per port ingress rule for allowing only VLAN tagged packets.

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2:0	**Admit Only VLAN** When set, untagged and priority tagged packets are filtered. The VLAN Enable bit in the Switch Engine Global Ingress Configuration Register (SWE_GLOBAL_INGRSS_CFG) needs to be set for these bits to have an affect. There is one enable bit per ingress port. Bits 2,1,0 correspond to switch ports 2,1,0 respectively.	R/W	000b

14.5.3.19 Switch Engine Port State Register (SWE_PORT_STATE)

Register #: 1843h Size: 32 bits

This register is used to configure the per port spanning tree state.

BITS	DESCRIPTION	TYPE	DEFAULT
31:6	**RESERVED**	RO	-
5:4	**Port State Port 2** These bits specify the spanning tree port states for Port 2. **00 = Forwarding** **01 = Blocking** **10 = Learning** **11 = Listening**	R/W	00b
3:2	**Port State Port 1** These bits specify the spanning tree port states for Port 1. **00 = Forwarding** **01 = Blocking** **10 = Learning** **11 = Listening**	R/W	00b
1:0	**Port State Port 0** These bits specify the spanning tree port states for Port 0(Host MAC). **00 = Forwarding** **01 = Blocking** **10 = Learning** **11 = Listening** **Note:** Typically, the Host MAC is kept in the forwarding state, since it is not a true network port.	R/W	00b

14.5.3.20 Switch Engine Priority to Queue Register (SWE_PRI_TO_QUE)

Register #: 1845h Size: 32 bits

This register specifies the Traffic Class table that maps the packet priority into the egress queues.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:14	**Priority 7 traffic Class** These bits specify the egress queue that is used for packets with a priority of 7.	R/W	11b
13:12	**Priority 6 traffic Class** These bits specify the egress queue that is used for packets with a priority of 6.	R/W	11b
11:10	**Priority 5 traffic Class** These bits specify the egress queue that is used for packets with a priority of 5.	R/W	10b
9:8	**Priority 4 traffic Class** These bits specify the egress queue that is used for packets with a priority of 4.	R/W	10b
7:6	**Priority 3 traffic Class** These bits specify the egress queue that is used for packets with a priority of 3.	R/W	01b
5:4	**Priority 2 traffic Class** These bits specify the egress queue that is used for packets with a priority of 2.	R/W	00b
3:2	**Priority 1 traffic Class** These bits specify the egress queue that is used for packets with a priority of 1.	R/W	00b
1:0	**Priority 0 traffic Class** These bits specify the egress queue that is used for packets with a priority of 0.	R/W	01b

14.5.3.21 Switch Engine Port Mirroring Register (SWE_PORT_MIRROR)

Register #: 1846h Size: 32 bits

This register is used to configure port mirroring.

BITS	DESCRIPTION	TYPE	DEFAULT
31:9	**RESERVED**	RO	-
8	**Enable RX Mirroring Filtered** When set, packets that would normally have been filtered are included in the receive mirroring function and are sent only to the sniffer port. When cleared, filtered packets are not mirrored. **Note:** The Ingress Filtered Count Registers will still count these packets as filtered and the Switch Engine Interrupt Pending Register (SWE_IPR) will still register a drop interrupt.	R/W	0b
7:5	**Sniffer Port** These bits specify the sniffer port that transmits packets that are monitored. Bits 7,6,5 correspond to switch ports 2,1,0 respectively. **Note:** Only one port should be set as the sniffer.	R/W	00b
4:2	**Mirrored Port** These bits specify if a port is to be mirrored. Bits 4,3,2 correspond to switch ports 2,1,0 respectively. **Note:** Multiple ports can be set as mirrored.	R/W	00b
1	**Enable RX Mirroring** This bit enables packets received on the mirrored ports to be also sent to the sniffer port.	R/W	0b
0	**Enable TX Mirroring** This bit enables packets transmitted on the mirrored ports to be also sent to the sniffer port.	R/W	0b

14.5.3.22 Switch Engine Ingress Port Type Register (SWE_INGRSS_PORT_TYP)

Register #: 1847h Size: 32 bits

This register is used to enable the special tagging mode used to determine the destination port based on the VLAN tag contents.

BITS	DESCRIPTION	TYPE	DEFAULT
31:6	**RESERVED**	RO	-
5:4	**Ingress Port Type Port 2** A setting of 11b enables the usage of the VLAN tag to specify the packet destination. All other values disable this feature.	R/W	00b
3:2	**Ingress Port Type Port 1** A setting of 11b enables the usage of the VLAN tag to specify the packet destination. All other values disable this feature.	R/W	00b
1:0	**Ingress Port Type Port 0** A setting of 11b enables the usage of the VLAN tag to specify the packet destination. All other values disable this feature.	R/W	00b

14.5.3.23 Switch Engine Broadcast Throttling Register (SWE_BCST_THROT)

Register #: 1848h Size: 32 bits

This register configures the broadcast input rate throttling.

BITS	DESCRIPTION	TYPE	DEFAULT
31:27	**RESERVED**	RO	-
26	**Broadcast Throttle Enable Port 2** This bit enables broadcast input rate throttling on Port 2.	R/W	0b
25:18	**Broadcast Throttle Level Port 2** These bits specify the number of bytes x 64 allowed to be received per every 1.72mS interval.	R/W	02h
17	**Broadcast Throttle Enable Port 1** This bit enables broadcast input rate throttling on Port 1.	R/W	0b
16:9	**Broadcast Throttle Level Port 1** These bits specify the number of bytes x 64 allowed to be received per every 1.72mS interval.	R/W	02h
8	**Broadcast Throttle Enable Port 0** This bit enables broadcast input rate throttling on Port 0(Host MAC).	R/W	0b
7:0	**Broadcast Throttle Level Port 0** These bits specify the number of bytes x 64 allowed to be received per every 1.72mS interval.	R/W	02h

14.5.3.24 Switch Engine Admit Non Member Register (SWE_ADMT_N_MEMBER)

Register #: 1849h Size: 32 bits

This register is used to allow access to a VLAN even if the ingress port is not a member.

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2:0	**Admit Non Member** When set, a received packet is accepted even if the ingress port is not a member of the destination VLAN. The VLAN still must be active in the switch. There is one bit per ingress port. Bits 2,1,0 correspond to switch ports 2,1,0 respectively.	R/W	000b

14.5.3.25 Switch Engine Ingress Rate Configuration Register (SWE_INGRSS_RATE_CFG)

Register #: 184Ah Size: 32 bits

This register, along with the settings accessible via the Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD), is used to configure the ingress rate metering/coloring.

BITS	DESCRIPTION	TYPE	DEFAULT
31:3	**RESERVED**	RO	-
2:1	**Rate Mode** These bits configure the rate metering/coloring mode. **00 = Source Port & Priority** **01 = Source Port Only** **10 = Priority Only** **11 = RESERVED**	R/W	00b
0	**Ingress Rate Enable** When set, ingress rates are metered and packets are colored and dropped if necessary.	R/W	0b

14.5.3.26 Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD)

Register #: 184Bh Size: 32 bits

This register is used to indirectly read and write the ingress rate metering/color table registers. A write to this address performs the specified access.

For a read access, the Operation Pending bit in the Switch Engine Ingress Rate Command Status Register (SWE_INGRSS_RATE_CMD_STS) indicates when the command is finished. The Switch Engine Ingress Rate Read Data Register (SWE_INGRSS_RATE_RD_DATA) can then be read.

For a write access, the Switch Engine Ingress Rate Write Data Register (SWE_INGRSS_RATE_WR_DATA) should be written first. The Operation Pending bit in the Switch Engine Ingress Rate Command Status Register (SWE_INGRSS_RATE_CMD_STS) indicates when the command is finished.

For details on 16-bit wide Ingress Rate Table registers indirectly accessible by this register, see Section 14.5.3.26.1 below.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7	**Ingress Rate RnW** These bits specify a read(1) or write(0) command.	R/W	0b
6:5	**Type** These bits select between the ingress rate metering/color table registers as follows: **00 = RESERVED** **01 = Committed Information Rate Registers (uses CIS Address field)** **10 = Committed Burst Register** **11 = Excess Burst Register**	R/W	00b
4:0	**CIR Address** These bits select one of the 24 Committed Information Rate registers. When Rate Mode is set to Source Port & Priority in the Switch Engine Ingress Rate Configuration Register (SWE_INGRSS_RATE_CFG), the first set of 8 registers (CIR addresses 0-7) are for to Port 0, the second set of 8 registers (CIR addresses 8-15) are for Port 1, and the third set of registers (CIR addresses 16-23) are for Port 2. Priority 0 is the lower register of each set (e.g. 0, 8, and 16). When Rate Mode is set to Source Port Only, the first register (CIR address 0) is for Port 0, the second register (CIR address 1) is for Port 1, and the third register (CIR address 2) is for Port 2. When Rate Mode is set to Priority Only, the first register (CIR address 0) is for priority 0, the second register (CIR address 1) is for priority 1, and so forth up to priority 23. **Note:** Values outside of the valid range may cause unexpected results.	R/W	0h

14.5.3.26.1 INGRESS RATE TABLE REGISTERS

The ingress rate metering/color table consists of 24 Committed Information Rate (CIR) registers (one per port/priority), a Committed Burst Size register, and an Excess Burst Size register. All metering/color table registers are 16-bits in size and are accessed indirectly via the Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD). Descriptions of these registers are detailed in Table 14.13 below.

Table 14.13 Metering/Color Table Register Descriptions

DESCRIPTION	TYPE	DEFAULT
Excess Burst Size This register specifies the maximum excess burst size in bytes. Bursts larger than this value that exceed the excess data rate are dropped. **Note:** Either this value or the Committed Burst Size should be set larger than or equal to the largest possible packet expected. **Note:** All of the Excess Burst token buckets are initialized to this default value. If a lower value is programmed into this register, the token buckets will need to be normally depleted below this value before this value has any affect on limiting the token bucket maximum values. This register is 16-bits wide.	R/W	0600h
Committed Burst Size This register specifies the maximum committed burst size in bytes. Bursts larger than this value that exceed the committed data rate are subjected to random dropping. **Note:** Either this value or the Excess Burst Size should be set larger than or equal to the largest possible packet expected. **Note:** All of the Committed Burst token buckets are initialized to this default value. If a lower value is programmed into this register, the token buckets will need to be normally depleted below this value before this value has any affect on limiting the token bucket maximum values. This register is 16-bits wide.	R/W	0600h
Committed Information Rate (CIR) These registers specify the committed data rate for the port/priority pair. The rate is specified in time per byte. The time is this value plus 1 times 20nS. There are 24 of these registers each 16-bits wide.	R/W	0014h

14.5.3.27 Switch Engine Ingress Rate Command Status Register (SWE_INGRSS_RATE_CMD_STS)

Register #: 184Ch Size: 32 bits

This register indicates the current ingress rate command status.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Operation Pending** When set, indicates that the read or write command is taking place. This bit is cleared once the command has finished.	RO SC	0b

14.5.3.28 Switch Engine Ingress Rate Write Data Register (SWE_INGRSS_RATE_WR_DATA)

Register #: 184Dh Size: 32 bits

This register is used to write the ingress rate table registers.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**Data** This is the data to be written to the ingress rate table registers as specified in the Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD). Refer to Section 14.5.3.26.1, "Ingress Rate Table Registers," on page 396 for details on these registers.	R/W	0000h

14.5.3.29 Switch Engine Ingress Rate Read Data Register (SWE_INGRSS_RATE_RD_DATA)

Register #: 184Eh Size: 32 bits

This register is used to read the ingress rate table registers.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:0	**Data** This is the read data from the ingress rate table registers as specified in the Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD). Refer to Section 14.5.3.26.1, "Ingress Rate Table Registers," on page 396 for details on these registers.	RO	0000h

14.5.3.30 Switch Engine Port 0 Ingress Filtered Count Register (SWE_FILTERED_CNT_MII)

Register #: 1850h Size: 32 bits

This register counts the number of packets filtered at ingress on Port 0(Host MAC). This count includes packets filtered due to broadcast throttling but does not include packets dropped due to ingress rate limiting (which are counted separately).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Filtered** This field is a count of packets filtered at ingress and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.3.31 Switch Engine Port 1 Ingress Filtered Count Register (SWE_FILTERED_CNT_1)

Register #: 1851h Size: 32 bits

This register counts the number of packets filtered at ingress on Port 1. This count includes packets filtered due to broadcast throttling but does not include packets dropped due to ingress rate limiting (which are counted separately).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Filtered** This field is a count of packets filtered at ingress and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.3.32 Switch Engine Port 2 Ingress Filtered Count Register (SWE_FILTERED_CNT_2)

Register #: 1852h Size: 32 bits

This register counts the number of packets filtered at ingress on Port 2. This count includes packets filtered due to broadcast throttling but does not include packets dropped due to ingress rate limiting (which are counted separately).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Filtered** This field is a count of packets filtered at ingress and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.3.33 Switch Engine Port 0 Ingress VLAN Priority Regeneration Table Register (SWE_INGRSS_REGEN_TBL_MII)

Register #: 1855h Size: 32 bits

This register provides the ability to map the received VLAN priority to a regenerated priority. The regenerated priority is used in determining the output priority queue. By default, the regenerated priority is identical to the received priority.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:21	**Regen7** These bits specify the regenerated priority for received priority 7.	R/W	7h
20:18	**Regen6** These bits specify the regenerated priority for received priority 6.	R/W	6h
17:15	**Regen5** These bits specify the regenerated priority for received priority 5.	R/W	5h
14:12	**Regen4** These bits specify the regenerated priority for received priority 4.	R/W	4h
11:9	**Regen3** These bits specify the regenerated priority for received priority 3.	R/W	3h
8:6	**Regen2** These bits specify the regenerated priority for received priority 2.	R/W	2h
5:3	**Regen1** These bits specify the regenerated priority for received priority 1.	R/W	1h
2:0	**Regen0** These bits specify the regenerated priority for received priority 0.	R/W	0h

14.5.3.34 Switch Engine Port 1 Ingress VLAN Priority Regeneration Table Register (SWE_INGRSS_REGEN_TBL_1)

Register #: 1856h Size: 32 bits

This register provides the ability to map the received VLAN priority to a regenerated priority. The regenerated priority is used in determining the output priority queue. By default, the regenerated priority is identical to the received priority.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:21	**Regen7** These bits specify the regenerated priority for received priority 7.	R/W	7h
20:18	**Regen6** These bits specify the regenerated priority for received priority 6.	R/W	6h
17:15	**Regen5** These bits specify the regenerated priority for received priority 5.	R/W	5h
14:12	**Regen4** These bits specify the regenerated priority for received priority 4.	R/W	4h
11:9	**Regen3** These bits specify the regenerated priority for received priority 3.	R/W	3h
8:6	**Regen2** These bits specify the regenerated priority for received priority 2.	R/W	2h
5:3	**Regen1** These bits specify the regenerated priority for received priority 1.	R/W	1h
2:0	**Regen0** These bits specify the regenerated priority for received priority 0.	R/W	0h

14.5.3.35 Switch Engine Port 2 Ingress VLAN Priority Regeneration Table Register (SWE_INGRSS_REGEN_TBL_2)

Register #: 1857h Size: 32 bits

This register provides the ability to map the received VLAN priority to a regenerated priority. The regenerated priority is used in determining the output priority queue. By default, the regenerated priority is identical to the received priority.

BITS	DESCRIPTION	TYPE	DEFAULT
31:24	**RESERVED**	RO	-
23:21	**Regen7** These bits specify the regenerated priority for received priority 7.	R/W	7h
20:18	**Regen6** These bits specify the regenerated priority for received priority 6.	R/W	6h
17:15	**Regen5** These bits specify the regenerated priority for received priority 5.	R/W	5h
14:12	**Regen4** These bits specify the regenerated priority for received priority 4.	R/W	4h
11:9	**Regen3** These bits specify the regenerated priority for received priority 3.	R/W	3h
8:6	**Regen2** These bits specify the regenerated priority for received priority 2.	R/W	2h
5:3	**Regen1** These bits specify the regenerated priority for received priority 1.	R/W	1h
2:0	**Regen0** These bits specify the regenerated priority for received priority 0.	R/W	0h

14.5.3.36 Switch Engine Port 0 Learn Discard Count Register (SWE_LRN_DISCRD_CNT_MII)

Register #: 1858h Size: 32 bits

This register counts the number of MAC addresses on Port 0(Host MAC) that were not learned or were overwritten by a different address due to address table space limitations.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Learn Discard** This field is a count of MAC addresses not learned or overwritten and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.3.37 Switch Engine Port 1 Learn Discard Count Register (SWE_LRN_DISCRD_CNT_1)

Register #: 1859h Size: 32 bits

This register counts the number of MAC addresses on Port 1 that were not learned or were overwritten by a different address due to address table space limitations.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Learn Discard** This field is a count of MAC addresses not learned or overwritten and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.3.38 Switch Engine Port 2 Learn Discard Count Register (SWE_LRN_DISCRD_CNT_2)

Register #: 185Ah Size: 32 bits

This register counts the number of MAC addresses on Port 2 that were not learned or were overwritten by a different address due to address table space limitations.

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Learn Discard** This field is a count of MAC addresses not learned or overwritten and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.3.39 Switch Engine Interrupt Mask Register (SWE_IMR)

Register #: 1880h Size: 32 bits

This register contains the Switch Engine interrupt mask, which masks the interrupts in the Switch Engine Interrupt Pending Register (SWE_IPR). All Switch Engine interrupts are masked by setting the Interrupt Mask bit. Clearing this bit will unmask the interrupts. Refer to Chapter 5, "System Interrupts," on page 49 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Interrupt Mask** When set, this bit masks interrupts from the Switch Engine. The status bits in the Switch Engine Interrupt Pending Register (SWE_IPR) are not affected.	R/W	1b

14.5.3.40 Switch Engine Interrupt Pending Register (SWE_IPR)

Register #: 1881h Size: 32 bits

This register contains the Switch Engine interrupt status. The status is double buffered. All interrupts in this register may be masked via the Switch Engine Interrupt Mask Register (SWE_IMR) register. Refer to Chapter 5, "System Interrupts," on page 49 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:15	**RESERVED**	RO	-
14:11	**Drop Reason B** When bit 8 is set, these bits indicate the reason a packet was dropped per the table below:	RC	0h

BIT VALUES	DESCRIPTION
0000	Admit Only VLAN was set and the packet was untagged or priority tagged.
0001	The destination address was not in the ALR table (unknown or broadcast), Enable Membership Checking on ingress was set, Admit Non Member was cleared and the source port was not a member of the incoming VLAN.
0010	The destination address was found in the ALR table but the source port was not in the forwarding state.
0011	The destination address was found in the ALR table but the destination port was not in the forwarding state.
0100	The destination address was found in the ALR table but Enable Membership Checking on ingress was set and the destination port was not a member of the incoming VLAN.
0101	The destination address was found in the ALR table but the Enable Membership Checking on ingress was set, Admit Non Member was cleared and the source port was not a member of the incoming VLAN.
0110	Drop Unknown was set and the destination address was a unicast but not in the ALR table.
0111	Filter Multicast was set and the destination address was a multicast and not in the ALR table.
1000	The packet was a broadcast but exceeded the Broadcast Throttling limit.
1001	The destination address was not in the ALR table (unknown or broadcast) and the source port was not in the forwarding state.
1010	The destination address was found in the ALR table but the source and destination ports were the same.
1011	The destination address was found in the ALR table and the Filter bit was set for that address.
1100	RESERVED
1101	RESERVED
1110	A packet was received with a VLAN ID of FFFh
1111	RESERVED

BITS	DESCRIPTION	TYPE	DEFAULT
10:9	**Source Port B** When bit 8 is set, these bits indicate the source port on which the packet was dropped. **00 = Port 0** **01 = Port 1** **10 = Port 2** **11 = RESERVED**	RC	00b
8	**Set B Valid** When set, bits 14:9 are valid.	RC	0b
7:4	**Drop Reason A** When bit 1 is set, these bits indicate the reason a packet was dropped. See the Drop Reason B description above for definitions of each value of this field.	RC	0h
3:2	**Source port A** When bit 1 is set, these bits indicate the source port on which the packet was dropped. **00 = Port 0** **01 = Port 1** **10 = Port 2** **11 = RESERVED**	RC	00b
1	**Set A Valid** When set, bits 7:2 are valid.	RC	0b
0	**Interrupt Pending** When set, a packet dropped event(s) is indicated.	RC	0b

14.5.4 Buffer Manager CSRs

This section details the Buffer Manager (BM) registers. These registers allow configuration and monitoring of the switch buffer levels and usage. A list of the general switch CSRs and their corresponding register numbers is included in Table 14.12.

14.5.4.1 Buffer Manager Configuration Register (BM_CFG)

Register #: 1C00h Size: 32 bits

This register enables egress rate pacing and ingress rate discarding.

BITS	DESCRIPTION	TYPE	DEFAULT
31:7	**RESERVED**	RO	-
6	**BM Counter Test** When this bit is set, Buffer Manager (BM) counters that normally clear to 0 when read, will be set to 7FFF_FFFC when read.	R/W	0b
5	**Fixed Priority Queue Servicing** When set, output queues are serviced with a fixed priority ordering. When cleared, output queues are serviced with a weighted round robin ordering.	R/W	0b
4:2	**Egress Rate Enable** When set, egress rate pacing is enabled. Bits 4,3,2 correspond to switch ports 2,1,0 respectively.	R/W	0b
1	**Drop on Yellow** When this bit is set, packets that exceed the Ingress Committed Burst Size (colored Yellow) are subjected to random discard. **Note:** See Section 14.5.3.26, "Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD)," on page 395 for information on configuring the Ingress Committed Burst Size.	R/W	0b
0	**Drop on Red** When this bit is set, packets that exceed the Ingress Excess Burst Size (colored Red) are discarded. **Note:** See Section 14.5.3.26, "Switch Engine Ingress Rate Command Register (SWE_INGRSS_RATE_CMD)," on page 395 for information on configuring the Ingress Excess Burst Size.	R/W	0b

14.5.4.2 Buffer Manager Drop Level Register (BM_DROP_LVL)

Register #: 1C01h Size: 32 bits

This register configures the overall buffer usage limits.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:8	**Drop Level Low** These bits specify the buffer limit that can be used per ingress port during times when 2 or 3 ports are active. Each buffer is 128 bytes. **Note:** A port is “active” when 36 buffers are in use for that port.	R/W	49h
7:0	**Drop Level High** These bits specify the buffer limit that can be used per ingress port during times when 1 port is active. Each buffer is 128 bytes. **Note:** A port is “active” when 36 buffers are in use for that port.	R/W	64h

14.5.4.3 Buffer Manager Flow Control Pause Level Register (BM_FC_PAUSE_LVL)

Register #: 1C02h Size: 32 bits

This register configures the buffer usage level when a Pause frame or backpressure is sent.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:8	**Pause Level Low** These bits specify the buffer usage level during times when 2 or 3 ports are active. Each buffer is 128 bytes. **Note:** A port is “active” when 36 buffers are in use for that port.	R/W	21h
7:0	**Pause Level High** These bits specify the buffer usage level during times when 1 port is active. Each buffer is 128 bytes. **Note:** A port is “active” when 36 buffers are in use for that port.	R/W	3Ch

14.5.4.4 Buffer Manager Flow Control Resume Level Register (BM_FC_RESUME_LVL)

Register #: 1C03h Size: 32 bits

This register configures the buffer usage level when a Pause frame with a pause value of 1 is sent.

BITS	DESCRIPTION	TYPE	DEFAULT
31:16	**RESERVED**	RO	-
15:8	**Resume Level Low** These bits specify the buffer usage level during times when 2 or 3 ports are active. Each buffer is 128 bytes. **Note:** A port is “active” when 36 buffers are in use for that port.	R/W	03h
7:0	**Resume Level High** These bits specify the buffer usage level during times when 0 or 1 ports are active. Each buffer is 128 bytes. **Note:** A port is “active” when 36 buffers are in use for that port.	R/W	07h

14.5.4.5 Buffer Manager Broadcast Buffer Level Register (BM_BCST_LVL)

Register #: 1C04h Size: 32 bits

This register configures the buffer usage limits for broadcasts, multicasts, and unknown unicasts.

BITS	DESCRIPTION	TYPE	DEFAULT
31:8	**RESERVED**	RO	-
7:0	**Broadcast Drop Level** These bits specify the maximum number of buffers that can be used by broadcasts, multicasts, and unknown unicasts. Each buffer is 128 bytes.	R/W	31h

14.5.4.6 Buffer Manager Port 0 Drop Count Register (BM_DRP_CNT_SRC_MII)

Register #: 1C05h Size: 32 bits

This register counts the number of packets dropped by the Buffer Manager that were received on Port 0(Host MAC). This count includes packets dropped due to buffer space limits and ingress rate limit discarding (Red and random Yellow dropping).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Dropped Count** These bits count the number of dropped packets received on Port 0 and is cleared when read. **Note:** The counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.4.7 Buffer Manager Port 1 Drop Count Register (BM_DRP_CNT_SRC_1)

Register #: 1C06h Size: 32 bits

This register counts the number of packets dropped by the Buffer Manager that were received on Port 1. This count includes packets dropped due to buffer space limits and ingress rate limit discarding (Red and random Yellow dropping).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Dropped Count** These bits count the number of dropped packets received on Port 1 and is cleared when read. **Note:** The counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.4.8 Buffer Manager Port 2 Drop Count Register (BM_DRP_CNT_SRC_2)

Register #: 1C07h Size: 32 bits

This register counts the number of packets dropped by the Buffer Manager that were received on Port 2. This count includes packets dropped due to buffer space limits and ingress rate limit discarding (Red and random Yellow dropping).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Dropped Count** These bits count the number of dropped packets received on Port 2 and is cleared when read. **Note:** The counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.4.9 Buffer Manager Reset Status Register (BM_RST_STS)

Register #: 1C08h Size: 32 bits

This register indicates when the Buffer Manager has been initialized by the reset process.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**BM Ready** When set, indicates the Buffer Manager tables have finished being initialized by the reset process. The initialization is performed upon any reset that resets the switch fabric.	RO SS	Note 14.63

Note 14.63 The default value of this bit is 0 immediately following any switch fabric reset and then self-sets to 1 once the ALR table is initialized.

14.5.4.10 Buffer Manager Random Discard Table Command Register (BM_RNDM_DSCRD_TBL_CMD)

Register #: 1C09h Size: 32 bits

This register is used to read and write the Random Discard Weight table. A write to this address performs the specified access. This table is used to set the packet drop probability verses the buffer usage.

For a read access, the Buffer Manager Random Discard Table Read Data Register (BM_RNDM_DSCRD_TBL_RDATA) can be read following a write to this register.

For a write access, the Buffer Manager Random Discard Table Write Data Register (BM_RNDM_DSCRD_TBL_WDATA) should be written before writing this register.

BITS	DESCRIPTION	TYPE	DEFAULT
31:5	**RESERVED**	RO	-
4	**Random Discard Weight Table RnW** Specifies a read (1) or a write (0) command.	R/W	0b
3:0	**Random Discard Weight Table Index** Specifies the buffer usage range that is accessed. There are a total of 16 probability entries. Each entry corresponds to a range of the number of buffers used by the ingress port. The ranges are structured to give more resolution towards the lower buffer usage end.	R/W	0h

BIT VALUES	BUFFER USAGE LEVEL
0000	0 to 7
0001	8 to 15
0010	16 to 23
0011	24 to 31
0100	32 to 39
0101	40 to 47
0110	48 to 55
0111	56 to 63
1000	64 to 79
1001	80 to 95
1010	96 to 111
1011	112 to 127
1100	128 to 159
1101	160 to 191
1110	192 to 223
1111	224 to 255

14.5.4.11 Buffer Manager Random Discard Table Write Data Register (BM_RNDM_DSCRD_TBL_WDATA)

Register #: 1C0Ah Size: 32 bits

This register is used to write the Random Discard Weight table.

Note: The Random Discard Weight table is not initialized upon reset or power-up. If a random discard is enabled, the full table should be initialized by the host.

BITS	DESCRIPTION	TYPE	DEFAULT
31:10	**RESERVED**	RO	-
9:0	**Drop Probability** These bits specify the discard probability of a packet that has been colored Yellow by the ingress metering. The probability is given in 1/1024's. For example, a setting of 1 is one in 1024, or approximately 0.1%. A setting of all ones (1023) is 1023 in 1024, or approximately 99.9%. There are a total of 16 probability entries. Each entry corresponds to a range of the number of buffers used by the ingress port, as specified in Section 14.5.4.10, "Buffer Manager Random Discard Table Command Register (BM_RNDM_DSCRD_TBL_CMD)".	R/W	000h

14.5.4.12 Buffer Manager Random Discard Table Read Data Register (BM_RNDM_DSCRD_TBL_RDATA)

Register #: 1C0Bh Size: 32 bits

This register is used to read the Random Discard Weight table.

BITS	DESCRIPTION	TYPE	DEFAULT
31:10	**RESERVED**	RO	-
9:0	**Drop Probability** These bits specify the discard probability of a packet that has been colored Yellow by the ingress metering. The probability is given in 1/1024's. For example, a setting of 1 is one in 1024, or approximately 0.1%. A setting of all ones (1023) is 1023 in 1024, or approximately 99.9%. There are a total of 16 probability entries. Each entry corresponds to a range of the number of buffers used by the ingress port, as specified in Section 14.5.4.10, "Buffer Manager Random Discard Table Command Register (BM_RNDM_DSCRD_TBL_CMD)".	RO	000h

14.5.4.13 Buffer Manager Egress Port Type Register (BM_EGRSS_PORT_TYPE)

Register #: 1C0Ch Size: 32 bits

This register is used to configure the egress VLAN tagging rules. See Section 6.5.6, "Adding, Removing, and Changing VLAN Tags," on page 79 for additional details.

BITS	DESCRIPTION	TYPE	DEFAULT
31:22	**RESERVED**	RO	-
21	**Insert Tag Port 2** When set, untagged packets will have a tag added that contains the Default VLAN ID and Priority of the *ingress* port. The un-tag bit in the VLAN table for the default VLAN ID also needs to be cleared in order for the tag to be inserted. This is only used when the Egress Port Type is set as Hybrid.	R/W	0b
20	**Change VLAN ID Port 2** When set, regular tagged packets will have their VLAN ID overwritten with the Default VLAN ID of the *egress* port. The Change Tag bit also needs to be set. The un-tag bit in the VLAN table for the incoming VLAN ID also needs to be cleared, otherwise the tag will be removed instead. Priority tagged packets will have VLAN ID overwritten with the Default VLAN ID of the *ingress* port independent of this bit. This is only used when the Egress Port Type is set as Hybrid.	R/W	0b
19	**Change Priority Port 2** When set, regular tagged packets will have their Priority overwritten with the Default Priority of the *egress* port. Priority tagged packets will have VLAN ID overwritten with the Default VLAN ID of the *ingress* port. For regular tagged packets, the Change Tag bit also needs to be set. The un-tag bit in the VLAN table for the incoming VLAN ID also needs to be cleared, otherwise the tag would be removed instead. This is only used when the Egress Port Type is set as Hybrid.	R/W	0b
18	**Change Tag Port 2** When set, allows the Change Tag and Change Priority bits to affect regular tagged packets. This bit has no affect on priority tagged packets. This is only used when the Egress Port Type is set as Hybrid.	R/W	0b

<table>
<tr><th>BITS</th><th>DESCRIPTION</th><th>TYPE</th><th>DEFAULT</th></tr>
<tr><td>17:16</td><td>Egress Port Type Port 2
These bits set the egress port type which determines the tagging/un-tagging rules.
<table><tr><th>BIT VALUES</th><th>EGRESS PORT TYPE</th></tr><tr><td>00</td><td>Dumb
Packets from regular ports pass untouched. Special tagged packets from the Host MAC port have their tagged stripped.</td></tr><tr><td>01</td><td>Access
Tagged packets (including special tagged packets from the Host MAC port) have their tagged stripped.</td></tr><tr><td>10</td><td>Hybrid
Supports a mix of tagging, un-tagging and changing tags. See Section 6.5.6, "Adding, Removing, and Changing VLAN Tags," on page 79 for additional details.</td></tr><tr><td>11</td><td>CPU
A special tag is added to indicate the source of the packet. See Section 6.5.6, "Adding, Removing, and Changing VLAN Tags," on page 79 for additional details.</td></tr></table></td><td>R/W</td><td>0b</td></tr>
<tr><td>15:14</td><td>RESERVED</td><td>RO</td><td>-</td></tr>
<tr><td>13</td><td>Insert Tag Port 1
Identical to Insert Tag Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>12</td><td>Change VLAN ID Port 1
Identical to Change VLAN ID Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>11</td><td>Change Priority Port 1
Identical to Change Priority Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>10</td><td>Change Tag Port 1
Identical to Change Tag Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>9:8</td><td>Egress Port Type Port 1
Identical to Egress Port Type Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>7:6</td><td>RESERVED</td><td>RO</td><td>-</td></tr>
<tr><td>5</td><td>Insert Tag Port 0(Host MAC)
Identical to Insert Tag Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>4</td><td>Change VLAN ID Port 0(Host MAC)
Identical to Change VLAN ID Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>3</td><td>Change Priority Port 0(Host MAC)
Identical to Change Priority Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>2</td><td>Change Tag Port 0(Host MAC)
Identical to Change Tag Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
<tr><td>1:0</td><td>Egress Port Type Port 0(Host MAC)
Identical to Egress Port Type Port 2 definition above.</td><td>R/W</td><td>0b</td></tr>
</table>

14.5.4.14 Buffer Manager Port 0 Egress Rate Priority Queue 0/1 Register (BM_EGRSS_RATE_00_01)

Register #: 1C0Dh Size: 32 bits

This register, along with the Buffer Manager Configuration Register (BM_CFG), is used to configure the egress rate pacing.

BITS	DESCRIPTION	TYPE	DEFAULT
31:26	**RESERVED**	RO	-
25:13	**Egress Rate Port 0 Priority Queue 1** These bits specify the egress data rate for the Port 0(Host MAC) priority queue 1. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	00000h
12:0	**Egress Rate Port 0 Priority Queue 0** These bits specify the egress data rate for the Port 0(Host MAC) priority queue 0. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	00000h

14.5.4.15 Buffer Manager Port 0 Egress Rate Priority Queue 2/3 Register (BM_EGRSS_RATE_02_03)

Register #: 1C0Eh Size: 32 bits

This register, along with the Buffer Manager Configuration Register (BM_CFG), is used to configure the egress rate pacing.

BITS	DESCRIPTION	TYPE	DEFAULT
31:26	**RESERVED**	RO	-
25:13	**Egress Rate Port 0 Priority Queue 3** These bits specify the egress data rate for the Port 0(Host MAC) priority queue 3. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	00000h
12:0	**Egress Rate Port 0 Priority Queue 2** These bits specify the egress data rate for the Port 0(Host MAC) priority queue 2. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	00000h

14.5.4.16 Buffer Manager Port 1 Egress Rate Priority Queue 0/1 Register (BM_EGRSS_RATE_10_11)

Register #: 1C0Fh Size: 32 bits

This register, along with the Buffer Manager Configuration Register (BM_CFG), is used to configure the egress rate pacing.

BITS	DESCRIPTION	TYPE	DEFAULT
31:26	**RESERVED**	RO	-
25:13	**Egress Rate Port 1 Priority Queue 1** These bits specify the egress data rate for the Port 1 priority queue 1. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	00000h
12:0	**Egress Rate Port 1 Priority Queue 0** These bits specify the egress data rate for the Port 1 priority queue 0. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	00000h

14.5.4.17 Buffer Manager Port 1 Egress Rate Priority Queue 2/3 Register (BM_EGRSS_RATE_12_13)

Register #: 1C10h Size: 32 bits

This register, along with the Buffer Manager Configuration Register (BM_CFG), is used to configure the egress rate pacing.

BITS	DESCRIPTION	TYPE	DEFAULT
31:26	**RESERVED**	RO	-
25:13	**Egress Rate Port 1 Priority Queue 3** These bits specify the egress data rate for the Port 1 priority queue 3. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	00000h
12:0	**Egress Rate Port 1 Priority Queue 2** These bits specify the egress data rate for the Port 1 priority queue 2. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	00000h

14.5.4.18 Buffer Manager Port 2 Egress Rate Priority Queue 0/1 Register (BM_EGRSS_RATE_20_21)

Register #: 1C11h Size: 32 bits

This register, along with the Buffer Manager Configuration Register (BM_CFG), is used to configure the egress rate pacing.

BITS	DESCRIPTION	TYPE	DEFAULT
31:26	**RESERVED**	RO	-
25:13	**Egress Rate Port 2 Priority Queue 1** These bits specify the egress data rate for the Port 2 priority queue 1. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	00000h
12:0	**Egress Rate Port 2 Priority Queue 0** These bits specify the egress data rate for the Port 2 priority queue 0. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	00000h

14.5.4.19 Buffer Manager Port 2 Egress Rate Priority Queue 2/3 Register (BM_EGRSS_RATE_22_23)

Register #: 1C12h Size: 32 bits

This register, along with the Buffer Manager Configuration Register (BM_CFG), is used to configure the egress rate pacing.

BITS	DESCRIPTION	TYPE	DEFAULT
31:26	**RESERVED**	RO	-
25:13	**Egress Rate Port 2 Priority Queue 3** These bits specify the egress data rate for the Port 2 priority queue 3. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	00000h
12:0	**Egress Rate Port 2 Priority Queue 2** These bits specify the egress data rate for the Port 2 priority queue 2. The rate is specified in time per byte. The time is this value plus 1 times 20nS.	R/W	00000h

14.5.4.20 Buffer Manager Port 0 Default VLAN ID and Priority Register (BM_VLAN_MII)

Register #: 1C13h Size: 32 bits

This register is used to specify the default VLAN ID and priority of Port 0(Host MAC).

BITS	DESCRIPTION	TYPE	DEFAULT
31:15	**RESERVED**	RO	-
14:12	**Default Priority** These bits specify the default priority that is used when a tag is inserted or changed on egress.	R/W	000b
11:0	**Default VLAN ID** These bits specify the default that is used when a tag is inserted or changed on egress.	R/W	000h

14.5.4.21 Buffer Manager Port 1 Default VLAN ID and Priority Register (BM_VLAN_1)

Register #: 1C14h Size: 32 bits

This register is used to specify the default VLAN ID and priority of Port 1.

BITS	DESCRIPTION	TYPE	DEFAULT
31:15	**RESERVED**	RO	-
14:12	**Default Priority** These bits specify the default priority that is used when a tag is inserted or changed on egress.	R/W	000b
11:0	**Default VLAN ID** These bits specify the default that is used when a tag is inserted or changed on egress.	R/W	000h

14.5.4.22 Buffer Manager Port 2 Default VLAN ID and Priority Register (BM_VLAN_2)

Register #: 1C15h Size: 32 bits

This register is used to specify the default VLAN ID and priority of Port 2.

BITS	DESCRIPTION	TYPE	DEFAULT
31:15	**RESERVED**	RO	-
14:12	**Default Priority** These bits specify the default priority that is used when a tag is inserted or changed on egress.	R/W	000b
11:0	**Default VLAN ID** These bits specify the default that is used when a tag is inserted or changed on egress.	R/W	000h

14.5.4.23 Buffer Manager Port 0 Ingress Rate Drop Count Register (BM_RATE_DRP_CNT_SRC_MII)

Register #: 1C16h Size: 32 bits

This register counts the number of packets received on Port 0(Host MAC) that were dropped by the Buffer Manager due to ingress rate limit discarding (Red and random Yellow dropping).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Dropped Count** These bits count the number of dropped packets received on Port 0(Host MAC) and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.4.24 Buffer Manager Port 1 Ingress Rate Drop Count Register (BM_RATE_DRP_CNT_SRC_1)

Register #: 1C17h Size: 32 bits

This register counts the number of packets received on Port 1 that were dropped by the Buffer Manager due to ingress rate limit discarding (Red and random Yellow dropping).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Dropped Count** These bits count the number of dropped packets received on Port 1 and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.4.25 Buffer Manager Port 2 Ingress Rate Drop Count Register (BM_RATE_DRP_CNT_SRC_2)

Register #: 1C18h Size: 32 bits

This register counts the number of packets received on Port 2 that were dropped by the Buffer Manager due to ingress rate limit discarding (Red and random Yellow dropping).

BITS	DESCRIPTION	TYPE	DEFAULT
31:0	**Dropped Count** These bits count the number of dropped packets received on Port 2 and is cleared when read. **Note:** This counter will stop at its maximum value of FFFF_FFFFh. Minimum rollover time at 100Mbps is approximately 481 hours.	RC	00000000h

14.5.4.26 Buffer Manager Interrupt Mask Register (BM_IMR)

Register #: 1C20h Size: 32 bits

This register contains the Buffer Manager interrupt mask, which masks the interrupts in the Buffer Manager Interrupt Pending Register (BM_IPR). All Buffer Manager interrupts are masked by setting the Interrupt Mask bit. Clearing this bit will unmask the interrupts. Refer to Chapter 5, "System Interrupts," on page 49 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:1	**RESERVED**	RO	-
0	**Interrupt Mask** When set, this bit masks interrupts from the Buffer Manager. The status bits in the Buffer Manager Interrupt Pending Register (BM_IPR) are not affected.	R/W	1b

14.5.4.27 Buffer Manager Interrupt Pending Register (BM_IPR)

Register #: 1C21h Size: 32 bits

This register contains the Buffer Manager interrupt status. The status is double buffered. All interrupts in this register may be masked via the Buffer Manager Interrupt Mask Register (BM_IMR) register. Refer to Chapter 5, "System Interrupts," on page 49 for more information.

BITS	DESCRIPTION	TYPE	DEFAULT
31:14	**RESERVED**	RO	-
13:10	**Drop Reason B** When bit 7 is set, these bits indicate the reason a packet was dropped per the table below: **BIT VALUES** / **DESCRIPTION** **0000** The destination address was not in the ALR table (unknown or broadcast), and the Broadcast Buffer Level was exceeded. **0001** Drop on Red was set and the packet was colored Red. **0010** There were no buffers available. **0011** There were no memory descriptors available. **0100** The destination address was not in the ALR table (unknown or broadcast) and there were no valid destination ports. **0101** The packet had a receive error and was >64 bytes **0110** The Buffer Drop Level was exceeded. **0111** RESERVED **1000** RESERVED **1001** Drop on Yellow was set, the packet was colored Yellow and was randomly selected to be dropped. **1010** RESERVED **1011** RESERVED **1100** RESERVED **1101** RESERVED **1110** RESERVED **1111** RESERVED	RC	0h
9:8	**Source Port B** When bit 7 is set, these bits indicate the source port on which the packet was dropped. **00 = Port 0** **01 = Port 1** **10 = Port 2** **11 = RESERVED**	RC	00b
7	**Status B Pending** When set, bits 13:8 are valid.	RC	0b

BITS	DESCRIPTION	TYPE	DEFAULT
6:3	**Drop Reason A** When bit 0 is set, these bits indicate the reason a packet was dropped. See the Drop Reason B description above for definitions of each value of this field.	RC	0h
2:1	**Source port A** When bit 0 is set, these bits indicate the source port on which the packet was dropped. **00 = Port 0** **01 = Port 1** **10 = Port 2** **11 = RESERVED**	RC	00b
0	**Set A Valid** When set, bits 6:1 are valid.	RC	0b

Chapter 15 Operational Characteristics

15.1 Absolute Maximum Ratings*

Supply Voltage (VDD33A1, VDD33A2, VDD33BIAS, VDD33IO) (Note 15.1) . . . . . 0V to +3.6V

Positive voltage on signal pins, with respect to ground (Note 15.2) . . . . . +6V

Negative voltage on signal pins, with respect to ground (Note 15.3) . . . . . -0.5V

Positive voltage on XI, with respect to ground. . . . . +4.6V

Positive voltage on XO, with respect to ground. . . . . +2.5V

Ambient Operating Temperature in Still Air (T_A). . . . . 0^oC to $+70^oC$

Storage Temperature. . . . . -55^oC to $+150^oC$

Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . . +/- 5kV

Note 15.1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 15.2 This rating does not apply to the following pins: XI, XO, EXRES.

Note 15.3 This rating does not apply to the following pins: EXRES.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 15.2, "Operating Conditions**", Section 15.4, "DC Specifications", or any other applicable section of this specification is not implied. Note, device signals are *NOT* 5 volt tolerant.

15.2 Operating Conditions**

Supply Voltage (VDD33A1, VDD33A2, VDD33BIAS, VDD33IO). . . . . +3.3V +/- 300mV

Ambient Operating Temperature in Still Air (T_A). . . . . 0^oC to $+70^oC$

**Proper operation of the LAN9312 is guaranteed only within the ranges specified in this section.

15.3 Power Consumption

This section details the power consumption of the LAN9312. Power consumption values are provided for both the device-only, and for the device plus the Ethernet components on ports 1 and 2.

Table 15.1 Supply and Current (10BASE-T Full-Duplex)

PARAMETER	TYPICAL (@ 3.3V)	MAXIMUM (@ 3.6V)	UNIT
Supply current at 3.3V (VDD33A1, VDD33A2, VDD33BIAS, VDD33IO)	165	185	mA
Power Dissipation (Device Only)	550	670	mW
Power Dissipation (Device and Ethernet components)	1245	1435	mW
Ambient Operating Temperature in Still Air (T_A)	25	Note 15.4	°C

Table 15.2 Supply and Current (100BASE-TX Full-Duplex)

PARAMETER	TYPICAL (@ 3.3V)	MAXIMUM (@ 3.6V)	UNIT
Supply current (VDD33A1, VDD33A2, VDD33BIAS, VDD33IO)	255	295	mA
Power Dissipation (Device Only)	845	1070	mW
Power Dissipation (Device and Ethernet components)	1130	1385	mW
Ambient Operating Temperature in Still Air (T_A)	25	Note 15.4	°C

Note 15.4 Over the conditions specified in Section 15.2, "Operating Conditions**".

Note: Power dissipation is determined by operating frequency, temperature, and supply voltage, as well as external source/sink current requirements.

15.4 DC Specifications

Table 15.3 I/O Buffer Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
IS Type Input Buffer						
Low Input Level	V_{ILI}	-0.3			V	
High Input Level	V_{IHI}			3.6	V	
Negative-Going Threshold	V_{ILT}	1.01	1.18	1.35	V	Schmitt trigger
Positive-Going Threshold	V_{IHT}	1.39	1.6	1.8	V	Schmitt trigger
SchmittTrigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	345	420	485	mV	
Input Leakage	I_{IN}	-10		10	uA	Note 15.5
Input Capacitance	C_{IN}			3	pF	
O8 Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	VDD33IO - 0.4			V	I_{OH} = -8mA
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	VDD33IO - 0.4			V	I_{OH} = -12mA
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
ICLK Type Buffer (XI Input)						Note 15.6
Low Input Level	V_{ILI}	-0.3		0.5	V	
High Input Level	V_{IHI}	1.4		3.6	V	

Note 15.5 This specification applies to all IS type inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add +/- 50uA per-pin (typical).

Note 15.6 XI can optionally be driven from a 25MHz single-ended clock oscillator.

Table 15.4 100BASE-TX Transceiver Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Peak Differential Output Voltage High	V_{PPH}	950	-	1050	mVpk	Note 15.7
Peak Differential Output Voltage Low	V_{PPL}	-950	-	-1050	mVpk	Note 15.7
Signal Amplitude Symmetry	V_{SS}	98	-	102	%	Note 15.7
Signal Rise and Fall Time	T_{RF}	3.0	-	5.0	nS	Note 15.7
Rise and Fall Symmetry	T_{RFS}	-	-	0.5	nS	Note 15.7
Duty Cycle Distortion	D_{CD}	35	50	65	%	Note 15.8

Table 15.4 100BASE-TX Transceiver Characteristics (continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Overshoot and Undershoot	V_{OS}	-	-	5	%	
Jitter				1.4	nS	Note 15.9

Note 15.7 Measured at line side of transformer, line replaced by 100Ω (+/- 1%) resistor.

Note 15.8 Offset from 16nS pulse width at 50% of pulse peak.

Note 15.9 Measured differentially.

Table 15.5 10BASE-T Transceiver Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Transmitter Peak Differential Output Voltage	V_{OUT}	2.2	2.5	2.8	V	Note 15.10
Receiver Differential Squelch Threshold	V_{DS}	300	420	585	mV	

Note 15.10 Min/max voltages guaranteed as measured with 100Ω resistive load.

15.5 AC Specifications

This section details the various AC timing specifications of the LAN9312.

Note: The I^2C timing adheres to the Philips *I^2C-Bus Specification*. Refer to the Philips *I^2C-Bus Specification* for detailed I^2C timing information.

15.5.1 Equivalent Test Load

Output timing specifications assume the 25pF equivalent test load illustrated in Figure 15.1 below.

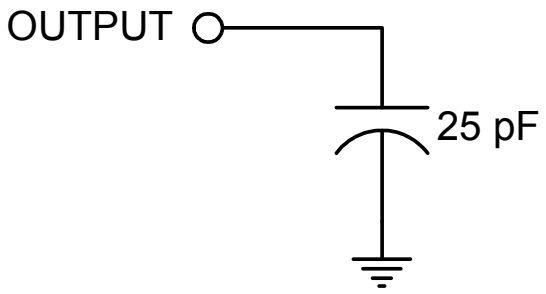


Figure 15.1 Output Equivalent Test Load

15.5.2 Reset and Configuration Strap Timing

This diagram illustrates the nRST pin timing requirements and its relation to the configuration strap pins and output drive. Assertion of nRST is not a requirement. However, if used, it must be asserted for the minimum period specified. Please refer to Section 4.2, "Resets," on page 36 for additional information.

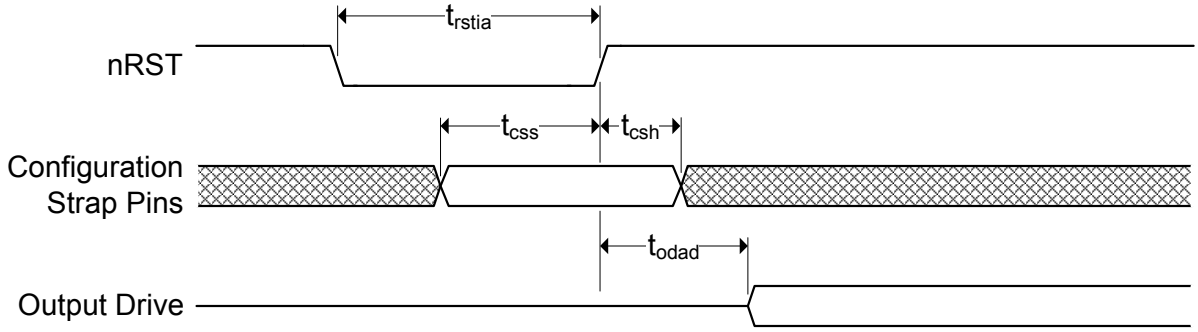


Figure 15.2 nRST Reset Pin Timing

Table 15.6 nRST Reset Pin Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{rstia}	nRST input assertion time	200			µS
t_{css}	Configuration strap pins setup to nRST deassertion	200			nS
t_{csh}	Configuration strap pins hold after nRST deassertion	10			nS
t_{odad}	Output drive after deassertion	30			nS

Note: Device configuration straps are latched as a result of nRST assertion. Refer to Section 4.2.4, "Configuration Straps," on page 40 for details.

15.5.3 Power-On Configuration Strap Valid Timing

This diagram illustrates the configuration strap valid timing requirements in relation to power-on. In order for valid configuration strap values to be read at power-on, the following timing requirements must be met.

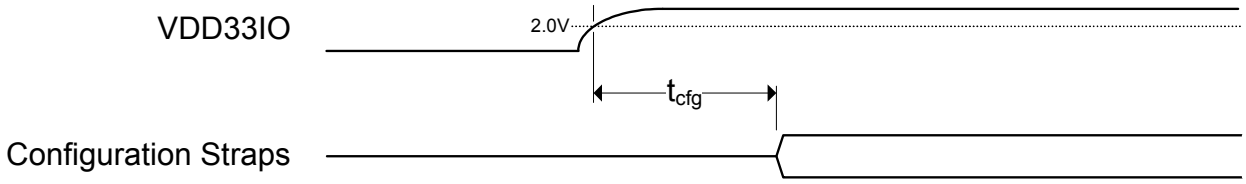


Figure 15.3 Power-On Configuration Strap Latching Timing

Table 15.7 Power-On Configuration Strap Latching Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{cfg}	Configuration strap valid time			15	mS

Note: Configuration straps must only be pulled high or low. Configuration straps must not be driven as inputs.

Note: Device configuration straps are also latched as a result of nRST assertion. Refer to Section 15.5.2, "Reset and Configuration Strap Timing," on page 445 and Section 4.2.4, "Configuration Straps," on page 40 for additional details.

15.5.4 PIO Read Cycle Timing

Please refer to Section 8.4.4, "PIO Reads," on page 106 for a functional description of this mode.

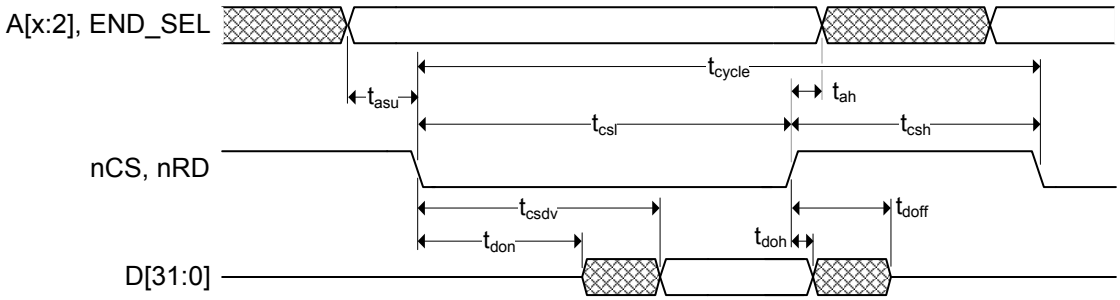


Figure 15.4 PIO Read Cycle Timing

Table 15.8 PIO Read Cycle Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{cycle}	Read Cycle Time	45			nS
t_{csl}	nCS, nRD Assertion Time	32			nS
t_{csh}	nCS, nRD De-assertion Time	13			nS
t_{csdv}	nCS, nRD Valid to Data Valid			30	nS
t_{asu}	Address setup to nCS, nRD Valid	0			nS
t_{ah}	Address Hold Time	0			nS
t_{don}	Data Buffer Turn On Time	0			nS
t_{doff}	Data Buffer Turn Off Time			9	nS
t_{doh}	Data Output Hold Time	0			nS

Note: A host PIO read cycle begins when both nCS and nRD are asserted. The cycle ends when either or both nCS and nRD are de-asserted. These signals may be asserted and de-asserted in any order.

15.5.5 PIO Burst Read Cycle Timing

Please refer to Section 8.4.5, "PIO Burst Reads," on page 107 for a functional description of this mode.

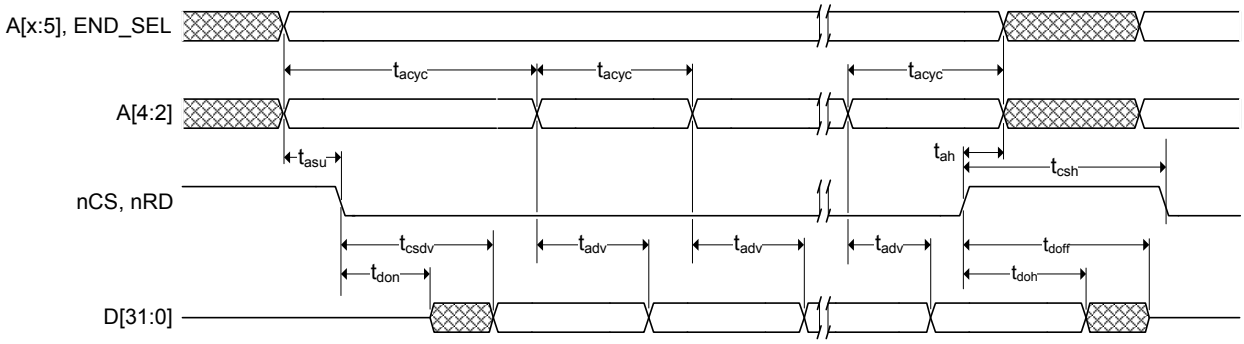


Figure 15.5 PIO Burst Read Cycle Timing

Table 15.9 PIO Burst Read Cycle Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{csh}	nCS, nRD De-assertion Time	13			nS
t_{csdv}	nCS, nRD Valid to Data Valid			30	nS
t_{acyc}	Address Cycle Time	45			nS
t_{asu}	Address Setup to nCS, nRD Valid	0			nS
t_{adv}	Address Stable to Data Valid			40	nS
t_{ah}	Address Hold Time	0			nS
t_{don}	Data Buffer Turn On Time	0			nS
t_{doff}	Data Buffer Turn Off Time			9	nS
t_{doh}	Data Output Hold Time	0			nS

Note: A host PIO burst read cycle begins when both nCS and nRD are asserted. The cycle ends when either or both nCS and nRD are de-asserted. These signals may be asserted and de-asserted in any order.

Note: Fresh data is supplied each time A[2] toggles.

15.5.6 RX Data FIFO Direct PIO Read Cycle Timing

Please refer to Section 8.4.6, "RX Data FIFO Direct PIO Reads," on page 108 for a functional description of this mode.

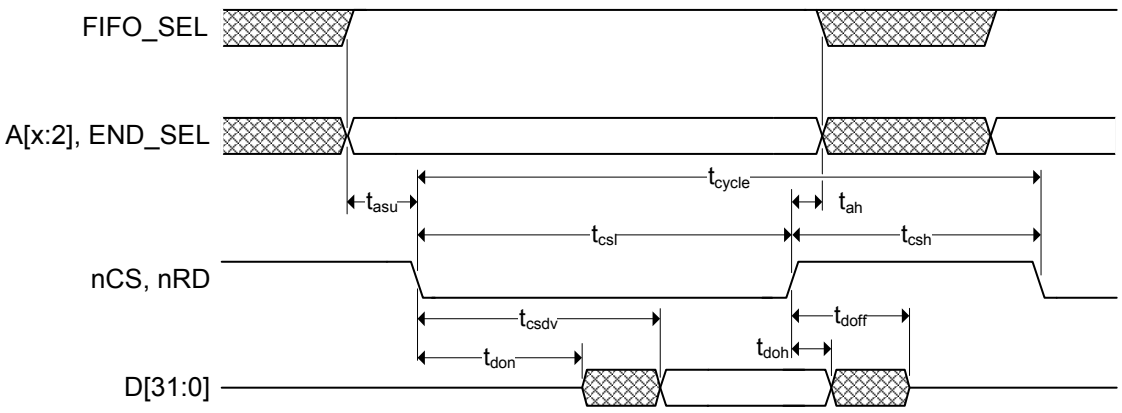


Figure 15.6 RX Data FIFO Direct PIO Read Cycle Timing

Table 15.10 RX Data FIFO Direct PIO Read Cycle Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{cycle}	Read Cycle Time	45			nS
t_{csl}	CS, nRD Assertion Time	32			nS
t_{csh}	nCS, nRD De-assertion Time	13			nS
t_{csdv}	nCS, nRD Valid to Data Valid			30	nS
t_{asu}	Address, FIFO_SEL Setup to nCS, nRD Valid	0			nS
t_{ah}	Address, FIFO_SEL Hold Time	0			nS
t_{don}	Data Buffer Turn On Time	0			nS
t_{doff}	Data Buffer Turn Off Time			9	nS
t_{doh}	Data Output Hold Time	0			nS

Note: A RX Data FIFO direct PIO read cycle begins when both nCS and nRD are asserted. The cycle ends when either or both nCS and nRD are de-asserted. They may be asserted and de-asserted in any order.

15.5.7 RX Data FIFO Direct PIO Burst Read Cycle Timing

Please refer to Section 8.4.7, "RX Data FIFO Direct PIO Burst Reads," on page 109 for a functional description of this mode.

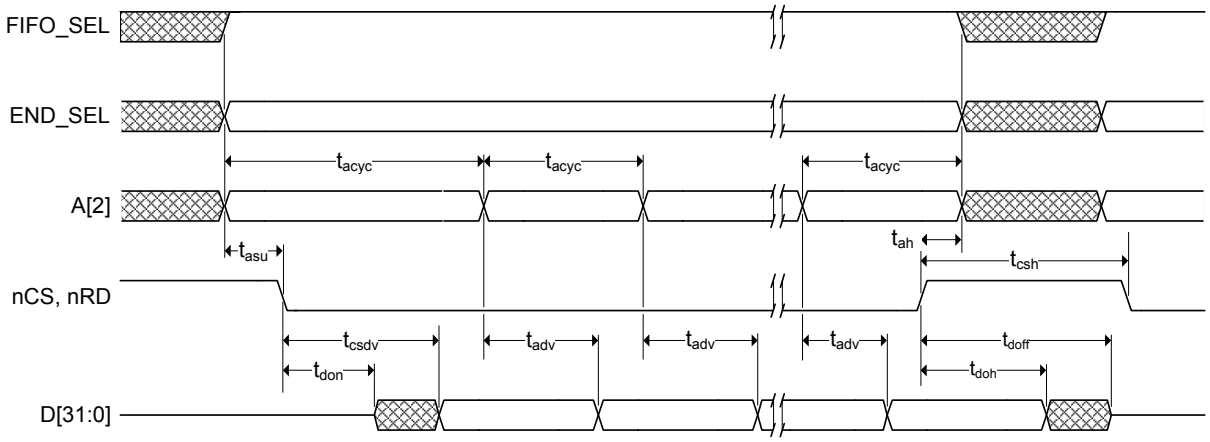


Figure 15.7 RX Data FIFO Direct PIO Burst Read Cycle Timing

Table 15.11 RX Data FIFO Direct PIO Burst Read Cycle Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{csh}	nCS, nRD De-assertion Time	13			nS
t_{csdv}	nCS, nRD Valid to Data Valid			30	nS
t_{acyc}	Address Cycle Time	45			nS
t_{asu}	Address, FIFO_SEL Setup to nCS, nRD Valid	0			nS
t_{adv}	Address Stable to Data Valid			40	nS
t_{ah}	Address, FIFO_SEL Hold Time	0			nS
t_{don}	Data Buffer Turn On Time	0			nS
t_{doff}	Data Buffer Turn Off Time			9	nS
t_{doh}	Data Output Hold Time	0			nS

Note: A RX Data FIFO direct PIO burst read cycle begins when both nCS and nRD are asserted. The cycle ends when either or both nCS and nRD are de-asserted. They may be asserted and de-asserted in any order.

Note: Fresh data is supplied each time A[2] toggles.

15.5.8 PIO Write Cycle Timing

Please refer to Section 8.4.8, "PIO Writes," on page 110 for a functional description of this mode.

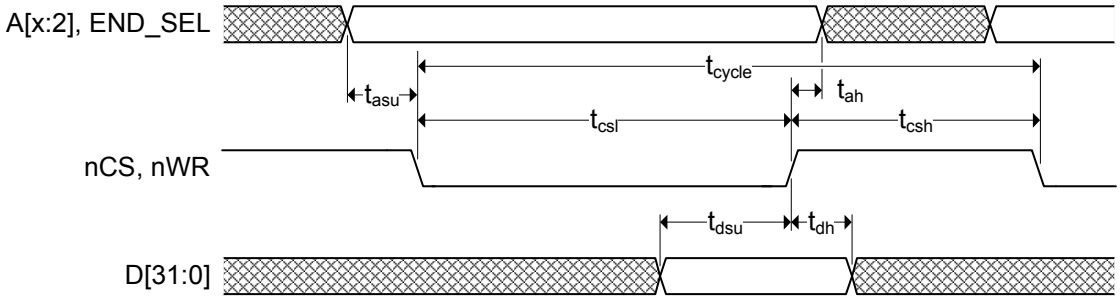


Figure 15.8 PIO Write Cycle Timing

Table 15.12 PIO Write Cycle Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{cycle}	Write Cycle Time	45			nS
t_{csl}	nCS, nWR Assertion Time	32			nS
t_{csh}	nCS, nWR De-assertion Time	13			nS
t_{asu}	Address Setup to nCS, nWR Assertion	0			nS
t_{ah}	Address Hold Time	0			nS
t_{dsu}	Data Setup to nCS, nWR De-assertion	7			nS
t_{dh}	Data Hold Time	0			nS

Note: A PIO write cycle begins when both nCS and nWR are asserted. The cycle ends when either or both nCS and nWR are de-asserted. These signals may be asserted and de-asserted in any order.

15.5.9 TX Data FIFO Direct PIO Write Cycle Timing

Please refer to Section 8.4.9, "TX Data FIFO Direct PIO Writes," on page 111 for a functional description of this mode.

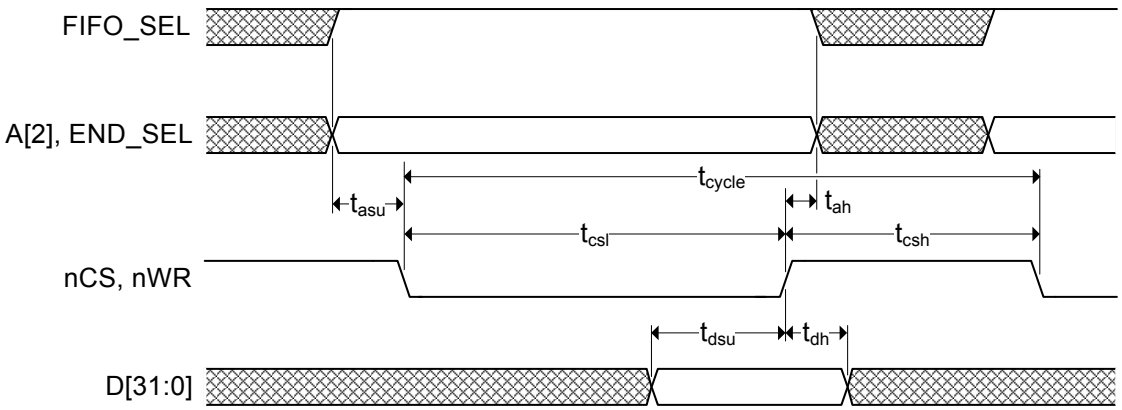


Figure 15.9 TX Data FIFO Direct PIO Write Cycle Timing

Table 15.13 TX Data FIFO Direct PIO Write Cycle Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{cycle}	Write Cycle Time	45			nS
t_{csl}	nCS, nWER Assertion Time	32			nS
t_{csh}	nCS, nWR De-assertion Time	13			nS
t_{asu}	Address, FIFO_SEL Setup to nCS, nWR Assertion	0			nS
t_{ah}	Address, FIFO_SEL Hold Time	0			nS
t_{dsu}	Data Setup to nCS, nWR De-assertion	7			nS
t_{dh}	Data Hold Time	0			nS

Note: A TX Data FIFO direct PIO write cycle begins when both nCS and nWR are asserted. The cycle ends when either or both nCS and nWR are de-asserted. They may be asserted and de-asserted in any order.

15.5.10 Microwire Timing

This section specifies the Microwire EEPROM interface timing requirements. Please refer to Section 10.2.3, "Microwire EEPROM," on page 144 for a functional description of this serial interface.

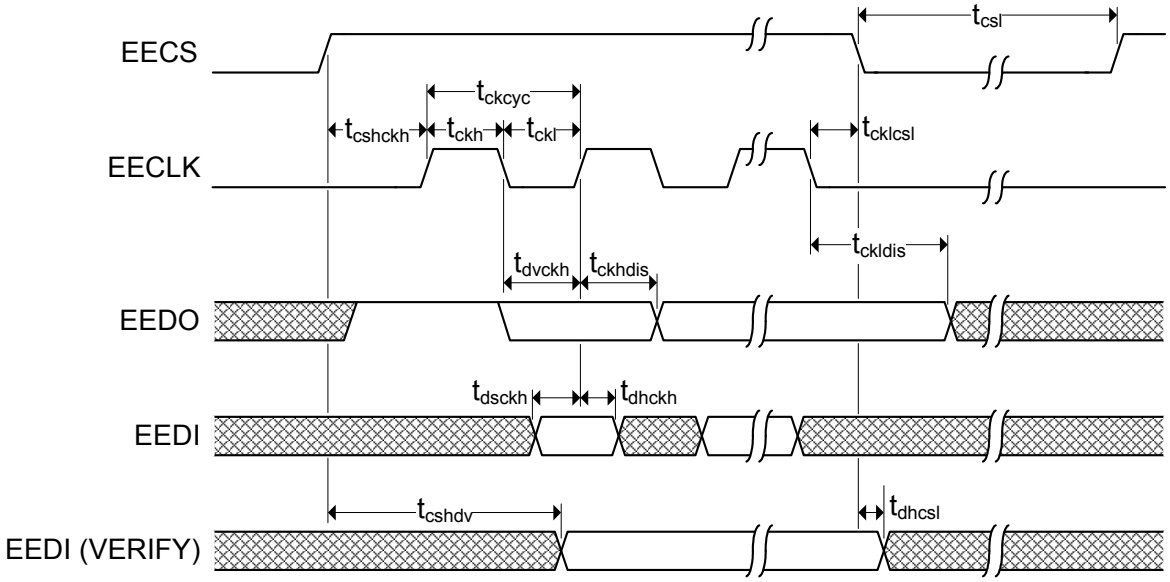


Figure 15.10 Microwire Timing

Table 15.14 Microwire Timing Values

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ckcyc}	EECLK cycle time	1110		1130	nS
t_{ckh}	EECLK high time	550		570	nS
t_{ckl}	EECLK low time	550		570	nS
t_{cshckh}	EECS high before rising edge of EECLK	1070			nS
t_{cklcsl}	EECLK falling edge to EECS low	30			nS
t_{dvckh}	EEDO valid before rising edge of EECLK	550			nS
t_{ckhdis}	EEDO disable after rising edge of EECLK	550			nS
t_{dsckh}	EEDI setup to rising edge of EECLK	90			nS
t_{dhckh}	EEDI hold after rising edge of EECLK	0			nS
t_{ckldis}	EECLK low to EEDO data disable	580			nS
t_{cshdv}	EEDI valid after EECS high (VERIFY)			600	nS
t_{dhcsl}	EEDI hold after EECS low (VERIFY)	0			nS
t_{csl}	EECS low	1070			nS

15.6 Clock Circuit

The LAN9312 can accept either a 25MHz crystal (preferred) or a 25MHz single-ended clock oscillator (+/- 50ppm) input. If the single-ended clock oscillator method is implemented, XO should be left unconnected and XI should be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XI/XO). See Table 15.15 for crystal specifications.

Table 15.15 LAN9312Crystal Specifications

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Crystal Cut			AT, typ			
Crystal Oscillation Mode			Fundamental Mode			
Crystal Calibration Mode			Parallel Resonant Mode			
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25°C	F_{tol}	-	-	+/-50	PPM	Note 15.11
Frequency Stability Over Temp	F_{temp}	-	-	+/-50	PPM	Note 15.11
Frequency Deviation Over Time	F_{age}	-	+/-3 to 5	-	PPM	Note 15.12
Total Allowable PPM Budget		-	-	+/-50	PPM	Note 15.13
Shunt Capacitance	C_O	-	7 typ	-	pF	
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	300	-	-	uW	
Equivalent Series Resistance	R_1	-	-	50	Ohm	
Operating Temperature Range		0	-	+70	°C	
n/a XI Pin Capacitance		-	3 typ	-	pF	Note 15.14
n/a XO Pin Capacitance		-	3 typ	-	pF	Note 15.14

Note 15.11 The maximum allowable values for Frequency Tolerance and Frequency Stability are application dependant. Since any particular application must meet the IEEE +/-50 PPM Total PPM Budget, the combination of these two values must be approximately +/-45 PPM (allowing for aging).

Note 15.12 Frequency Deviation Over Time is also referred to as Aging.

Note 15.13 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3 as +/- 50 PPM.

Note 15.14 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The XO/XI pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

Chapter 16 Package Outlines

16.1 128-VTQFP Package Outline

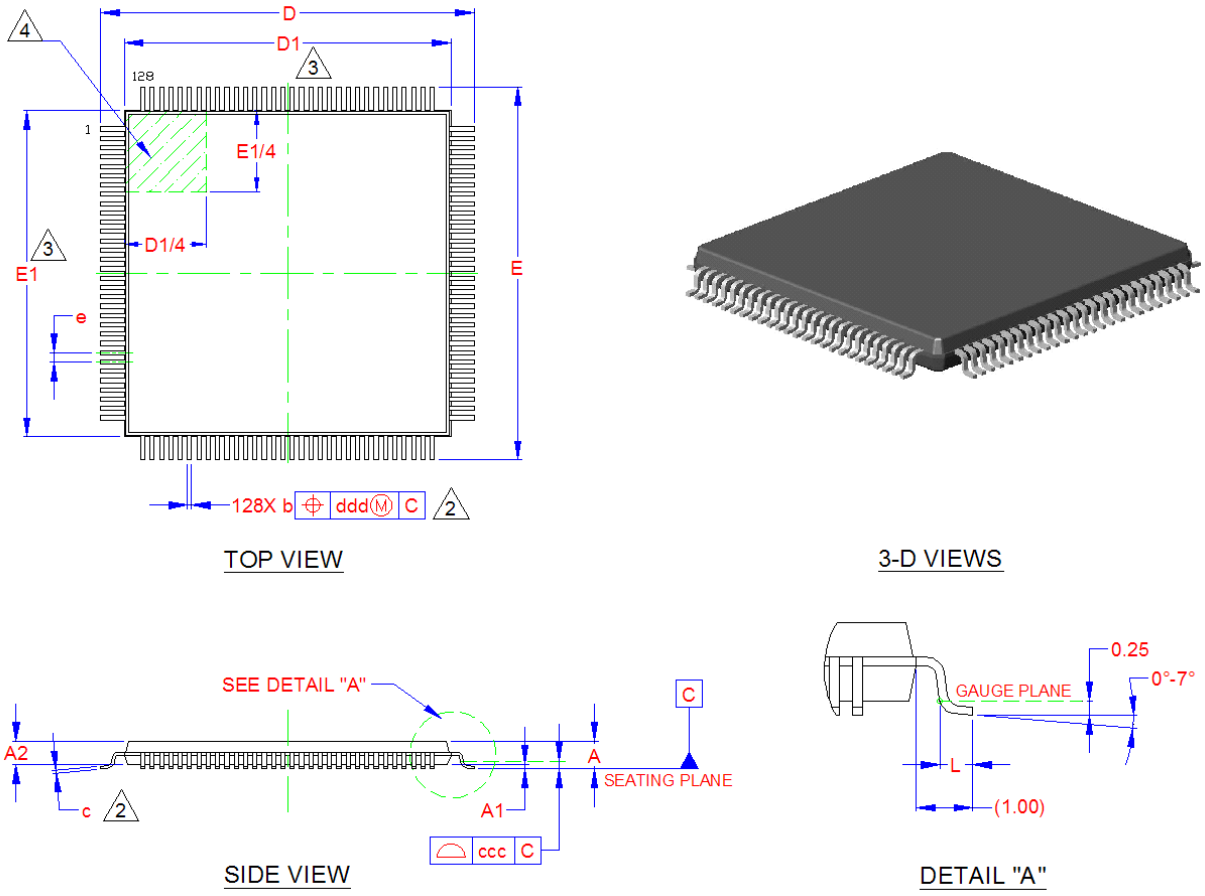


Figure 16.1 128-VTQFP Package Definition

Table 16.1 128-VTQFP Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	-	-	1.20	Overall Package Height
A1	0.05	-	0.15	Standoff
A2	0.95	1.00	1.05	Body Thickness
D/E	15.80	16.00	16.20	X/Y Span
D1/E1	13.80	14.00	14.20	X/Y Plastic Body Size
L	0.45	0.60	0.75	Lead Foot Length
b	0.13	0.18	0.23	Lead Width
c	0.09	-	0.20	Lead Foot Thickness
e		0.40 BSC		Lead Pitch
ddd	0.00	-	0.07	True Position Spread
ccc	-	-	0.08	Coplanarity

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Dimensions b & c apply to the flat section of the lead foot between 0.10 and 0.25mm from the lead tip. The base metal is exposed at the lead tip.
3. Dimensions D1 and E1 do not include mold protrusions. Maximum allowed protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. The pin 1 identifier may vary, but is always located within the zone indicated

.

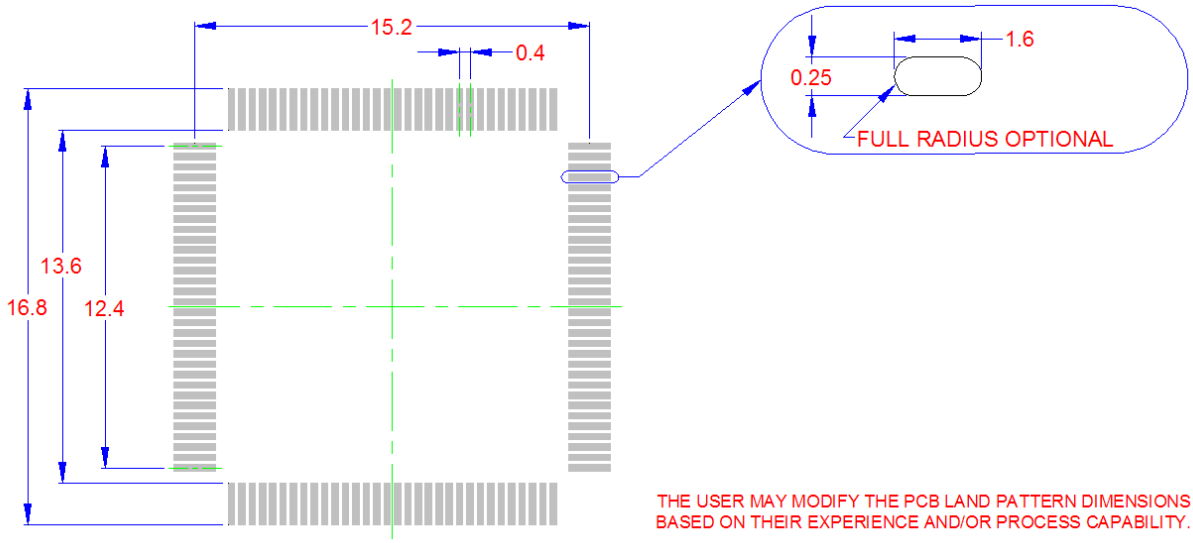


Figure 16.2 128-VTQFP Recommended PCB Land Pattern

16.2 128-XVTQFP Package Outline

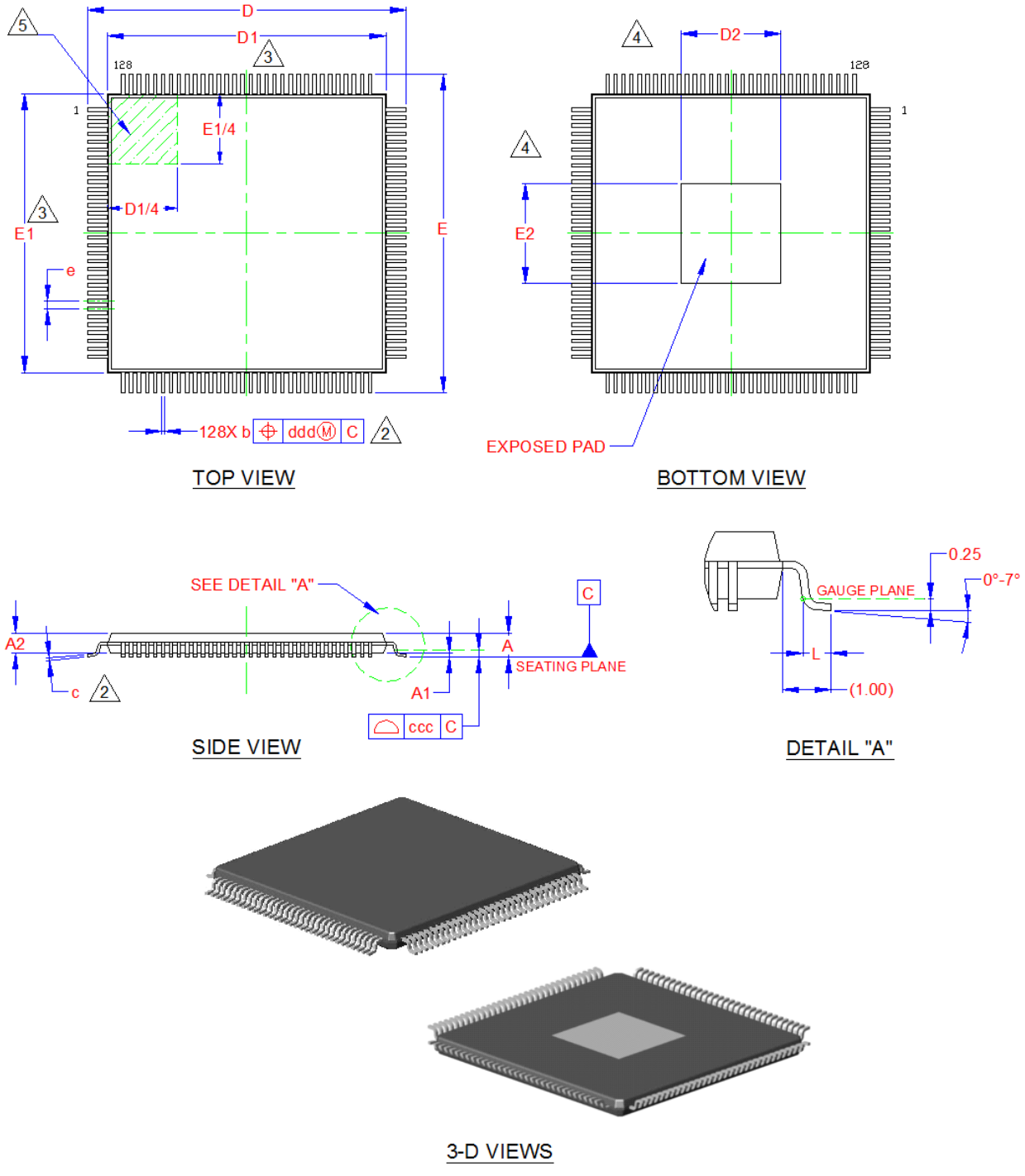


Figure 16.3 128-XVTQFP Package Definition

Table 16.2 128-XVTQFP Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	-	-	1.20	Overall Package Height
A1	0.05	-	0.15	Standoff
A2	0.95	1.00	1.05	Body Thickness
D/E	15.80	16.00	16.20	X/Y Span
D1/E1	13.80	14.00	14.20	X/Y Plastic Body Size
D2/E2	4.85	5.00	5.15	X/Y Exposed Pad Size
L	0.45	0.60	0.75	Lead Foot Length
b	0.13	0.18	0.23	Lead Width
c	0.09	-	0.20	Lead Foot Thickness
e		0.40 BSC		Lead Pitch
ddd	0.00	-	0.07	True Position Spread
ccc	-	-	0.08	Coplanarity

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Dimensions b & c apply to the flat section of the lead foot between 0.10 and 0.25mm from the lead tip. The base metal is exposed at the lead tip.
3. Dimensions D1 and E1 do not include mold protrusions. Maximum allowed protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimensions D2 and E2 represent the size of the exposed pad. The exposed pad shall be coplanar with the bottom of the package within 0.05mm.
5. The pin 1 identifier may vary, but is always located within the zone indicated

.

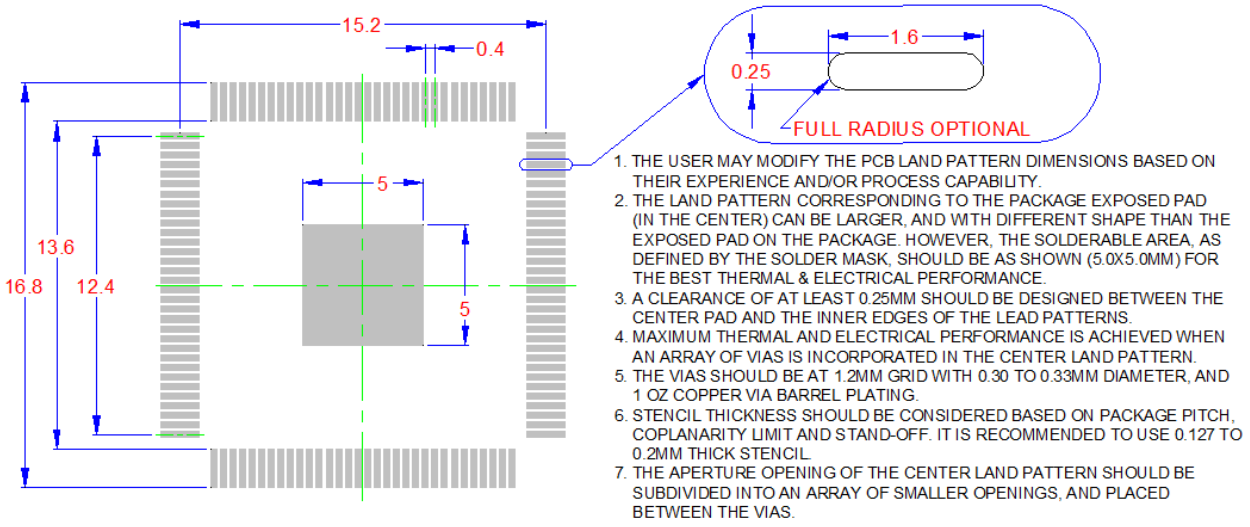


Figure 16.4 128-XVTQFP Recommended PCB Land Pattern

Chapter 17 Datasheet Revision History

Table 17.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 2.0 (02-14-13)	Chapter 3, "Pin Description and Configuration," on page 26	Changed “Refer to the LAN9312 application note for additional connection information.” to “Refer to the LAN9312 reference schematic for additional connection information.” in the VDD18TX1, VDD18TX2, VDD18PLL, VDD33IO, VDD18CORE, VDD33A1, VDD33A2, and VDD33BIAS pin descriptions.
Rev. 1.9 (03-13-12)	Order Codes	Updated ordering codes to include tape and reel options.
Rev. 1.8 (07-07-11)	Figure 16.3 128-XVTQFP Package Definition on page 457, Table 16.2, “128-XVTQFP Dimensions,” on page 458, and Figure 16.4 128-XVTQFP Recommended PCB Land Pattern on page 458	Updated 128-XVTQFP package dimensions and figures.
Rev. 1.7 (06-29-10)	Table 3.5, “EEPROM Pins,” on page 31	Added note to EE_SDA and EE_SCL pin descriptions stating “If I^2C is selected, an external pull-up is required when using an EEPROM and is recommended if no EEPROM is attached.”
	Table 3.5, “EEPROM Pins,” on page 31	Added note to EEDO/EEPROM_TYPE pin descriptions stating “When not using a Microwire or I^2C EEPROM, an external pull-down resistor is recommended on this pin.”
	Section 14.2.8.4, "Virtual PHY Identification LSB Register (VPHY_ID_LSB)," on page 251 and Section 14.4.2.4, "Port x PHY Identification LSB Register (PHY_ID_LSB_x)," on page 293	Clarified default values using binary.
	Section 14.5.2.23, "Port x MAC Transmit Configuration Register (MAC_TX_CFG_x)," on page 345	Added note to IFG Config field description: **Note:** IFG Config values less than 15 are unsupported.
	Section 14.3.6, "Host MAC MII Access Register (HMAC_MII_ACC)," on page 278	Corrected MIIBZY bit type to read only, self-clearing
	Table 6.1, “Switch Fabric Flow Control Enable Logic,” on page 59	Corrected rightmost column title to “TX FLOW CONTROL ENABLE”
	Figure 15.2 nRST Reset Pin Timing on page 445	Updated figure shading.
Rev. 1.6 (08-19-09)	All	Standard SMSC formatting applied.

Table 17.1 Customer Revision History (continued)

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.5 (10-28-08)	Section 14.2.4.1, "EEPROM Command Register (E2P_CMD)," on page 197	Corrected CFG_LOADED bit type from “RO” to “R/WC”
	Section 15.6, "Clock Circuit," on page 454	Changed max ESR value from 30 to 50 Ohms and corrected typos in operating temerpature range.
	All	Fixed various typos
Rev. 1.3 (07-03-08)	Port x PHY Special Control/Status Register (PHY_SPECIAL_CONTROL_STATUS_x) on page 307	Updated RESERVED bits 11:5 definition to “RESERVED - Write as 0000010b, ignore on read”, changed default to 0000010b, and made field R/W.
	Wake-Up Frame Detection section of Host MAC Chapter and MAC_CR register description	Added note at end of WUFF section and to the BCAST bit of the MAC_CR register stating: When wake-up frame detection is enabled via the WUEN bit of the HMAC_WUCSR register, a broadcast wake-up frame will wake-up the device despite the state of the Disable Broadcast Frames (BCAST) bit in the HMAC_CR register.
	HMAC_WUCSR register	Fixed error in GUE bit description: “....the MAC Address [1:0] bits...” changed to “...the MAC Address [0] bits....”.
	Port x PHY Auto-Negotiation Advertisement Register (PHY_AN_ADV_x) on page 294	Bits 15 and 9 made RESERVED.
	Section 15.6, "Clock Circuit," on page 454	Changed minimum drive level from 0.5mW to 300uW

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