

Features

■ Flexible Multi-Function Block (MFB) Architecture

- SuperWIDE™ logic (up to 136 inputs)
- Arithmetic capability
- Single- or Dual-port SRAM
- FIFO
- Ternary CAM

■ sysCLOCK™ PLL Timing Control

- Multiply and divide between 1 and 32
- Clock shifting capability
- External feedback capability

■ sysIO™ Interfaces

- LVCMOS 1.8, 2.5, 3.3V
 - Programmable impedance
 - Hot-socketing
 - Flexible bus-maintenance (Pull-up, pull-down, bus-keeper, or none)
 - Open drain operation
- SSTL 2, 3 (I & II)
- HSTL (I, III, IV)
- PCI 3.3
- GTL+
- LVDS
- LVPECL
- LVTTTL

■ Expanded In-System Programmability (ispXP™)

- Instant-on capability
- Single chip convenience
- In-System Programmable via IEEE 1532 Interface
- Infinitely reconfigurable via IEEE 1532 or sysCONFIG™ microprocessor interface
- Design security

■ High Speed Operation

- 4.0ns pin-to-pin delays, 300MHz f_{MAX}
- Deterministic timing

■ Low Power Consumption

- Typical static power: 20 to 50mA (1.8V), 30 to 60mA (2.5/3.3V)
- 1.8V core for low dynamic power

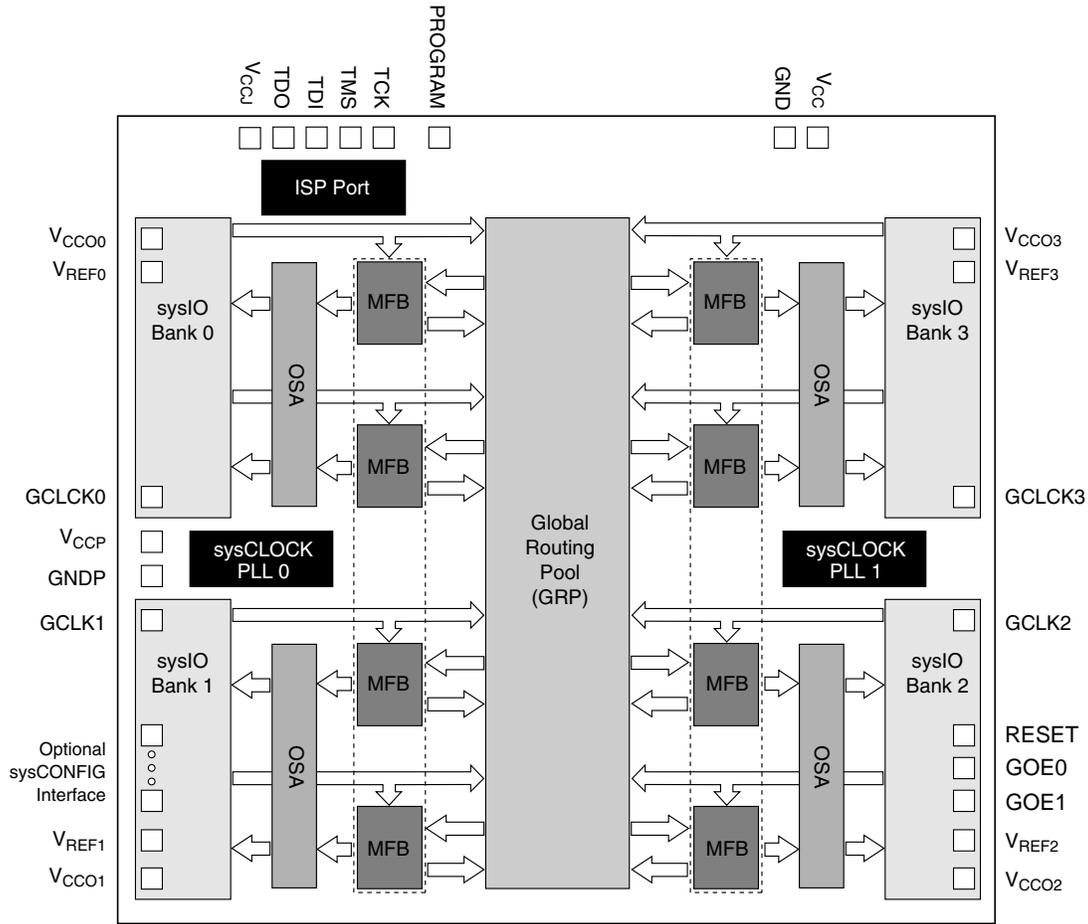
■ Easy System Integration

- 3.3V (5000MV), 2.5V (5000MB) and 1.8V (5000MC) power supply operation
- 5V tolerant I/O for LVCMOS 3.3 and LVTTTL interfaces
- IEEE 1149.1 interface for boundary scan testing
- sysIO quick configuration
- Density migration
- Multiple density and package options
- PQFP and fine pitch BGA packaging
- Lead-free package options

Table 1. ispXPLD 5000MX Family Selection Guide

	ispXPLD 5256MX	ispXPLD 5512MX	ispXPLD 5768MX	ispXPLD 51024MX
Macrocells	256	512	768	1,024
Multi-Function Blocks	8	16	24	32
Maximum RAM Bits	128K	256K	384K	512K
Maximum CAM Bits	48K	96K	144K	192K
sysCLOCK PLLs	2	2	2	2
t_{PD} (Propagation Delay)	4.0ns	4.5ns	5.0ns	5.2ns
t_S (Register Set-up Time)	2.2ns	2.8ns	2.8ns	3.0ns
t_{CO} (Register Clock to Out Time)	2.8ns	3.0ns	3.2ns	3.7ns
f_{MAX} (Maximum Operating Frequency)	300MHz	275MHz	250MHz	250MHz
System Gates	75K	150K	225K	300K
I/Os	141	149/193/253	193/317	317/381
Packages	256 fpBGA	208 PQFP 256 fpBGA 484 fpBGA	256 fpBGA 484 fpBGA	484 fpBGA 672 fpBGA

Figure 1. ispXPLD 5000MX Block Diagram



Introduction

The ispXPLD 5000MX family represents a new class of device, referred to as the eXpanded Programmable Logic Devices (XPLDs). These devices extend the capability of Lattice’s popular SuperWIDE ispMACH 5000 architecture by providing flexible memory capability. The family supports single- or dual-port SRAM, FIFO, and ternary CAM operation. Extra logic has also been included to allow efficient implementation of arithmetic functions. In addition, sysCLOCK PLLs and sysIO interfaces provide support for the system-level needs of designers.

The devices provide designers with a convenient one-chip solution that provides logic availability at boot-up, design security, and extreme reconfigurability. The use of advanced process technology provides industry-leading performance with combinatorial propagation delay as low as 4.0ns, 2.8ns clock-to-out delay, 2.2ns set-up time, and operating frequency up to 300MHz. This performance is coupled with low static and dynamic power consumption. The ispXPLD 5000MX architecture provides predictable deterministic timing.

The availability of 3.3, 2.5 and 1.8V versions of these devices along with the flexibility of the sysIO interface helps users meet the challenge of today’s mixed voltage designs. Inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. Boundary scan testability further eases integration into today’s complex systems. A variety of density and package options increase the likelihood of a good fit for a particular application. Table 1 shows the members of the ispXPLD 5000MX family.

Architecture

The ispXPLD 5000MX devices consist of Multi-Function Blocks (MFBs) interconnected with a Global Routing Pool. Signals enter and leave the device via one of four sysIO banks. Figure 1 shows the block diagram of the ispXPLD

5000MX. Incoming signals may connect to the global routing pool or the registers in the MFBs. An Output Sharing Array (OSA) increases the number of I/O available to each MFB, allowing a complete function high-performance access to the I/O. There are four clock pins that drive four global clock nets within the device. Two sysCLOCK PLLs are provided to allow the synthesis of new clocks and control of clock skews.

Multi-Function Block (MFB)

Each MFB in the ispXPLD 5000MX architecture can be configured in one of the six following modes. This provides a flexible approach to implementing logic and memory that allows the designer to achieve the mix of functions that are required for a particular design, maximizing resource utilization. The six modes supported by the MFB are:

- SuperWIDE Logic Mode
- True Dual-port SRAM Mode
- Pseudo Dual-port SRAM Mode
- Single-port SRAM Mode
- FIFO Mode
- Ternary CAM Mode

The MFB consists of a multi-function array and associated routing. Depending on the chosen functions the multi-function array uses up to 68 inputs from the GRP and the four global clock and reset signals. The array outputs data along with certain control functions to the macrocells. Output signals can be routed internally for use elsewhere in the device and to the sysIO banks for output. Figure 2 shows the block diagram of the MFB. The various configurations are described in more detail in the following sections.

Figure 2. MFB Block Diagram

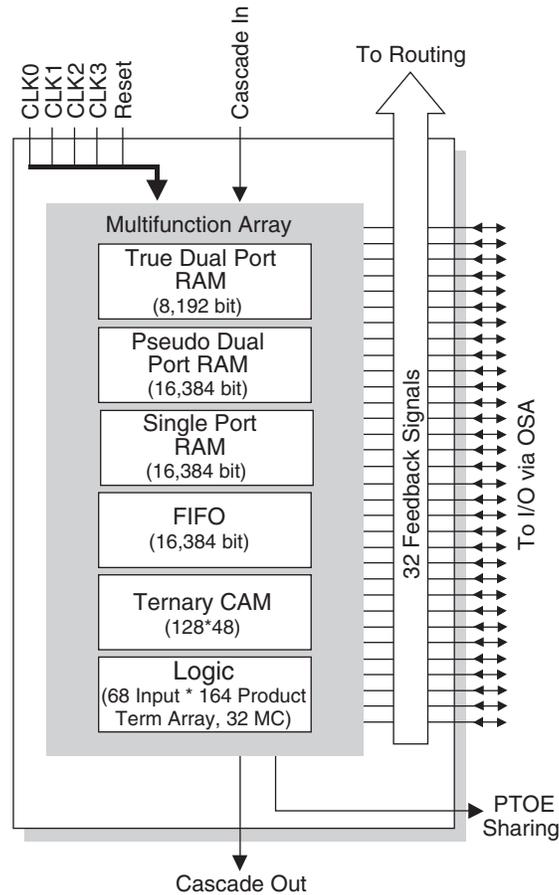


Table 12. ispXPLD 5000MX Supported I/O Standards

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal V_{TT}
LVTTL	3.3V	N/A	N/A
LVC MOS-3.3	3.3V	N/A	N/A
LVC MOS-2.5	2.5V	N/A	N/A
LVC MOS-1.8	1.8V	N/A	N/A
PCI 3.3V	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	0.75V
HSTL, Class IV	1.5V	0.9V	0.75V
GTL+	N/A	1.0V	1.5V
LVPECL, Differential	2.5V, 3.3V	N/A	N/A
LVDS	2.5V, 3.3V	N/A	N/A

Table 13. Differential Interface Standard Support¹

		sysIO Buffer
LVDS	Driver	Supported
	Receiver	Supported with standard termination
LVPECL	Driver	Supported with external resistor network
	Receiver	Supported with termination

Control, Clock, sysCONFIG and JTAG Signals

Global clock pins support the same sysIO standards as general purpose I/O. When required the V_{REF} signal is derived from the adjacent bank. When differential standards are supported two adjacent clock pins are paired to form the input. The TOE, PROGRAM, CFG0 and DONE pins of the ispXPLD 5000MX device are the only pins that do not have sysIO capabilities. The JTAG TAP pins support only LVC MOS 3.3, 2.5 and 1.8V standards. The voltage is controlled by V_{CCJ} . These pins only support the LVTTL and LVC MOS standards applicable to the power supply voltage of the device. The global reset global output enable pins are associated with Bank 2 and support all of the sysIO standards.

Hotsocketing

The I/O on the ispXPLD 5000MX devices are well suited for those applications that require hot socketing capability, when configured as LVC MOS or LVTTL. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Programmable Drive Strength

The drive strength of I/Os that are programmed as LVC MOS is tightly controlled and can be programmed to a variety of different values. Thus the impedance an output driver can be closely match to the characteristic impedance of the line it is driving. This allows users to eliminate the need for external series termination resistors.

Absolute Maximum Ratings^{1, 2, 3}

	ispXPLD 5000MC 1.8V	ispXPLD 5000MB/V 2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied ^{4, 5}	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied . . .	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to ($V_{IHMAX} + 2$) volts not to exceed 6V is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with $V_{IN} > 3.6V$ is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices (ispXPLD 5000MC)	1.65	1.95	V
	Supply Voltage for 2.5V Devices (ispXPLD 5000MB)	2.3	2.7	V
	Supply Voltage for 3.3V Devices (ispXPLD 5000MV)	3	3.6	V
V_{CCP}	PLL Block Supply Voltage for PLL 1.8V Devices	1.65	1.95	V
	PLL Block Supply Voltage for PLL 2.5V Devices	2.3	2.7	V
	PLL Block Supply Voltage for PLL 3.3V Devices	3	3.6	V
T_J	Junction Temperature (Commercial Operation)	0	90	C
	Junction Temperature (Industrial Operation)	-40	105	C

E²CMOS Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle ¹	1,000	—	Cycles

1. Valid over commercial temperature range.

Hot Socketing Characteristics^{1, 2, 3, 4}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V$	—	+/-50	+/-800	μA

1. Insensitive to sequence of V_{CC} and V_{CCO} when $V_{CCO} \leq 1.0V$. For $V_{CCO} > 1.0V$, V_{CC} min must be present. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO} , provided $(V_{IN} - V_{CCO}) \leq 3.6V$.
2. $0 \leq V_{CC} \leq V_{CC} (MAX)$, $0 \leq V_{CCO} \leq V_{CCO} (MAX)$
3. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} . Device defaults to pull-up until non-volatile cells are active.
4. LVTTTL, LVCMOS only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}^1	Input or I/O Leakage	$0 \leq V_{IN} \leq (V_{CCO} - 0.2V)$	—	—	10	μA
		$(V_{CCO} - 0.2V) < V_{IN} \leq 3.6V$	—	—	40	μA
I_{IH}^4	Input High Leakage Current	$3.6V < V_{IN} \leq 5.5V$ and $3.0V \leq V_{CCO} \leq 3.6V$	—	—	3	mA
I_{PU}^3	I/O Active Pullup Current	$0 \leq V_{IN} \leq 0.7 V_{CCO}$	-30	—	-150	μA
I_{PD}	I/O Active Pulldown Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$	30	—	150	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCO}$	30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	μA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	μA
V_{BHT}	Bus Hold Trip Points	$0 \leq V_{IN} \leq V_{IH} (MAX)$	$V_{CCO} * 0.35$	—	$V_{CCO} * 0.65$	μA
C1	I/O Capacitance ²	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—	8	—	pf
C2	Clock Capacitance ²	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—	8	—	pf
C3	Global Input Capacitance ²	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T_A 25°C, $f=1.0MHz$

3. I_{PU} on JTAG pins has a maximum of -175 μA for 5512MX devices.

4. 5V tolerant inputs and I/Os should be placed in banks where $3.0V \leq V_{CCO} \leq 3.6V$. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.

Supply Current

Symbol	Parameter	Condition	Min.	Typ. ³	Max.	Units
ispXPLD 5256						
$I_{CC}^{1,2}$	Operating Power Supply Current	$V_{CC} = 3.3V, f = 1.0MHz$	—	26	—	mA
		$V_{CC} = 2.5V, f = 1.0MHz$	—	26	—	mA
		$V_{CC} = 1.8V, f = 1.0MHz$	—	16	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	$V_{CCO} = 3.3V, f = 1.0MHz, \text{ unloaded}$	—	4	—	mA
		$V_{CCO} = 2.5V, f = 1.0MHz, \text{ unloaded}$	—	4	—	mA
		$V_{CCO} = 1.8V, f = 1.0MHz, \text{ unloaded}$	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	$V_{CCP} = 3.3V, f = 10MHz$	—	11	—	mA
		$V_{CCP} = 2.5V, f = 10MHz$	—	11	—	mA
		$V_{CCP} = 1.8V, f = 10MHz$	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	$V_{CCJ} = 3.3V$	—	1	—	mA
		$V_{CCJ} = 2.5V$	—	1	—	mA
		$V_{CCJ} = 1.8V$	—	1	—	mA
ispXPLD 5512						
$I_{CC}^{1,2}$	Operating Power Supply Current	$V_{CC} = 3.3V, f = 1.0MHz$	—	33	—	mA
		$V_{CC} = 2.5V, f = 1.0MHz$	—	33	—	mA
		$V_{CC} = 1.8V, f = 1.0MHz$	—	22	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	$V_{CCO} = 3.3V, f = 1.0MHz, \text{ unloaded}$	—	4	—	mA
		$V_{CCO} = 2.5V, f = 1.0MHz, \text{ unloaded}$	—	4	—	mA
		$V_{CCO} = 1.8V, f = 1.0MHz, \text{ unloaded}$	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	$V_{CCP} = 3.3V, f = 10MHz$	—	11	—	mA
		$V_{CCP} = 2.5V, f = 10MHz$	—	11	—	mA
		$V_{CCP} = 1.8V, f = 10MHz$	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	$V_{CCJ} = 3.3V$	—	1	—	mA
		$V_{CCJ} = 2.5V$	—	1	—	mA
		$V_{CCJ} = 1.8V$	—	1	—	mA
ispXPLD 5768						
$I_{CC}^{1,2}$	Operating Power Supply Current	$V_{CC} = 3.3V, f = 1.0MHz$	—	40	—	mA
		$V_{CC} = 2.5V, f = 1.0MHz$	—	40	—	mA
		$V_{CC} = 1.8V, f = 1.0MHz$	—	30	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	$V_{CCO} = 3.3V, f = 1.0MHz, \text{ unloaded}$	—	4	—	mA
		$V_{CCO} = 2.5V, f = 1.0MHz, \text{ unloaded}$	—	4	—	mA
		$V_{CCO} = 1.8V, f = 1.0MHz, \text{ unloaded}$	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	$V_{CCP} = 3.3V, f = 10MHz$	—	11	—	mA
		$V_{CCP} = 2.5V, f = 10MHz$	—	11	—	mA
		$V_{CCP} = 1.8V, f = 10MHz$	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	$V_{CCJ} = 3.3V$	—	1	—	mA
		$V_{CCJ} = 2.5V$	—	1	—	mA
		$V_{CCJ} = 1.8V$	—	1	—	mA

ispXPLD 5000MX Family External Switching Characteristics^{1, 2, 3}

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.									
t _{PD}	Data Propagation Delay, 5-PT Bypass	—	4.0	—	4.5	—	5.0	—	5.2	—	7.5	ns
t _{PD_PTSA}	Data propagation delay	—	4.8	—	5.7	—	6.0	—	6.5	—	9.5	ns
t _S	MFB Register Setup Time Before Clock, 5-PT Bypass	2.2	—	2.8	—	2.8	—	3.0	—	4.5	—	ns
t _{S_PTSA}	MFB Register Setup Time Before Clock	2.5	—	3.1	—	3.1	—	3.6	—	5.5	—	ns
t _{SIR}	MFB Register Setup Time Before Clock, Input Register Path	1.0	—	1.0	—	1.0	—	0.5	—	1.7	—	ns
t _H	MFB Register Hold Time Before Clock, 5-PT Bypass	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t _{H_PTSA}	MFB Register Hold Time Before Clock	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t _{HIR}	MFB Register Hold Time Before Clock, Input Register Path	0.5	—	0.5	—	0.5	—	1.0	—	1.3	—	ns
t _{CO}	MFB Register Clock-to-Out-put Delay	—	2.8	—	3.0	—	3.2	—	3.7	—	5.0	ns
t _R	External Reset Pin to Output Delay	—	4.0	—	4.5	—	5.0	—	5.0	—	7.5	ns
t _{RW}	Reset Pulse Duration	1.8	—	1.8	—	1.8	—	2.0	—	3.0	—	ns
t _{LPTOE/DIS}	Input to Output Local Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
t _{SPTOE/DIS}	Input to Output Shared Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
t _{GOE/DIS}	Global OE Input to Output Enable/Disable	—	4.5	—	5.5	—	5.5	—	6.5	—	7.5	ns
t _{CW}	Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t _{GW}	Gate Width Low (for Low Transparent) or High (for High Transparent)	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t _{WIR}	Input Register Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t _{SKEW}	Clock-to-Out Skew, Block Level	—	0.6	—	0.6	—	0.6	—	0.6	—	1.0	ns
f _{MAX} ⁴	Clock Frequency with Internal Feedback	—	300	—	275	—	250	—	250	—	150	MHz
f _{MAX} (Ext.)	Clock Frequency with External Feedback, 1/ (t _S + t _{CO})	—	200	—	171	—	166	—	149	—	105	MHz
f _{MAX} (Tog.)	Clock Frequency Max. Toggle	—	333	—	333	—	333	—	277	—	200	MHz
f _{MAX} (CAMC) ⁵	Clock Frequency to CAM (Configure Mode)	—	280	—	280	—	230	—	230	—	168	MHz
f _{MAX} (CAM) ⁵	Clock Frequency to CAM (Compare Mode)	—	150	—	150	—	150	—	135	—	90	MHz

ispXPLD 5000MX Family External Switching Characteristics (Continued)^{1, 2, 3}

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.									
f_{MAX} (RAM) ⁵	Clock Frequency to RAM in:											
	Single Port Mode	—	155	—	155	—	155	—	155	—	93	MHz
	Dual Port Mode	—	155	—	155	—	155	—	155	—	93	MHz
	Pseudo Dual Port Mode	—	180	—	180	—	160	—	160	—	106	MHz
f_{MAX} (FIFO) ⁵	Clock Frequency to FIFO	—	225	—	220	—	210	—	210	—	132	MHz
t_{PWR_ON}	Power-on Time	—	200	—	200	—	200	—	200	—	200	μ s

Timing v.1.8

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.
5. CAM, FIFO, RAM f_{MAX} specification used shared PT Clk.

ispXPLD 5000MX Family Internal Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.									
In/Out Delays													
t _{IN}	Input Buffer Delay	—	—	0.70	—	0.91	—	0.96	—	1.11	—	1.30	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	—	0.40	—	0.35	—	0.35	—	0.35	—	0.55	ns
t _{RST}	Global RESET Pin Delay	—	—	3.77	—	4.24	—	4.71	—	4.71	—	7.07	ns
t _{GOE}	Global OE Pin Delay	—	—	1.98	—	2.66	—	2.34	—	2.87	—	3.27	ns
t _{BUF}	Delay through Output Buffer	—	—	1.16	—	1.30	—	1.45	—	1.60	—	2.17	ns
t _{EN}	Output Enable Time	—	—	2.52	—	2.84	—	3.16	—	3.63	—	4.23	ns
t _{DIS}	Output Disable Time	—	—	1.92	—	2.40	—	2.40	—	2.40	—	3.60	ns
Routing Delays													
t _{ROUTE}	Delay through SRP	—	—	1.95	—	2.06	—	2.34	—	2.24	—	3.66	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	—	0.60	—	0.60	—	0.60	—	0.47	—	1.63	ns
t _{PTSA}	Product Term Sharing Array Delay	—	—	0.50	—	0.50	—	0.53	—	0.83	—	1.34	ns
t _{FBK}	Internal Feedback Delay	—	—	0.19	—	0.02	—	0.39	—	0.03	—	0.60	ns
t _{GCLK}	Global Clock Tree Delay	—	—	0.52	—	0.32	—	0.72	—	0.82	—	0.78	ns
t _{BCLK}	Block PT Clock Delay	—	—	0.12	—	0.14	—	0.15	—	0.15	—	0.23	ns
t _{PTCLK}	Macrocell PT Clock Delay	—	—	0.12	—	0.14	—	0.15	—	0.15	—	0.23	ns
t _{PLL_DELAY}	Programmable PLL Delay Increment	—	—	0.30	—	0.30	—	0.30	—	0.30	—	0.30	ns
t _{BSR}	Block PT Reset Delay	—	—	0.72	—	0.81	—	0.90	—	0.94	—	1.35	ns
t _{PTSR}	Macrocell PT Set/Reset Delay	—	—	0.60	—	0.75	—	0.75	—	0.75	—	1.13	ns
t _{LPTOE}	Macrocell PT OE Delay	—	—	0.83	—	1.19	—	1.04	—	1.52	—	1.31	ns
t _{SPTOE}	Segment PT OE Delay	—	—	0.83	—	1.19	—	1.04	—	1.52	—	1.31	ns
t _{OSA}	Output Sharing Array Delay	—	—	0.80	—	0.90	—	1.00	—	1.00	—	1.50	ns
t _{PTOE}	Global PT OE Delay	—	—	0.83	—	1.04	—	1.04	—	1.04	—	1.56	ns
t _{PDB}	5-PT Bypass Propagation Delay	—	—	0.20	—	0.23	—	0.25	—	0.25	—	0.38	ns
t _{PDI}	Macrocell Propagation Delay	—	—	0.50	—	0.93	—	0.72	—	0.72	—	1.04	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.									
Registered Delays													
t _S	D-Register Setup Time, Global Clock	—	0.28	—	0.31	—	0.35	—	0.55	—	0.52	—	ns
t _{S_PT}	D-Register Setup Time, PT Clock	—	-0.13	—	-0.11	—	-0.10	—	-0.10	—	-0.07	—	ns
t _H	D-Register Hold Time	—	1.90	—	2.56	—	2.50	—	2.40	—	4.00	—	ns
t _{COi}	Register Clock to OSA Time	—	—	0.72	—	1.03	—	0.68	—	0.93	—	1.50	ns
t _{CESi}	Clock Enable Setup Time	—	1.07	—	1.20	—	1.33	—	1.33	—	2.00	—	ns
t _{CEHi}	Clock Enable Hold Time	—	0.00	—	0.00	—	0.00	—	0.00	—	0.00	—	ns
t _{SIR}	D-Input Register Setup Time, Global Clock	—	0.66	—	0.20	—	0.53	—	0.12	—	0.08	—	ns
t _{SIR_PT}	D-Input Register Setup Time, PT Clock	—	0.42	—	0.37	—	0.34	—	0.34	—	0.22	—	ns
t _{HIR}	D-Input Register Hold Time, Global Clock	—	0.84	—	1.31	—	1.01	—	1.41	—	2.91	—	ns
t _{HIR_PT}	D-Input Register Hold Time, PT Clock	—	0.00	—	0.00	—	0.00	—	0.00	—	0.00	—	ns
Latched Delays													
t _{SL}	Latch Setup Time, Global Clock	—	0.18	—	0.00	—	0.00	—	0.00	—	0.00	—	ns
t _{SL_PT}	Latch Setup Time, PT Clock	—	0.18	—	0.00	—	0.00	—	0.00	—	0.34	—	ns
t _{HL}	Latch Hold Time	—	-0.06	—	0.00	—	0.00	—	0.00	—	-0.03	—	ns
t _{GOi}	Latch Gate to OSA Time	—	—	0.07	—	0.08	—	0.08	—	0.08	—	0.13	ns
t _{PDLi}	Propagation Delay through Latch to OSA Transparent	—	—	0.52	—	0.58	—	0.65	—	0.65	—	0.97	ns
Reset and Set Delays													
t _{SRI}	Asynchronous Reset or Set to OSA Delay	—	—	0.23	—	0.26	—	0.29	—	0.29	—	0.43	ns
t _{SRR}	Asynchronous Reset or Set Recovery	—	—	0.42	—	0.47	—	0.53	—	0.55	—	0.79	ns
eXtended Function Routing Delays													
t _{ROUEMF}	Delay through SRP when Implementing Memory Functions	—	—	2.00	—	2.25	—	2.51	—	2.61	—	3.76	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{CASC}	Additional Delay for PT Cascading between MFBs	—	—	0.71	—	0.80	—	0.89	—	0.92	—	1.33	ns
t _{CICOMFB}	Carry Chain Delay, MFB to MFB	—	—	0.35	—	0.39	—	0.44	—	0.46	—	0.66	ns
t _{CICOMC}	Carry Chain Delay, Macro-Cell to Macro-Cell	—	—	0.10	—	0.11	—	0.13	—	0.13	—	0.19	ns
t _{FLAG}	Routing Delay for Extended Function Flags	—	—	2.62	—	2.94	—	3.27	—	3.40	—	4.91	ns
t _{FLAGEXP}	Additional Flag Delay when Expanding Data Widths	t _{FLAGFULL} , t _{FLAGAFULL} , t _{FLAGEMPTY} , t _{FLAGAEMPTY}	—	2.57	—	2.89	—	3.21	—	3.34	—	4.82	ns
t _{SUM}	Counter Sum Delay	t _{PTSA}	—	0.80	—	0.90	—	1.00	—	1.04	—	1.50	ns
Optional Adjusters													
t _{BLA}	Block Loading Adder	t _{ROUTE}	—	0.04	—	0.04	—	0.05	—	0.05	—	0.07	ns
t _{EXP}	PT Expander Adder	t _{ROUTE}	—	0.53	—	0.60	—	0.66	—	0.69	—	0.99	ns
t _{INDIO}	Additional Delay for the Input Register	t _{INREG}	—	0.50	—	0.56	—	0.63	—	0.65	—	0.94	ns
t _{PLL_SEC_DELAY}	Secondary PLL Output Delay	t _{PLL_DELAY}	—	0.91	—	0.91	—	0.91	—	0.91	—	0.91	ns
t _{INEXP}	MFB Input Extender	t _{ROUTE}	—	0.62	—	0.70	—	0.78	—	0.81	—	1.16	ns
Input and Output Buffer Delays													
t _{IOI}	Input Buffer Selection Adder	t _{GCLK_IN} , t _{IN} , t _{GOE} , t _{RST}	Refer to sysIO Adjuster Tables										ns
t _{IOO}	Output Buffer Selection Adder	t _{BUF}	Refer to sysIO Adjuster Tables										ns
FIFO													
t _{FIFOWCLKS}	Write Data Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{FIFOWCLKH}	Write Data Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{FIFOCLKSKEW}	Opposite Clock Cycle Delay	—	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83	ns
t _{FIFOFULL}	Write Clock to Full Flag Delay	—	—	3.08	—	3.08	—	3.85	—	3.85	—	4.00	ns
t _{FIFOAFULL}	Write Clock to Almost Full Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns
t _{FIFOEMPTY}	Read Clock to Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns
t _{FIFOAEMPTY}	Read Clock to Almost Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.									
t _{FIFOWES}	Write-Enable setup before Write Clock	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
t _{FIFOWEH}	Write-Enable hold after Write Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
t _{FIFORES}	Read-Enable setup before Read Clock	—	2.69	—	2.35	—	2.79	—	2.38	—	4.14	—	ns
t _{FIFOREH}	Read-Enable hold after Read Clock	—	-3.17	—	-3.17	—	-2.53	—	-2.53	—	-2.44	—	ns
t _{FIFORSTO}	Reset to Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
t _{FIFORSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
t _{FIFORSTPW}	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
t _{FIFORCLKO}	Read Clock to FIFO Out Delay	—	—	3.73	—	3.73	—	4.66	—	4.66	—	4.84	ns
CAM – Update Mode													
t _{CAMMSS}	Memory Select Setup before CLK	—	1.40	—	0.70	—	1.50	—	1.40	—	1.44	—	ns
t _{CAMMSH}	Memory Select Hold after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMENMSKS}	Enable Mask Register Setup Time before CLK	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMENMSKH}	Enable Mask Register Setup Time after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMADDS}	Address Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMADDH}	Address Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMDATAS}	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
t _{CAMDATAH}	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMDACS}	“Don’t Care” Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMDACH}	“Don’t Care” Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMRWS}	R/W Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMRWH}	R/W Enable Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMCES}	Clock Enable Setup Time before Clock	—	1.55	—	1.55	—	1.94	—	1.94	—	2.02	—	ns
t _{CAMCEH}	Clock Enable Hold Time after Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.									
t _{CAMWMSKS}	Write Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMWMSKH}	Write Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMRSTO}	Reset to CAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
t _{CAMRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
t _{CAMRSTPW}	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
CAM – Compare Mode													
t _{CAMDATAS}	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
t _{CAMDATAH}	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMENMSKS}	Enable Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMENMSKH}	Enable Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMCASC}	CAM Width Expansion Delay	—	—	0.40	—	0.40	—	0.50	—	0.50	—	0.51	ns
t _{CAMCO}	Clock to Output (Address Out) Delay	—	—	6.19	—	6.13	—	6.81	—	6.61	—	9.63	ns
t _{CAMMATCH}	Clock to Match Flag Delay	—	—	6.19	—	6.13	—	6.07	—	6.61	—	10.22	ns
t _{CAMMMATCH}	Clock to Multi-Match Flag Delay	—	—	5.50	—	5.50	—	6.38	—	6.38	—	7.72	ns
t _{CAMRSTFLAG}	CAM Reset to Flags Delay	—	—	3.16	—	3.16	—	3.95	—	3.95	—	4.11	ns
Single Port RAM													
t _{SPADDDATA}	Address to Data Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	7.76	ns
t _{SPMSS}	Memory Select Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{SPMSH}	Memory Select Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{SPCES}	Clock Enable Setup before Clock Time	—	2.30	—	2.30	—	2.30	—	2.30	—	9.80	—	ns
t _{SPCEH}	Clock Enable Hold time after Clock Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
t _{SPADDS}	Address Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.									
t _{SPADDH}	Address Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{SPRWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{SPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{SPDATAS}	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{SPDATAH}	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{SPCLKO}	Clock to Output Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	9.86	ns
t _{SPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—	4.29	ns
t _{SPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56	—	ns
t _{SPRSTPW}	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19	—	ns
Pseudo Dual Port RAM													
t _{PDPMSS}	Memory Select Setup Before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{PDPMSH}	Memory Select Hold time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{PDPRCES}	Clock Enable Setup before Read Clock Time	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
t _{PDPRCEH}	Clock Enable Hold time after Read Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
t _{PDPWCES}	Clock Enable Setup before Write Clock Time	—	1.87	—	1.87	—	2.34	—	2.34	—	2.43	—	ns
t _{PDPWCEH}	Clock Enable Hold time after Write Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
t _{PDPRADDS}	Read Address Setup before Read Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{PDPRADDH}	Read Address Hold after Read Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{PDPWADDS}	Write Address Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{PDPWADDH}	Write Address Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{PDPRW}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.									
t _{PDPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{PDPDATAS}	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{PDPDATAH}	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{PDPRCLKO}	Read Clock to Output Delay	—	—	5.08	—	5.02	—	5.66	—	5.45	—	8.54	ns
t _{PDPCCLKSKEW}	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83	—	ns
t _{PDPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
t _{PDPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
t _{PDPRSTPW}	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
Dual Port RAM													
t _{DPMSAS}	Memory Select A Setup Before R/W A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{DPMSAH}	Memory Select Hold time after R/W A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{DPCEAS}	Clock Enable A Setup before Clock A Time	—	3.72	—	3.72	—	3.72	—	3.72	—	4.84	—	ns
t _{DPCEAH}	Clock Enable A Hold time after Clock A Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
t _{DPADDAS}	Address A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{DPADDAH}	Address A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{DPRWAS}	R/W A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{DPRWAH}	R/W A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{DPDATAAS}	Write Data A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{DPDATAAH}	Write Data A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{DPMSBS}	Memory Select B Setup Before R/W B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{DPMSBH}	Memory Select Hold time after R/W B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.									
t _{DPCEBS}	Clock Enable B Setup before Clock B Time	—	2.33	—	2.33	—	2.33	—	2.33	—	3.03	—	ns
t _{DPCEBH}	Clock Enable Hold B after Clock B Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
t _{DPADDBS}	Address B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{DPADDBH}	Address B Hold time after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{DPRWBS}	R/W B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{DPRWBH}	R/W B Hold time after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{DPDATABS}	Write Data B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{DPDATABH}	Write Data B Hold after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{DPCLKAO}	Read Clock A to Output Delay	—	—	5.97	—	5.92	—	5.86	—	5.65	—	9.86	ns
t _{DPCLKBO}	Read Clock B to Output Delay	—	—	5.16	—	5.16	—	5.16	—	5.16	—	6.71	ns
t _{DPCLKSKEW}	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.40	—	1.40	—	1.83	—	ns
t _{DPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—	4.29	ns
t _{DPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56	—	ns
t _{DPRSTPW}	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19	—	ns

Timing v.1.8

1. The PT-delay to clock of RAM/FIFO/CAM should be t_{BCLK} instead of t_{PTCLK}.
2. The PT-delay to set/reset of RAM/FIFO/CAM should be t_{BSR} instead of t_{PTSR}.

ispXPLD 5000MB (2.5V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t _{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-4FN256C	256	2.5	4.0	Lead-free fpBGA	256	141	C
	LC5256MB-5FN256C	256	2.5	5.0	Lead-free fpBGA	256	141	C
	LC5256MB-75FN256C	256	2.5	7.5	Lead-free fpBGA	256	141	C
LC5512MB	LC5512MB-45QN208C	512	2.5	4.5	Lead-free PQFP	208	149	C
	LC5512MB-75QN208C	512	2.5	7.5	Lead-free PQFP	208	149	C
	LC5512MB-45FN256C	512	2.5	4.5	Lead-free fpBGA	256	193	C
	LC5512MB-75FN256C	512	2.5	7.5	Lead-free fpBGA	256	193	C
	LC5512MB-45FN484C	512	2.5	4.5	Lead-free fpBGA	484	253	C
	LC5512MB-75FN484C	512	2.5	7.5	Lead-free fpBGA	484	253	C
LC5768MB	LC5768MB-5FN256C	768	2.5	5.0	Lead-free fpBGA	256	193	C
	LC5768MB-75FN256C	768	2.5	7.5	Lead-free fpBGA	256	193	C
	LC5768MB-5FN484C	768	2.5	5.0	Lead-free fpBGA	484	317	C
	LC5768MB-75FN484C	768	2.5	7.5	Lead-free fpBGA	484	317	C
LC51024MB	LC51024MB-52FN484C	1024	2.5	5.2	Lead-free fpBGA	484	317	C
	LC51024MB-75FN484C	1024	2.5	7.5	Lead-free fpBGA	484	317	C
	LC51024MB-52FN672C	1024	2.5	5.2	Lead-free fpBGA	672	381	C
	LC51024MB-75FN672C	1024	2.5	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MB (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t _{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-5FN256I	256	2.5	5.0	Lead-free fpBGA	256	141	I
	LC5256MB-75FN256I	256	2.5	7.5	Lead-free fpBGA	256	141	I
LC5512MB	LC5512MB-75QN208I	512	2.5	7.5	Lead-free PQFP	208	149	I
	LC5512MB-75FN256I	512	2.5	7.5	Lead-free fpBGA	256	193	I
	LC5512MB-75FN484I	512	2.5	7.5	Lead-free fpBGA	484	253	I
LC5768MB	LC5768MB-75FN256I	768	2.5	7.5	Lead-free fpBGA	256	193	I
	LC5768MB-75FN484I	768	2.5	7.5	Lead-free fpBGA	484	317	I
LC51024MB	LC51024MB-75FN484I	1024	2.5	7.5	Lead-free fpBGA	484	317	I
	LC51024MB-75FN672I	1024	2.5	7.5	Lead-free fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t _{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-4FN256C	256	3.3	4.0	Lead-free fpBGA	256	141	C
	LC5256MV-5FN256C	256	3.3	5.0	Lead-free fpBGA	256	141	C
	LC5256MV-75FN256C	256	3.3	7.5	Lead-free fpBGA	256	141	C
LC5512MV	LC5512MV-45QN208C	512	3.3	4.5	Lead-free PQFP	208	149	C
	LC5512MV-75QN208C	512	3.3	7.5	Lead-free PQFP	208	149	C
	LC5512MV-45FN256C	512	3.3	4.5	Lead-free fpBGA	256	193	C
	LC5512MV-75FN256C	512	3.3	7.5	Lead-free fpBGA	256	193	C
	LC5512MV-45FN484C	512	3.3	4.5	Lead-free fpBGA	484	253	C
	LC5512MV-75FN484C	512	3.3	7.5	Lead-free fpBGA	484	253	C