

**Octal Intelligent Subscriber Line Audio-processing Circuit
Ve790 Series****APPLICATIONS**

- Voice over IP/DSL — Integrated Access Devices (IAD), Smart Residential Gateways (SRG), Home Gateway/Router
- Fiber — Fiber in the Loop (FITL), Fiber to the Home (FTTH)
- DLC-MUX
- CO

FEATURES

- High performance digital signal processor provides programmable control of all major line card functions
 - A-law/ μ -law and linear codec/filter
 - Transmit and receive gain
 - Two-wire AC impedance
 - Transhybrid balance
 - Equalization
 - DC loop feeding
 - Smooth or abrupt polarity reversal
 - Loop supervision
 - Off-hook debounce circuit
 - Ground-key and ring-trip filters
 - Internal ringing generation and integrated ring-trip detection
 - Adaptive hybrid balance
 - Line and circuit testing
 - Meets GR-909 and GR-844 test requirements
 - Tone generation (DTMF, FSK, random noise, and arbitrary tone)
 - Metering generation at 12 kHz and 16 kHz
 - Envelope shaping and level control
 - Modem Tone Detection
- Selectable PCM/MPI or GCI digital interfaces
 - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- General purpose I/O pins
- +3.3 V DC operation
- Exceeds LSSGR and ITU requirements
- Supports external ringing with on-chip ring-trip circuit
 - Automatic or manual ring-trip modes
- Supports Caller Number Identification (CID)

ORDERING INFORMATION

Device	Package
Le792288DGC	144-pin BGA (Green Package)

DESCRIPTION

The Le792288 Octal Intelligent Subscriber Line Audio-processing Circuit (ISLAC™) device, in combination with Ve790 series SLIC devices, implements an eight-channel universal telephone line interface. This enables the design of a single, low cost, high performance, fully software programmable line interface for multiple country applications. All AC, DC, and signaling parameters are fully programmable via microprocessor or GCI interfaces. Additionally, the Le792288 Octal ISLAC device has integrated self-test and line-test capabilities to resolve faults to the line or line circuit. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective.

RELATED LITERATURE

- 081237 Le79232 ISLIC™ Device Data Sheet
- 081185 Le79252 ISLIC™ Device Data Sheet
- 081191 Le75282 LCAS Data Sheet
- 080923 Le792x2/Le79228 Chip Set User's Guide

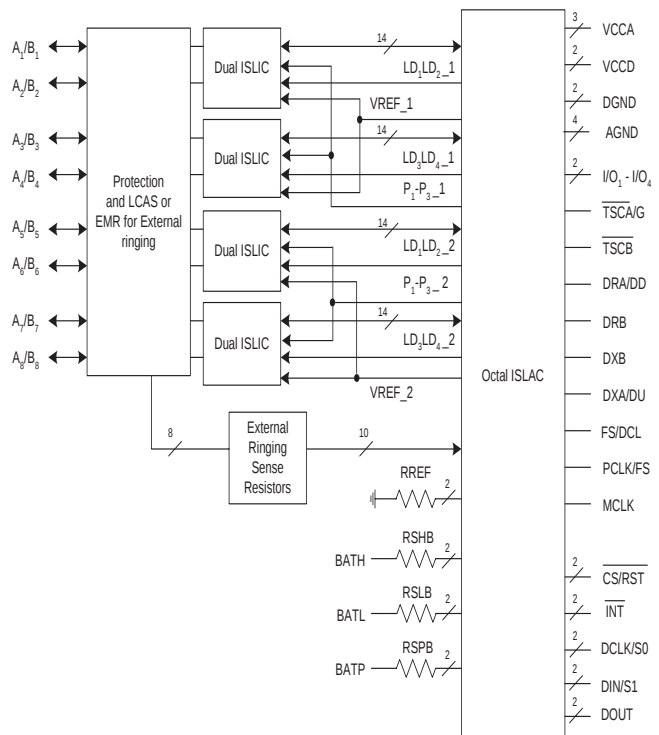
BLOCK DIAGRAM

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PRODUCT DESCRIPTION

The Le792288 voice chip set integrates all the functions of the subscriber line for eight subscriber lines. Multiple Ve790 series SLIC devices and an Le792288 Octal ISLAC™ device provide the following basic functions:

1. The Ve790 series SLIC device: A high voltage, bipolar IC that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The Le792288 Octal ISLAC device: A low voltage CMOS IC that provides conversion and DSP functions for eight channels. Complete schematics of line cards using the Le792288 Octal ISLAC device for internal and external ringing are shown in the Application Circuits section.

The Ve790 series SLIC device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the Octal ISLAC device to operate in eight different modes that control power consumption and signaling. This enables it to have full control over the subscriber loop. The Ve790 series SLIC device is designed to be used exclusively with the Le792288x Octal ISLAC device as part of a multiple-line chip set.

The Ve790 series SLIC device implements a linear loop-current feeding method with the enhancement of intelligent thermal management in a controlled manner. This limits the amount of power dissipated on the Ve790 series SLIC chip by dissipating excess power in external resistors.

The Le792288 device is configured as two four-channel groups that share a common clock and PCM interface. Each four-channel group has its own chip select and serial interface for individual programming. The signal names for each four-channel SLAC device are differentiated by _1 or _2. Generic naming of each signal is C_X , where the subscript C equals the channel number 1 through 4 and the $_X$ equals the four-channel group number 1 or 2.

Each Le792288 Octal ISLAC device contains high-performance codec/filter circuits that provide A/D and D/A conversion for voice (codec/filter), DC-feed and supervision signals for eight subscriber channels. The Le792288 Octal ISLAC device contain DSP cores that handle signaling, DC-feed, supervision and line diagnostics for all eight channels.

The DSP cores selectively interface with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The Le792288 Octal ISLAC device provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, these chip sets provide system level solutions for the loop supervisory functions and metering. In total, they provide a programmable solution that can satisfy worldwide line card requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with the WinSLAC™ software. This PC software is provided free of charge and allows the designer to enter a description of system requirements. WinSLAC then computes the necessary coefficients and plots the predicted system results.

The Ve790 series SLIC device interface unit inside the Le792288 Octal ISLAC device processes information regarding the line voltages, loop currents and battery voltage levels. These inputs allow the Le792288 Octal ISLAC device to place several key Ve790 series SLIC device performance parameters under software control.

The main functions that can be observed and/or controlled through the Le792288 Octal ISLAC device backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth reversal
- Subscriber line matching
- Ringing generation
- Sophisticated line and circuit tests

To accomplish these functions, the Ve790 series SLIC device collects the following information and feeds it, in analog form, to the Le792288 Octal ISLAC device:

- The metallic (IMT) and longitudinal (ILG) loop currents
- The AC (VTX) and DC (VSAB) loop voltages

The outputs supplied by the Le792288 Octal ISLAC device to the Ve790 series SLIC device are then:

- A voltage (VHLi*) that provides control for the following high-level Ve790 series SLIC device outputs:
 - DC loop current
 - Internal ringing signal
 - 12 or 16 kHz metering signal
- A low-level voltage proportional to the voice signal (VOUTi)
- A voltage that controls longitudinal offset for test purposes (VLBi)

The Le792288 Octal ISLAC device performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Transhybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC™ software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or μ -law.

Besides the Octal ISLAC device functions, the Le792288 Octal ISLAC device provides all the sensing, feedback, and clocking necessary to completely control Ve790 series SLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The Le792288 Octal ISLAC device supplies complete mode control to the Ve790 series SLIC device using the control bus and (P1-P3) tri-level load signal (LDi).

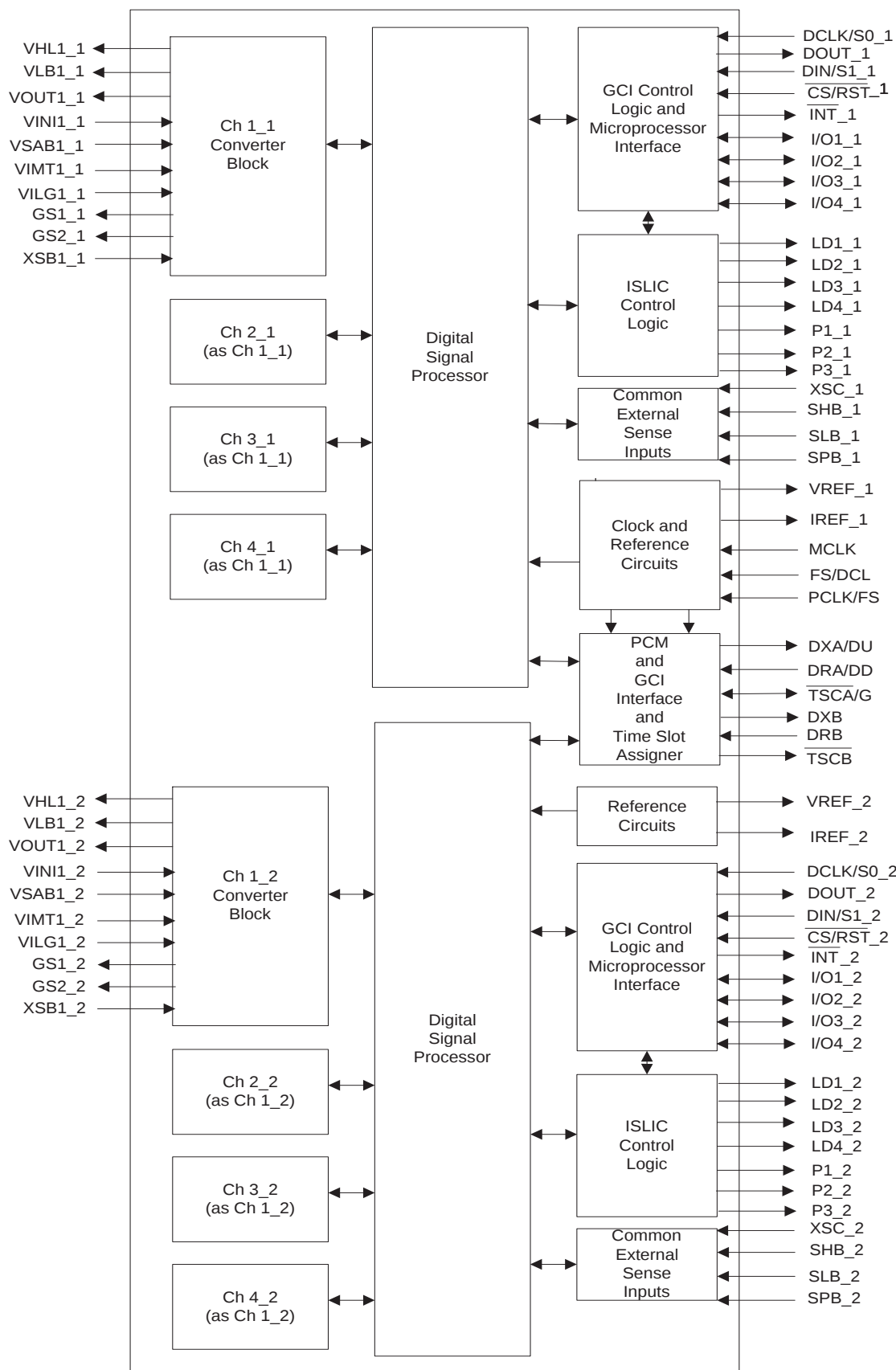
The Le792288 Octal ISLAC device provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

For subscriber line diagnostics, AC and DC line conditions can be monitored using built in test tools. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit. The user can choose to send the actual PCM measurement data directly to a higher level processor by way of the voice channel. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and telephones to be identified.

***Note:**

"i" denotes channel number

Le792288 Device Internal Block Diagram

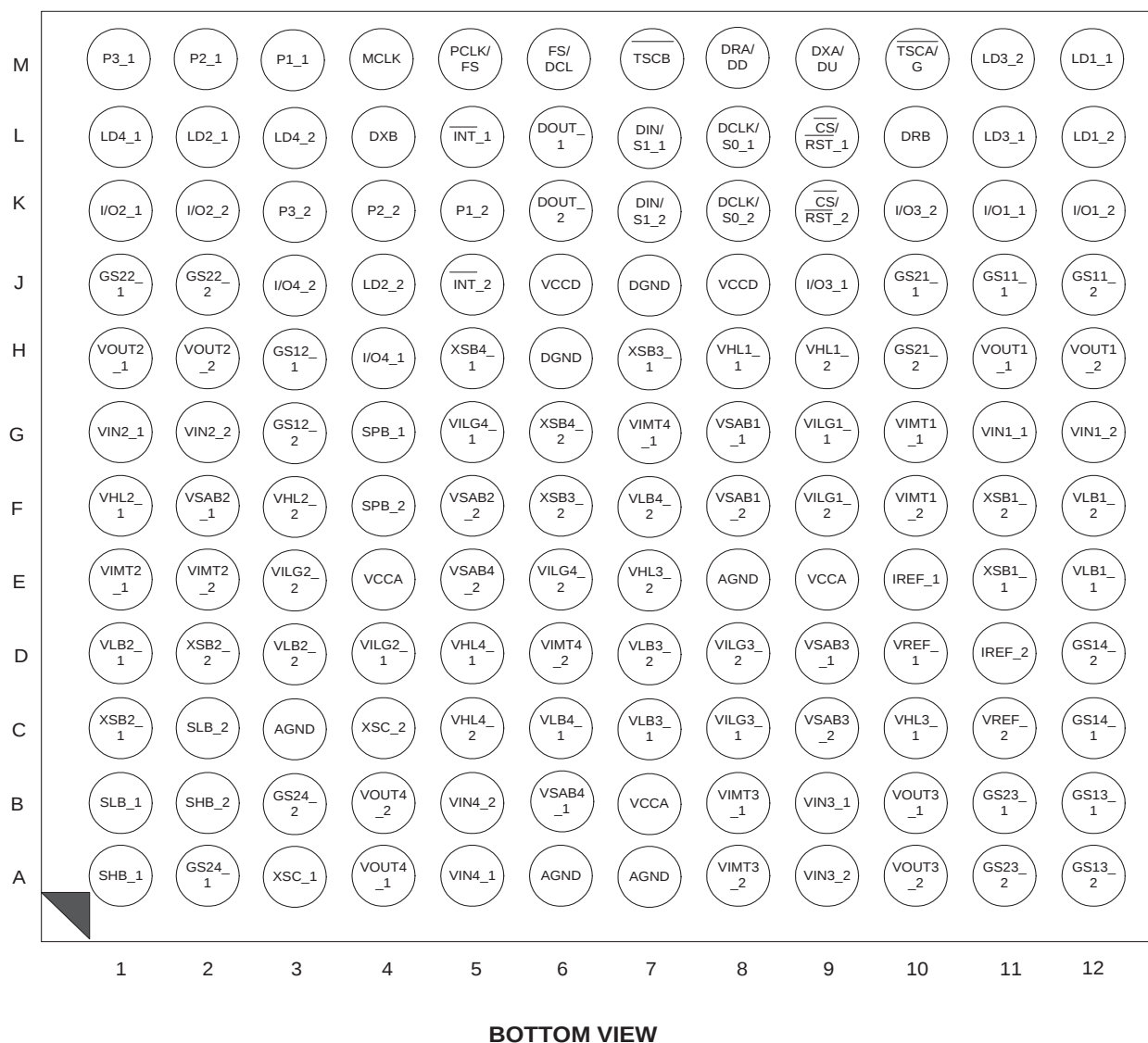


Features of the Le792288 Chip Set

- Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions
- Supports high density, multi-channel architecture
- Single hardware design meets multiple country requirements through software programming of:
 - Ringing waveform and frequency (for balanced ringing)
 - DC loop-feed characteristics and current-limit
 - Loop-supervision detection thresholds
 - Off-hook debounce circuit
 - Ground-key and ring-trip filters
 - Off-hook detect de-bounce interval
 - Two-wire AC impedance
 - Transhybrid balance impedance
 - Transmit and receive gains
 - Equalization
 - Digital I/O pins
 - A-law/ μ -law and linear selection
- Supports internal and external battery-backed or earth-backed ringing
 - Self-contained ringing generation and control
 - Supports external ringing generator and ring relay
 - Ring relay operation synchronized to zero crossings of ringing voltage and current
 - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Supports metering generation with envelope shaping
- Smooth or abrupt polarity reversal
- Adaptive transhybrid balance
 - Continuous or adapt and freeze
- Supports both loop-start and ground-start signaling
- Exceeds LSSGR and CCITT central office requirements
- Selectable PCM or GCI interface
 - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- On-hook transmission
- Power/service denial mode
- Line-feed characteristics independent of battery voltage
- Only 3.3 V and battery supplies needed
- Low idle-power per line
- Linear power-feed with intelligent power-management feature
- Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Tone generation
 - DTMF
 - FSK
 - Random noise
 - Arbitrary tone
- Built-in voice path test modes
- Power-cross, fault, and foreign voltage detection
- Meets GR-909 and GR-844 test requirements
- Integrated line-test features
 - Leakage
 - Line and ringer capacitance
 - Loop resistance
- Integrated self-test features
 - Echo gain, distortion, and noise
- Small physical size
- One relay driver and one test load switch per Ve790 series SLIC channel

CONNECTION DIAGRAM

Figure 1. 144-Pin BGA Connection Diagram



PIN DESCRIPTIONS

Pin Name	Type	Description
AGND, DGND	Ground	Separate analog and digital grounds are provided to allow noise isolation; however, the two grounds are connected inside the part, and the grounds must also be connected together on the circuit board.
$\overline{\text{CS}}/\text{RST_X}$	Input	For PCM backplane operation, a logic low on this pin for 16 or more DCLK cycles resets the sequential logic in the Le792288 Octal ISLAC device into a known mode. A logic low placed on this pin for less than 15 DCLK cycles is a chip select and enables serial data transmission into DIN or out of the DOUT port. For GCI operation, a logic low on this pin for 1 μs or longer resets the sequential logic into a known mode. This pin is 5-V tolerant.
DCLK/SO_X	Input	Provides data control for MPI interface control. For GCI operation, this pin is device address bit 0. This pin is 5-V tolerant.
DIN/S1_X	Input	For PCM backplane operation, control data is serially written into the Le792288 Octal ISLAC device via the DIN pin with the MSB first. DIN can be tied to DOUT for a single bi-directional interface. The data clock (DCLK) determines the data rate. For GCI operation, this pin is device address bit 1. This pin is 5 V tolerant.
DOUT_X	Output	For PCM backplane operation, control data is serially read out of the Le792288 Octal ISLAC device via the DOUT pin with the MSB first. DOUT can be tied to DIN for a single bi-directional interface. The data clock (DCLK) determines the data rate. DOUT is high impedance except when data is being transmitted from the Le792288 Octal ISLAC device under control of $\overline{\text{CS}}/\text{RST}$. This pin is 5-V tolerant.
DRA/DD, DRB	Input	For the PCM highway, the receive PCM data is input serially through the DRA or DRB ports. The data input is received every 125 μs and is shifted in, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. The receive port can receive information for direct control of the Ve790 series SLIC device. This mode is selected in Device Configuration Register 2 (RTSEN=1, RTSMD=1). When selected, this data is received in an independently programmable timeslot from the PCM data. For the GCI mode, downstream receive and control data is accepted on this pin. This pin is 5 V tolerant.
DXA/DU, DXB	Output	For the PCM highway, the transmit PCM data is transmitted serially through the DXA or DXB ports. The transmission data output is available every 125 μs and is shifted out, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. DXA and DXB are high impedance between bursts and while the device is in the inactive mode. Can also select a mode (RTSEN= 1, RTSMD=1 or 0 in Device Configuration Register 2) that transmits the Signaling Register MSB contents first, in an independently programmable timeslot from the PCM data. This data is transmitted in all modes except disconnect. For the GCI mode, upstream transmit and signaling data is transferred on this pin. This pin is 5 V tolerant.
FS/DCL	Input	For PCM operation, pin is Frame Sync. PCM operation is selected by the presence of an 8 kHz Frame Sync signal on this pin in conjunction with the PCLK on the PCLK/FS pin (see below). This 8 kHz pulse identifies the beginning of a frame. The Le792288 Octal ISLAC device references individual timeslots with respect to this input, which must be synchronized to PCLK. GCI operation is selected by the presence of the downstream clock DCL, on this pin in conjunction with the presence of a FS on the PCLK/FS pin. In GCI mode, the data rate is 2 MHz and DCL must be either 2 or 4 MHz. This pin is 5 V tolerant.
GS1 _{1_X} – GS1 _{4_X} , GS2 _{1_X} – GS2 _{4_X}	Output	Gain select nodes for VILG and VIMT inputs. This node provides a tie point to VREF. When selected, the node becomes high impedance.
VILG _{1_X} – VILG _{4_X}	Input	Longitudinal current input from SLIC. Voltage generated by RLG is sensed by this pin. Tie pin to VREF if channel unused.
VIMT _{1_X} – VIMT _{4_X}	Input	Metallic current input from SLIC. Voltage generated by RMT is sensed by this pin. Tie pin to VREF if channel unused.
$\overline{\text{INT_X}}$	Output	For PCM operation, when a subscriber line requires service, this pin goes to a logic 0 to interrupt a higher level processor. Several registers work together to control operation of the interrupt: Signaling and Global Interrupt Registers with their associated Mask Registers, and the Interrupt Register. See the description at channel configuration register 6 (Mask) for operation. Logic drive is selectable between open drain and TTL-compatible outputs.
I/O _{1_X} – I/O _{4_X}	Input/ Output	General purpose logic input/output connection for each of 8 channels. These control lines can be programmed as an input or output in the Global I/O Direction Register. When programmed as outputs, they can control an external logic device. When programmed as inputs, they can monitor external logic circuits. Data for these pins can be written or read individually (from the channel specific I/O Register) or as a group (from the Global I/O Data Register).
IREF_X	Input	External resistor (R_{REF}) connected between this pin and analog ground generates an accurate, on-chip reference current for the A/D's and D/A's on the Le792288 Octal ISLAC device.
LD _{1_X} – LD _{4_X}	Output	The LD pins output 3-level voltages. When LD _i is a logic 0 (< 0.4 V), the destination of the code on P ₁ –P ₃ is the relay control latches in the ISLIC control register. When LD _i is a logic 1 (>V _{CC} –0.4 V), the destination of P ₁ –P ₃ is the mode control latches. LD _i is driven to VREF when the contents of the ISLIC control register must not change.

Pin Name	Type	Description
MCLK	Input	For PCM backplane operation, the DSP master clock may connect here. A signal is required only for PCM backplane operation when PCLK is not used as the master clock. MCLK can be a wide variety of frequencies, but must be synchronous to FS. Upon initialization, the MCLK input is disabled, and relevant circuitry is driven by a connection to PCLK. 5 V tolerant.
PCLK/FS	Input	For PCM operation, this is PCM Clock. PCM operation is selected by the presence of a PCLK signal on this pin in conjunction with the FS on the FS/DCL pin (see above). For PCM backplane operation, connect a data clock, which determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK can be any integer multiple of the FS frequency. The minimum clock frequency for linear/companded data plus signaling data is 256 kHz. For GCI operation, this pin is Frame Sync. The FS signal is an 8 kHz pulse that identifies the beginning of a frame. The Le792288 Octal ISLAC device references individual timeslots with respect to this input, which must be synchronized to DCL. This pin is 5-V tolerant.
P ₁ _X – P ₃ _X	Output	Control the operating modes of the Ve790 series SLIC devices connected to the Le792288 Octal ISLAC device.
SHB_X, SLB_X, SPB_X	Input	Resistors that sense the high, low and positive battery voltages connect here. If only one negative battery is used, connect both negative battery resistors to the same supply. If the positive battery is not used, leave the pin unconnected. These pins are current inputs whose voltage is held at VREF.
$\overline{\text{TSCA}}/\text{G}$	Output (PCM) Input (GCI)	For PCM backplane operation, $\overline{\text{TSCA}}$ or $\overline{\text{TSCB}}$ is active low when PCM data is output on the DXA or DXB pins, respectively. The outputs are open-drain and are normally inactive (high impedance). Pull-up loads should be connected to VCCD. When GCI mode is selected, one of two GCI modes may be selected by connecting $\overline{\text{TSCA}}/\text{G}$ to DGND or VCCD.
$\overline{\text{TSCB}}$	Output	
VCCA, VCCD	Supply	Analog and digital power supply inputs. VCCA and VCCD are provided to allow for noise isolation and proper power supply decoupling techniques. For best performance, all of the VCC power supply pins should be connected together at the connector of the printed circuit board.
VHL ₁ _X – VHL ₄ _X	Output	High-level loop control. Voltages on these pins are used to control DC-feed, internal ringing, metering and polarity reversal for each Ve790 series SLIC device.
VIN ₁ _X – VIN ₄ _X	Input	Analog transmit signals (VTX) from each Ve790 series SLIC device connect to these pins. The Le792288 Octal ISLAC device converts these signals to digital words and processes them. After processing, they are multiplexed into serial time slots and sent out of the DXA/DU pin. Tie pin to VREF if channel unused.
VOUT ₁ _X – VOUT ₄ _X	Output	Analog receive voltage signals are sent out of the Le792288 Octal ISLAC device from these pins. A resistor converts these signals to currents which drive the Ve790 series SLIC device.
VLB ₁ _X – VLB ₄ _X	Output	Normally connected to VCCA internally. They supply longitudinal reference voltages to the Ve790 series SLIC devices during certain test procedures. These outputs are connected internally to VCCA during Ve790 series SLIC Active, Standby, Ringing, and Disconnect modes. During test modes, it can be connected to the receive D/A.
VREF_X	Output	This pin provides a 1.4 V, single-ended reference to the Ve790 series SLIC four-channel group that the Le792288 Octal ISLAC device is connected.
VSAB ₁ _X – VSAB ₄ _X	Input	Connect to the VSAB pins of the Ve790 series SLIC channels.
XSB ₁ _X – XSB ₄ _X	Input	External ringing sense pin. This pin senses the current through RSRB to measure the ringing voltage on the line.
XSC_X	Input	External ring generator sense. This pin senses the current RSRC to measure the ringing bus voltage.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	$-60^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
Ambient Temperature, under Bias	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
Ambient relative humidity (non condensing)	5 to 95%
V_{CCA} with respect to (AGND or DGND)	-0.4 to $+4.0$ V
V_{CCD} with respect to (AGND or DGND)	-0.4 to $+4.0$ V
V_{CCA} with respect to V_{CCD}	± 0.4 V
VIN, VIMT, VILG, VSAB with respect to (AGND or DGND)	-0.4 to $(V_{CCA} + 0.4)$ V
5-V tolerant pins	-0.4 to $(V_{CCD} + 2.37)$ or 5.5 V, whichever is less
AGND	DGND ± 0.4 V
Latch up immunity, 25°C (any pin)	± 100 mA
Latch up immunity, 85°C : (pin I/O _{4_X})	± 50 mA
Latch up immunity, 85°C : (all other pins)	± 100 mA
Any other pin with respect to DGND	-0.4 V to V_{CC}

Package Assembly

Green package devices are assembled with enhanced environmental compatible lead (Pb), halogen, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Legerity guarantees the performance of this device over commercial (0° to 70°C) and industrial (-40° to 85°C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	-40 to $+85^{\circ}\text{C}$
Ambient Relative Humidity	15 to 85%

Electrical Ranges

Analog Supply V_{CCA}	$+3.3$ V $\pm 5\%$, $V_{CCD} \pm 50$ mV
Digital Supply V_{CCD}	$+3.3$ V $\pm 5\%$
DGND	0 V
AGND	DGND ± 10 mV
5V tolerant pins with respect to DGND	DGND to 5.25V

ELECTRICAL CHARACTERISTICS

DC Specifications

Typical values are for TA = 25°C and nominal supply voltage. Minimum and maximum values are over the temperature and supply

No.	Item	Condition	Min	Typ	Max	Unit	Note	
1	Input Low Voltage, I/O ₁ –I/O ₄		–0.05	—	1.36 V	V		
	All other digital inputs		–0.50	—	0.80 V			
2	Input High Voltage, I/O ₁ –I/O ₄		2.46	—	V _{CC} +0.4			μA
	All other digital inputs		2.0	—	5.25			
3	Input Leakage Current, I/O ₁ –I/O ₄	0 to V _{CC}	–10	—	+10	μA		
	All other digital inputs	0 to 5.25 V	–120	—	+180			
4	Input hysteresis (PCLK/FS, FS/DCL, DRA, DRB, MCLK, DCLK/S0, DIN/S1)		0.15	0.225	0.3	V	2	
	I/O ₁ –I/O ₄		0.16	0.25	0.34			
5	Ternary output voltages, LD ₁ –LD ₄							
	High voltage	I _{out} = 1 mA	V _{CC} –0.4	—	—			
	Low voltage	I _{out} = 2 mA	—	—	0.4			
	Medium voltage	±10 μA	—	VREF	—			
6	Output Low Voltage (DXA/DU, DIO, I/O ₁ –I/O ₄ , INT, TSCA, TSCB, DXB)	I _{ol} = 10mA	—	—	0.4	V		
7	Output Low Voltage (P ₁ –P ₃)	I _{ol} = 5 mA	—	—	0.4			
8	Output High Voltage (All digital outputs except INT in open drain mode and TSCA, TSCB)	I _{oh} = 400 μA	V _{CC} –0.4	—	—			
9	Input Leakage Current (VIN ₁ –VIN ₄ , VSAB ₁ –VSAB ₄ , VILG ₁ –VILG ₄ , VIMT ₁ –VIMT ₄ , GS1 ₁ –GS1 ₄ , GS2 ₁ –GS2 ₄)		–1	±0.2	1	μA		
10	Full scale input voltage (VIN ₁ –VIN ₄)					V		
	μ-law	3.205 dBm0	—	VREF ±1.02	—			
	A-law	3.14 dBm0						
11	Input Voltage (VSAB ₁ –VSAB ₄ or VIMT ₁ –VIMT ₄ or VILG ₁ –VILG ₄)	V _{ov} –VREF where V _{ov} is input overload voltage	—	1.02	—			
12	Offset voltage allowed on VIN ₁ –VIN ₄		–50	—	+50	mV	4	
13	VOUT ₁ –VOUT ₄ offset Voltage	DISN off	–40	—	+40			
		DISN on	–80	—	+80			
14	VHL ₁ –VHL ₄ D/A absolute error	% of D/A code	–15 -2%		+15 +2%			
15	Output voltage, VREF	Load current = 0 to 10 mA, Source or Sink	1.32	1.4	1.48	V		
16	Capacitance load on VREF and GS1 ₁ –GS1 ₄ , GS2 ₁ –GS2 ₄ or VOUT ₁ –VOUT ₄		0	—	200	pF	2	
17	Output drive current, VOUT ₁ –VOUT ₄ or VLB ₁ –VLB ₄	Source or Sink	–1	—	+1	mA		
18	Maximum output voltage, VOUT ₁ –VOUT ₄	VOUT–VREF with peak digital input	—	1.02	—	V	8	
19	VLB ₁ –VLB ₄ operating voltage	Source current < 250μA Sink current < 25 μA.	VREF –1.02	—	VREF +1.02			
20	Maximum output voltage on VHL	VHL–VREF with peak digital input, VFD = 0	—	1.02	—			

No.	Item	Condition	Min	Typ	Max	Unit	Note
21	VSAB ₁ –VSAB ₄ , VIMT ₁ –VIMT ₄ , VILG ₁ –VILG ₄ A/D absolute error	% of input voltage	–5 –2%	—	+5 +2%	mV	9
22	Battery read A/D absolute error	% of input voltage	–2 –6%	—	+2 +6%	V	9
23	Gain from VSAB ₁ –VSAB ₄ to VHL ₁ –VHL ₄ (KRFB)	VFD = 1	–4.8	–5	–5.2	V/V	
24	VSAB ₁ –VSAB ₄ to VHL ₁ –VHL ₄ output offset (KRFB)		–50	0	50	mV	
25	Gain from VSAB ₁ –VSAB ₄ to VHL ₁ –VHL ₄	VFD = 0, hook bit feedback	–	–0.128	–	V/V	
26	% error of VLB ₁ –VLB ₄ voltage (For VLB equation, see the <i>Chip Set User's Guide</i>)	% of input voltage	–5	0	+5	%	
27	Capacitance load on VLB ₁ –VLB ₄		0	—	120	pF	2
28	Capacitance load on XSB ₁ –XSB ₄ , XSC		0	—	400		
29	Power Dissipation	One channel active (Ve790 series SLIC state register set to active); seven channels inactive (Ve790 series SLIC state register set to Standby)	—	336	434	mW	
		All channels active (Ve790 series SLIC state register set to Active)	—	528	680		
		All channels inactive (Ve790 series SLIC state register set to Standby)	—	285	376		

Voltage ranges are shown in [Operating Ranges on page 10](#), except where noted.

Transmission Specifications

Table 1. 0 dBm0 Voltage Definitions with Unity Gain in X, R, GX, GR, AX, and AR

Signal at Digital Interface	Transmit	Receive	Unit
A-law digital mW or equivalent (0 dBm0)	0.5026	0.5026	Vrms
μ-law digital mW or equivalent (0 dBm0)	0.4987	0.4987	
±5,800 peak linear coded sine wave	0.5026	0.5025	

Note: Expressed voltage levels on VOUT or input to VIN are equivalent to a digital milliwatt on the digital interface.

No.	Item	Condition	Min	Typ	Max	Unit	Note				
1	Insertion Loss A-D	Input: 1014Hz, 0 dBm0 AR = AX = GR = GX = 0 dB, DISN, R, X, B and Z disabled	-0.25	0	+0.25	dB	3, 7				
	D-A										
	A-D + D-A							Temperature = 25°C	-0.15	0	+0.15
								Variation over temperature	-0.1	0	+0.1
2	Level set error (Error between setting and actual value)	A-D AX + GX D-A AR + GR	-0.1	0	0.1						
3	DR to DX gain in full digital loopback mode	DR Input: 1014 Hz, -10 dBm0 AR=AX=GR=GX=0 dB, DISN, R, X, B and Z filters default	-0.3	0	+0.3						
4	Idle Channel Noise, Psophometric Weighted (A-law)	A-D (PCM output)	—	—	-69	dBm0p	5				
		D-A (V _{OUT})	—	—	-78						
5	Idle Channel Noise, C Message weighted (μ-law)	A-D (PCM output)	—	—	+19	dBmC0					
		D-A (V _{OUT})	—	—	+12						
6	Coder Offset decision value, Xn	A-D, Input signal = 0 V	-7	0	+7	Bits	2				
7	PSRR Image frequency (VCC) A-D	Input: 4.8 to 7.8 kHz, 200 mVp-p Measure at: 8000 Hz – Input frequency	37	—	—	dB	1				
8	PSRR Image frequency (VCC) D-A		37	—	—						
9	DISN gain accuracy	Gdisn = -0.9375 to 0.9375 Vin = 0 dBm0		+0.2		dB					
10	End-to-end group delay	1014Hz; -10dBm0 B = Z = 0; X = R = 1	—	—	525	μS	2, 6, 8				
11	Crosstalk TX to RX same channel RX to TX	0 dBm0 300 Hz to 3400 Hz	—	—	-75	dBm0	2				
		0 dBm0 300 Hz to 3400 Hz	—	—							
12	Crosstalk TX or RX to TX other channel TX or RX to RX	0 dBm0 1014 Hz	—	—	-76						
		0 dBm0 1014 Hz	—	—	-78						

Notes:

- Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.
- Guaranteed by design.
- Overall 1.014 kHz insertion loss error of the Le792288 Octal ISLAC device is guaranteed to be 0.34 dB
- These voltages are referred to VREF.
- When relative levels (dBm0) are used, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR) from 0 to -12 dB.
- Group delay spec valid only when Channels 1–4 or 5–8 occupy consecutive slots in the frame. Programming channels in non-consecutive timeslots can add up to 1 frame delay in the Group delay measurements. The Group delay specification is defined as the sum of the minimum values of the group delays for transmit and the receive paths when the B, X, R, and Z filters are disabled with null coefficients. See Figure 4 for Group Delay Distortion.
- Requires that the calibration command (7Ch) must be performed to achieve this performance.
- An additional frame of delay can be added if PCLK frequencies less than 1.536 MHz are used.
- In the absence of any error, the analog level of VREF + 1.02 V represents a digital code of 7FFFh, and the analog level of VREF - 1.02 V represents a digital code of 8000h.

Transmit and Receive Paths

In this section, the transmit path is defined as the analog input to the Le792288 Octal ISLAC device (VIN_n) to the PCM voice output of the Le792288 Octal ISLAC device A-law/μ-law speech compressor. The receive path is defined as the PCM voice input to the Le792288 Octal ISLAC device speech expander to the analog output of the Le792288 Octal ISLAC device (VOUT_n). All limits defined in this section are tested with B = 0, Z = 0 and X = R = GR = 1.

When AR is enabled, a nominal gain of -6.02 dB is added to the analog section of the receive path.

When AX is enabled, a nominal gain of +6.02 dB is added to the analog section of the transmit path.

When relative levels (dBm0) are used in any of the following transmission characteristics, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR) from 0 to -12 dB.

These transmission characteristics are valid for 0 to 70° C.

Attenuation Distortion

The attenuation of the signal in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 2 and Figure 3. The reference signal level is -10 dBm0. The minimum transmit attenuation at 60 Hz is 24 dB.

Figure 2. Transmit Path Attenuation vs. Frequency

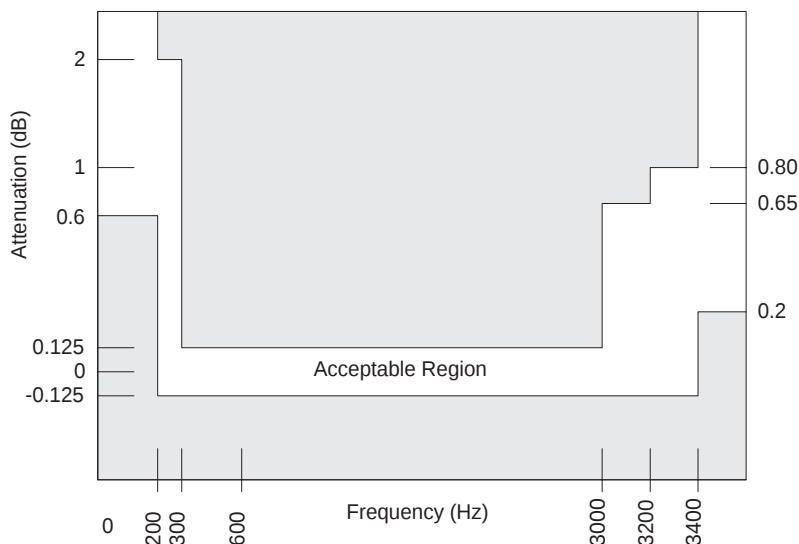
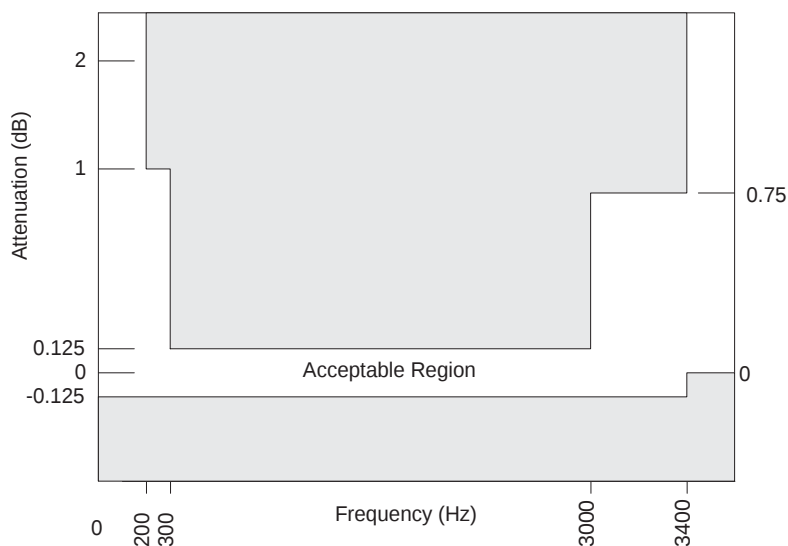


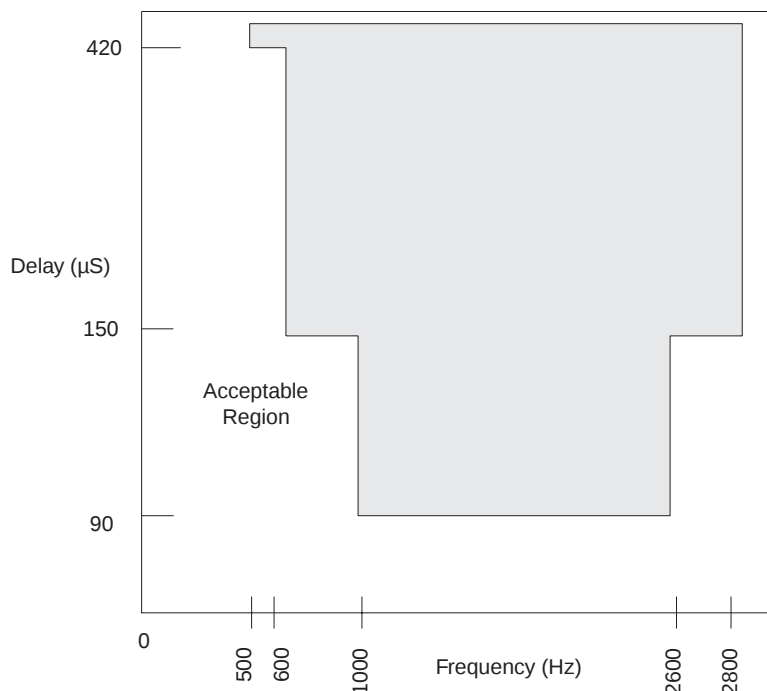
Figure 3. Receive Path Attenuation vs. Frequency



Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 4. The minimum value of the group delay is taken as the reference. The signal level is -10 dBm0.

Figure 4. Group Delay Distortion



Single Frequency Distortion

The output signal level, at any single frequency in the range of 300 to 3400 Hz, other than that due to an applied 0 dBm0 sine wave signal with frequency f in the same frequency range, is less than -46 dBm0. With f swept between 0 to 300 Hz and 3.4 to 12 kHz, any generated output signals other than f are less than -28 dBm0. This specification is valid for either transmission path.

Gain Linearity

The gain deviation relative to the gain at -10 dBm0 is within the limits shown in Figure 5 (A-law) and Figure 6 (μ -law) for either transmission path when the input is a sine wave signal of 1014 Hz.

Figure 5. A-law Gain Linearity with Tone Input (Both Paths)

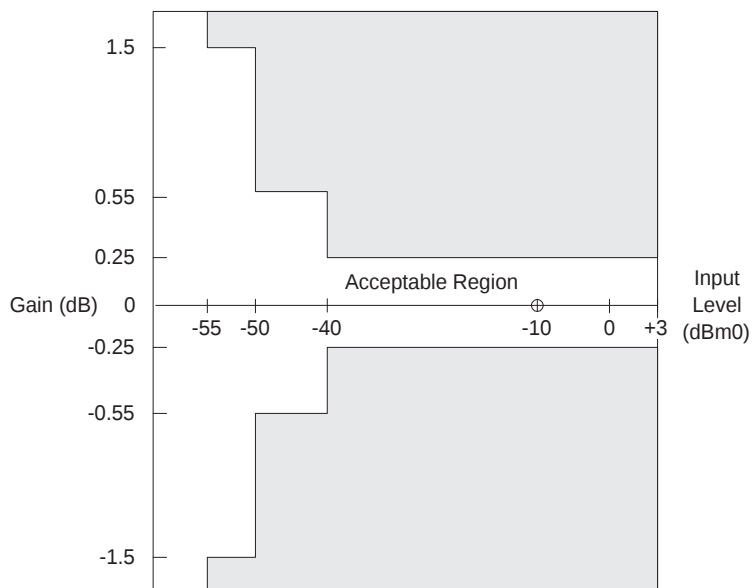
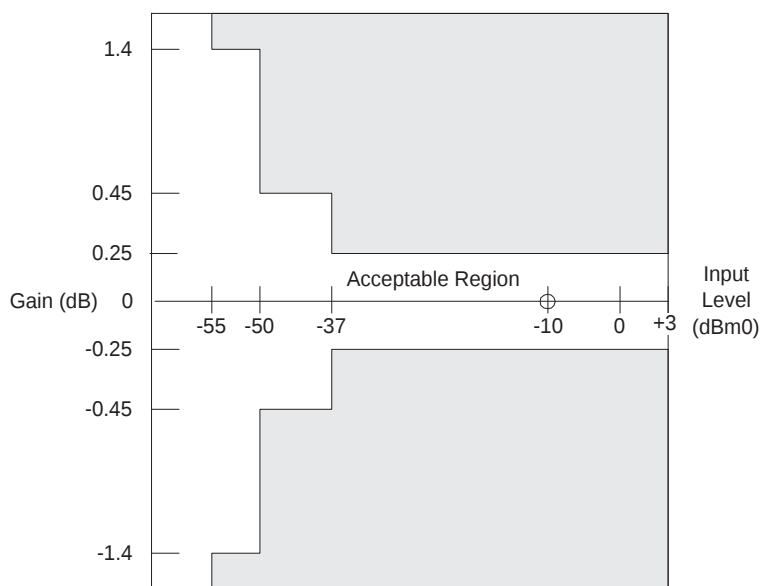


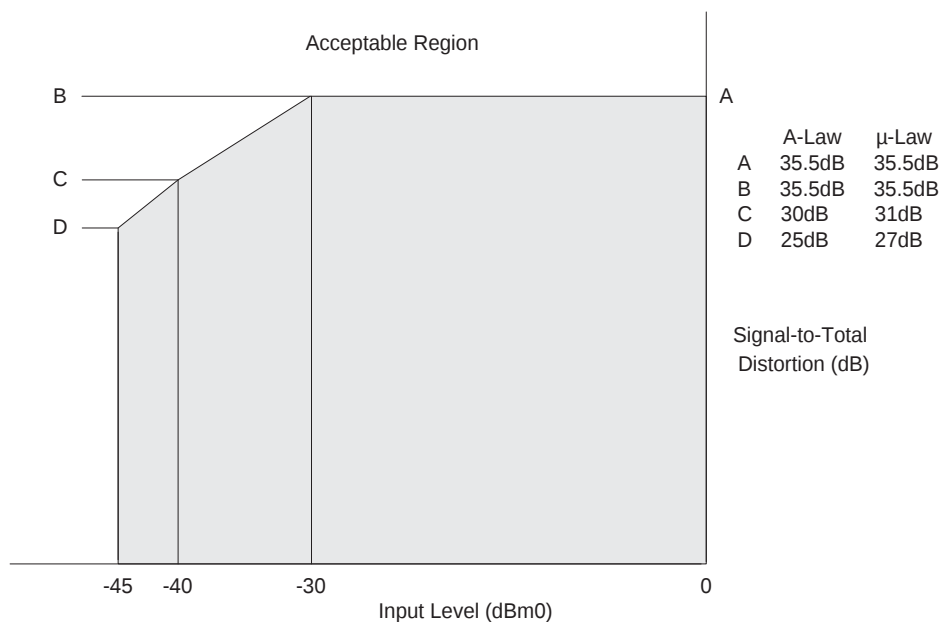
Figure 6. μ -law Gain Linearity with Tone Input (Both Paths)



Total Distortion Including Quantizing Distortion

The signal to total distortion ratio will exceed the limits shown in [Figure 7](#) for either path when the input signal is a sine wave signal of frequency 1014 Hz.

Figure 7. Total Distortion with Tone Input, Both Paths

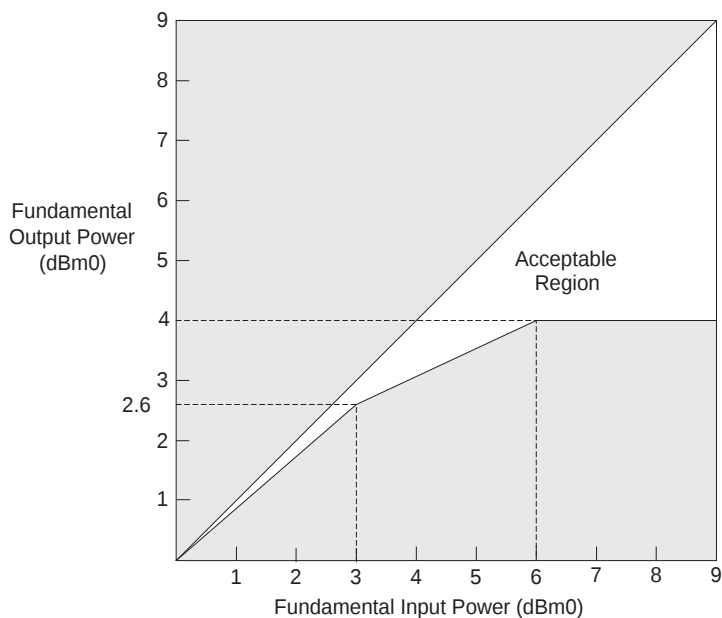


Overload Compression

[Figure 8](#) shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

(1) $1 \text{ dB} < GX \leq +12 \text{ dB}$; (2) $-12 \text{ dB} \leq GR < -1 \text{ dB}$; (3) Digital voice output connected to digital voice input; and (4) measurement analog to analog.

Figure 8. A/A Overload Compression



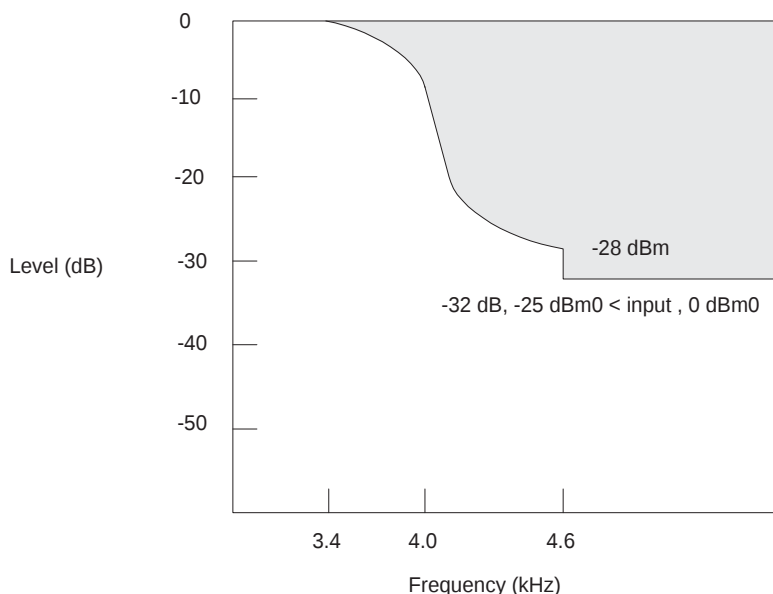
Discrimination Against Out-of-Band Input Signals

When an out-of-band sine wave signal with frequency and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in the following table

Table 2. Minimum Specifications for Out-of-Band Input Signals

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	-25 dBm0 < A ≤ 0 dBm0	18 dB
45 Hz < f < 65 Hz	-25 dBm0 < A ≤ 0 dBm0	25 dB
65 Hz < f < 100 Hz	-25 dBm0 < A ≤ 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	-25 dBm0 < A ≤ 0 dBm0	see Figure 9
4600 Hz < f < 100 kHz	-25 dBm0 < A ≤ 0 dBm0	32 dB

Figure 9. Discrimination Against Out-of-Band Signals



Note:

The attenuation of the waveform below amplitude A between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Attenuation} = \left[14 - 14 \sin\left(\frac{\pi(4000 - f)}{1200}\right) \right] \text{ dB}$$

Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

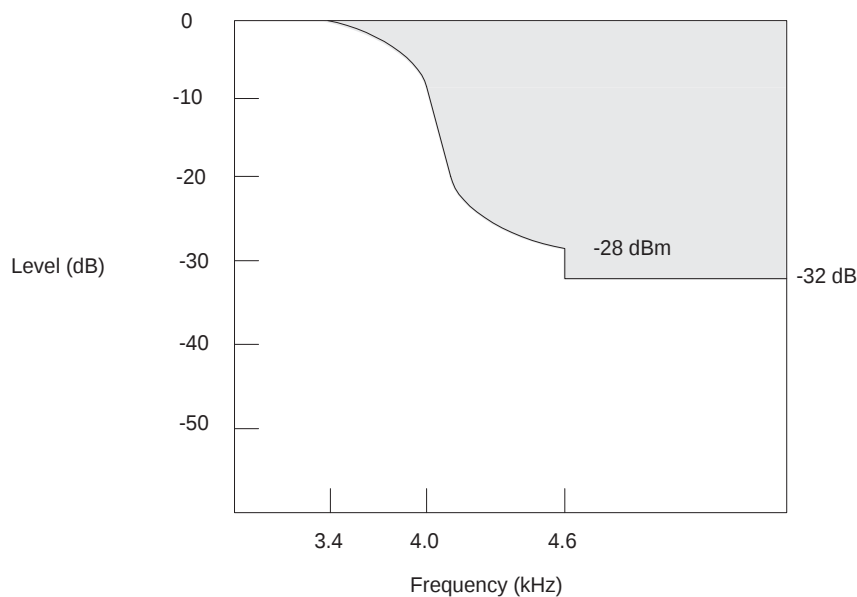
Table 3. Limits for Spurious Out-of-Band Signals

Frequency	Level
4.6 kHz to 40 kHz	-32 dBm0
40 kHz to 240 kHz	-46 dBm0
240 kHz to 1 MHz	-36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 10. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

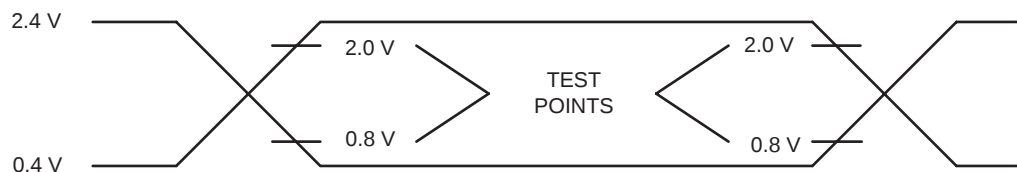
$$A = \left[-14 - 14 \sin\left(\frac{\pi(f - 4000)}{1200}\right) \right] \text{ dBm0}$$

Figure 10. Spurious Out-of-Band Signals



SWITCHING CHARACTERISTICS

Figure 11. Switching Characteristics



VCC = 3.3 V $\pm$ 5%, AGND = DGND = 0 V.

Microprocessor Interface

Min and max values are valid for all digital outputs with a 150 pF load. Pictorial definitions for these parameters can be found on [Figure 13 on page 22](#) and [Figure 14 on page 23](#).

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{DCY}	Data clock period	122	—	—	ns	
2	t_{DCH}	Data clock HIGH pulse width	48	—	—		1
3	t_{DCL}	Data clock LOW pulse width	48	—	—		1
4	t_{DCR}	Rise time of clock	—	—	25		
5	t_{DCF}	Fall time of clock	—	—	25		
6	t_{ICSS}	Chip select setup time, Input mode	30	—	$t_{DCY}-10$		
7	t_{ICSH}	Chip select hold time, Input mode	0	—	$t_{DCY}-20$		
8	t_{ICSL}	Chip select pulse width, Input mode	—	$8t_{DCY}$	—		7
9	t_{ICSO}	Chip select off time, Input mode	2000	—	—		1, 6
10	t_{IDS}	Input data setup time	25	—	$t_{DCY}-10$		
11	t_{IDH}	Input data hold time	30	—	$t_{DCY}-10$		
13	t_{OCSS}	Chip select setup time, Output mode	30	—	$t_{DCY}-10$		
14	t_{OCCH}	Chip select hold time, Output mode	0	—	$t_{DCH}-20$		
15	t_{OCSL}	Chip select pulse width, Output mode	—	$8t_{DCY}$	—		
16	t_{OCSO}	Chip select off time, output Mode	2000	—	—		1, 6
17	t_{ODD}	Output data turn on delay	—	—	35		5
18	t_{ODH}	Output data hold time	3	—	—		
19	t_{ODOF}	Output data turn off delay	3	—	35		
20	t_{ODC}	Output data valid	3	—	35		

PCM Interface

Min and max values are valid for $\overline{TSCA}$ and $\overline{TSCB}$ with an 150 pF load and are valid for DXA and DXB with an 80 pF load. Pictorial definitions for these parameters can be found on [Figure 15 on page 23](#) and [Figure 16 on page 24](#).

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
22	t_{PCY}	PCM clock period	122	—	7812.5	ns	2, 9
23	t_{PCH}	PCM clock HIGH pulse width	48	—	—		
24	t_{PCL}	PCM clock LOW pulse width	48	—	—		
25	t_{PCF}	Fall time of clock	—	—	15		
26	t_{PCR}	Rise time of clock	—	—	15		
27	t_{FSS}	FS setup time	30	—	$t_{PCY}-30$		
28	t_{FSH}	FS hold time	50	—	$125000-3t_{PCY}-30$		
29	t_{TSD}	Delay to $\overline{TSCX}$ valid	5	—	40		3
30	t_{TSO}	Delay to $\overline{TSCX}$ off	5	—	40		4
31	t_{DXD}	PCM data output delay	5	—	40		
32	t_{DXH}	PCM data output hold time	5	—	40		
33	t_{DXZ}	PCM data output delay to high-Z	10	—	40		4
34	t_{DRS}	PCM data input setup time	25	—	$t_{PCY}-10$		
35	t_{DRH}	PCM data input hold time	5	—	$t_{PCY}-20$		
36	t_{FST}	PCM or frame sync jitter time	-97	—	97		

Master Clock

Master Clock can be sourced by MCLK or PCLK input by appropriate configuration of DCRI (see [Figure 12](#)). For a 2.048 MHz $\pm$ 100 PPM, 4.096 MHz $\pm$ 100 PPM, or 8.192 $\pm$ 100 PPM operation:

No.	Symbol	Parameter	Min	Typ	Max	Unit	No
37	t_{MCY}	Period	122	—	7812	ns	2, 8, 9
38	t_{MCR}	Rise time of clock	—	—	15		
39	t_{MCF}	Fall time of clock	—	—	15		
40	t_{MCH}	Master Clock HIGH pulse width	48	—	—		
41	t_{MCL}	Master Clock LOW pulse width	48	—	—		

Note:

1. DCLK may be stopped in the High or Low state indefinitely without loss of information. When $\overline{CS}$ makes a transition to the High state, the last byte received will be interpreted by the Microprocessor Interface logic.
2. The PCM clock (PCLK) frequency must be an integer multiple of the frame sync (FS) frequency and synchronous to the MCLK frequency. The actual PCLK rate is dependent on the number of channels allocated within a frame. A PCLK of 1.544 MHz can be used for standard US transmission systems. The minimum clock frequency is 128 kHz.
3. $\overline{TSCX}$ is delayed from FS by a typical value of $N \cdot t_{PCY}$, where N is the value stored in the time/clock slot register.
4. $\overline{TSCX}$ is an open drain driver. t_{TSO} is defined as the delay time the output driver turns off after the PCLK transaction. The actual delay time is dependent on the load circuitry. The maximum load capacitance on $\overline{TSCX}$ is 150 pF and the minimum pull-up resistance is 360 Ω .
5. The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.
6. The Le792288 Octal ISLAC device requires 2.0 μ s between MPI operations. If the MPI is being accessed while the MCLK (or PCLK if combined with MCLK) input is not active, a Chip Select Off time of 20 μ s is required when accessing coefficient RAM. Immediately after reset, $t_{CSO} = \frac{2\mu s \cdot 8.192 \text{ MHz}}{f_{PCLK}}$, where f_{PCLK} is the applied PCLK frequency. Once DCR1 is programmed for the applied PCLK and MCLK, t_{CSO} is per table specification.
7. If chip select is held low for 16 or more DCLK cycles, the part will reset.
8. Master Clock's frequency can range from 512 kHz to 8.192 MHz and can be set with: Write/Read Device Configuration Register 1, and if necessary Write/Read Master Clock Correction Register.
9. If PCLK is greater or equal to 512 kHz, the preferred configuration is Master Clock derived from PCLK. If a separate MCLK is used, it must be synchronous to PCLK. If PCLK is less than 512 kHz, a separate MCLK (synchronous with PCLK) with f_0 greater or equal to 512 kHz must be used.

WAVEFORMS

Figure 12. Master Clock Timing

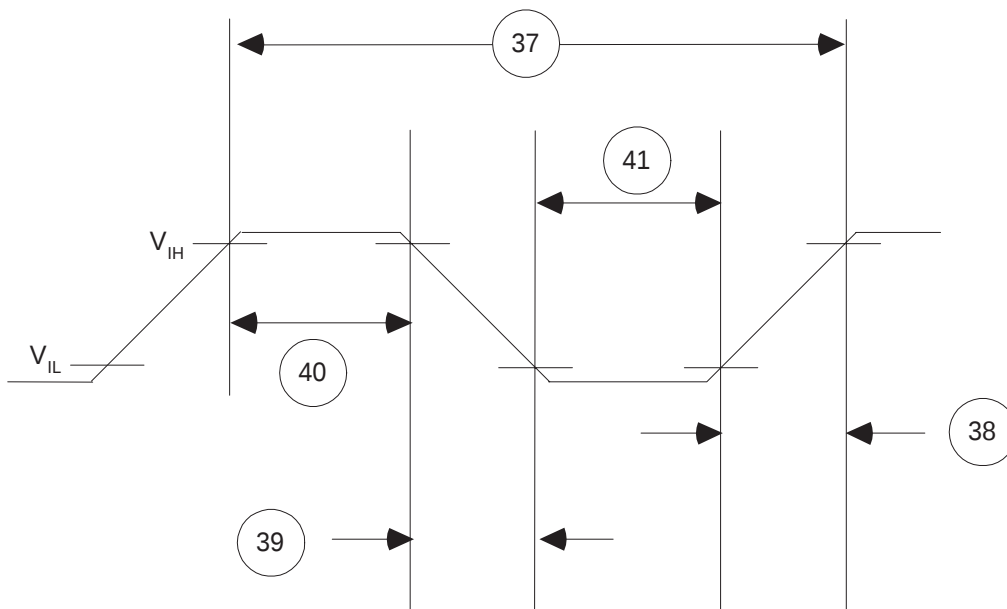


Figure 13. Microprocessor Interface (Input Mode)

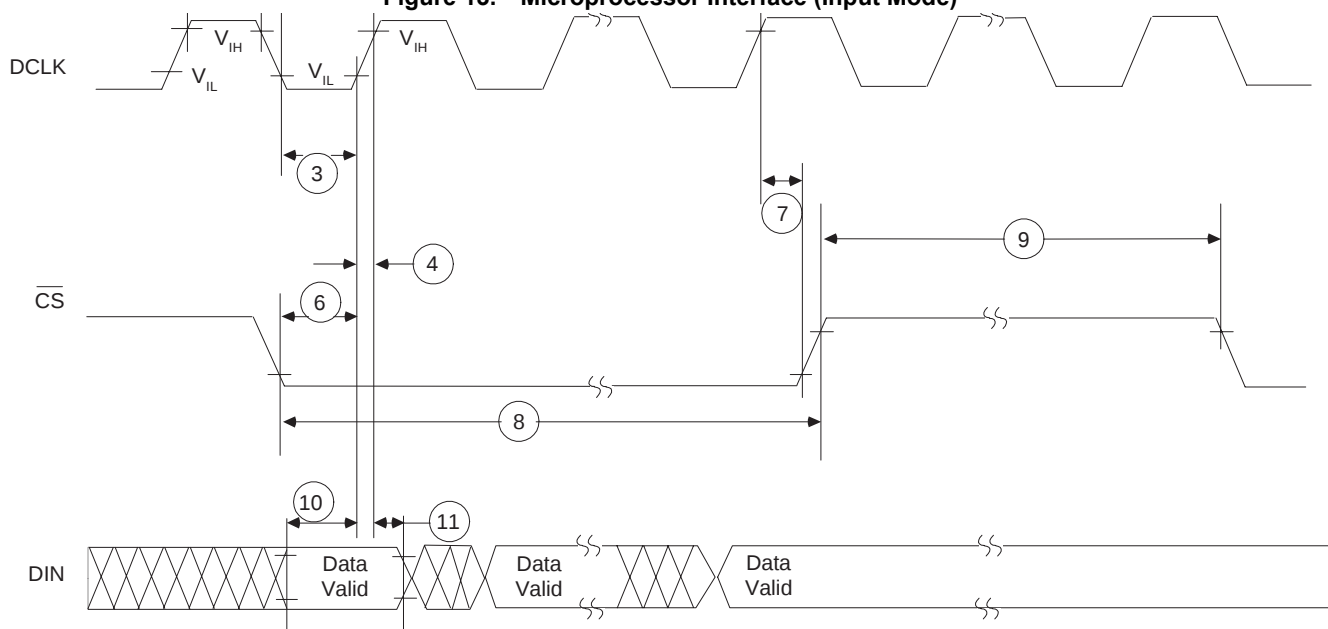


Figure 14. Microprocessor Interface (Output Mode)

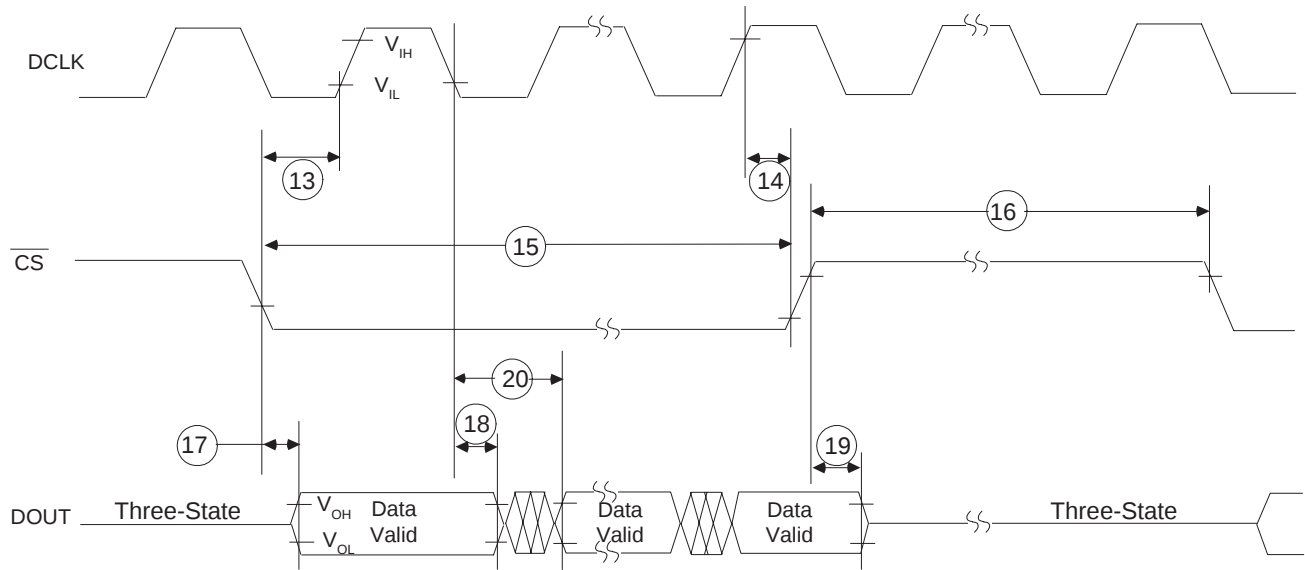


Figure 15. PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)

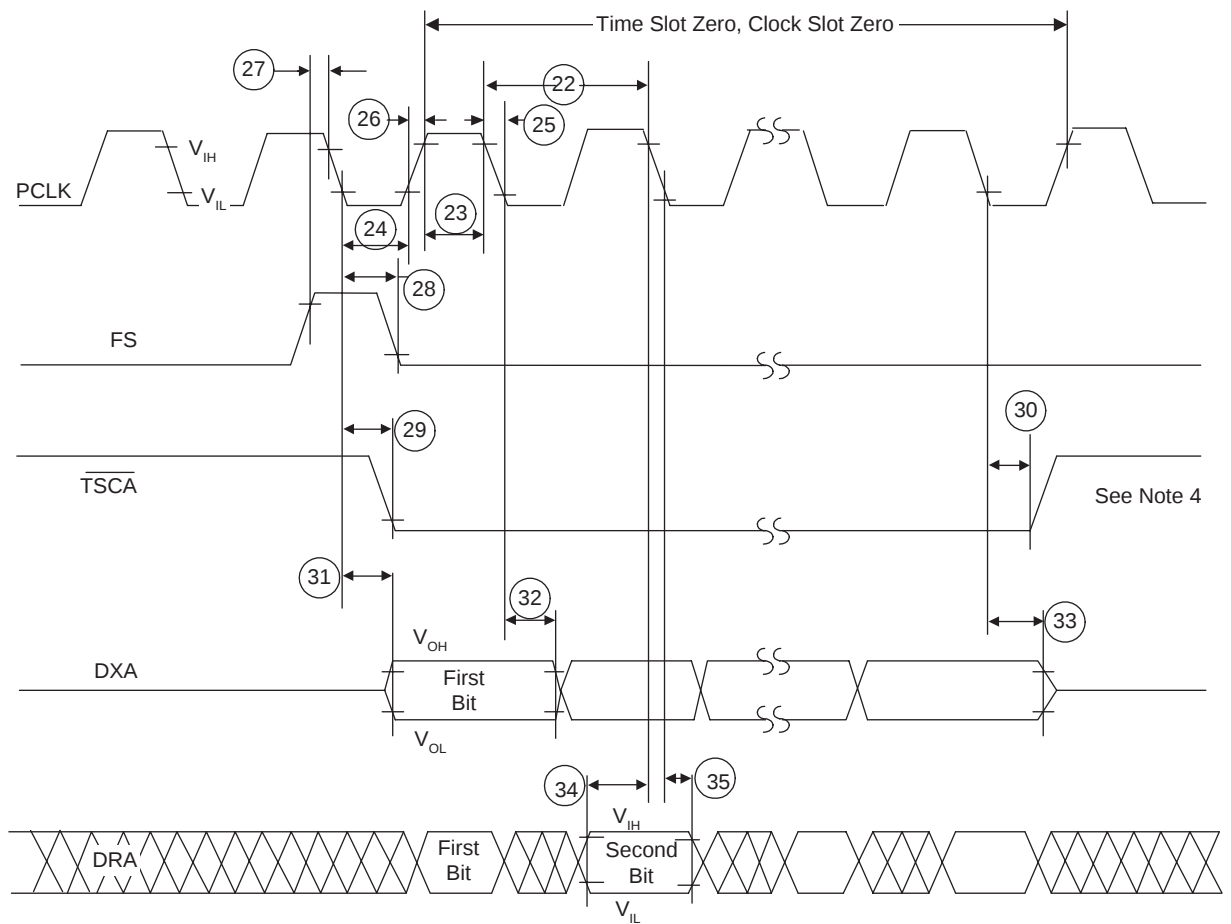
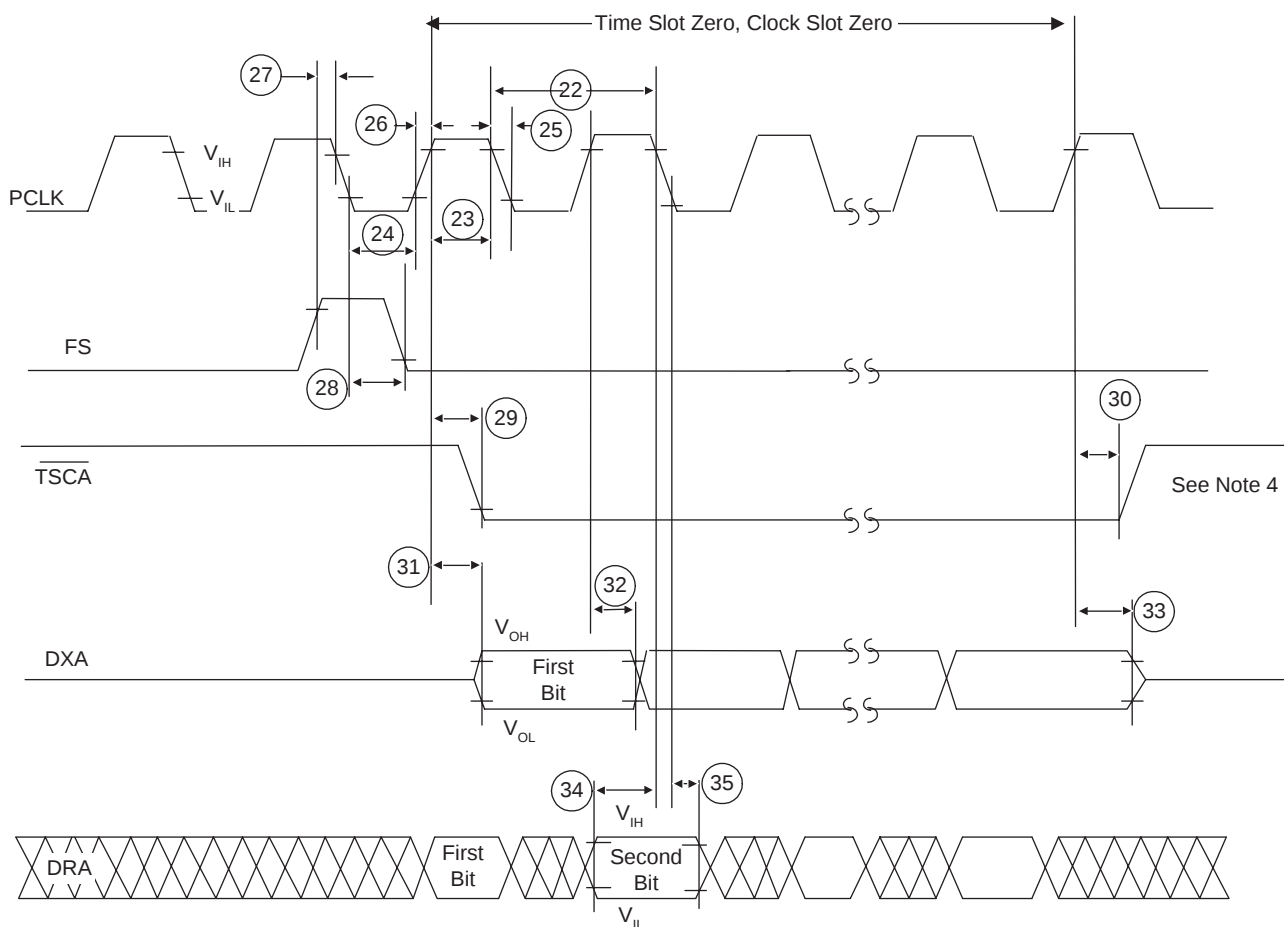


Figure 16. PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)

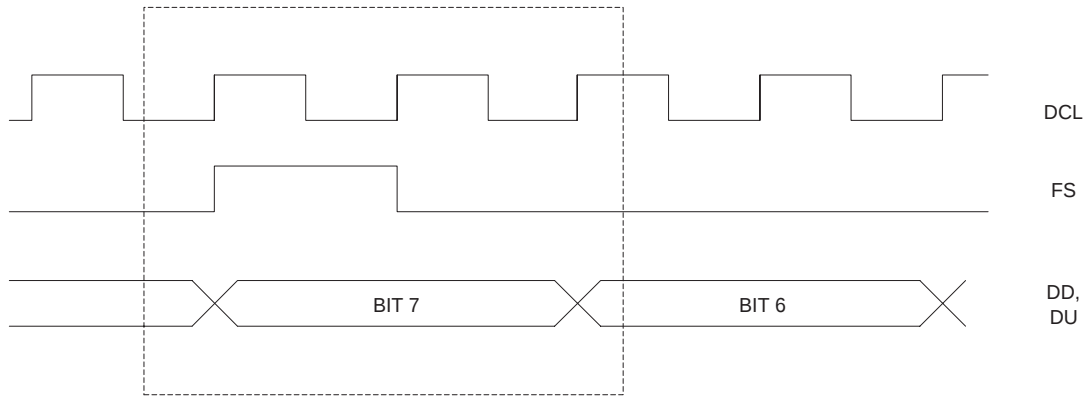


GCI Timing Specifications

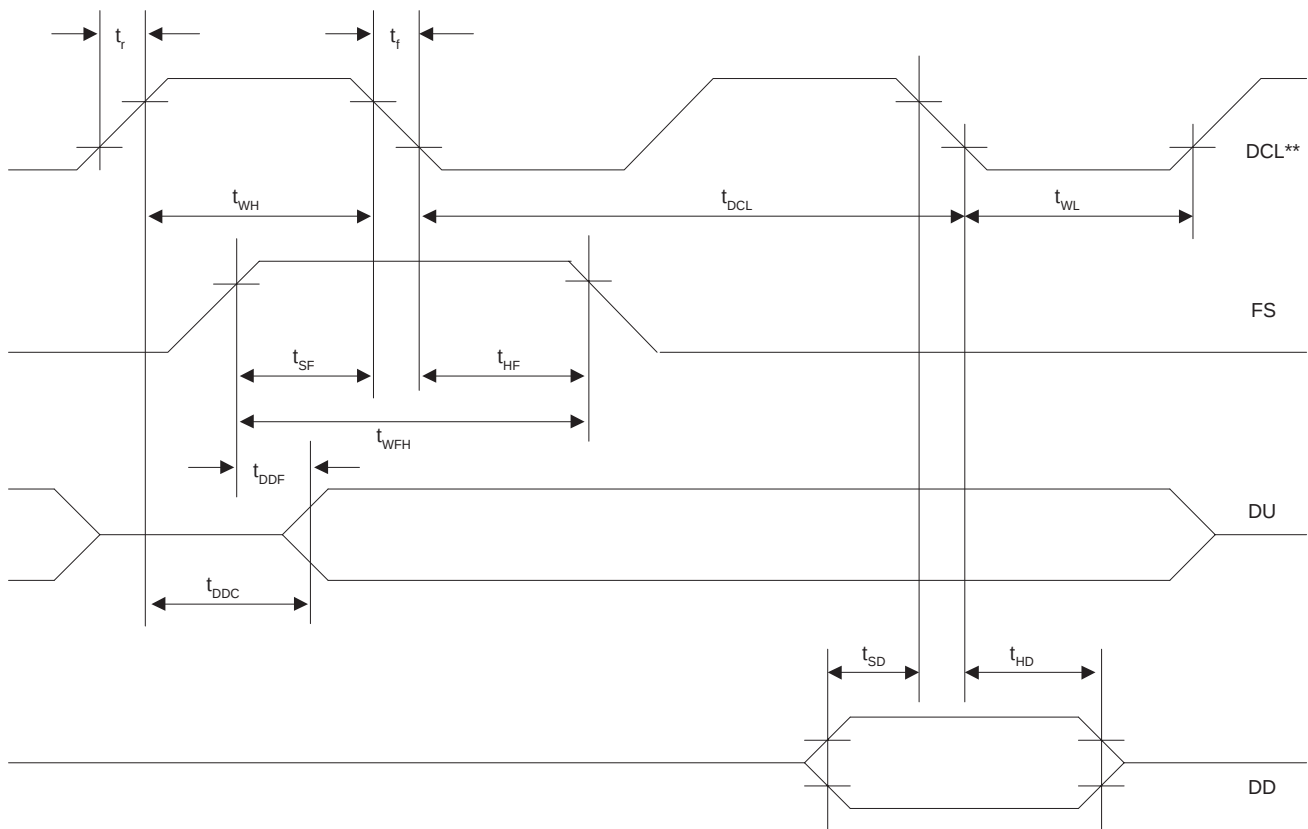
For a 2.048 MHz $\pm$ 100 PPM, 4.096 MHz $\pm$ 100 PPM, or 8.192 $\pm$ 100 PPM operation:

Symbol	Signal	Parameter	Min	Typ	Max	Unit
t_R, t_F	DCL	Rise/fall time	—	—	60	ns
t_{DCL}	DCL	Period, $F_{DCL} = 2048$ kHz $F_{DCL} = 4096$ kHz	478 239	—	498 249	
t_{WH}, t_{WL}	DCL	Pulse width	90	—	—	
t_R, t_F	FS	Rise/fall time	—	—	60	
t_{SF}	FS	Setup time	70	—	$t_{DCL}-50$	
t_{HF}	FS	Hold time	50	—	—	
t_{WFH}	FS	High pulse width	130	—	—	
t_{DDC}	DU	Delay from DCL edge	—	—	100	
t_{DDF}	DU	Delay from FS edge	—	—	150	
t_{SD}	DD	Data setup	$t_{WH}+20$	—	—	
t_{HD}	DD	Data hold	50	—	—	

GCI Waveforms



DETAIL A



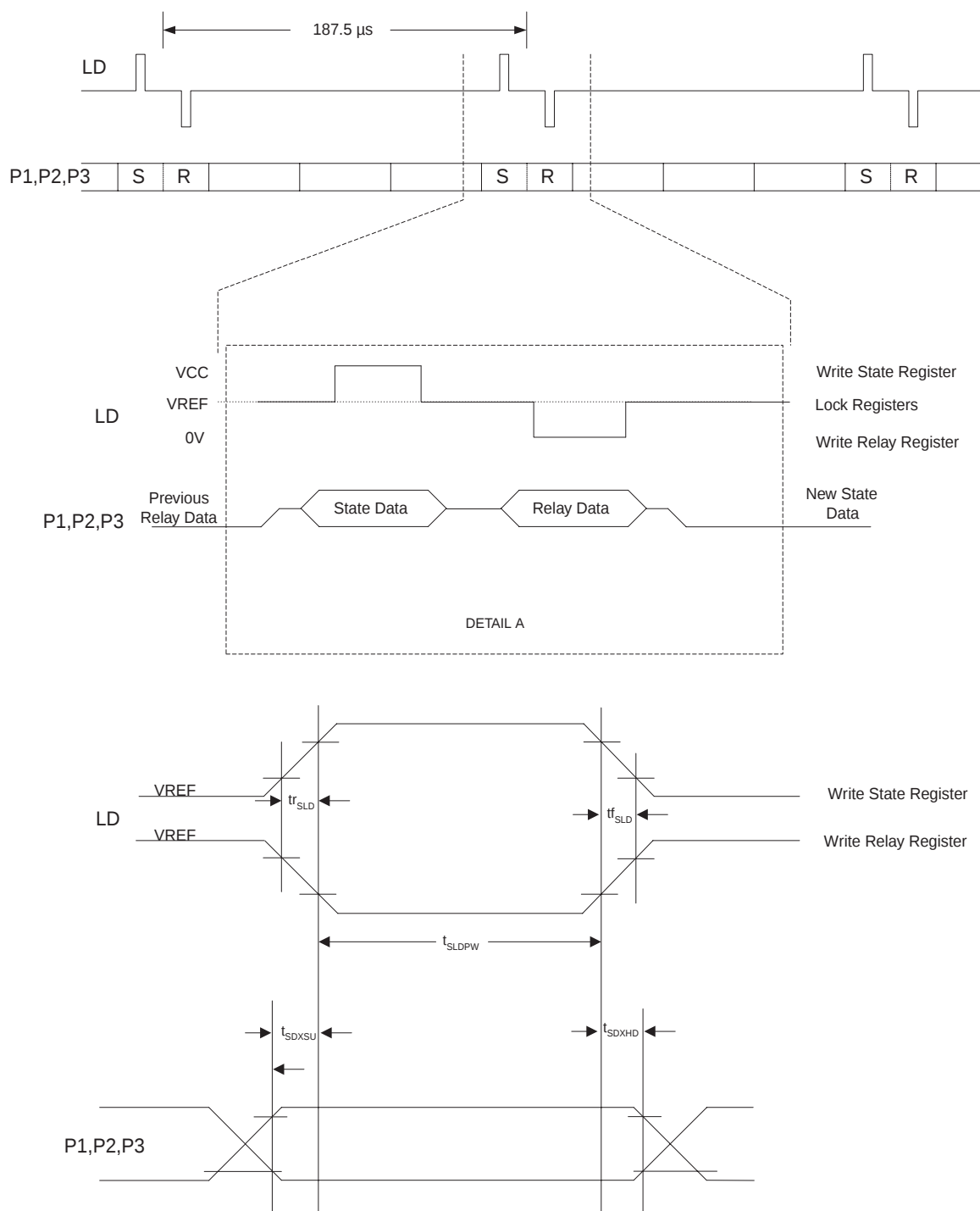
** Timing diagram valid for
 $F_{DCL} = 2048$ or 4096 KHz

SLIC DEVICE TIMING SPECIFICATIONS

(See [Figure 17.](#))

Symbol	Signal	Parameter	Min	Typ	Max	Unit
t_{rSLD}	LD	Rise time			2	μs
t_{fSLD}	LD	Fall time			2	
t_{SLDPW}	LD	LD minimum pulse width	3			
t_{SDXSU}	P1,P2,P3	P1–3 data Setup time	4.5			
t_{SDXHD}	P1,P2,P3	P1–3 data hold time	4.5			

Figure 17. SLIC Device Bus Timing Waveform



APPLICATION CIRCUITS

Figure 18. Internal Ringing Line Schematic

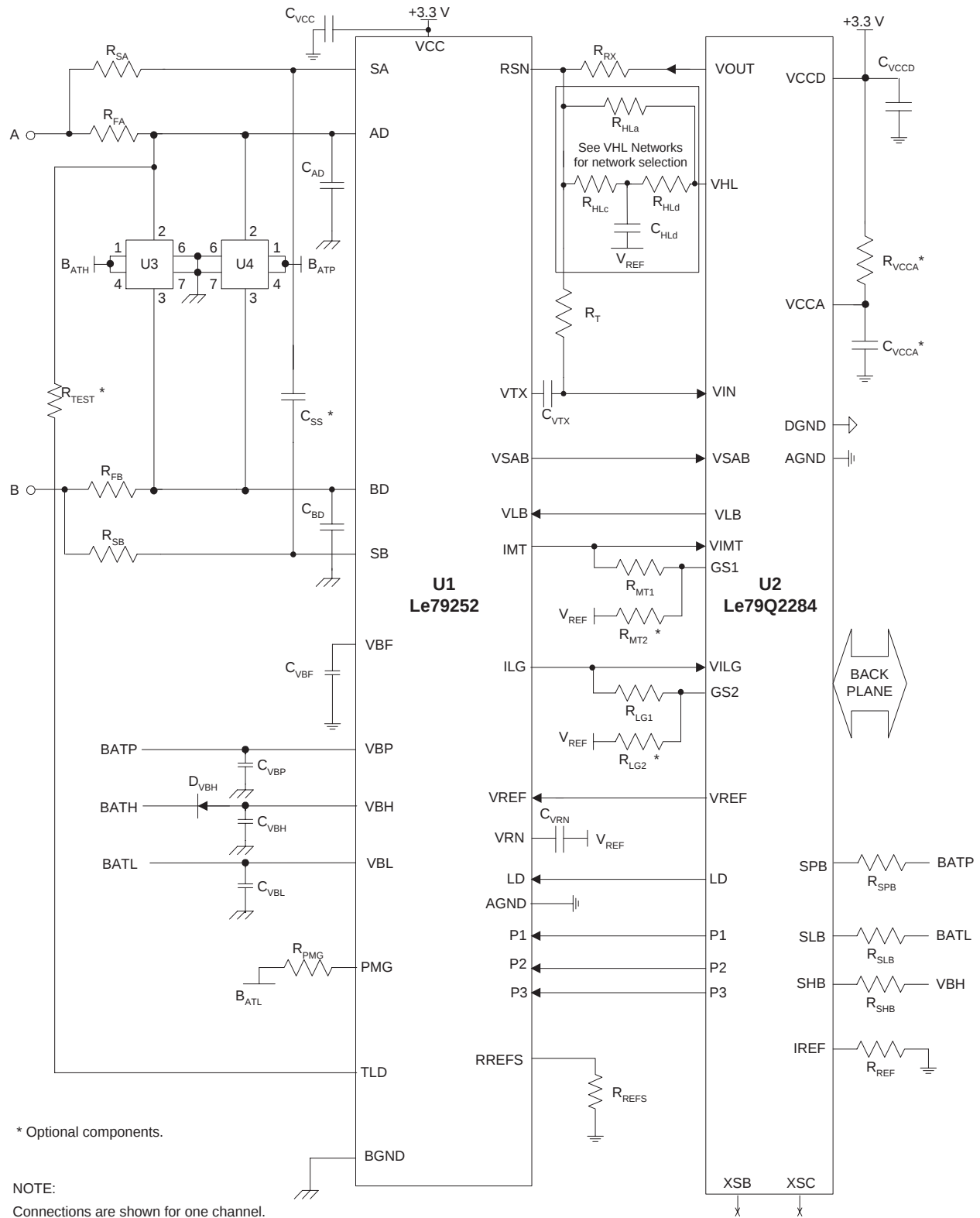
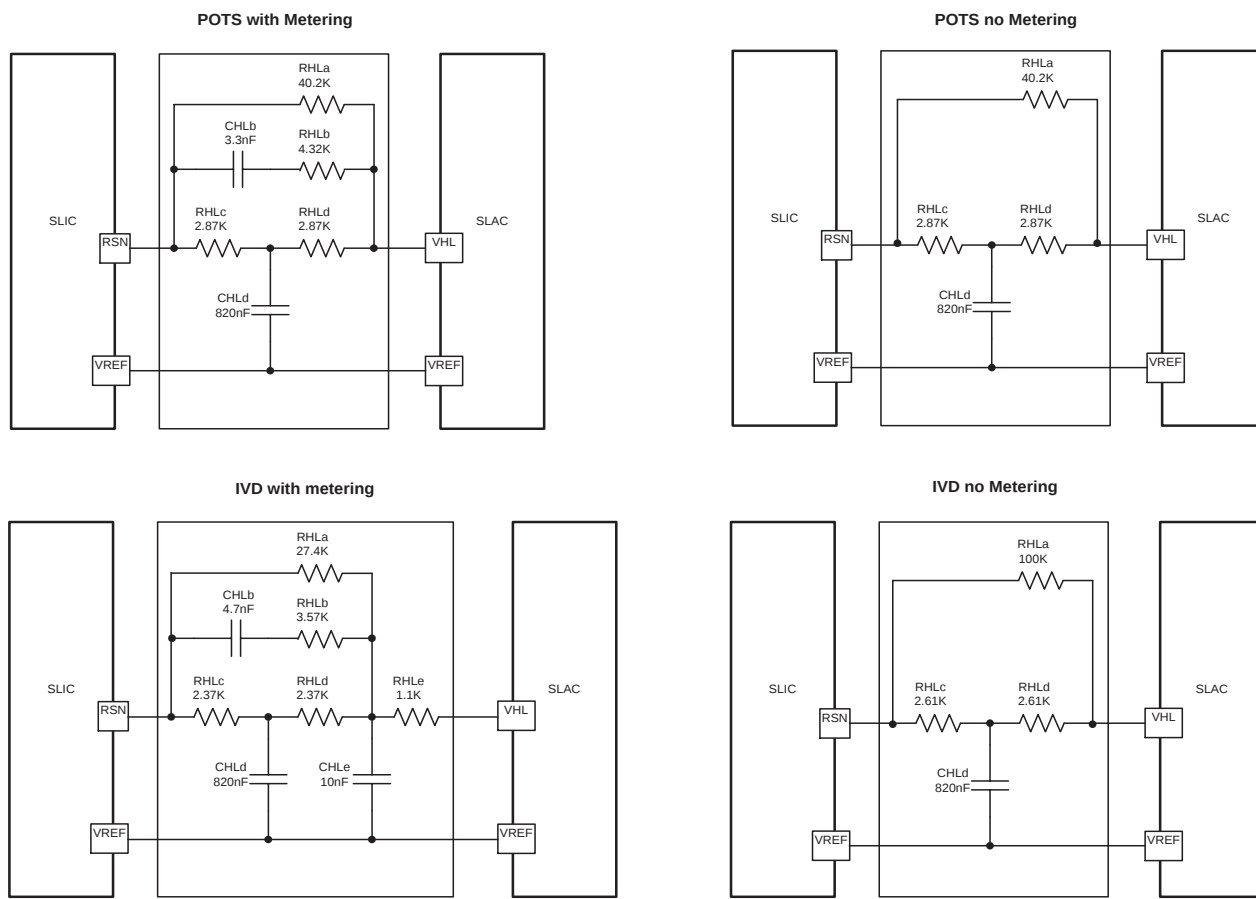


Figure 19. VHL networks for POTS and IVD Applications with and without Metering

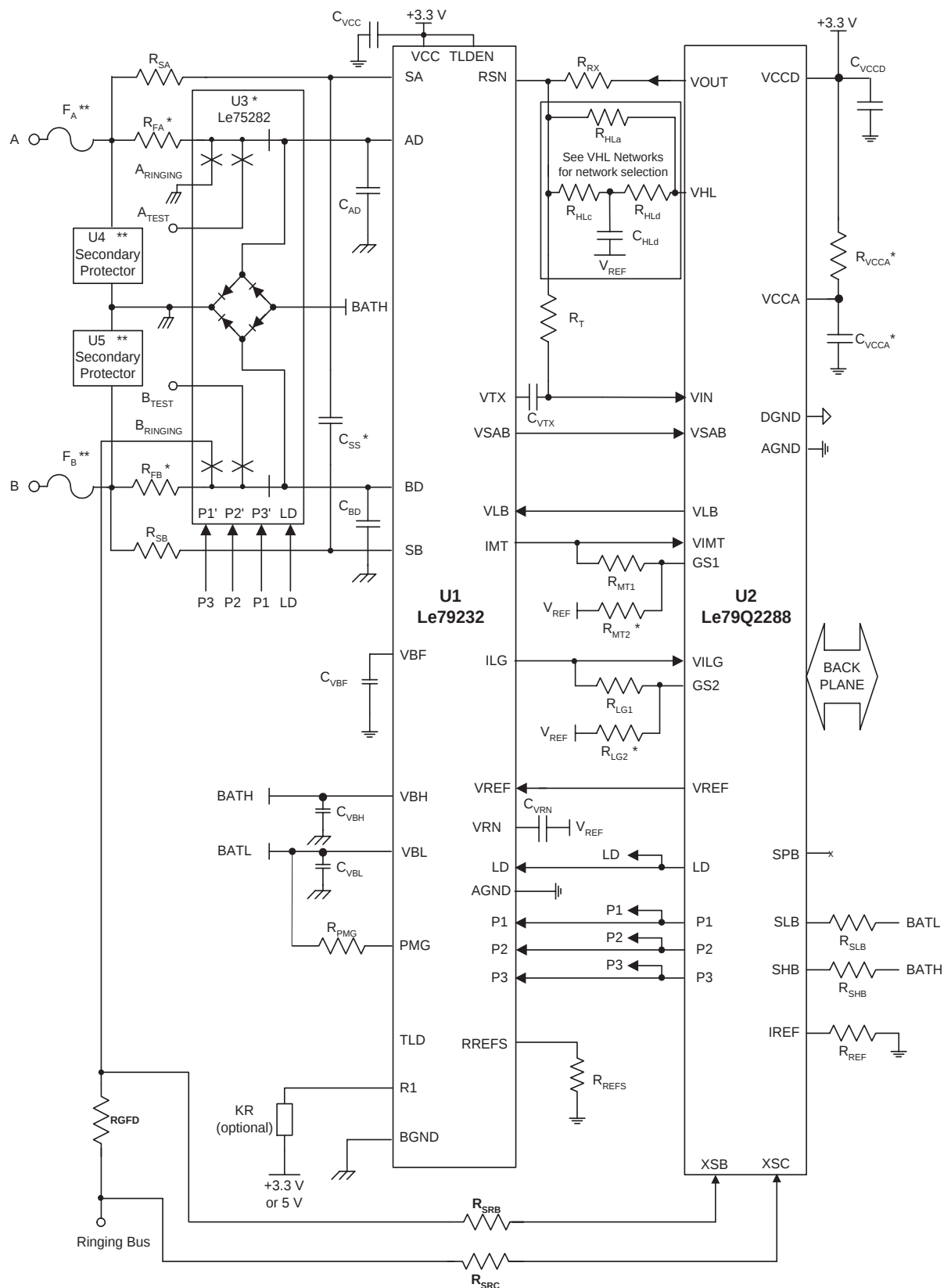


LINE CARD PARTS LIST- INTERNAL RINGING

The following list defines the parts and part values required to meet target specification limits for 8 line card channels..

Item	Qty	Type	Value	Tol.	Rating	Comments
U1	4	Le79252				Dual ISLIC device
U2	1	Le792288				Octal ISLAC device
U3	8	TISP8200M				Bourns® Negative Overvoltage Protector
U4	8	TISP8201M				Bourns® Positive Overvoltage Protector
DVBH	2	Diode	100 mA		100 V	Optional
RFA, RFB	8 ea	Resistor	50 Ω	2%	2 W	Fusible or PTC protection resistors
RSA, RSB	8 ea	Resistor	200 k Ω	1%	3/4 W	Sense resistors
RT	8	Resistor	80.6 k Ω	1%	1/10 W	Impedance control resistor
RRX	8	Resistor	90.9 k Ω	1%	1/10 W	Receive path gain resistor
CVTX	8	Capacitor	100 nF	10%	50 V	
RREF	2	Resistor	69.8 k Ω	1%	1/10 W	Current reference setting resistor
RSHB, RSLB, RSPB	2 ea	Resistor	750 k Ω	1%	1/10 W	Battery sense resistors
RHLa	8	Resistor	40.2 k Ω	1%	1/10 W	Only required for metering.
RHLb	8	Resistor	4.32 k Ω	1%	1/10 W	Only required for metering.
RHLc, RHLd	8 ea	Resistor	2.87 k Ω	1%	1/10 W	Feed resistors, see VHL networks for IVD values
CHLb	8	Capacitor	3.3 nF	10%	10 V	Only required for metering. - Not Polarized
CHLd	8	Capacitor	0.82 μ F	10%	10 V	Feed capacitor - Ceramic
CSS	8	Capacitor	33 or 56 pF	5%	100 V	Only required for metering > 2.2 Vrms, otherwise omit. Ceramic, use 33 pF for 3.2 Vrms max. or 56 pF for 5.0 Vrms max. metering.
RMT1	8	Resistor	3.01 k Ω	1%	1/10 W	Metallic loop current gain resistor
RMT2	8	Resistor	75 k Ω	1%	1/10 W	(Optional) Metallic loop current resistor for high gain selection
RLG1	8	Resistor	6.04 k Ω	1%	1/10 W	Longitudinal loop current gain resistor
RLG2	8	Resistor	150 k Ω	1%	1/10 W	(Optional) Longitudinal loop current resistor for high gain selection
RREFS	4	Resistor	56.2 k Ω	1%	1/10 W	
RPMG	8	Resistor	510 Ω	5%	1 W	Value should be adjusted to suit application.
RTEST	8	Resistor	2 k Ω	1%	1/2 W	(Optional) Test load
CAD, CBD	8 ea	Capacitor	15 nF	10%	200 V	Ceramic, X7R dielectric
CBATH, CBATL, CBATP	4 ea	Capacitor	100 nF	20%	100 V	Ceramic
CVBF	8	Capacitor	1 nF	20%	100 V	Ceramic
CVRN	8	Capacitor	100 nF	20%	10 V	
RVCCA	2	Resistor	3.3 Ω	1%	1/10 W	(Optional) Required for IVD and metering applications
CVCCA	2	Capacitor	33 μ F	20%	6.3 V	(Optional) Required for IVD and metering applications - Tantalum.

Figure 20. External Ringing Line Schematic



* Optional components.

** Consult Legerity for an optimized protection recommendation.

NOTE: Connections are shown for one channel.

LINE CARD PARTS LIST - EXTERNAL RINGING

The following list defines the parts and part values required to meet target specification limits for 8 line card channels.

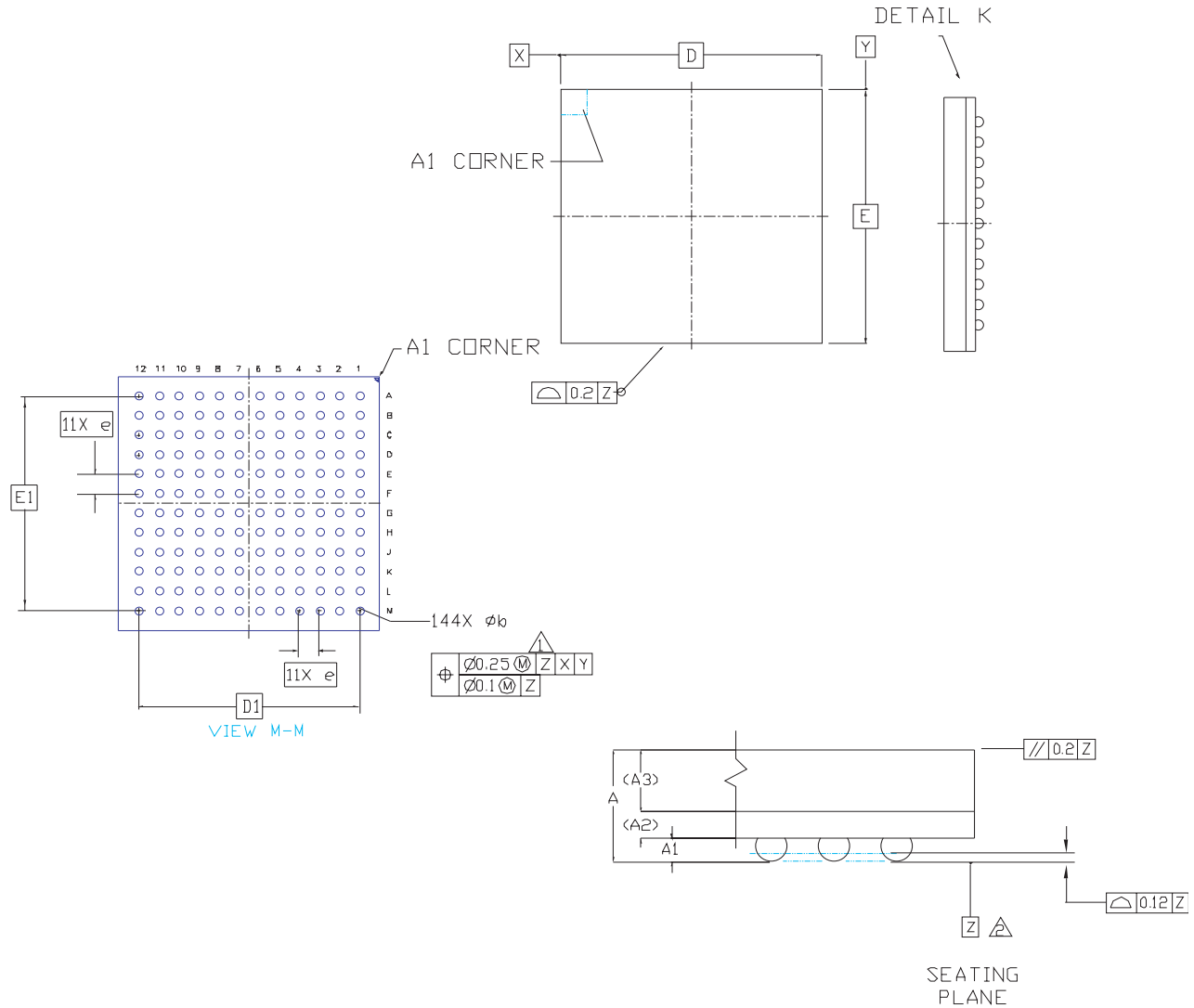
Item	Qty	Type	Value	Tol.	Rating	Comments
U1	4	Le79232				Dual ISLIC device
U2	1	Le792288				Octal ISLAC device
U3	4	Le75282				(Optional) Dual Line Card Access Switch
U4, U5	8 ea	TISP4250H3				Bourns® Overvoltage Protector
RFA, RFB	8 ea	Resistor	50 Ω	2%	2 W	Fusible or PTC protection resistors, not required when Le75282 is used
RSA, RSB	8 ea	Resistor	200 k Ω	1%	1/2 W	Sense resistors, pulse withstanding component
RT	8	Resistor	80.6 k Ω	1%	1/10 W	Impedance control resistor
RRX	8	Resistor	90.9 k Ω	1%	1/10 W	Receive path gain resistor
CVTX	8	Capacitor	100 nF	10%	50 V	
RREF	2	Resistor	69.8 k Ω	1%	1/10 W	Current reference setting resistor
RSHB, RSLB	2 ea	Resistor	750 k Ω	1%	1/10 W	Battery sense resistors
RHLa	8	Resistor	40.2 k Ω	1%	1/10 W	Only required for metering.
RHLb	8	Resistor	4.32 k Ω	1%	1/10 W	Only required for metering.
RHLc, RHLd	8 ea	Resistor	2.87 k Ω	1%	1/10 W	Feed resistors, see VHL networks for IVD values
CHLb	8	Capacitor	3.3 nF	10%	10 V	Only required for metering. - Not Polarized
CHLd	8	Capacitor	0.82 μ F	10%	10 V	Feed capacitor -Ceramic
RMT1	8	Resistor	3.01 k Ω	1%	1/10 W	Metallic loop current gain resistor
RMT2	8	Resistor	75 k Ω	1%	1/10 W	(Optional) Metallic loop current resistor for high gain selection
RLG1	8	Resistor	6.04 k Ω	1%	1/10 W	Longitudinal loop current gain resistor
RLG2	8	Resistor	150 k Ω	1%	1/10 W	(Optional) Longitudinal loop current resistor for high gain selection
RREFS	4	Resistor	56.2 k Ω	1%	1/10 W	
RPMG	8	Resistor	510 Ω	5%	1 W	Value should be adjusted to suit application.
RTEST	8	Resistor	2 k Ω	1%	1/2 W	(Optional) Test load (not shown on Application Circuit)
CAD, CBD	8 ea	Capacitor	15 nF	10%	200 V	Ceramic, X7R dielectric
CBATH, CBATL	4 ea	Capacitor	100 nF	20%	100 V	Ceramic
CSS	8	Capacitor	56 pF	5%	100 V	Only required for metering > 2.2 Vrms - Ceramic
CVBF	8	Capacitor	1 nF	20%	100 V	Ceramic
CVRN	8	Capacitor	100 nF	20%	10 V	
RVCCA	2	Resistor	3.3 Ω	1%	1/10 W	(Optional) Required for IVD and metering applications
CVCCA	2	Capacitor	33 μ F	20%	6.3 V	(Optional) Required for IVD and metering applications - Tantalum
RGFD	8	Resistor	510 Ω	2%	2W	

RSRB	8	Resistor	750 k Ω	1%	1/4 W	
RSRC	2	Resistor	750 k Ω	1%	1/4 W	
KR	8	Relay	+3.3V or +5 V Coil			(Optional) Test Out DPDT relay (contacts not shown on schematic)

PHYSICAL DIMENSIONS

144-Pin Ball Grid Array (BGA)

LFBGA 144BALLS 13X13X1.6 1.0MM PITCH
PACKAGE OUTLINE DRAWING



DIM	MIN	MAX	NOTES		
A	1.25	1.6	⚠ DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z. ⚠ DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS. ⚠ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.		
A1	0.27	0.47			
A2	0.32 REF				
A3	0.8 REF				
b	0.4	0.6			
D	13 BSC				
E	13 BSC				
e	1 BSC				
D1	11 BSC				
E1	11 BSC				
			UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
			MM	ASME_Y14.5M	98ASH70694A-A

REVISION HISTORY

Revision A1 to B1

- Changed OPN to reflect green package
- Replaced DIO references with DIN and DOUT
- Removed 80-pin TQFP references; TTL-compatible removed from I/O pins
- In [Absolute Maximum Ratings, on page 10](#), Latch up immunity modified for pin I/O4
- In [DC Specifications, on page 11](#), No.2, changed min from 2.36 to 2.46 min; condition criteria added to No. 14, 21, 22, 26
- In [Transmission Specifications, on page 12](#), No. 1, modified conditions and changed min/max from 0.34 to 0.25
- Updated Application Circuits and BOMs

Revision B1 to C1

- Document updated from Preliminary Data Sheet to Final Data Sheet.
- Pin Descriptions on pages 8 and 9, GS, VILG, VIMT, and VIN descriptions enhanced.
- In DC Specifications on page 11, No. 4, DCLK/S0 added to Input hysteresis.
- In Microprocessor Interface on page 20, loading for all digital outputs changed to 150 pF.
- In Microprocessor Interface on page 20, rise and fall time of clock are increased from 15 ns to 25 ns. Also, output data turn on and turn off delay and output data valid are all reduced from 50 ns to 35 ns.
- Pages 27 - 32, Application Circuits and Line Card Parts Lists updated.
- Page 28, VHL Networks for POTS and IVD Applications added.

Revision C1 to D1

- [DC Specifications, on page 11](#), No. 29 Power Dissipation, Condition changed from three channels inactive to seven channels inactive.
- [PCM Interface, on page 20](#), output loading added. DXA and DXB loading changed from 150 pF to 80 pF.

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