

LM161/LM361 High Speed Differential Comparators

Check for Samples: [LM161](#), [LM361](#)

FEATURES

- Independent strobes
- Ensured high speed: 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies: $\pm 15\text{V}$
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

DESCRIPTION

The LM161/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies ($\pm 15\text{V}$).

Complementary outputs having maximum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disk file systems.

CONNECTION DIAGRAMS

SOIC or PDIP Package

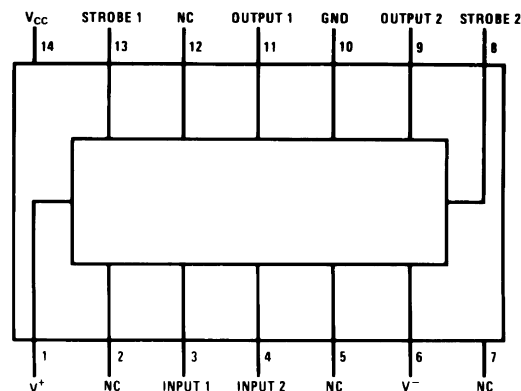


Figure 1. Top View
Package Numbers D0014A, NFF0014A

TO-100 Package

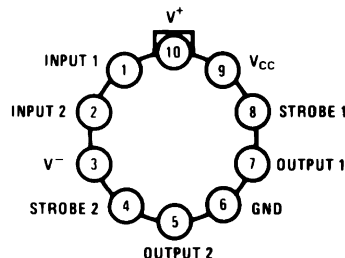


Figure 2. Package Number LME0010C



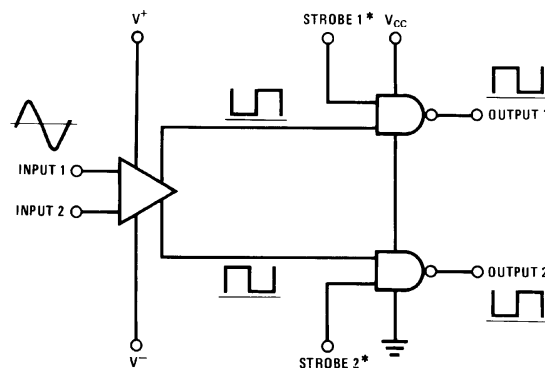
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LOGIC DIAGRAM



*Output is low when current is drawn from strobe pin.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾

Positive Supply Voltage, V ⁺	+16V
Negative Supply Voltage, V ⁻	-16V
Gate Supply Voltage, V _{CC}	+7V
Output Voltage	+7V
Differential Input Voltage	±5V
Input Common Mode Voltage	±6V
Power Dissipation	600 mW
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	T_{MIN} T_{MAX}
LM161	-55°C to +125°C
	-25°C to +85°C
LM361	0°C to +70°C
Lead Temp. (Soldering, 10 seconds)	260°C
For Any Device Lead Below V ⁻	0.3V

(1) The device may be damaged by use beyond the maximum ratings.

Operating Conditions

Operating Conditions			Min	Typ	Max
Supply Voltage V ⁺	LM161		5V		15V
	LM361		5V		15V
Supply Voltage V ⁻	LM161		-6V		-15V
	LM361		-6V		-15V
Supply Voltage V _{CC}	LM161		4.5V	5V	5.5V
	LM361		4.75V	5V	5.25V
ESD Tolerance ⁽¹⁾					1600V
Soldering Information ⁽²⁾	PDIP Package	Soldering (10 seconds) ⁽²⁾			260°C
	SOIC Package	Vapor Phase (60 seconds)			215°C
		Infrared (15 seconds)			220°C

(1) Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

(2) See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics⁽¹⁾⁽²⁾⁽¹⁾
 $(V^+ = +10V, V_{CC} = +5V, V^- = -10V, T_{MIN} \leq T_A \leq T_{MAX}, \text{ unless noted})$

Parameter	Conditions	Limits						Units
		LM161			LM361			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			1	3		1	5	mV
Input Bias Current	T _A =25°C		5	20		10	30	μA μA
Input Offset Current	T _A =25°C		2	3		2	5	μA μA
Voltage Gain	T _A =25°C		3			3		V/mV
Input Resistance	T _A =25°C, f=1 kHz		20			20		kΩ
Logical “1” Output Voltage	V _{CC} =4.75V, I _{SOURCE} =−0.5 mA	2.4	3.3		2.4	3.3		V
Logical “0” Output Voltage	V _{CC} =4.75V, I _{SINK} =6.4 mA			0.4			0.4	V
Strobe Input “1” Current (Output Enabled)	V _{CC} =5.25V, V _{STROBE} =2.4V			200			200	μA
Strobe Input “0” Current (Output Disabled)	V _{CC} =5.25V, V _{STROBE} =0.4V			−1.6			−1.6	mA
Strobe Input “0” Voltage	V _{CC} =4.75V			0.8			0.8	V
Strobe Input “1” Voltage	V _{CC} =4.75V	2			2			V
Output Short Circuit Current	V _{CC} =5.25V, V _{OUT} =0V	−18		−55	−18		−55	mA
Supply Current I ⁺	V ⁺ =10V, V [−] =−10V, V _{CC} =5.25V, −55°C≤T _A ≤125°C			4.5				mA
Supply Current I ⁺	V ⁺ =10V, V [−] =−10V, V _{CC} =5.25V, 0°C≤T _A ≤70°C						5	mA
Supply Current I [−]	V ⁺ =10V, V [−] =−10V, V _{CC} =5.25V, −55°C≤T _A ≤125°C			10				mA
Supply Current I [−]	V ⁺ =10V, V [−] =−10V, V _{CC} =5.25V, 0°C≤T _A ≤70°C						10	mA
Supply Current I _{CC}	V ⁺ =10V, V [−] =−10V, V _{CC} =5.25V, −55°C≤T _A ≤125°C			18				mA
Supply Current I _{CC}	V ⁺ =10V, V [−] =−10V, V _{CC} =5.25V, 0°C≤T _A ≤70°C						20	mA
Transient Response	V _{IN} = 50 mV overdrive ⁽³⁾							
Propagation Delay Time (t _{pd(0)})	T _A =25°C		14	20		14	20	ns
Propagation Delay Time (t _{pd(1)})	T _A =25°C		14	20		14	20	ns
Delay Between Output A and B	T _A =25°C		2	5		2	5	ns
Strobe Delay Time (t _{pd(0)})	T _A =25°C		8			8		ns
Strobe Delay Time (t _{pd(1)})	T _A =25°C		8			8		ns

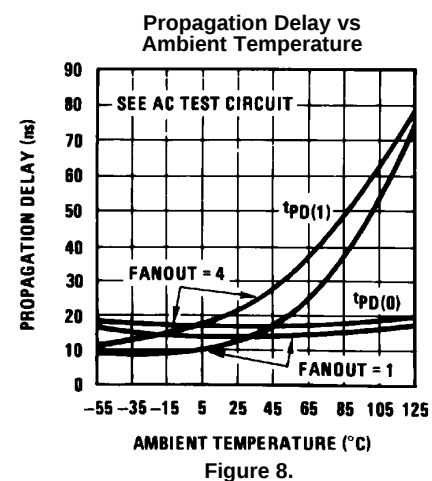
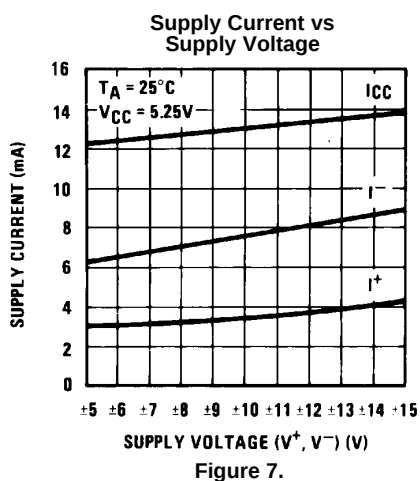
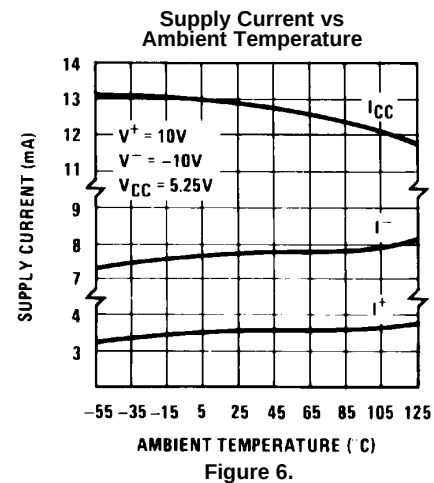
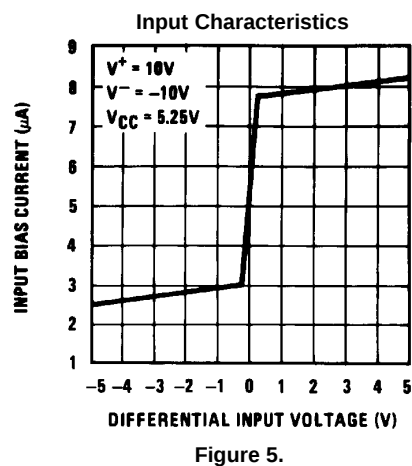
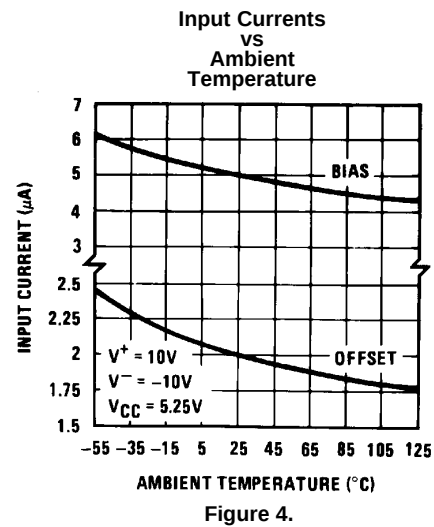
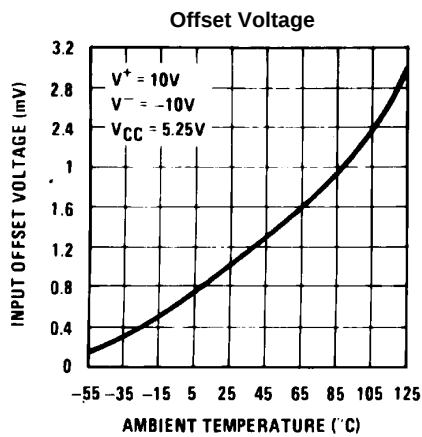
(1) Typical thermal impedances are as follows:

	H Package	J Package	N Package
θ_{JA}	165°C/W (Still Air) 67°C/W (400 LF/Min Air Flow)	112°C/W	105°C/W
θ_{JC}	25°C/W		

(2) Refer to RETS161X for LM161H and LM161J military specifications.

(3) Measurements using AC Test circuit, Fanout = 1. The devices are faster at low supply voltages.

Typical Performance Characteristics



Typical Performance Characteristics (continued)

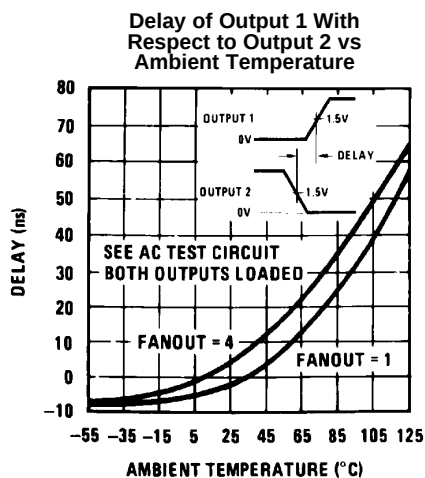


Figure 9.

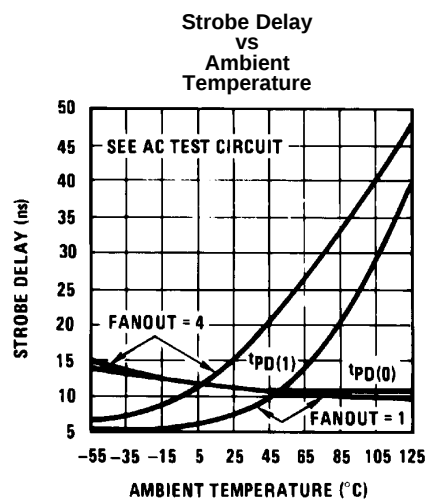


Figure 10.

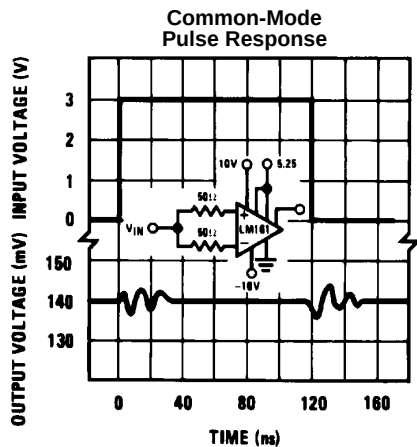


Figure 11.

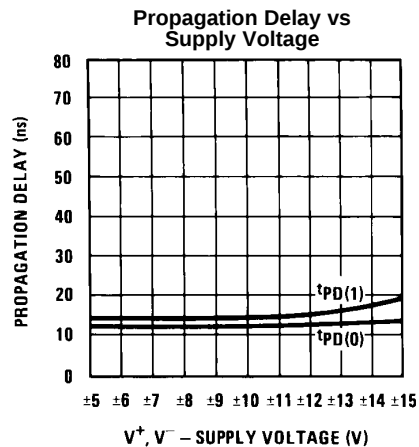
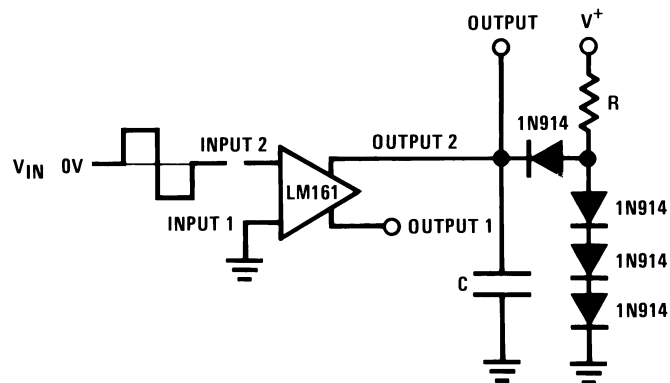


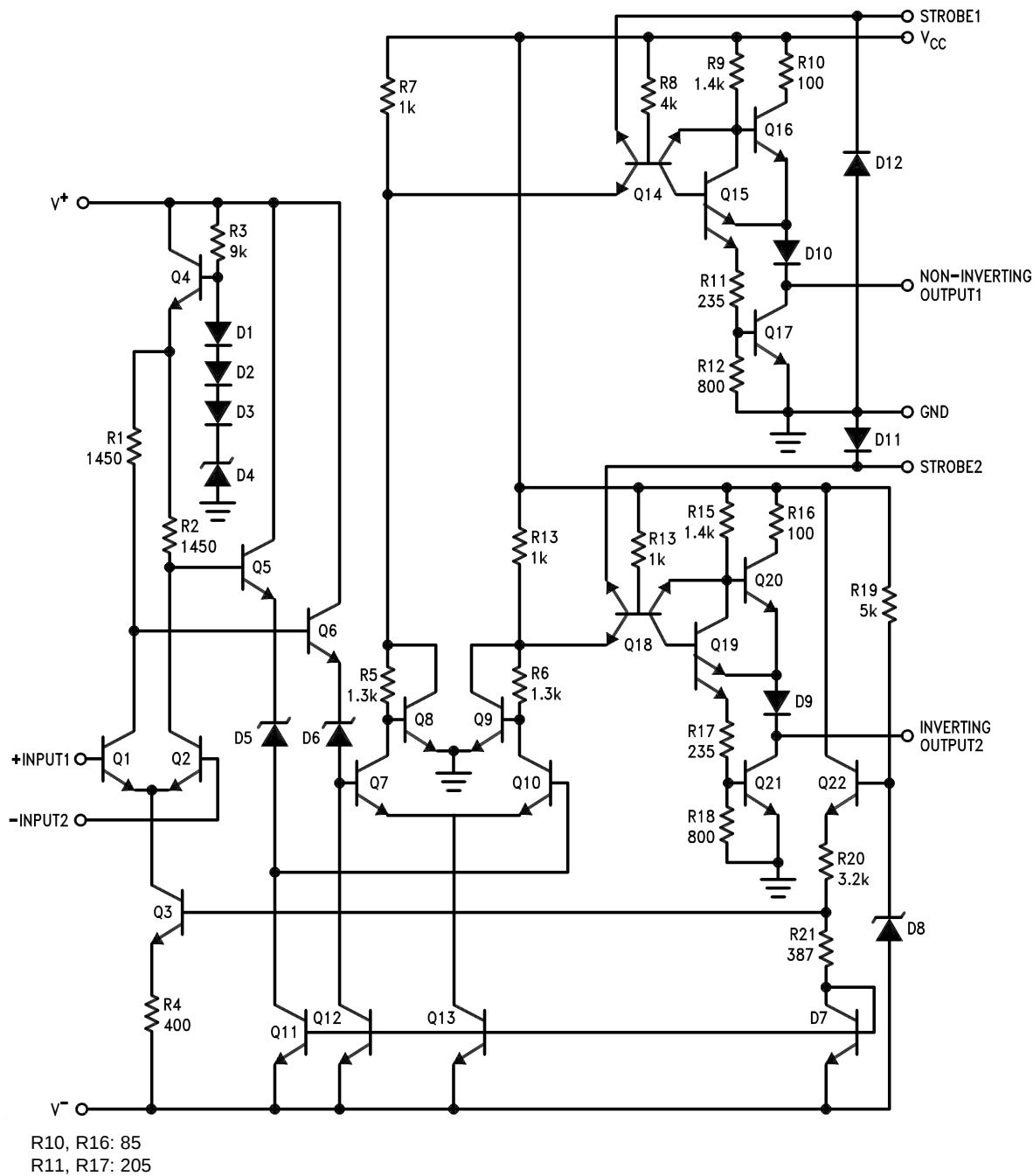
Figure 12.

AC TEST CIRCUIT

$V_{IN} = \pm 50 \text{ mV}$	FANOUT = 1	FANOUT = 4	$V^- = -10\text{V}$	$C = 15 \text{ pF}$	$C = 30 \text{ pF}$
$V^+ = +10\text{V}$	$R = 2.4\text{k}$	$R = 680\Omega$	$V_{CC} = 5.25\text{V}$		

SCHEMATIC DIAGRAM

LM161



REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM361H	ACTIVE	TO-100	LME	10	500	TBD	Call TI	Call TI	0 to 70	(LM361H ~ LM361H)	Samples
LM361H/NOPB	ACTIVE	TO-100	LME	10	500	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	0 to 70	(LM361H ~ LM361H)	Samples
LM361M	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	0 to 70	LM361M	
LM361M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM361M	Samples
LM361MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM361M	Samples
LM361N/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM361N	Samples
LM529CH	ACTIVE	TO-100	LME	10	500	TBD	Call TI	Call TI	0 to 70	(LM361H ~ LM361H)	Samples
LM529CN	OBSOLETE	PDIP	NFF	14		TBD	Call TI	Call TI	0 to 70	LM361N	
NE529A	OBSOLETE	PDIP	NFF	14		TBD	Call TI	Call TI	0 to 70	LM361N	
NE529K	ACTIVE	TO-100	LME	10	500	TBD	Call TI	Call TI	0 to 70	(LM361H ~ LM361H)	Samples
SE529K	ACTIVE	TO-100	LME	10	500	TBD	Call TI	Call TI	0 to 70	(LM361H ~ LM361H)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- ⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- ⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- ⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- ⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM361MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

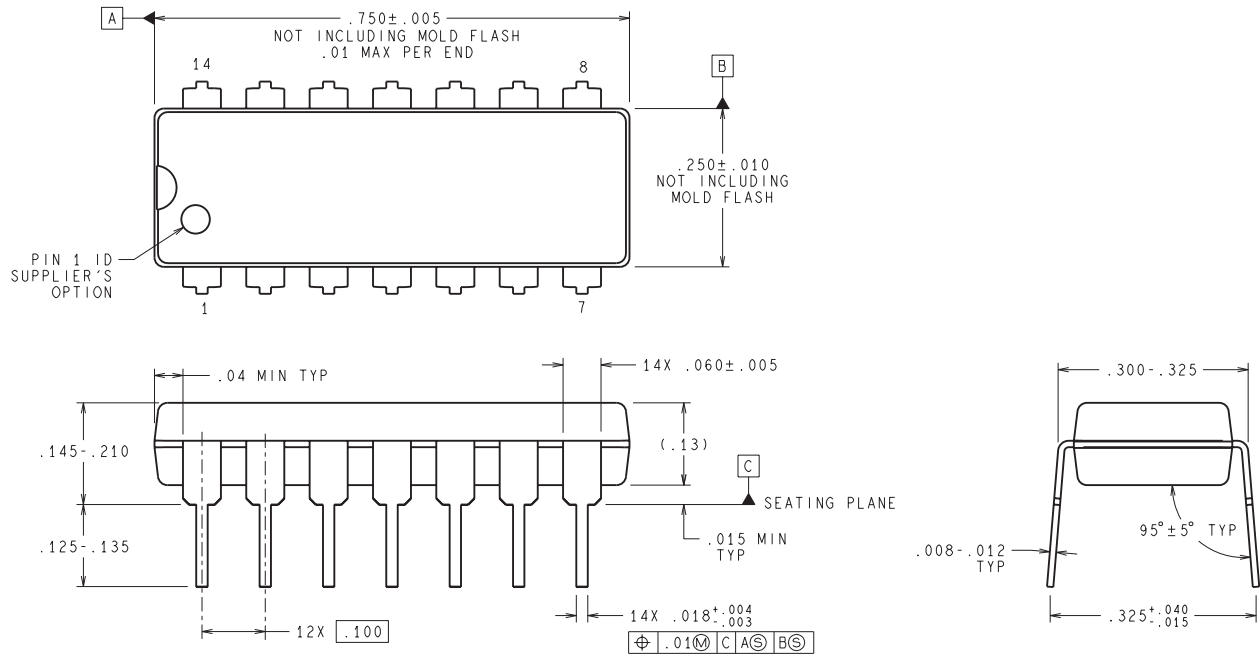
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM361MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

METAL CYLINDRICAL PACKAGE



- 

NFF0014A



DIMENSIONS ARE IN INCHES
DIMENSIONS IN () FOR REFERENCE ONLY

N14A (Rev G)

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

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