LM4941 **Boomer**® Audio Power Amplifier Series **1.25 Watt Fully Differential Audio Power Amplifier With RF Suppression and Shutdown**

Check for Samples: **LM4941**, **LM4941SDBD**, **LM4941TMBD**

FEATURES

- **Improved RF Suppression, By Up to 20dB Over Previous Designs in Selected Applications**
- **Fully Differential Amplification**
- **Available in Space-Saving DSBGA Package**
- **Ultra Low Current Shutdown Mode**
- **Can Drive Capacitive Loads up to 100pF**
- **Improved Pop & Click Circuitry Eliminates Noises During Turn-On and Turn-Off Transitions**
- **2.4 - 5.5V Operation**
- **No Output Coupling Capacitors, Snubber Networks or Bootstrap Capacitors Required**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Portable Electronic Devices**

KEY SPECIFICATIONS

- **Improved PSRR at 217Hz 95dB (typ)**
- **Power Output, V_{DD} = 5.0V, R_L = 8Ω, 1% THD+N 1.25W (typ)**
- **Power Output, V_{DD} = 3.0V, R_L = 8Ω, 1% THD+N 430mW (typ)**
- **Shutdown Current 0.1µA (typ)**

DESCRIPTION

The LM4941 is a fully differential audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1.25 watts of continuous average power to a 8Ω load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply. The LM4941 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other small form factor applications where minimal PCB space is a primary requirement.

The LM4941 also features proprietary internal circuitry that suppresses the coupling of RF signals into the chip. This is important because certain types of RF signals (such as GSM) can couple into audio amplifiers in such a way that part of the signal is heard through the speaker. The RF suppression circuitry in the LM4941 makes it well-suited for portable applications in which strong RF signals generated by an antenna from or a cellular phone or other portable electronic device may couple audibly into the amplifier.

Other features include a low-power consumption shutdown mode, internal thermal shutdown protection, and advanced pop & click circuitry.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

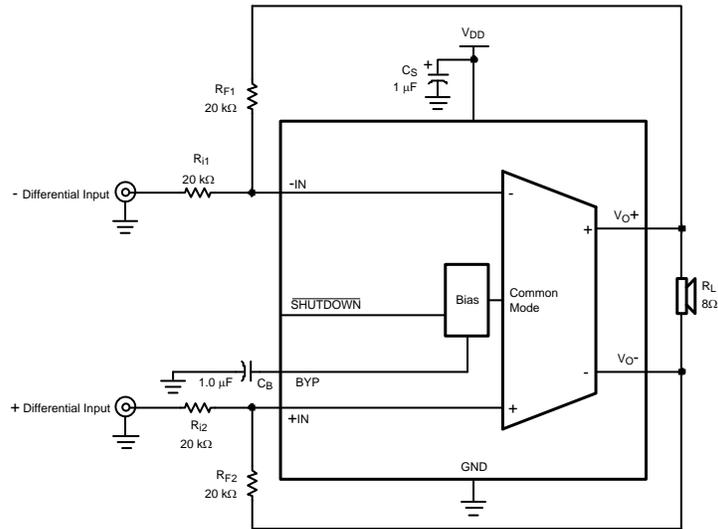All trademarks are the property of their respective owners.

Typical Application

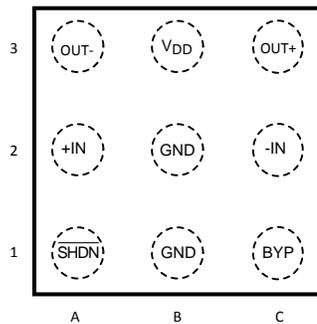**Figure 1. Typical Audio Amplifier Application Circuit**

Connection Diagram

Figure 2. 9-Bump DSBGA - Top View
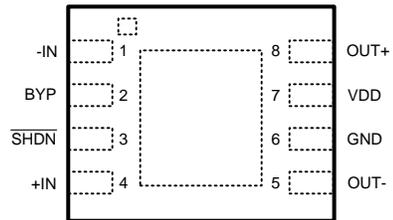**See YFQ0009 Package**

Figure 3. 8-Pin WSON - Top View
See NGS0008C Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation[4][5]		Internally Limited
ESD Susceptibility[6]		2000V
ESD Susceptibility[7]		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (TM)	100°C/W
	θ_{JA} (WSON)	71°C/W
Soldering Information		See AN-1187 (SNOA401)

(1)   All voltages are measured with respect to the ground pin, unless otherwise specified.
(2)   *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3)   If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4)   The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} – T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4941, see power derating curve for additional information.
(5)   Maximum Power Dissipation (P_{DMAX}) in the device occurs at an output power level significantly below full output power. P_{DMAX} can be calculated using Equation 3 shown in the Application section. It may also be obtained from the Power Dissipation graphs.
(6)   Human body model, 100pF discharged through a 1.5kΩ resistor.
(7)   Machine Model, 220pF – 240pF discharged through all pins.

Operating Ratings

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ 85°C
Supply Voltage	2.4V ≤ V_{DD} ≤ 5.5V

Electrical Characteristics V_{DD} = 5V[1][2]

The following specifications apply for V_{DD} = 5V, A_V = 1V/V, and 8Ω load unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4941		Units (Limits)
			Typical[3]	Limit[4][5]	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, no load V_{IN} = 0V, R_L = 8Ω	1.7 1.7	2.3	mA (max) mA
I_{SD}	Shutdown Current	V_{SHDN} = GND	0.1	0.8	µA (max)
P_O	Output Power	THD+N = 1% (max); f = 1 kHz R_L = 8Ω	1.25	1.15	W (min)
		THD+N = 10% (max); f = 1 kHz R_L = 8Ω	1.54		W
THD+N	Total Harmonic Distortion + Noise	P_O = 0.7 W; f = 1kHz	0.04		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P} Sine			
		f = 217Hz[6]	95	80	dB (min)
		f = 1kHz[6]	90		dB

(1)   All voltages are measured with respect to the ground pin, unless otherwise specified.
(2)   *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3)   Typicals are measured at 25°C and represent the parametric norm.
(4)   Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5)   Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6)   10Ω terminated input.

LM4941, LM4941SDBD, LM4941TMBD

Electrical Characteristics V_{DD} = 5V[(1)(2)] (continued)

The following specifications apply for V_{DD} = 5V, A_V = 1V/V, and 8Ω load unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4941		Units (Limits)
			Typical[(3)]	Limit[(4)(5)]	
CMRR	Common-Mode Rejection Ratio	f = 217Hz, V_{CM} = 200mV_{P-P} Sine	70		dB
		f = 20Hz–20kHz , V_{CM} = 200mV_{pp}	70		dB
V_{OS}	Output Offset Voltage	V_{IN} = 0V	2	6	mV (max)
V_{SDIH}	Shutdown Voltage Input High			1.4	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V (max)
SNR	Signal-to-Noise Ratio	P_O = 1W, f = 1kHz	108		dB
T_{WU}	Wake-up Time from Shutdown	C_{BYPASS} = 1µF	12		ms

Electrical Characteristics V_{DD} = 3V[(1)(2)]

The following specifications apply for V_{DD} = 3V, A_V = 1V/V, and 8Ω load unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4941		Units (Limits)
			Typical[(3)]	Limit[(4)(5)]	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, no load V_{IN} = 0V, R_L = 8Ω	1.6 1.6	2.2	mA (max) mA
I_{SD}	Shutdown Current	V_{SHDN} = GND	0.1	0.8	µA (max)
P_O	Output Power	THD+N = 1% (max); f = 1 kHz R_L = 8Ω	0.43		W
		THD+N = 10% (max); f = 1 kHz R_L = 8Ω	0.54		W
THD+N	Total Harmonic Distortion + Noise	P_O = 0.25W; f = 1kHz	0.05		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP} Sine			
		f = 217Hz[(6)]	95		dB
		f = 1kHz[(6)]	90		dB
CMRR	Common-Mode Rejection Ratio	f = 217Hz, V_{CM} = 200mV_{PP} Sine	70		dB
V_{OS}	Output Offset Voltage	V_{IN} = 0V	2	6	mV (max)
V_{SDIH}	Shutdown Voltage Input High			1.4	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V (max)
T_{WU}	Wake-up Time from Shutdown	C_{BYPASS} = 1µF	8		ms

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) 10Ω terminated input.

Product Folder Links: *LM4941 LM4941SDBD LM4941TMBD*

External Components Description

([Figure 1](#))

Components		Functional Description
1.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the Power Supply Bypassing section for information concerning proper placement and selection of the supply bypass capacitor.
2.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, Proper Selection of External Components, for information concerning proper placement and selection of C_B.
3.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_F.
4.	R_F	External feedback resistance which sets the closed-loop gain in conjunction with R_i.

Typical Performance Characteristics

Data taken with Bandwidth = 80kHz, A_V = 1V/V and inputs are AC-coupled except where specified.
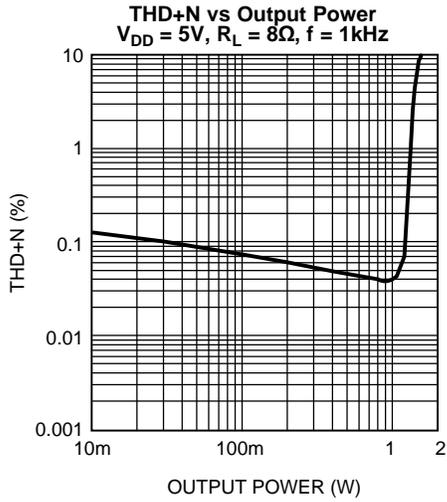
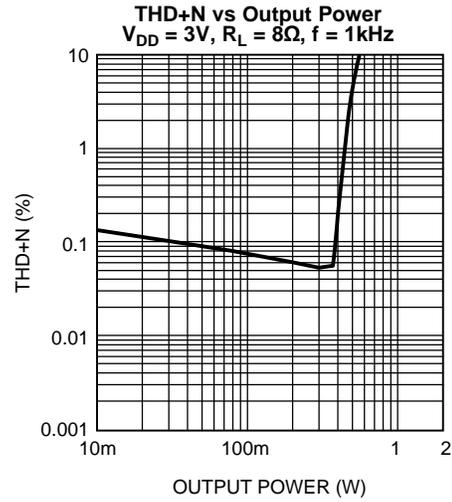**THD+N vs Output Power**
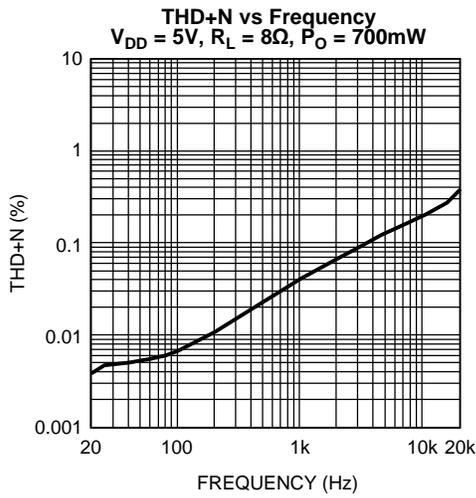V_{DD} = 5V, R_L = 8Ω, f = 1kHz

Figure 4.

THD+N vs Output Power
V_{DD} = 3V, R_L = 8Ω, f = 1kHz

Figure 5.

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 700mW

Figure 6.

THD+N vs Frequency
V_{DD} = 3V, R_L = 8Ω, P_O = 250mW

Figure 7.

PSRR vs Frequency
V_{DD} = 5V, R_L = 8Ω, Inputs terminated

Figure 8.

PSRR vs Frequency
V_{DD} = 3V, R_L = 8Ω, Inputs terminated

Figure 9.

Product Folder Links: *LM4941 LM4941SDBD LM4941TMBD*

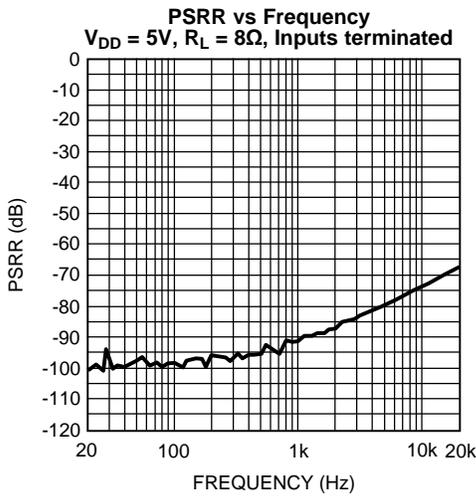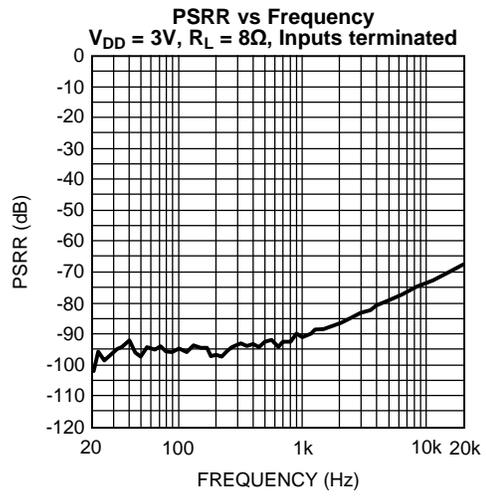## Typical Performance Characteristics (continued)

Data taken with Bandwidth = 80kHz, A_V = 1V/V and inputs are AC-coupled except where specified.

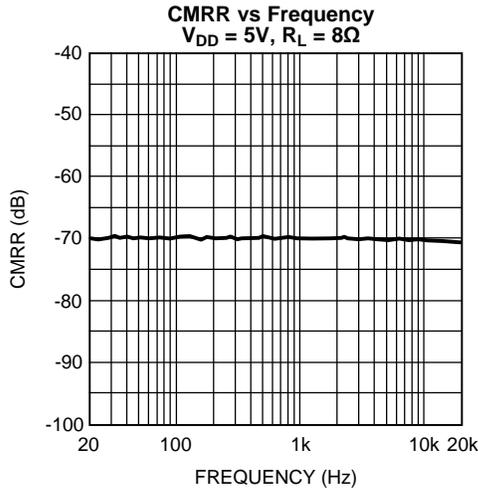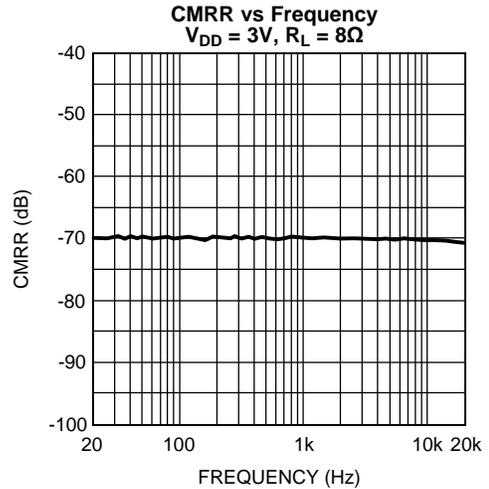**CMRR vs Frequency**
V_{DD} = 5V, R_L = 8Ω

Figure 10.

CMRR vs Frequency
V_{DD} = 3V, R_L = 8Ω

Figure 11.

PSRR vs Common Mode Voltage
V_{DD} = 5V, R_L = 8Ω, f = 217Hz

Figure 12.

PSRR vs Common Mode Voltage
V_{DD} = 3V, R_L = 8Ω, f = 217Hz

Figure 13.

Power Dissipation vs Output Power
V_{DD} = 5V, R_L = 8Ω

Figure 14.

Power Dissipation vs Output Power
V_{DD} = 3V, R_L = 8Ω

Figure 15.

Product Folder Links: *LM4941 LM4941SDBD LM4941TMBD*

Typical Performance Characteristics (continued)

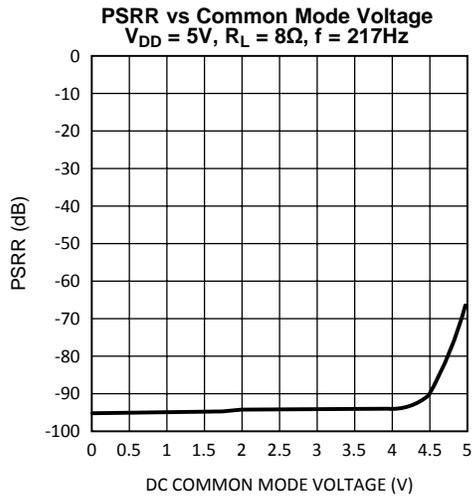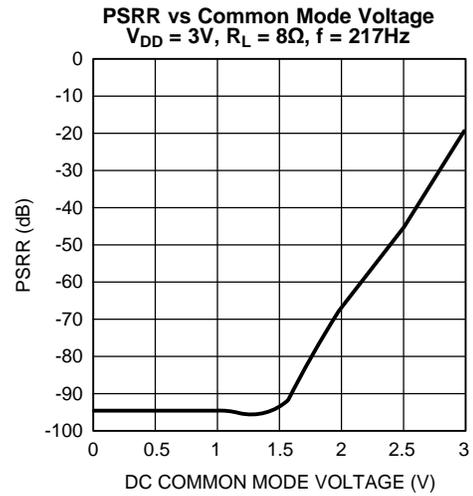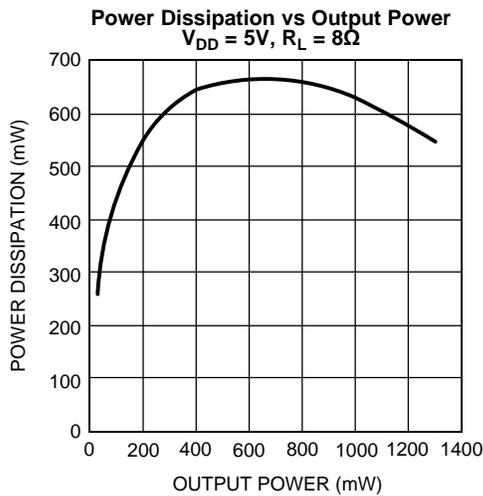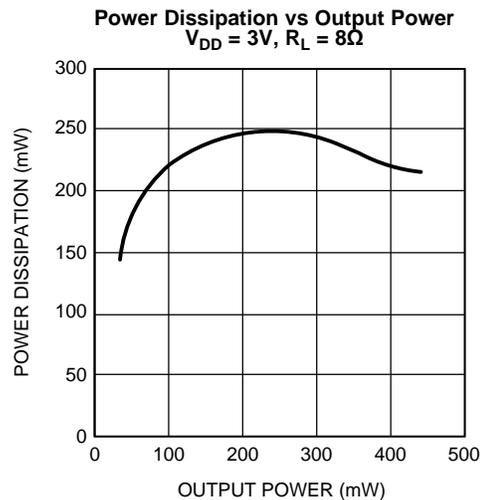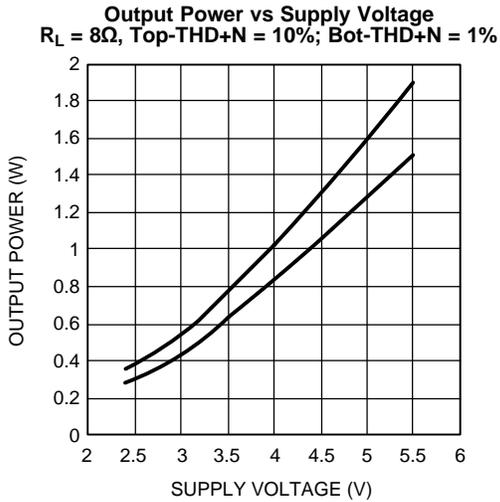Data taken with Bandwidth = 80kHz, A_V = 1V/V and inputs are AC-coupled except where specified.

Output Power vs Supply Voltage
R_L = 8Ω, Top-THD+N = 10%; Bot-THD+N = 1%

Figure 16.

Clipping Voltage vs Supply Voltage

Figure 17.

Output Power vs Load Resistance
Top-V_{DD} = 5V, 10% THD+N, Topmid-V_{DD} = 5V, 1% THD+N
Bot-V_{DD} = 3V, 10% THD+N, Botmid-V_{DD} = 3V, 1% THD+N

Figure 18.

IDDQ vs Supply Voltage

Figure 19.

Power Derating Curve
f_{IN} = 1kHz, R_L = 8Ω

Figure 20.

Product Folder Links: *LM4941 LM4941SDBD LM4941TMBD*

APPLICATION INFORMATION

OPTIMIZING RF IMMUNITY

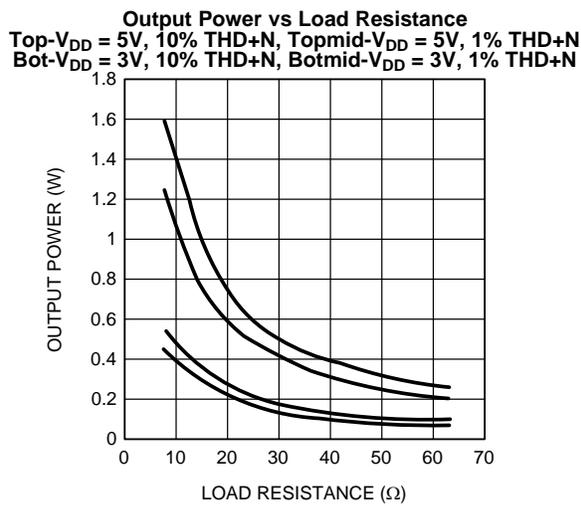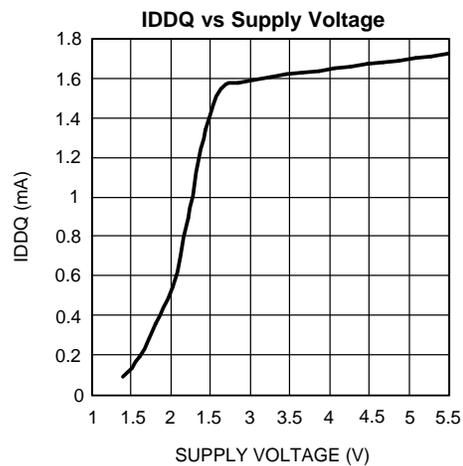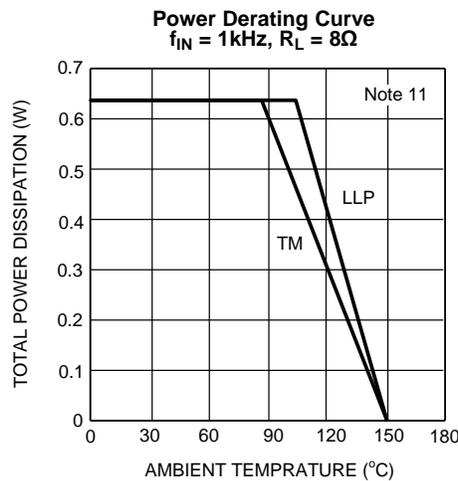The internal circuitry of the LM4941 suppresses the amount of RF signal that is coupled into the chip. However, certain external factors, such as output trace length, output trace orientation, distance between the chip and the antenna, antenna strength, speaker type, and type of RF signal, may affect the RF immunity of the LM4941. In general, the RF immunity of the LM4941 is application specific. Nevertheless, optimal RF immunity can be achieved by using short output traces and increasing the distance between the LM4941 and the antenna.

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM4941 is a fully differential audio amplifier that features differential input and output stages. Internally this is accomplished by two circuits: a differential amplifier and a common mode feedback amplifier that adjusts the output voltages so that the average value remains V_{DD} / 2. When setting the differential gain, the amplifier can be considered to have "halves". Each half uses an input and feedback resistor (R_i and R_F) to set its respective closed-loop gain (see Figure 1). With $R_{i1} = R_{i2}$ and $R_{F1} = R_{F2}$, the gain is set at $-R_F$ / R_i for each half. This results in a differential gain of

$$A_{VD} = -R_F/R_i \tag{1}$$

It is extremely important to match the input resistors to each other, as well as the feedback resistors to each other for best amplifier performance. See the Proper Selection of External Components section for more information. A differential amplifier works in a manner where the difference between the two input signals is amplified. In most applications, input signals will be 180° out of phase with each other. The LM4941 can be used, however, as a single-ended input amplifier while still retaining its fully differential benefits because it simply amplifies the difference between the inputs.

All of these applications provide what is known as a "bridged mode" output (bridge-tied-load, BTL). This results in output signals that are 180° out of phase with respect to each other. Bridged mode operation is different from the single-ended amplifier configuration that connects the load between the amplifier output and ground. A bridged amplifier design has distinct advantages over the single-ended configuration: it provides differential drive to the load, thus doubling maximum possible output swing for a specific supply voltage. Four times the output power is possible compared with a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. Choose an amplifier's closed-loop gain without causing excess clipping.

A bridged configuration, such as the one used in the LM4941, also creates a second advantage over single-ended amplifiers. Since the differential outputs are biased at half-supply, no net DC voltage exists across the load. This assumes that the input resistor pair and the feedback resistor pair are properly matched (see Proper Selection of External Components). BTL configuration eliminates the output coupling capacitor required in single-supply, single-ended amplifier configurations. If an output coupling capacitor is not used in a single-ended output configuration, the half-supply bias across the load would result in both increased internal IC power dissipation as well as permanent loudspeaker damage. Further advantages of bridged mode operation specific to fully differential amplifiers like the LM4941 include increased power supply rejection ratio, common-mode noise reduction, and click and pop reduction.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \text{ Single-Ended} \tag{2}$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation versus a single-ended amplifier operating at the same conditions.

$$P_{DMAX} = 4 * (V_{DD})^2 / (2\pi^2 R_L) \text{ Bridge Mode} \tag{3}$$

Since the LM4941 has bridged outputs, the maximum internal power dissipation is four times that of a single-ended amplifier. Even with this substantial increase in power dissipation, the LM4941 does not require additional heatsinking under most operating conditions and output loading. From Equation 3, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 625mW. The maximum power dissipation point obtained from Equation 3 must not be greater than the power dissipation results from Equation 4:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \tag{4}$$

The LM4941's θ_{JA} in a DSBGA package is 100°C/W. Depending on the ambient temperature, T_A, of the system surroundings, Equation 4 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 3 is greater than that of Equation 4, then either the supply voltage must be decreased, the load impedance increased, the ambient temperature reduced, or the θ_{JA} reduced with heatsinking. In many cases, larger traces near the output, V_{DD}, and GND pins can be used to lower the θ_{JA}. The larger areas of copper provide a form of heatsinking allowing higher power dissipation. For the typical application of a 5V power supply, with an 8Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 87.5°C provided that device operation is around the maximum power dissipation point. Recall that internal power dissipation is a function of output power. If typical operation is not around the maximum power dissipation point, the LM4941 can operate at higher ambient temperatures. Refer to the Typical Performance Characteristics curves for power dissipation information.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection ratio (PSRR). The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10µF and 0.1µF bypass capacitors that increase supply stability. This, however, does not eliminate the need for bypassing the supply nodes of the LM4941. The LM4941 will operate without the bypass capacitor C_B, although the PSRR may decrease. A 1µF capacitor is recommended for C_B. This value maximizes PSRR performance. Lesser values may be used, but PSRR decreases at frequencies below 1kHz. The issue of C_B selection is thus dependant upon desired PSRR and click and pop performance as explained in the section Proper Selection of External Components.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4941 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. The device may then be placed into shutdown mode by toggling the SHDN pin to logic low. It is best to switch between ground and supply for maximum performance. While the device may be disabled with shutdown voltages in between ground and supply, the idle current may be greater than the typical value of 0.1µA. In either case, the SHDN pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor. This scheme ensures that the shutdown pin will not float, thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical when optimizing device and system performance. Although the LM4941 is tolerant to a variety of external component combinations, consideration of component values must be made when maximizing overall system quality.

The LM4941 is unity-gain stable, giving the designer maximum system flexibility. The LM4941 should be used in low closed-loop gain configurations to minimize THD+N values and maximize signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than $1V_{RMS}$ are available from sources such as audio codecs. When used in its typical application as a fully differential power amplifier the LM4941 does not require input coupling capacitors for input sources with DC common-mode voltages of less than V_{DD}. Exact allowable input common-mode voltage levels are actually a function of V_{DD}, R_i, and R_F and may be determined by Equation 5:

$$V_{CMi} < (V_{DD}-1.2)(R_i+R_F)/R_F-V_{DD}/2(R_i/R_F) \tag{5}$$

$$-R_F / R_i = A_{VD} \tag{6}$$

When using DC coupled inputs, special care must be taken to match the values of the input resistors (R_{i1} and R_{i2}) to each other. Because of the balanced nature of differential amplifiers, resistor matching differences can result in net DC currents across the load. This DC current can increase power consumption, internal IC power dissipation, reduce PSRR, and possibly damaging the loudspeaker. The chart below demonstrates this problem by showing the effects of differing values between the feedback resistors while assuming that the input resistors are perfectly matched. The results below apply to the application circuit shown in Figure 1, and assumes that V_{DD} = 5V, R_L = 8Ω, and the system has DC coupled inputs tied to ground.

Tolerance	R_{i1}	R_{i2}	V_{01}–V_{02}	I_{LOAD}
20%	0.8R	1.2R	−0.500V	62.5mA
10%	0.9R	1.1R	−0.250V	31.25mA
5%	0.95R	1.05R	−0.125V	15.63mA
1%	0.99R	1.01R	−0.025V	3.125mA
0%	R	R	0	0

Since the same variations can have a significant effect on PSRR and CMRR performance, it is highly recommended that the input resistors be matched to 1% tolerance or better for best performance.
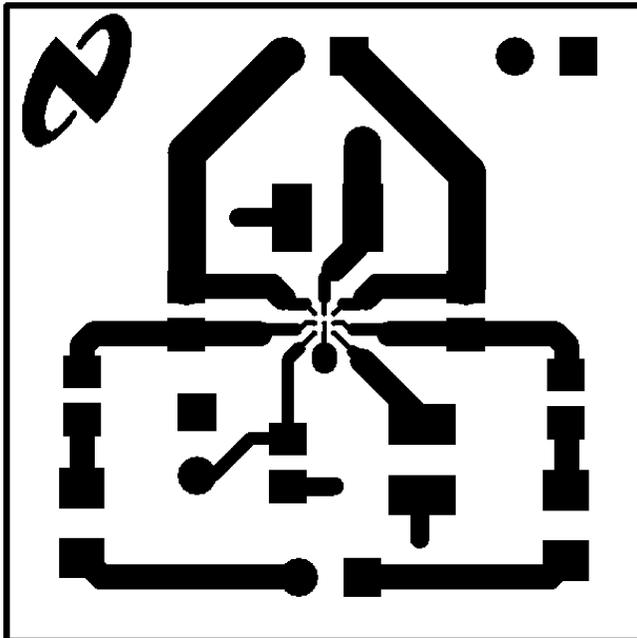
Recommended TM Board Layout

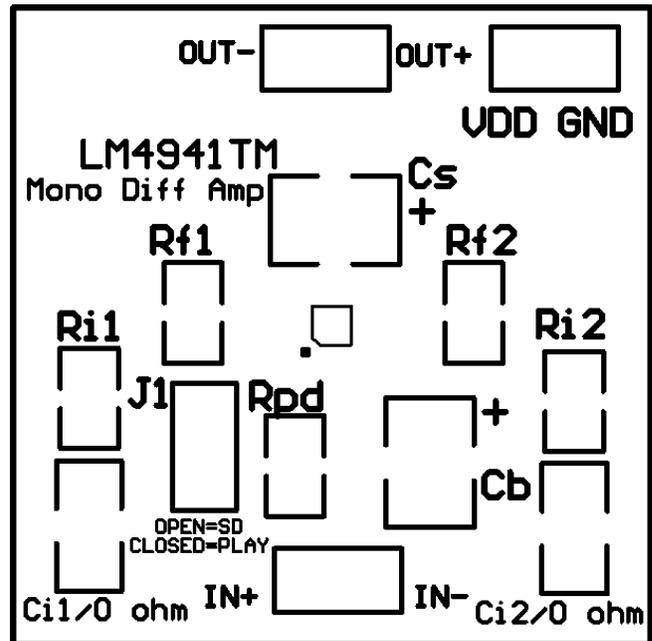Figure 21. Recommended TM Board Layout: Top Layer

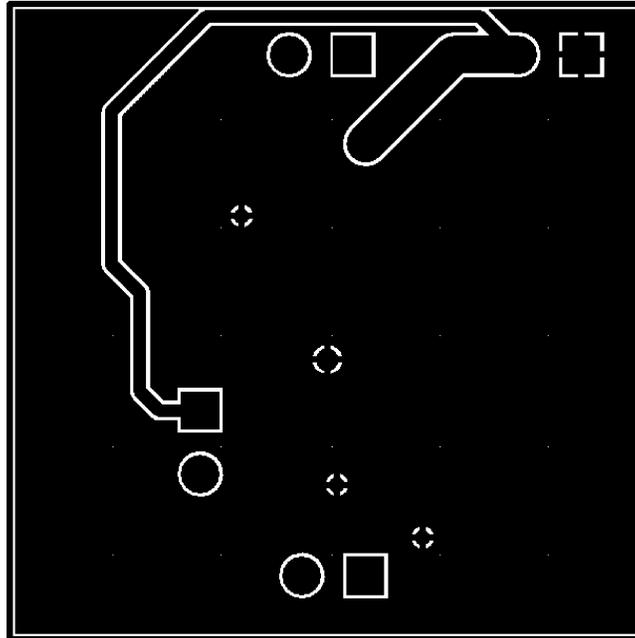Figure 22. Recommended TM Board Layout: Top Overlay

Figure 23. Recommended TM Board Layout: Bottom Layer
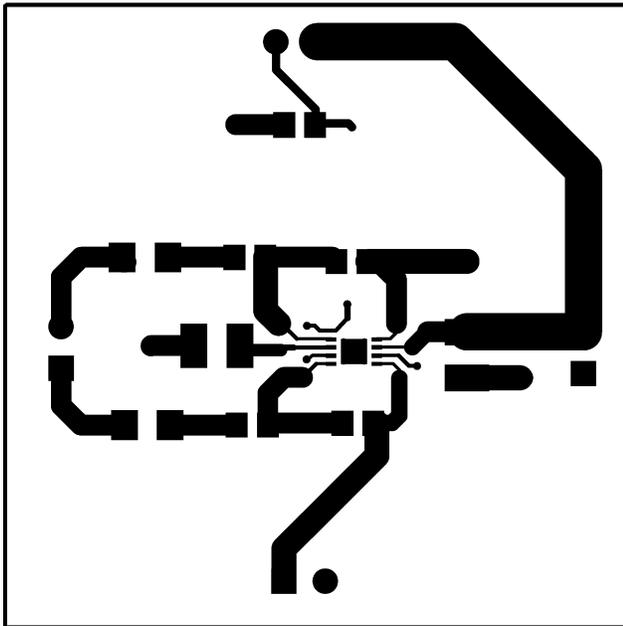
Recommended WSON Board Layout

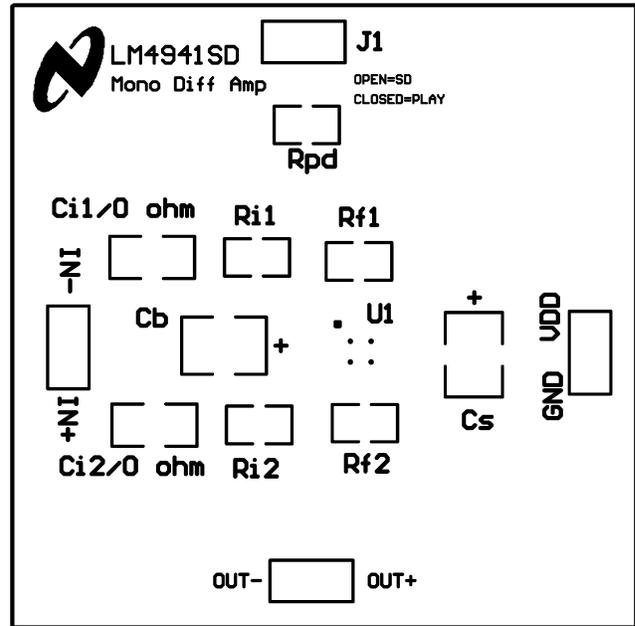**Figure 24. Recommended WSON Board Layout: Top Layer**

Figure 25. Recommended WSON Board Layout: Top Overlay

Product Folder Links: LM4941 LM4941SDBD LM4941TMBD
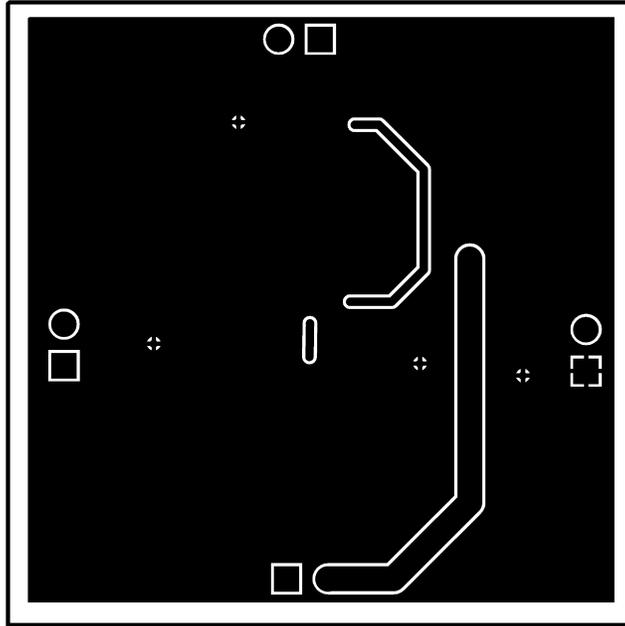
Figure 26. Recommended WSON Board Layout: Bottom Layer

LM4941 Reference Design Boards Bill Of Materials

Designator	Value	Tolerance	Part Description	Comments
Ri1, Ri2	20kΩ	0.10%	1/10W, 0.1% 0805 Resistor	
Rf1, Rf2	20kΩ	0.10%	1/10W, 0.1% 0805 Resistor	
Ci1, Ci2	0Ω		1/10W, 0.1% 0805 Resistor	
Cb, Cs	1µF	10%	16V Tantalum 1210 Capacitor	
In, Out, VDD, J1			0.100" 1x2 header, Vertical mount	Input, Output, VDD/GND, Shutdown Control

Product Folder Links: *LM4941 LM4941SDBD LM4941TMBD*

REVISION HISTORY

Rev	Date	Description
1.0	06/28/06	Initial release.
1.1	07/10/06	Added the WSON pkg mktg outline (per Kashif J.)
1.2	08/04/06	Added the WSON package and marking diagrams.
1.3	10/12/06	Edited some of the Typical Performance curves' labels and some text edits.
1.4	10/25/06	Added the WSON boards.
1.5	11/07/06	Text edits.
1.6	11/15/06	Replaced curve 20170381 with 20170382 and input text edits.
1.7	03/09/07	Changed the Limit value from 70 to 80 on the PSRR in the EC 5V EC table.
C	05/03/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4941SD/NOPB	ACTIVE	WSON	NGS	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		4941	Samples
LM4941SDX/NOPB	ACTIVE	WSON	NGS	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		4941	Samples
LM4941TM/NOPB	ACTIVE	DSBGA	YFQ	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	G H6	Samples
LM4941TMX/NOPB	ACTIVE	DSBGA	YFQ	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	G H6	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
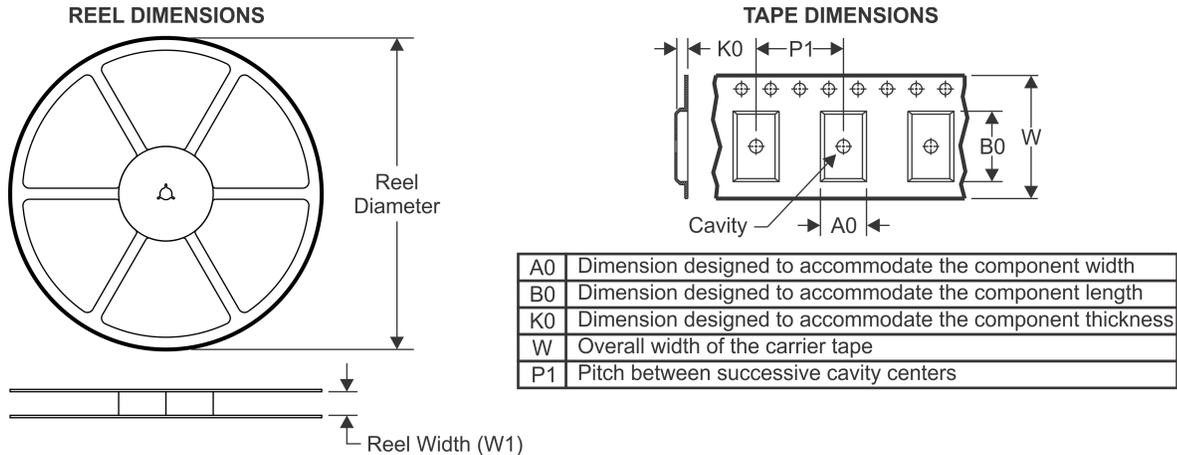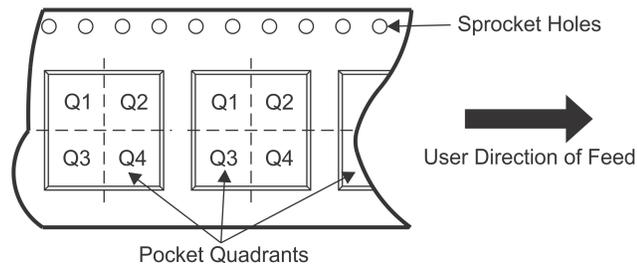
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4941SD/NOPB	WSON	NGS	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LM4941SDX/NOPB	WSON	NGS	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LM4941TM/NOPB	DSBGA	YFQ	9	250	178.0	8.4	1.35	1.35	0.76	4.0	8.0	Q1
LM4941TMX/NOPB	DSBGA	YFQ	9	3000	178.0	8.4	1.35	1.35	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS
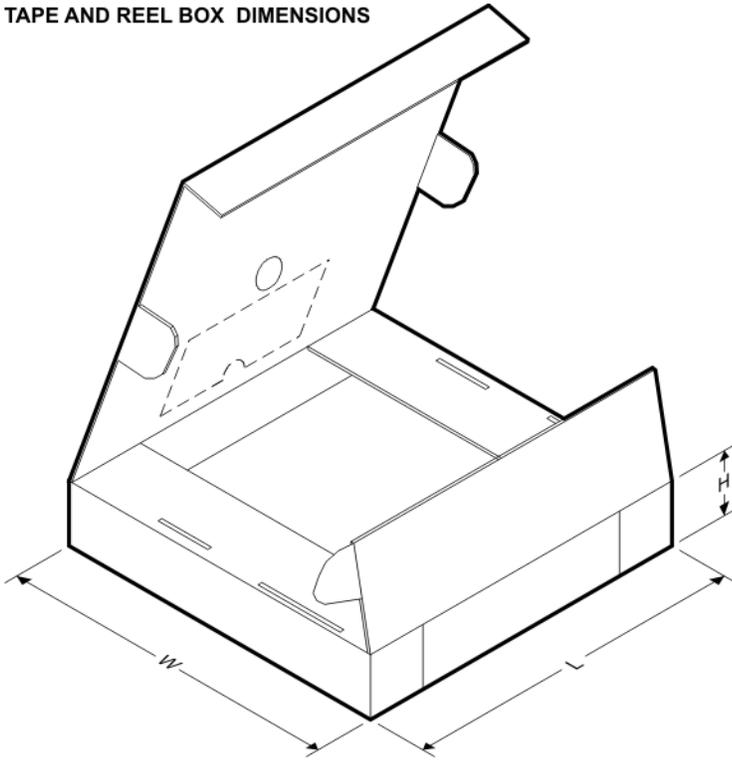
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4941SD/NOPB	WSON	NGS	8	1000	210.0	185.0	35.0
LM4941SDX/NOPB	WSON	NGS	8	4500	367.0	367.0	35.0
LM4941TM/NOPB	DSBGA	YFQ	9	250	210.0	185.0	35.0
LM4941TMX/NOPB	DSBGA	YFQ	9	3000	210.0	185.0	35.0

YFQ0009

PKG SYMM
℄

PKG SYMM ℄

(0.4)

9X ⌀ 0.24
      0.21

(0.4)

LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

TOP SIDE COATING

BUMP A1 CORNER

0.600±0.075

[C]

0.125
0.050

BUMP

SILICON

0.205
0.165

9X ⌀ 0.28
      0.25

⊕ | 0.005Ⓢ | C | AⓈ | BⓈ

[B]

D

SYMM
℄

3

SYMM
℄
2

1

0.4

E

[A]

C   B   A

0.4
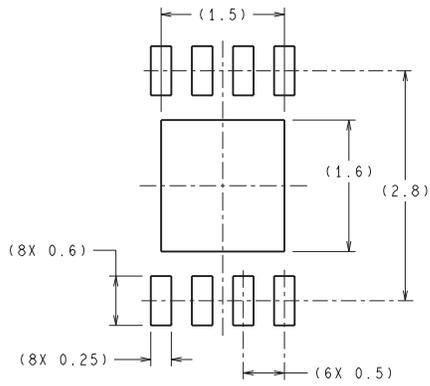
TMD09XXX (Rev A)
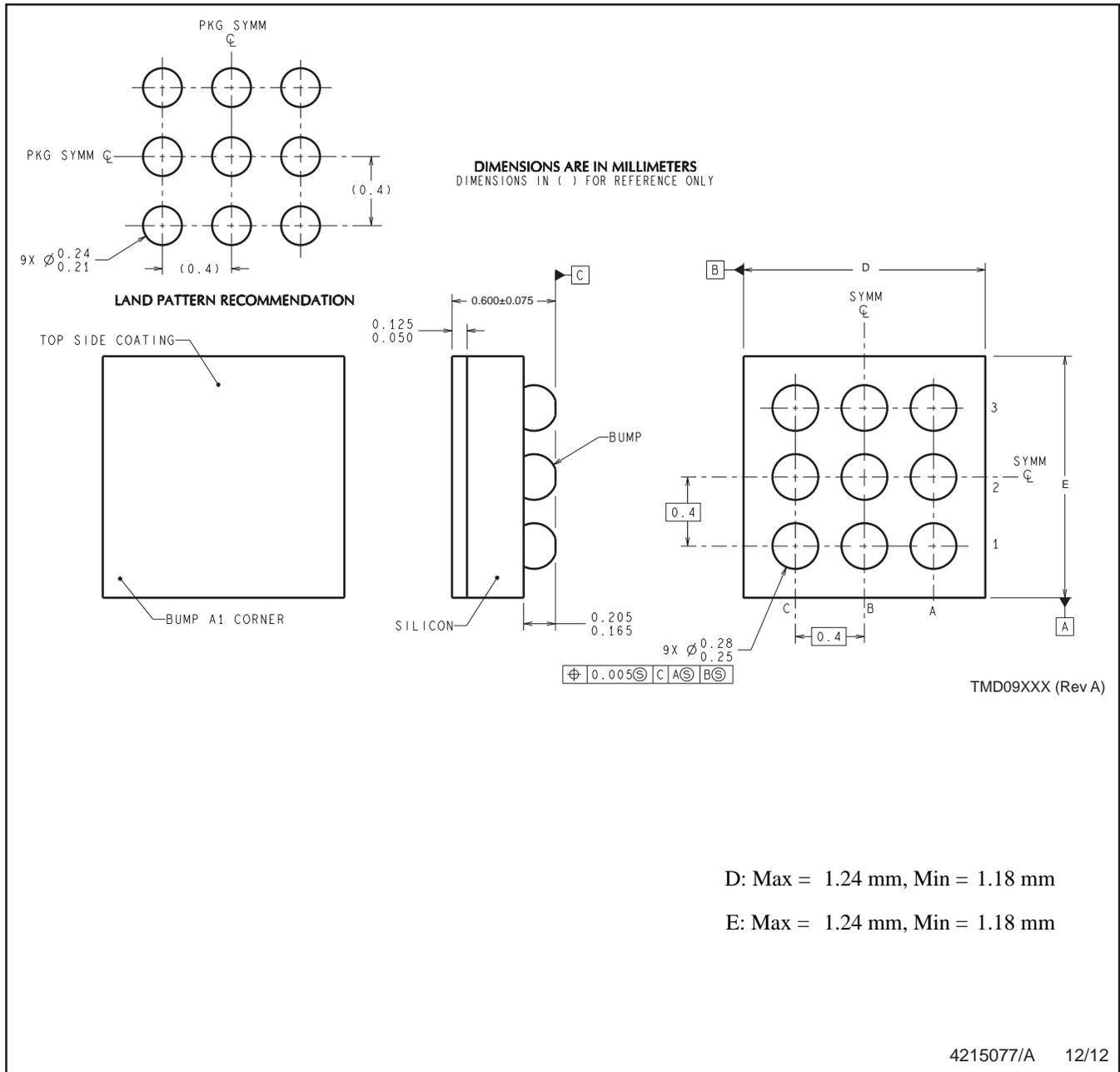
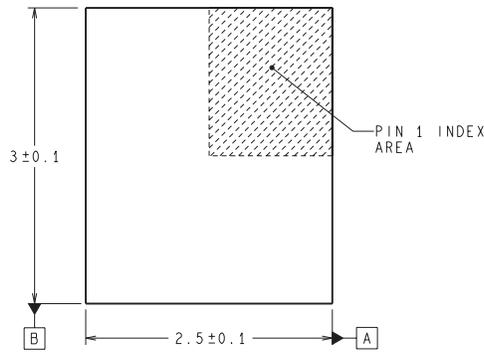D: Max = 1.24 mm, Min = 1.18 mm

E: Max = 1.24 mm, Min = 1.18 mm

4215077/A   12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
           B. This drawing is subject to change without notice.

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NGS0008C

(1.5)

(1.6)

(2.8)

(8X 0.6)

(8X 0.25)

(6X 0.5)

RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

(0.1)

3±0.1

PIN 1 INDEX
AREA

2.5±0.1

B

A

C

0.8 MAX

(0.2)

PIN 1 ID

(45° X 0.25)

1.5±0.1

1   4

1.6±0.1

8X 0.4±0.1

8X 0.25±0.05

⊕ | 0.1 Ⓜ | C | AⓈ | BⓈ

8   5

6X | 0.5

2X | 1.5
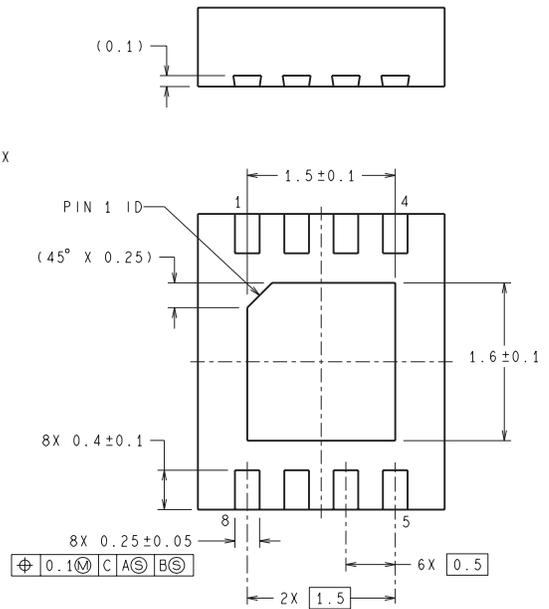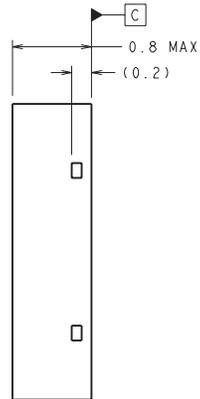
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