National Semiconductor

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LM7321 Single/ LM7322 Dual Rail-to-Rail Input/Output ±15V, High Output Current and Unlimited Capacitive Load Operational Amplifier

General Description

The LM7321/LM7322 are rail-to-rail input and output amplifiers with wide operating voltages and high output currents. The LM7321/LM7322 are efficient, achieving 18 V/µs slew rate and 20 MHz unity gain bandwidth while requiring only 1 mA of supply current per op amp. The LM7321/LM7322 performance is fully specified for operation at 2.7V, ±5V and ±15V.

The LM7321/LM7322 are designed to drive unlimited capacitive loads without oscillations. All LM7321 and LM7322 parts are tested at −40°C, 125°C, and 25°C, with modern automatic test equipment. High performance from −40°C to 125°C, detailed specifications, and extensive testing makes them suitable for industrial, automotive, and communications applications.

Greater than rail-to-rail input common mode voltage range with 50 dB of common mode rejection across this wide voltage range, allows both high side and low side sensing. Most device parameters are insensitive to power supply voltage, and this makes the parts easier to use where supply voltage may vary, such as automotive electrical systems and battery powered equipment. These amplifiers have true rail-to-rail output and can supply a respectable amount of current (15 mA) with minimal head- room from either rail (300 mV) at low distortion (0.05% THD+Noise). There are several package options for each part. Standard SOIC versions of both parts make upgrading existing designs easy. LM7322 is offered in a space saving 8-Pin MSOP package. The LM7321 is offered in small SOT23-5 package, which makes it easy to place this part close to sensors for better circuit performance.

Features

(V_S = ±15, T_A = 25°C, Typical values unless specified.)

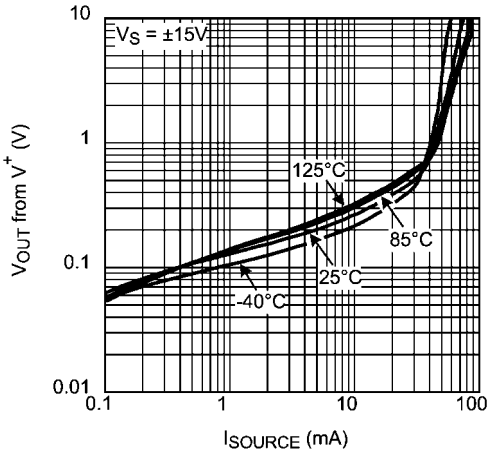
- Wide supply voltage range — 2.5V to 32V
- Output current — +65 mA/−100 mA
- Gain bandwidth product — 20 MHz
- Slew rate — 18 V/µs
- Capacitive load tolerance — Unlimited
- Input common mode voltage — 0.3V beyond rails
- Input voltage noise — 15 nV/√Hz
- Input current noise — 1.3 pA/√Hz
- Supply current/channel — 1.1 mA
- Distortion THD+Noise — −86 dB
- Temperature range — −40°C to 125°C
- Tested at −40°C, 25°C and 125°C at 2.7V, ±5V, ±15V.

Applications

- Driving MOSFETs and power transistors
- Capacitive proximity sensors
- Driving analog optocouplers
- High side sensing
- Below ground current sensing
- Photodiode biasing
- Driving varactor diodes in PLLs
- Wide voltage range power supplies
- Automotive
- International power supplies

Typical Performance Characteristics

Output Swing vs. Sourcing Current



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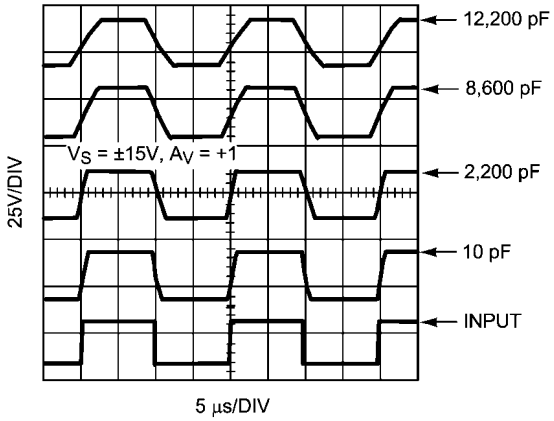
Large Signal Step Response



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2 kV
Machine Model	200V
Charge-Device Model	1 kV
V_{IN} Differential	±10V
Output Short Circuit Current	(Note 3)
Supply Voltage ($V_S = V^+ - V^-$)	35V
Voltage at Input/Output pins	V^+ +0.8V, V^- −0.8V
Storage Temperature Range	−65°C to 150°C
Junction Temperature (Note 4)	150°C
Soldering Information:	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

Operating Ratings

Supply Voltage ($V_S = V^+ - V^-$)	2.5V to 32V
Temperature Range (Note 4)	−40°C to 125°C
Package Thermal Resistance, θ_{JA},(Note 4)	
5-Pin SOT-23	325°C/W
8-Pin MSOP	235°C/W
8-Pin SOIC	165°C/W

2.7V Electrical Characteristics (Note 5)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_{OUT} = 1.35V, and R_L > 1 MΩ to 1.35V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 2.2V	−5 **−6**	±0.7	+5 **+6**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = 0.5V & V_{CM} = 2.2V (Note 8)		±2		µV/C
I_B	Input Bias Current	V_{CM} = 0.5V (Note 9)	−2.0 **−2.5**	−1.2		µA
		V_{CM} = 2.2V (Note 9)		0.45	1.0 **1.5**	
I_{OS}	Input Offset Current	V_{CM} = 0.5V and V_{CM} = 2.2V		20	200 **300**	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.0V	70 **60**	100		dB
		0V ≤ V_{CM} ≤ 2.7V	55 **50**	70		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V_S ≤ 30V	78 **74**	104		dB
CMVR	Common Mode Voltage Range	CMRR > 50 dB		−0.3	−0.1 **0.0**	V
			2.8 **2.7**	3.0		
A_{VOL}	Open Loop Voltage Gain	0.5V ≤ V_O ≤ 2.2V R_L = 10 kΩ to 1.35V	65 **62**	72		dB
		0.5V ≤ V_O ≤ 2.2V R_L = 2 kΩ to 1.35V	59 **55**	66		
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to 1.35V V_{ID} = 100 mV		50	150 **160**	mV from either rail
		R_L = 2 kΩ to 1.35V V_{ID} = 100 mV		100	250 **280**	
	Output Voltage Swing Low	R_L = 10 kΩ to 1.35V V_{ID} = −100 mV		20	120 **150**	
		R_L = 2 kΩ to 1.35V V_{ID} = −100 mV		40	120 **150**	

Symbol	Parameter	Condition	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
I_{OUT}	Output Current	Sourcing V_{ID} = 200 mV, V_{OUT} = 0V (Note 3)	30 **20**	48		mA
		Sinking V_{ID} = −200 mV, V_{OUT} = 2.7V (Note 3)	40 **30**	65		
I_S	Supply Current	LM7321		0.95	1.3 **1.9**	mA
		LM7322		2.0	2.5 **3.8**	
SR	Slew Rate (Note 10)	A_V = +1, V_I = 2V Step		8.5		V/µs
f_u	Unity Gain Frequency	R_L = 2 kΩ, C_L = 20 pF		7.5		MHz
GBW	Gain Bandwidth	f = 50 kHz		16		MHz
e_n	Input Referred Voltage Noise Density	f = 2 kHz		11.9		$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise Density	f = 2 kHz		0.5		$pA/\sqrt{Hz}$
THD+N	Total Harmonic Distortion + Noise	V^+ = 1.9V, V^- = −0.8V f = 1 kHz, R_L = 100 kΩ, A_V = +2 V_{OUT} = 210 mV_{PP}		−77		dB
CT Rej.	Crosstalk Rejection	f = 100 kHz, Driver R_L = 10 kΩ		60		dB

±5V Electrical Characteristics (Note 5)

Unless otherwise specified, all limited guaranteed for T_A = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = 0V, V_{OUT} = 0V, and R_L > 1 MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
V_{OS}	Input Offset Voltage	V_{CM} = −4.5V and V_{CM} = 4.5V	−5 **−6**	±0.7	+5 **+6**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = −4.5V and V_{CM} = 4.5V (Note 8)		±2		µV/°C
I_B	Input Bias Current	V_{CM} = −4.5V (Note 9)	−2.0 **−2.5**	−1.2		µA
		V_{CM} = 4.5V (Note 9)		0.45	1.0 **1.5**	
I_{OS}	Input Offset Current	V_{CM} = −4.5V and V_{CM} = 4.5V		20	200 **300**	nA
CMRR	Common Mode Rejection Ratio	−5V ≤ V_{CM} ≤ 3V	80 **70**	100		dB
		−5V ≤ V_{CM} ≤ 5V	65 **62**	80		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V_S ≤ 30V, V_{CM} = −4.5V	78 **74**	104		dB
CMVR	Common Mode Voltage Range	CMRR > 50 dB		−5.3	−5.1 **−5.0**	V
			5.1 **5.0**	5.3		
A_{VOL}	Open Loop Voltage Gain	−4V ≤ V_O ≤ 4V R_L = 10 kΩ to 0V	74 **70**	80		dB
		−4V ≤ V_O ≤ 4V R_L = 2 kΩ to 0V	68 **65**	74		

Symbol	Parameter	Condition		Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to 0V V_{ID} = 100 mV			100	250 **280**	mV from either rail
		R_L = 2 kΩ to 0V V_{ID} = 100 mV			160	350 **450**	
	Output Voltage Swing Low	R_L = 10 kΩ to 0V V_{ID} = −100 mV			35	200 **250**	
		R_L = 2 kΩ to 0V V_{ID} = −100 mV			80	200 **250**	
I_{OUT}	Output Current	Sourcing V_{ID} = 200 mV, V_{OUT} = −5V (Note 3)		35 **20**	70		mA
		Sinking V_{ID} = −200 mV, V_{OUT} = 5V (Note 3)		50 **30**	85		
I_S	Supply Current	V_{CM} = −4.5V	LM7321		1.0	1.3 **2**	mA
			LM7322		2.3	2.8 **3.8**	
SR	Slew Rate (Note 10)	A_V = +1, V_I = 8V Step			12.3		V/µs
f_u	Unity Gain Frequency	R_L = 2 kΩ, C_L = 20 pF			9		MHz
GBW	Gain Bandwidth	f = 50 kHz			16		MHz
e_n	Input Referred Voltage Noise Density	f = 2 kHz			14.3		$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise Density	f = 2 kHz			1.35		$pA/\sqrt{Hz}$
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, R_L = 100 kΩ, A_V = +2 V_{OUT} = 8 V_{PP}			−79		dB
CT Rej.	Crosstalk Rejection	f = 100 kHz, Driver R_L = 10 kΩ			60		dB

±15V Electrical Characteristics (Note 5)

Unless otherwise specified, all limited guaranteed for T_A = 25°C, V^+ = 15V, V^- = −15V, V_{CM} = 0V, V_{OUT} = 0V, and R_L > 1MΩ to 15V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
V_{OS}	Input Offset Voltage	V_{CM} = −14.5V and V_{CM} = 14.5V	−6 **−8**	±0.7	+6 **+8**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = −14.5V and V_{CM} = 14.5V (Note 8)		±2		µV/°C
I_B	Input Bias Current	V_{CM} = −14.5V (Note 9)	−2 **−2.5**	−1.1		µA
		V_{CM} = 14.5V (Note 9)		0.45	1.0 **1.5**	
I_{OS}	Input Offset Current	V_{CM} = −14.5V and V_{CM} = 14.5V		30	300 **500**	nA
CMRR	Common Mode Rejection Ratio	−15V ≤ V_{CM} ≤ 12V	80 **75**	100		dB
		−15V ≤ V_{CM} ≤ 15V	72 **70**	80		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V_S ≤ 30V, V_{CM} = −14.5V	78 **74**	100		dB
CMVR	Common Mode Voltage Range	CMRR > 50 dB		−15.3	−15.1 **−15**	V
			15.1 **15**	15.3		

Symbol	Parameter	Condition		Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
A_{VOL}	Open Loop Voltage Gain	$-13V \le V_O \le 13V$ R_L = 10 kΩ to 0V		75 **70**	85		dB
		$-13V \le V_O \le 13V$ R_L = 2 kΩ to 0V		70 **65**	78		
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to 0V V_{ID} = 100 mV			150	300 **350**	mV from either rail
		R_L = 2 kΩ to 0V V_{ID} = 100 mV			250	550 **650**	
	Output Voltage Swing Low	R_L = 10 kΩ to 0V V_{ID} = −100 mV			60	200 **250**	
		R_L = 2 kΩ to 0V V_{ID} = −100 mV			130	300 **400**	
I_{OUT}	Output Current	Sourcing V_{ID} = 200 mV, V_{OUT} = −15V (Note 3)		40	65		mA
		Sinking V_{ID} = −200 mV, V_{OUT} = 15V (Note 3)		60	100		
I_S	Supply Current	V_{CM} = −14.5V	LM7321		1.1	1.7 **2.4**	mA
			LM7322		2.5	4 **5.6**	
SR	Slew Rate (Note 10)	A_V = +1, V_I = 20V Step			18		V/µs
f_u	Unity Gain Frequency	R_L = 2 kΩ, C_L = 20 pF			11.3		MHz
GBW	Gain Bandwidth	f = 50 kHz			20		MHz
e_n	Input Referred Voltage Noise Density	f = 2 kHz			15		$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise Density	f = 2 kHz			1.3		$pA/\sqrt{Hz}$
THD+N	Total Harmonic Distortion +Noise	f = 1 kHz,R_L 100 kΩ, A_V = +2, V_{OUT} = 23 V_{PP}			−86		dB
CT Rej.	Crosstalk Rejection	f = 100 kHz, Driver R_L = 10 kΩ			60		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)

Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S \le$ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5 ms.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 6: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 7: All limits are guaranteed by testing or statistical analysis.

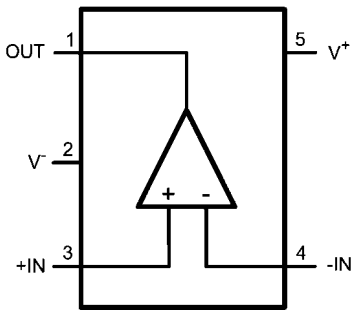
Note 8: Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Note 9: Positive current corresponds to current flowing into the device.

Note 10: Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

Connection Diagrams

5-Pin SOT-23



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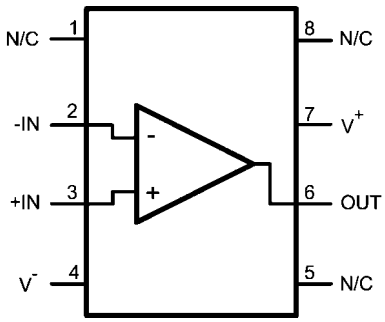
Top View

8-Pin SOIC



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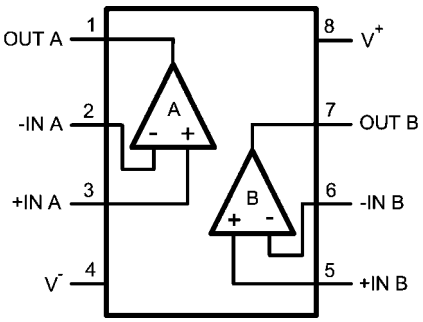
Top View

8-Pin MSOP/SOIC



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Top View

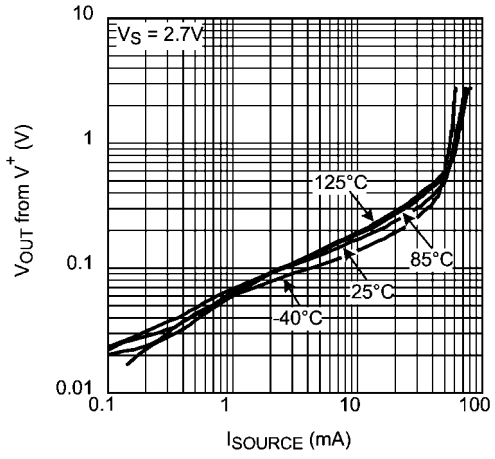
Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
5-Pin SOT-23	LM7321MF	AU4A	1k Units Tape and Reel	MF05A
	LM7321MFE		250 Units Tape and Reel	
	LM7321MFX		3k Units Tape and Reel	
8-Pin MSOP	LM7322MM	AZ4A	1k Units Tape and Reel	MUA08A
	LM7322MME		250 Units Tape and Reel	
	LM7322MMX		3.5k Units Tape and Reel	
8-Pin SOIC	LM7321MA	LM7321MA	95 Units/Rail	M08A
	LM7321MAX		2.5k Units Tape and Reel	
	LM7322MA	LM7322MA	95 Units/Rail	
	LM7322MAX		2.5k Units Tape and Reel	

Typical Performance Characteristics

Unless otherwise specified: T_A = 25°C.

Output Swing vs. Sourcing Current



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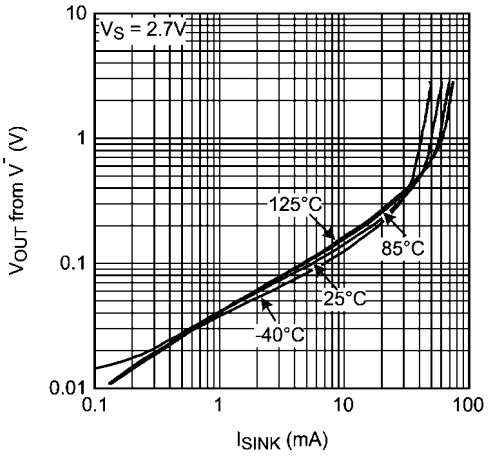
Output Swing vs. Sinking Current



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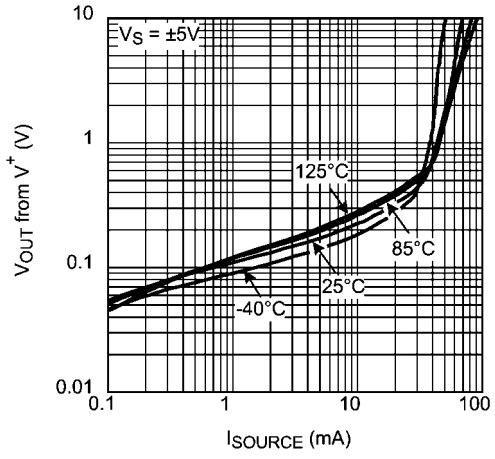
Output Swing vs. Sourcing Current



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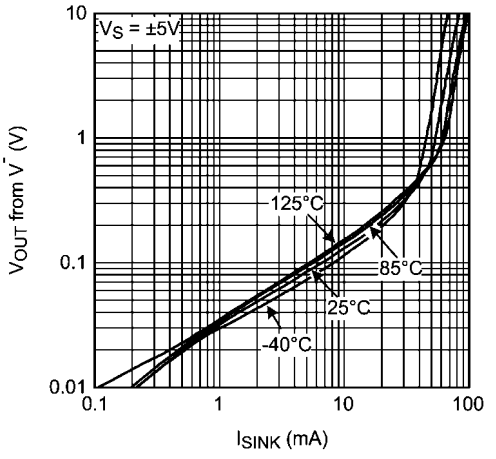
Output Swing vs. Sinking Current



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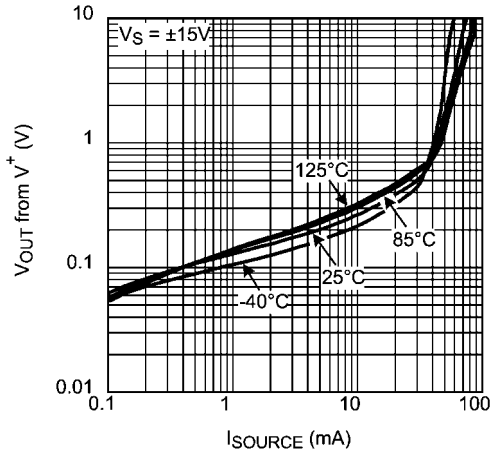
Output Swing vs. Sourcing Current



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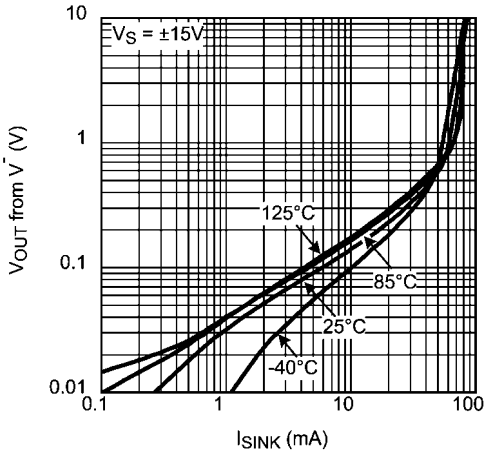
Output Swing vs. Sinking Current



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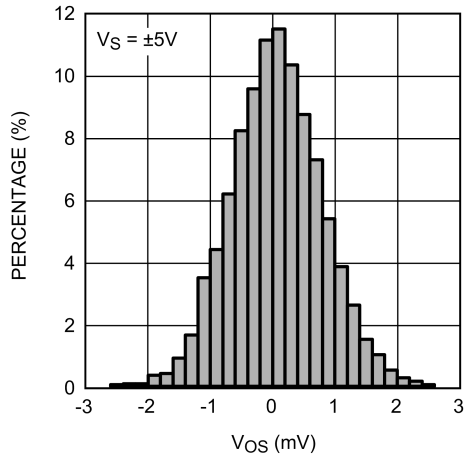
V_{OS} Distribution



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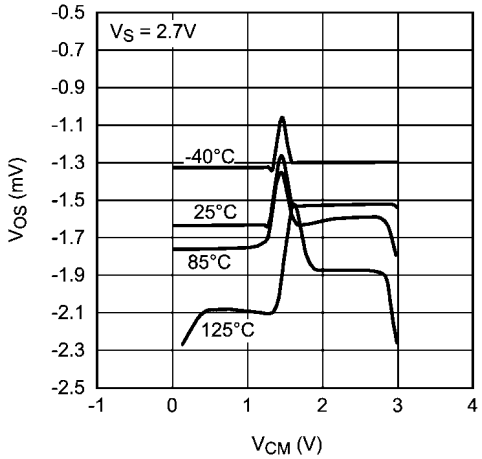
V_{OS} vs. V_{CM} (Unit 1)



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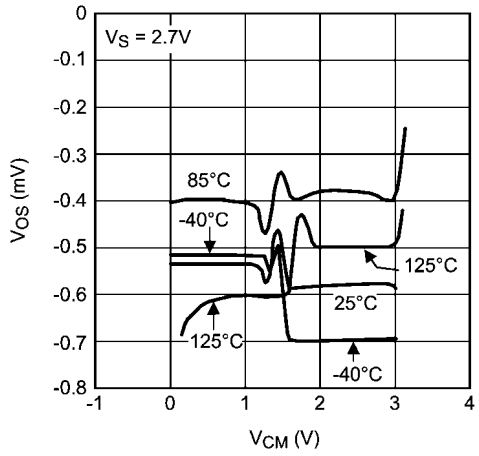
V_{OS} vs. V_{CM} (Unit 2)



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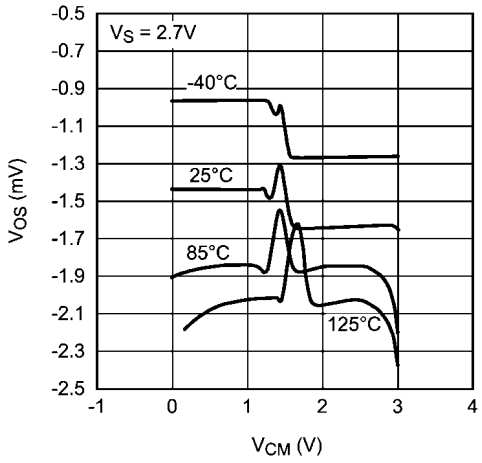
V_{OS} vs. V_{CM} (Unit 3)



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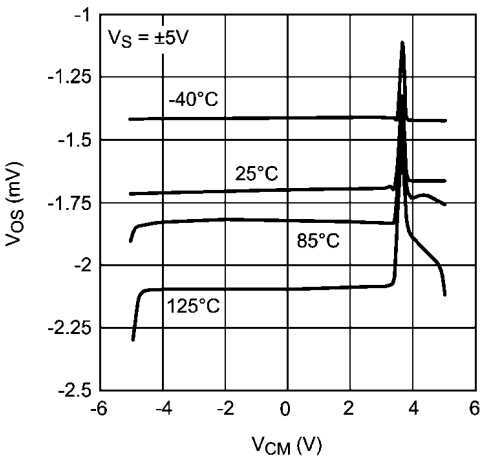
V_{OS} vs. V_{CM} (Unit 1)



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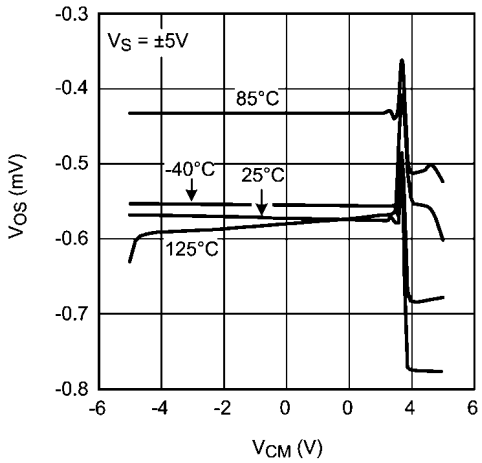
V_{OS} vs. V_{CM} (Unit 2)



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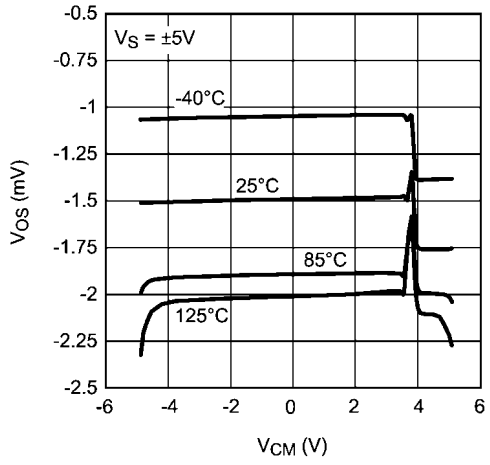
V_{OS} vs. V_{CM} (Unit 2)



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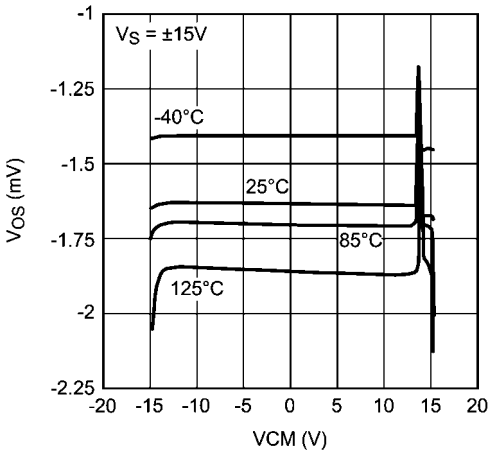
V_{OS} vs. V_{CM} (Unit 1)



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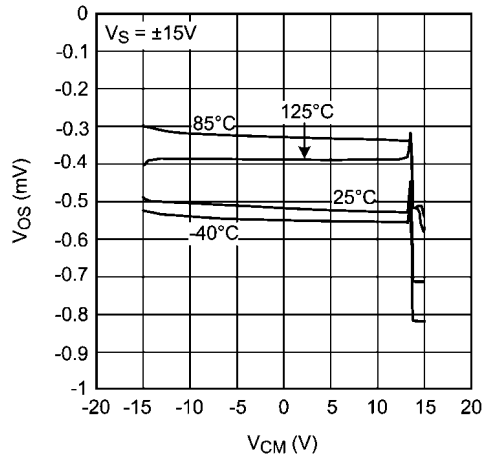
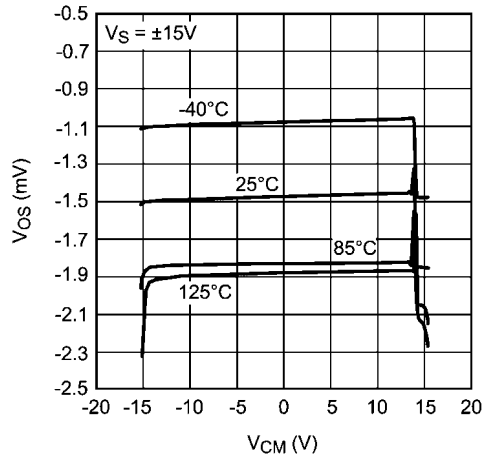
V_{OS} vs. V_{CM} (Unit 2)



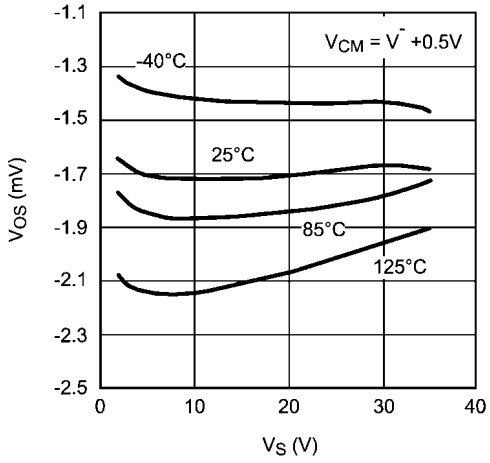
20205714

V_{OS} vs. V_{CM} (Unit 3)



20205715

V_{OS} vs. V_S (Unit 1)



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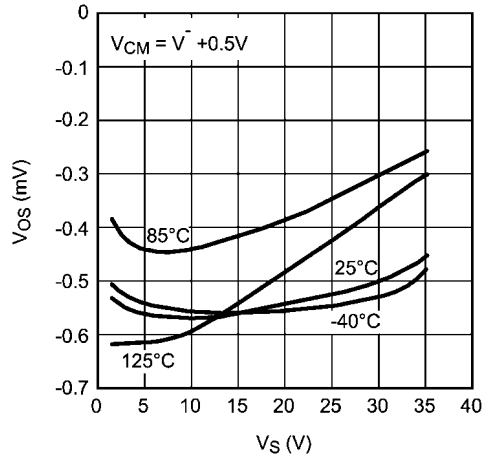
V_{OS} vs. V_S (Unit 2)



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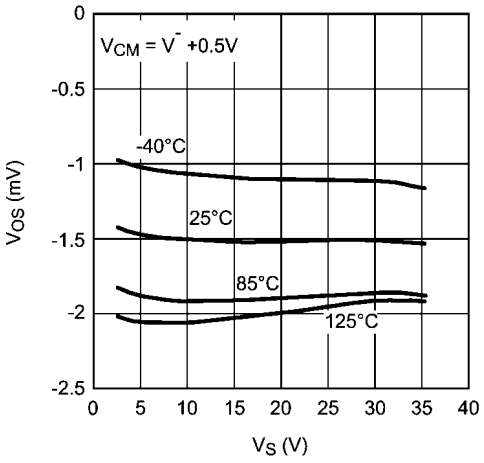
V_{OS} vs. V_S (Unit 3)



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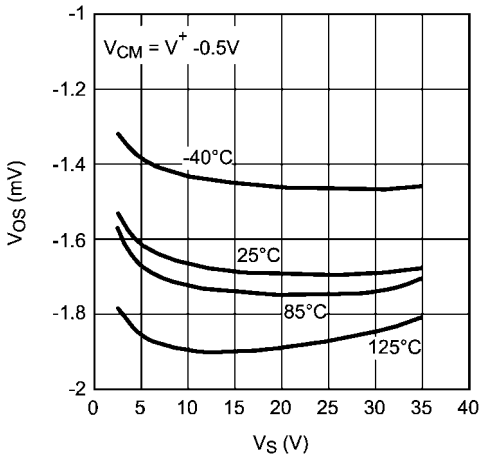
V_{OS} vs. V_S (Unit 1)



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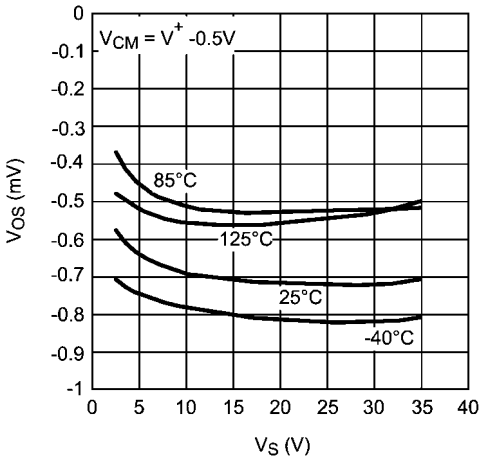
V_{OS} vs. V_S (Unit 2)



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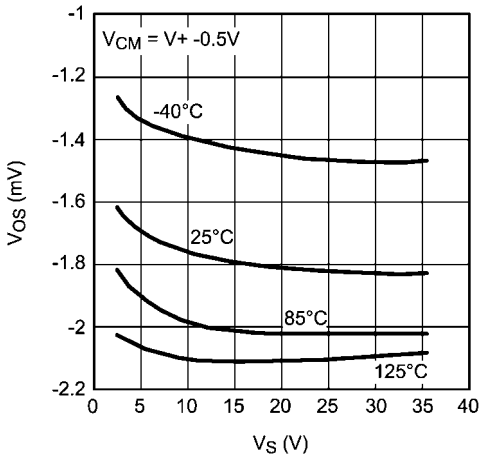
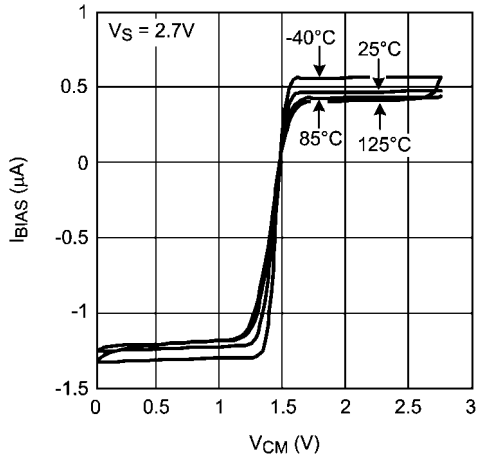
V_{OS} vs. V_S (Unit 3)



20205755

I_{BIAS} vs. V_{CM}



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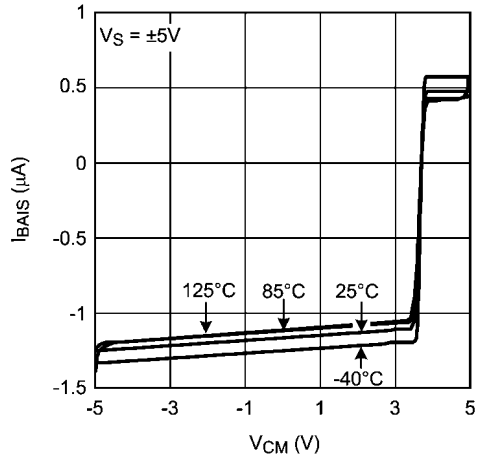

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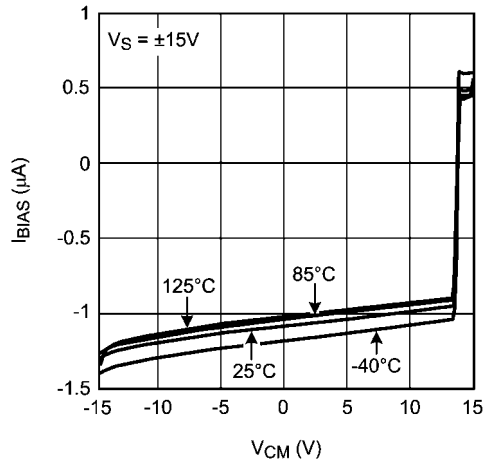
I_{BIAS} vs. V_{CM}



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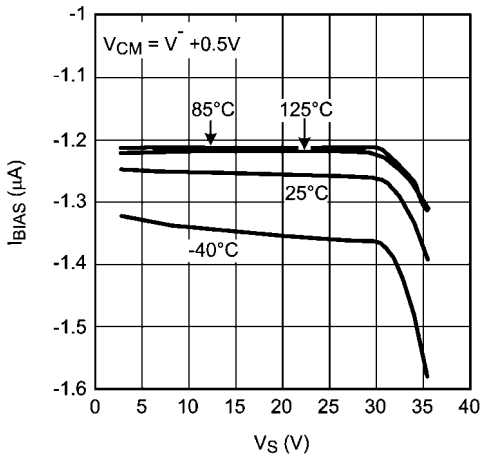
I_{BIAS} vs. V_S



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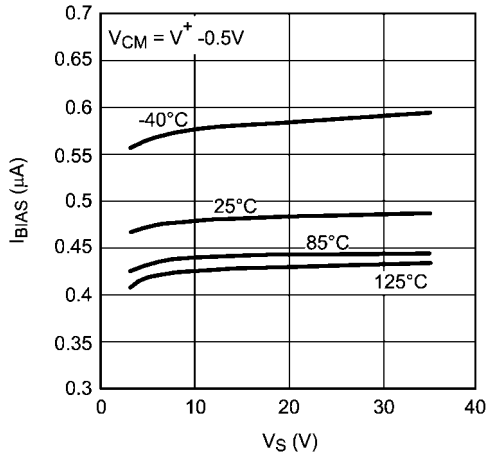
I_{BIAS} vs. V_S



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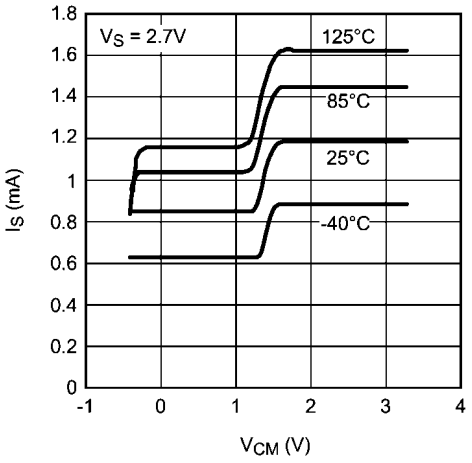
I_S vs. V_{CM} (LM7321)



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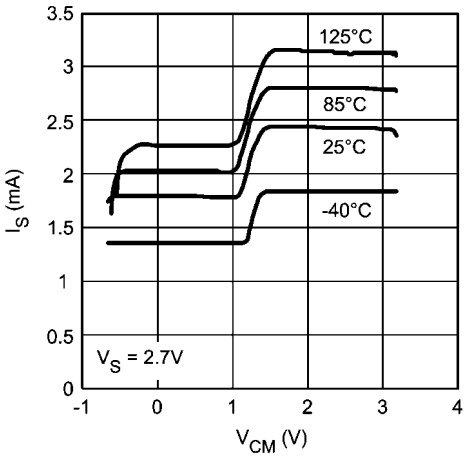
I_S vs. V_{CM} (LM7322)



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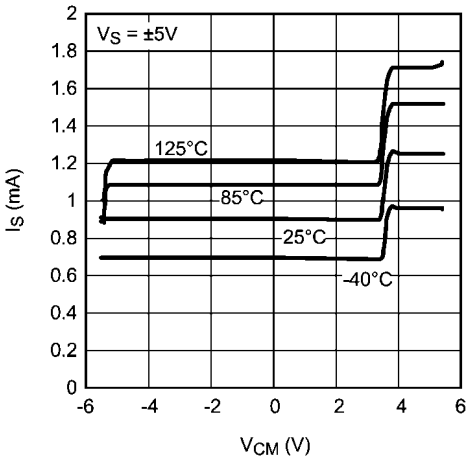
I_S vs. V_{CM} (LM7321)



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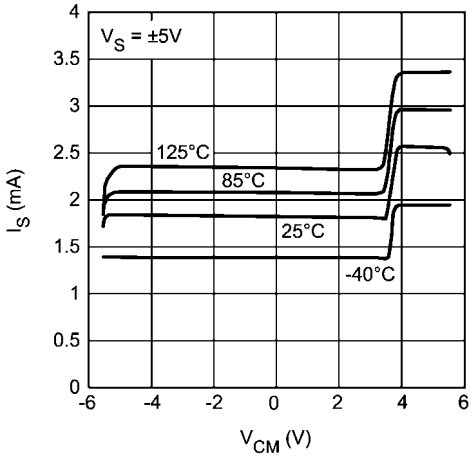
I_S vs. V_{CM} (LM7322)



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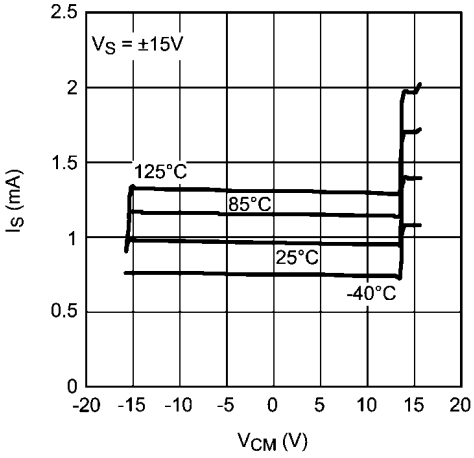
I_S vs. V_{CM} (LM7321)



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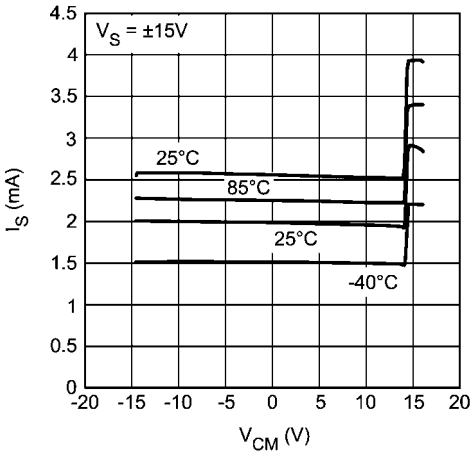
I_S vs. V_{CM} (LM7322)



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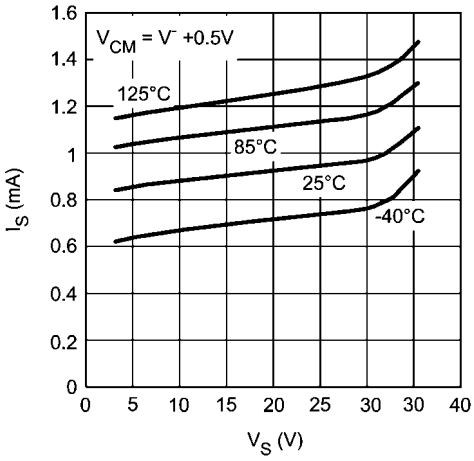
I_S vs. V_S (LM7321)



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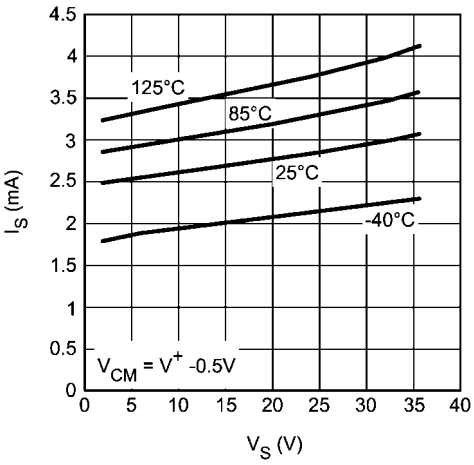
I_S vs. V_S (LM7322)



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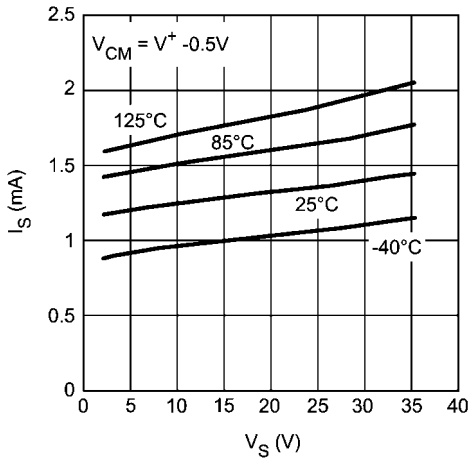
I_S vs. V_S (LM7321)



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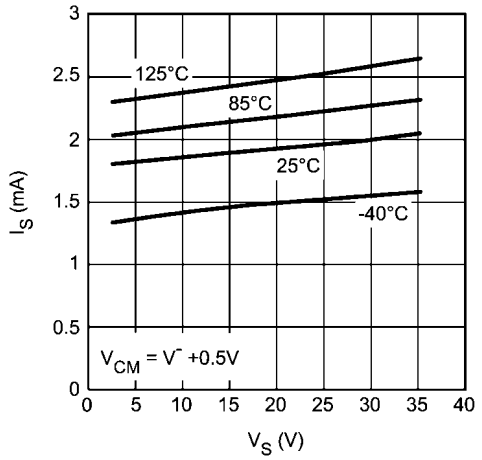
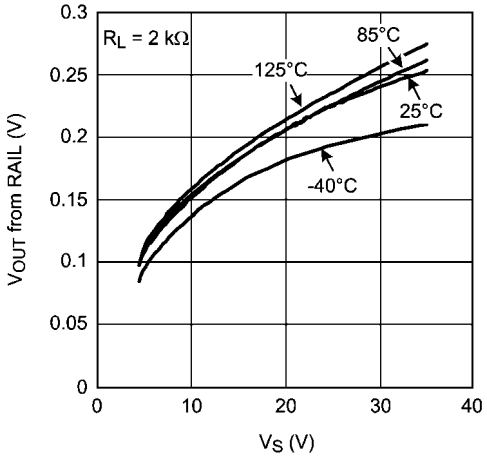
I_S vs. V_S (LM7322)



20205778

Positive Output Swing vs. Supply Voltage



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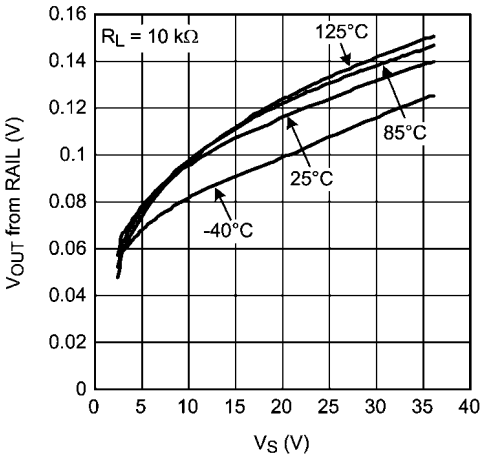
Positive Output Swing vs. Supply Voltage



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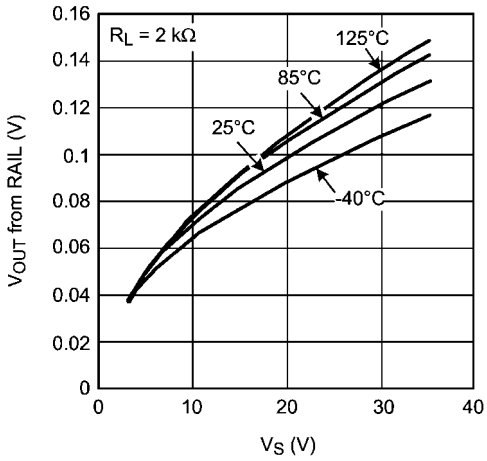
Negative Output Swing vs. Supply Voltage



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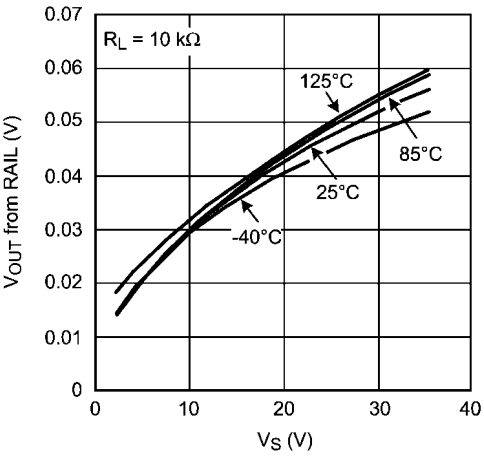
Negative Output Swing vs. Supply Voltage



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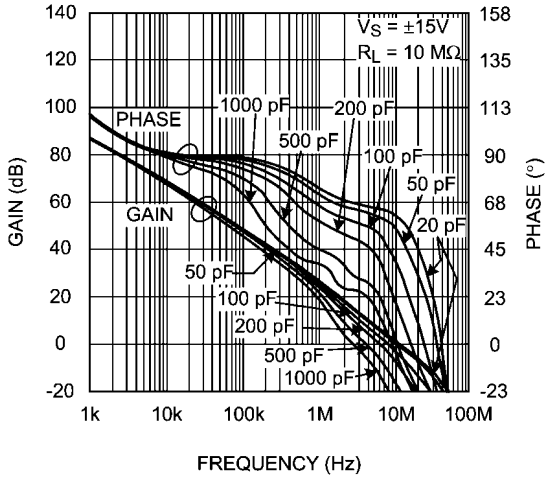
Open Loop Frequency Response with Various Capacitive Load



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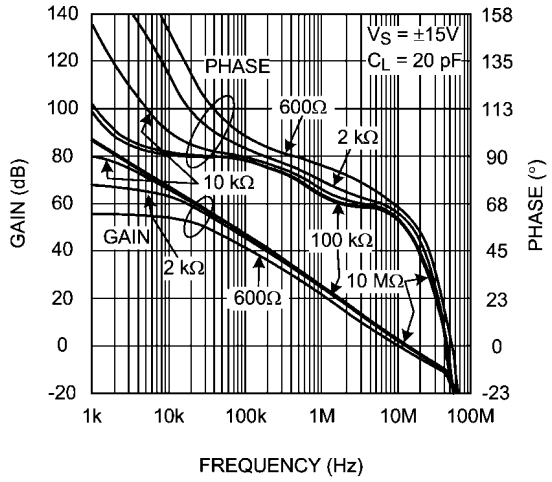
Open Loop Frequency Response with Various Resistive Load



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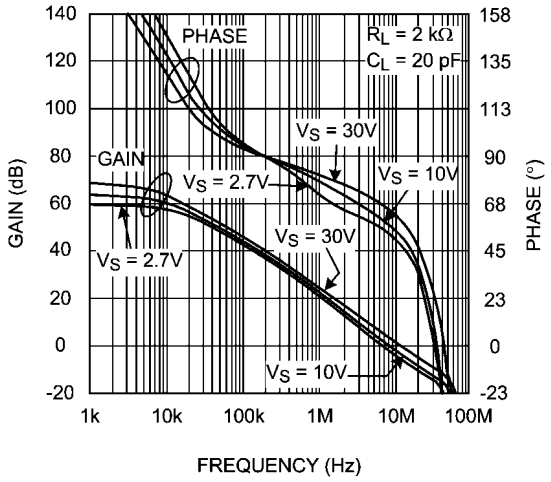
Open Loop Frequency Response with Various Supply Voltage



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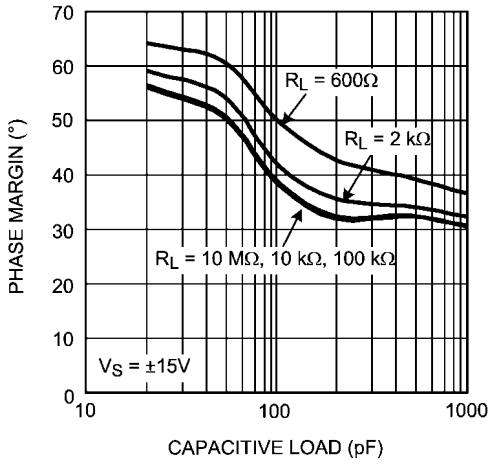
Phase Margin vs. Capacitive Load



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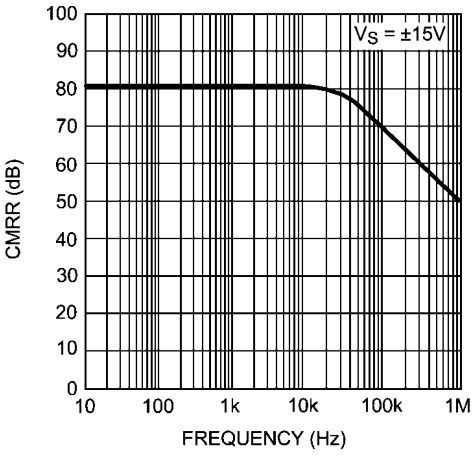
CMRR vs. Frequency



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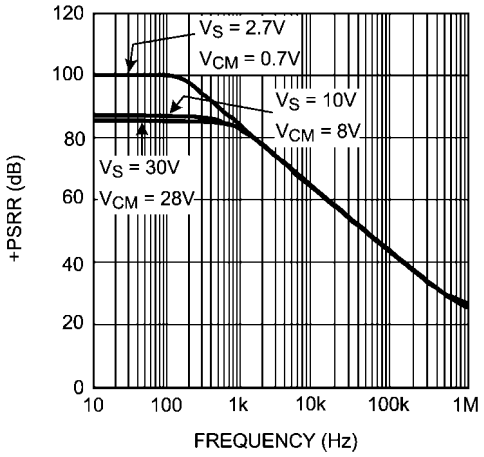
+PSRR vs. Frequency



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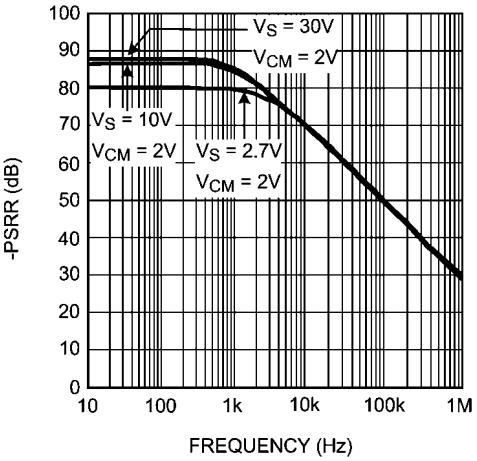
–PSRR vs. Frequency



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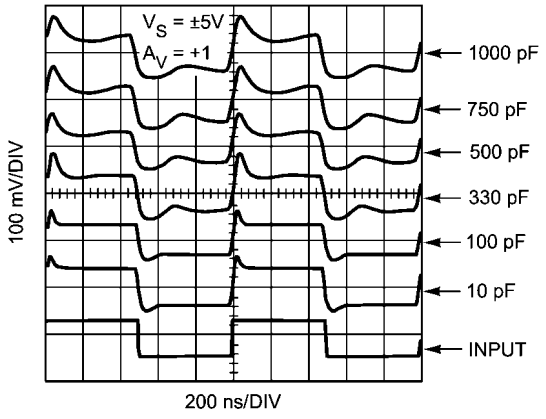
Small Signal Step Response



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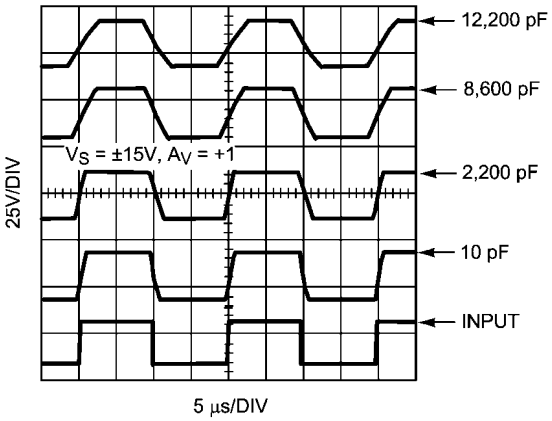
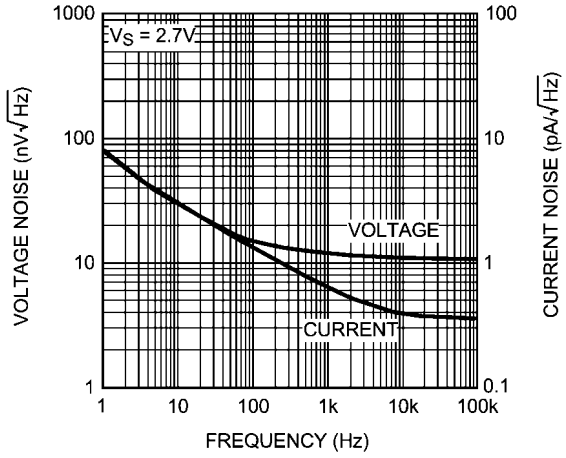
Large Signal Step Response



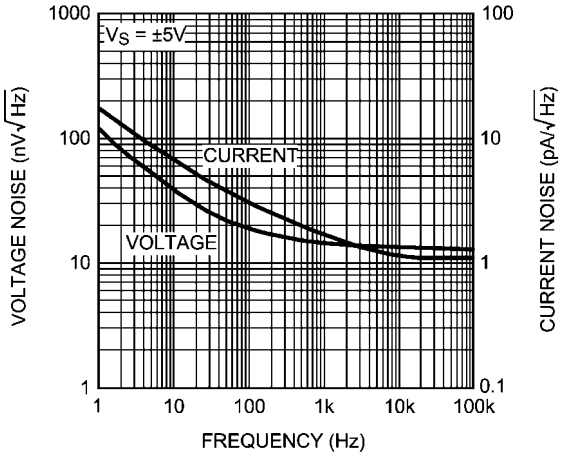
20205749

Input Referred Noise Density vs. Frequency



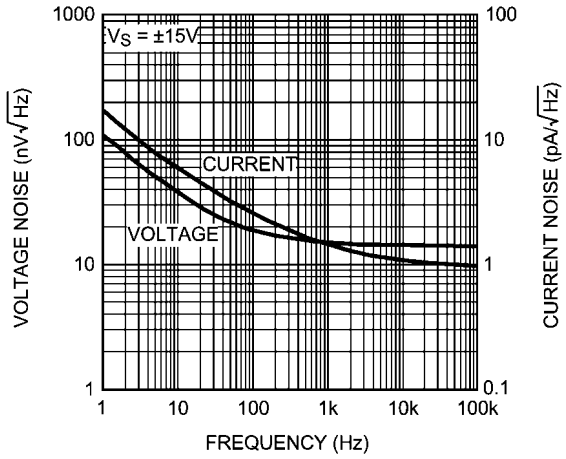
20205742

Input Referred Noise Density vs. Frequency



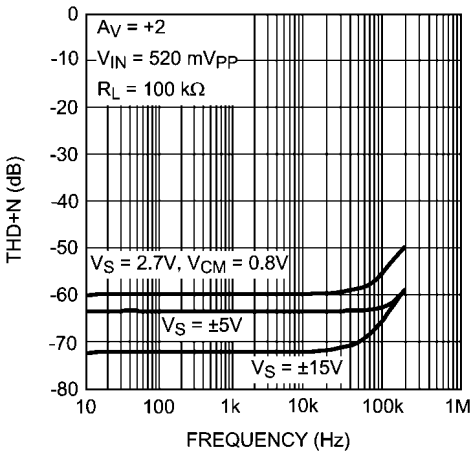
20205743

Input Referred Noise Density vs. Frequency



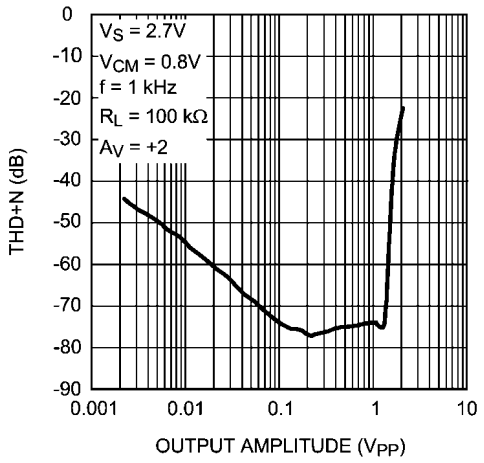
20205744

THD+N vs. Frequency



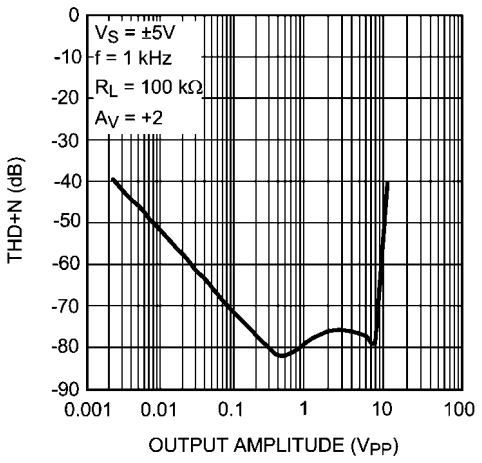
20205745

THD+N vs. Output Amplitude



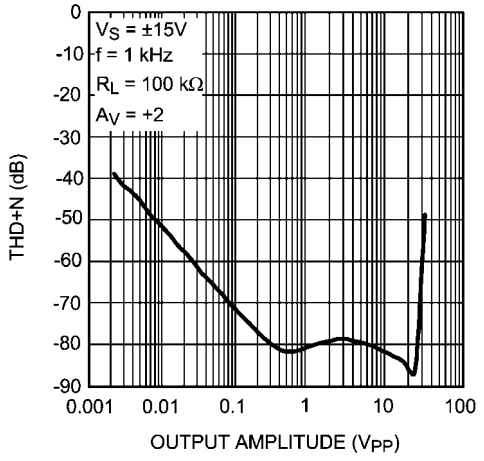
20205746

THD+N vs. Output Amplitude



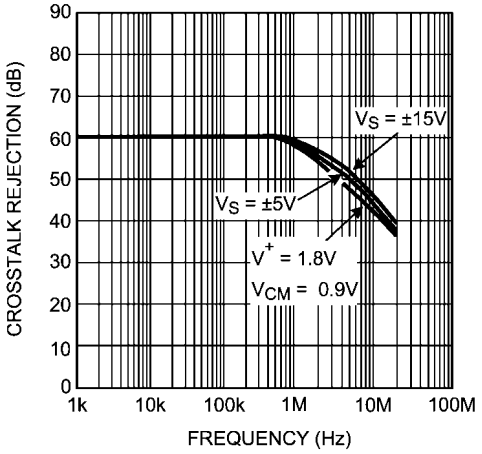
20205747

THD+N vs. Output Amplitude



20205748

Crosstalk Rejection vs. Frequency



20205768

Application Information

DRIVING CAPACITIVE LOADS

The LM7321/LM7322 are specifically designed to drive unlimited capacitive loads without oscillations as shown in *Figure 1*.

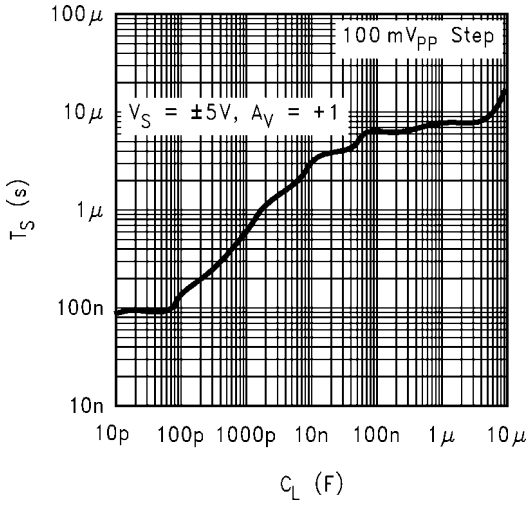


FIGURE 1. ±5% Settling Time vs. Capacitive Load

In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads as shown in *Figure 2* and *Figure 3*.

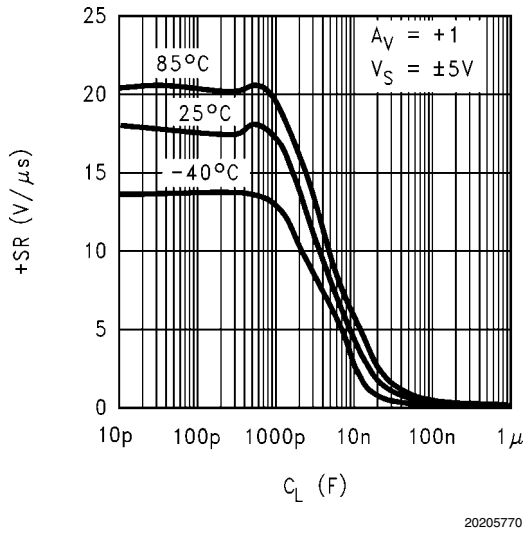


FIGURE 2. +SR vs. Capacitive Load

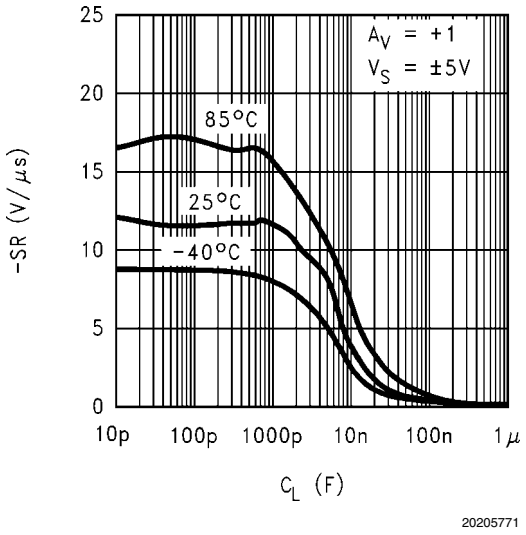


FIGURE 3. –SR vs. Capacitive Load

The combination of these features is ideal for applications such as TFT flat panel buffers, A/D converter input amplifiers, etc.

However, as in most op amps, addition of a series isolation resistor between the op amp and the capacitive load improves the settling and overshoot performance.

Output current drive is an important parameter when driving capacitive loads. This parameter will determine how fast the output voltage can change. Referring to the Slew Rate vs. Capacitive Load Plots (typical performance characteristics section), two distinct regions can be identified. Below about 10,000 pF, the output Slew Rate is solely determined by the op amp's compensation capacitor value and available current into that capacitor. Beyond 10 nF, the Slew Rate is determined by the op amp's available output current. Note that because of the lower output sourcing current compared to the sinking one, the Slew Rate limit under heavy capacitive loading is determined by the positive transitions. An estimate of positive and negative slew rates for loads larger than 100 nF can be made by dividing the short circuit current value by the capacitor.

For the LM7321/LM7322, the available output current increases with the input overdrive. Referring to *Figure 4* and *Figure 5*, Output Short Circuit Current vs. Input Overdrive, it can be seen that both sourcing and sinking short circuit current increase as input overdrive increases. In a closed loop amplifier configuration, during transient conditions while the fed back output has not quite caught up with the input, there will be an overdrive imposed on the input allowing more output current than would normally be available under steady state condition. Because of this feature, the op amp's output stage quiescent current can be kept to a minimum, thereby reducing power consumption, while enabling the device to deliver large output current when the need arises (such as during transients).

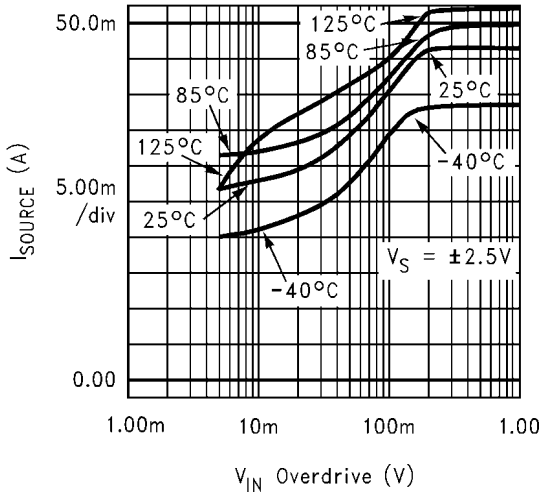


FIGURE 4. Output Short Circuit Sourcing Current vs. Input Overdrive

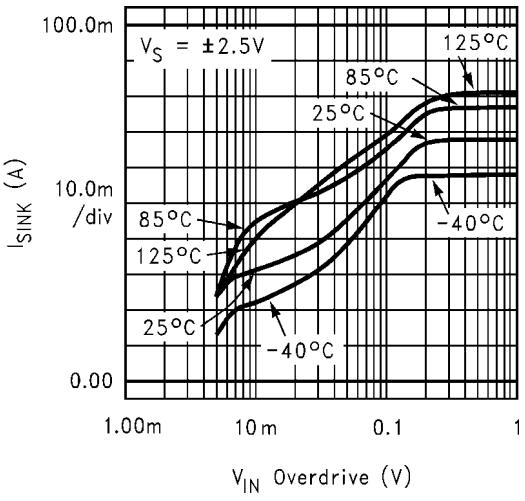


FIGURE 5. Output Short Circuit Sinking Current vs. Input Overdrive

Figure 6 shows the output voltage, output current, and the resulting input overdrive with the device set for A_V = +1 and the input tied to a 1 V_{PP} step function driving a 47 nF capacitor. As can be seen, during the output transition, the input overdrive reaches 1V peak and is more than enough to cause the output current to increase to its maximum value (see *Figure 4* and *Figure 5* plots). Note that because of the larger output sinking current compared to the sourcing one, the output negative transition is faster than the positive one.

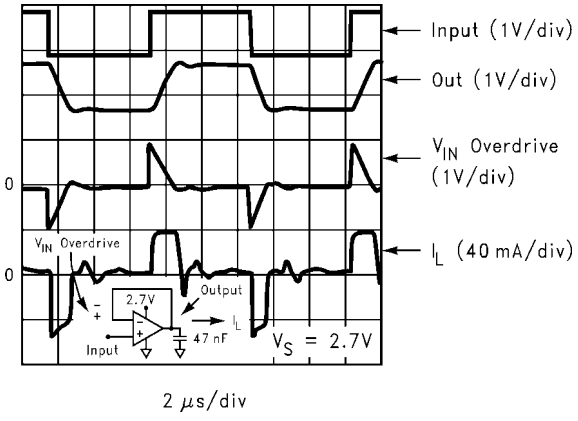


FIGURE 6. Buffer Amplifier Scope Photo

ESTIMATING THE OUTPUT VOLTAGE SWING

It is important to keep in mind that the steady state output current will be less than the current available when there is an input overdrive present. For steady state conditions, the Output Voltage vs. Output Current plot (Typical Performance Characteristics section) can be used to predict the output swing. *Figure 7* and *Figure 8* show this performance along with several load lines corresponding to loads tied between the output and ground. In each cases, the intersection of the device plot at the appropriate temperature with the load line would be the typical output swing possible for that load. For example, a 1 kΩ load can accommodate an output swing to within 250 mV of V⁻ and to 330 mV of V⁺ (V_S = ±15V) corresponding to a typical 29.3 V_{PP} unclipped swing.

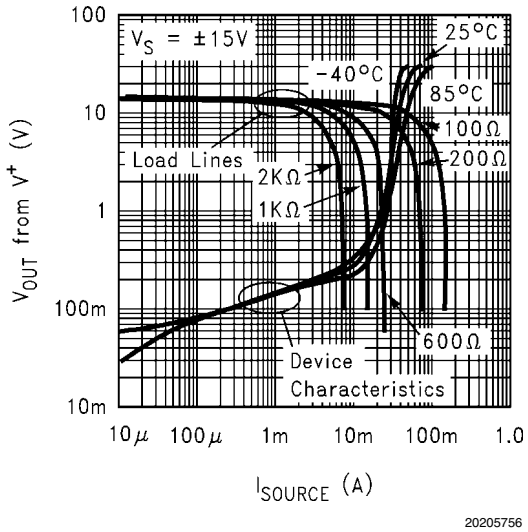


FIGURE 7. Output Sourcing Characteristics with Load Lines

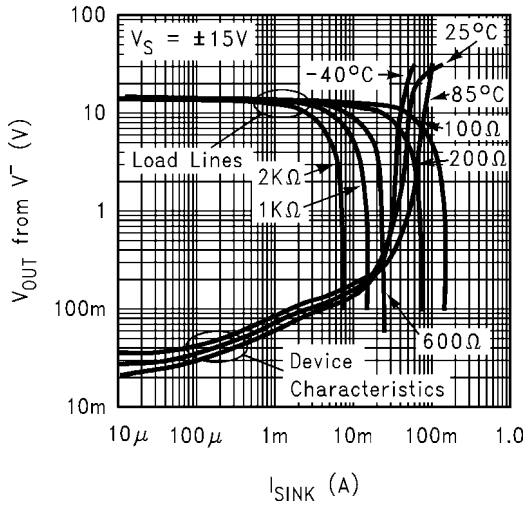


FIGURE 8. Output Sinking Characteristics with Load Lines

SETTLING TIME WITH LARGE CAPACITIVE LOADS

Figure 9 below, shows a typical application where the LM7321/LM7322 is used as a buffer amplifier for the V_{COM} signal employed in a TFT LCD flat panel:

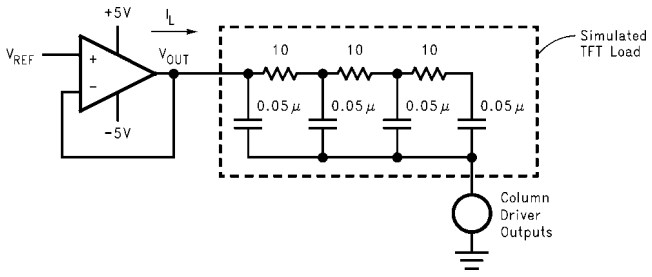


FIGURE 9. V_{COM} Driver Application Schematic

Figure 10 shows the time domain response of the amplifier when used as a V_{COM} buffer/driver with V_{REF} at ground. In this application, the op amp loop will try and maintain its output voltage based on the voltage on its non-inverting input (V_{REF}) despite the current injected into the TFT simulated load. As long as this load current is within the range tolerable by the LM7321/LM7322 (45 mA sourcing and 65 mA sinking for ±5V supplies), the output will settle to its final value within less than 2 µs.

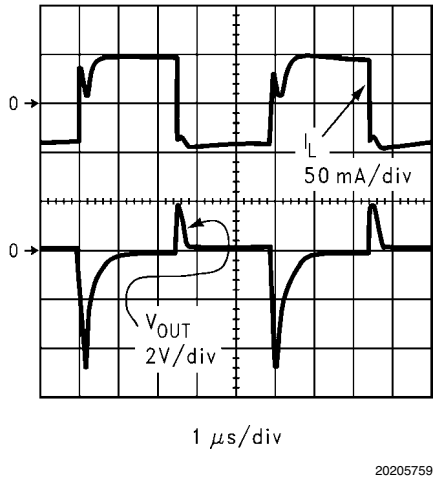


FIGURE 10. V_{COM} Driver Performance Scope Photo

OUTPUT SHORT CIRCUIT CURRENT AND DISSIPATION ISSUES

The LM7321/LM7322 output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions. Below supply voltage of 6V, the output short circuit condition can be tolerated indefinitely.

With the op amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power itself could include an average value (due to a DC load current) and an AC component. DC load current would flow if there is an output voltage offset, or the output AC average current is non-zero, or if the op amp operates in a single supply application where the output is maintained somewhere in the range of linear operation.

Therefore:

$P_{TOTAL} = P_Q + P_{DC} + P_{AC}$

$P_Q = I_S \cdot V_S$ Op Amp Quiescent Power Dissipation

$P_{DC} = I_O \cdot (V_r - V_o)$ DC Load Power

P_{AC} = See Table 1 below AC Load Power

where:

I_S: Supply Current

V_S: Total Supply Voltage ($V^+ - V^-$)

V_O: Average Output Voltage

V_r: V^+ for sourcing and V^- for sinking current

Table 1 below shows the maximum AC component of the load power dissipated by the op amp for standard Sinusoidal, Triangular, and Square Waveforms:

TABLE 1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} (W.Ω/V²)		
Sinusoidal	Triangular	Square
50.7 x 10^{-3}	46.9 x 10^{-3}	62.5 x 10^{-3}

The table entries are normalized to V_S^2/R_L. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor V_S^2/R_L. For example, with ±12V supplies, a 600Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = (46.9 \times 10^{-3}) \cdot [242/600] = 45.0 \text{ mW}$$

The maximum power dissipation allowed at a certain temperature is a function of maximum die junction temperature ($T_{J(MAX)}$) allowed, ambient temperature T_A, and package thermal resistance from junction to ambient, θ_{JA}.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

For the LM7321/LM7322, the maximum junction temperature allowed is 150°C at which no power dissipation is allowed. The power capability at 25°C is given by the following calculations:

For MSOP package:

$$P_{D(MAX)} = \frac{150°C - 25°C}{235°C/W} = 0.53W$$

For SOIC package:

$$P_{D(MAX)} = \frac{150°C - 25°C}{165°C/W} = 0.76W$$

Similarly, the power capability at 125°C is given by:

For MSOP package:

$$P_{D(MAX)} = \frac{150°C - 125°C}{235°C/W} = 0.11W$$

For SOIC package:

$$P_{D(MAX)} = \frac{150°C - 125°C}{165°C/W} = 0.15W$$

Figure 11 shows the power capability vs. temperature for MSOP and SOIC packages. The area under the maximum thermal capability line is the operating area for the device. When the device works in the operating area where P_{TOTAL} is less than $P_{D(MAX)}$, the device junction temperature will remain below 150°C. If the intersection of ambient temperature and package power is above the maximum thermal capability line, the junction temperature will exceed 150°C and this should be strictly prohibited.

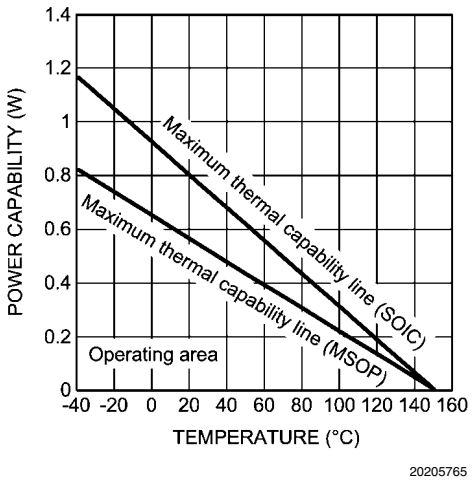


FIGURE 11. Power Capability vs. Temperature

When high power is required and ambient temperature can't be reduced, providing air flow is an effective approach to reduce thermal resistance therefore to improve power capability.

Other Application Hints

The use of supply decoupling is mandatory in most applications. As with most relatively high speed/high output current Op Amps, best results are achieved when each supply line is decoupled with two capacitors; a small value ceramic capacitor (~0.01 µF) placed very close to the supply lead in addition to a large value Tantalum or Aluminum (> 4.7 µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor will act as the charge "bucket" for fast load current spikes at the op amp output. The combination of these capacitors will provide supply decoupling and will help keep the op amp oscillation free under any load.

SIMILAR HIGH OUTPUT DEVICES

The LM7332 is a dual rail-to-rail amplifier with a slightly lower GBW capable of sinking and sourcing 100 mA. It is available in SOIC and MSOP packages.

The LM4562 is dual op amp with very low noise and 0.7 mV voltage offset.

The LME49870 and LME49860 are single and dual low noise amplifiers that can work from ±22 volt supplies.

OTHER HIGH PERFORMANCE SOT-23 AMPLIERS

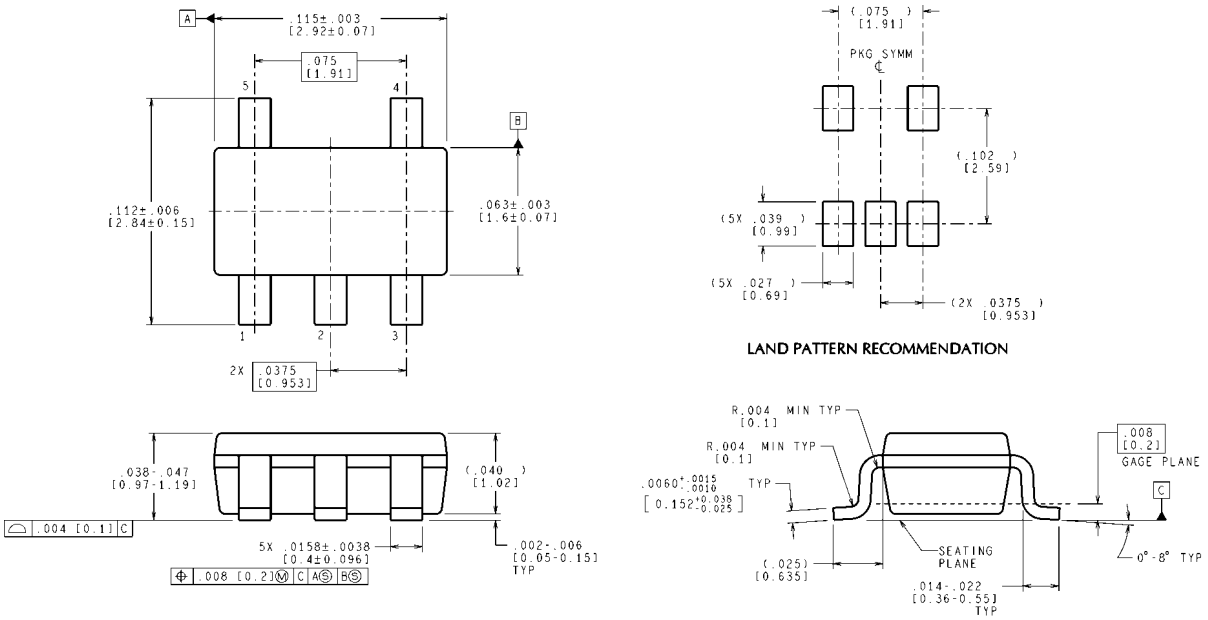
The LM7341 is a 4 MHz rail-to-rail input and output part that requires only 0.6 mA to operate, and can drive unlimited capacitive load. It has a voltage gain of 97 dB, a CMRR of 93 dB, and a PSRR of 104 dB.

The LM6211 is a 20 MHz part with CMOS input, which runs on ±12 volt or 24 volt single supplies. It has rail-to-rail output and low noise.

The LM7121 has a gain bandwidth of 235 MHz.

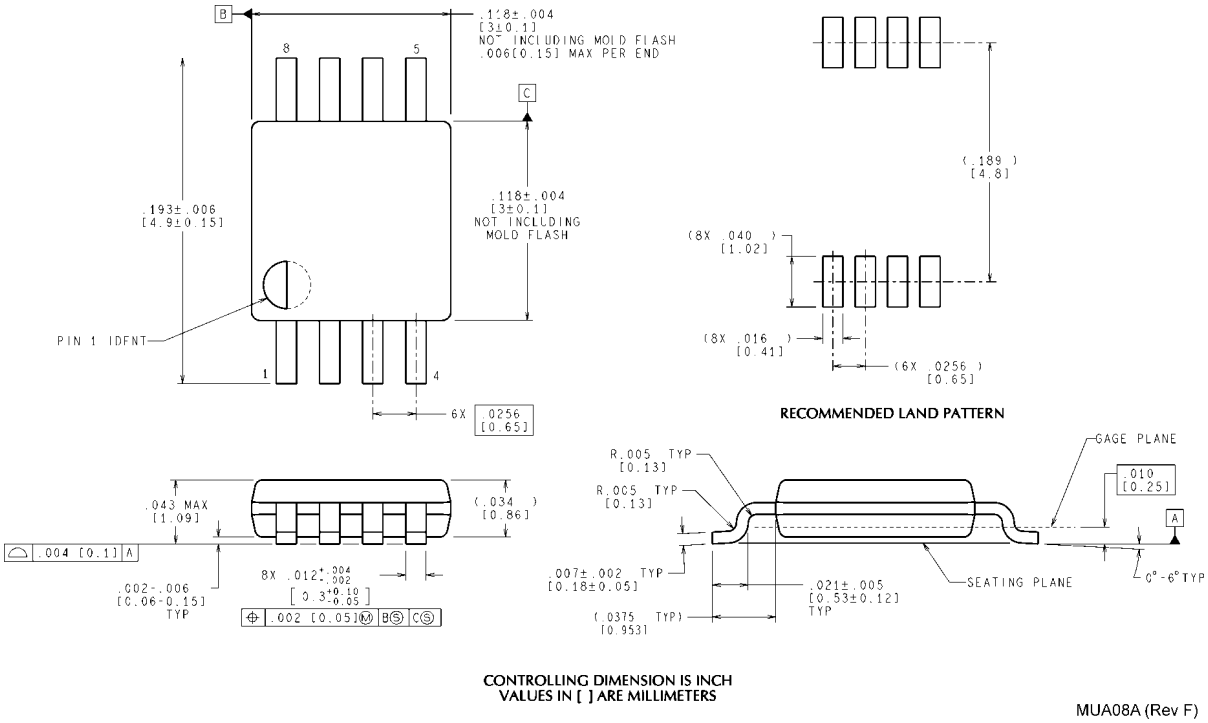
Detailed information on these parts can be found at www.national.com.

Physical Dimensions inches (millimeters) unless otherwise noted



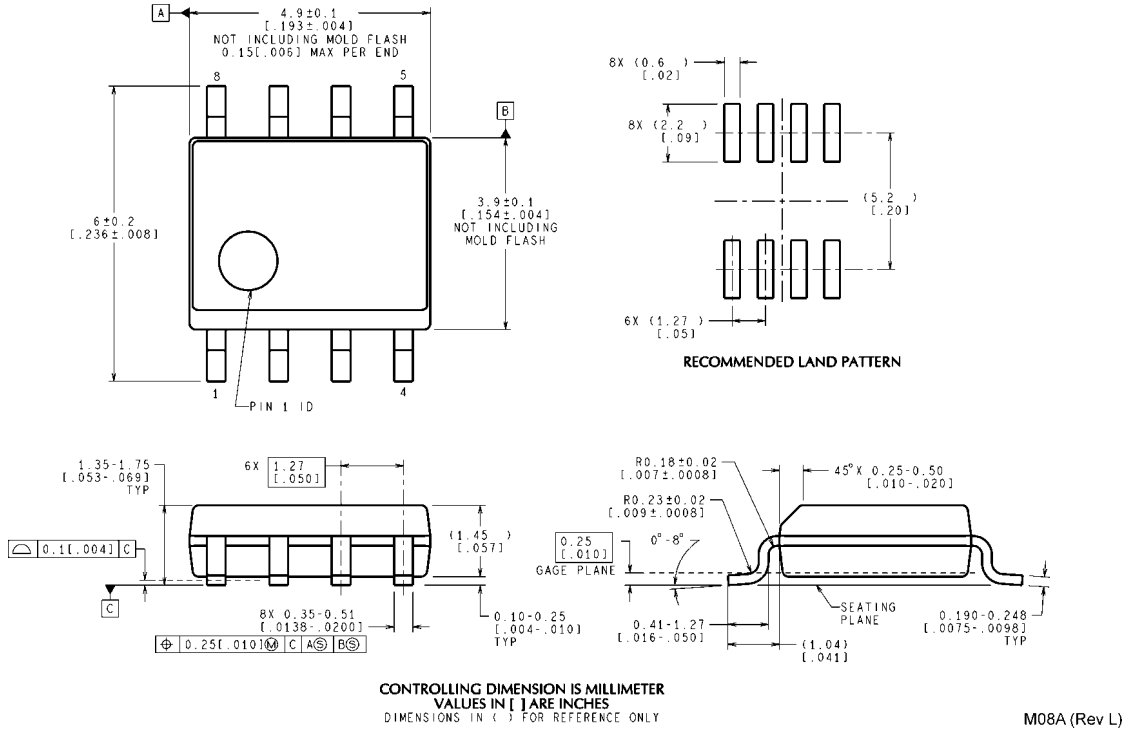
MF05A (Rev D)

5-Pin SOT-23
NS Package Number MF05A



MUA08A (Rev F)

8-Pin MSOP
NS Package Number MUA08A



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M08A (Rev L)

8-Pin SOIC
NS Package Number M08A

Notes

Notes

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