

LMC8101 Rail-to-Rail Input and Output, 2.7V Op Amp in DSBGA Package With Shutdown

Check for Samples: [LMC8101](#)

FEATURES

- $V_S = 2.7V$, $T_A = 25^\circ C$, R_L to $V^+/2$, Typical Values Unless Specified.
- Rail-to-Rail Inputs
- Rail-to-Rail Output Swing Within 35mV of Supplies ($R_L = 2k\Omega$)
- Packages Offered:
 - DSBGA package 1.39mm x 1.41mm
 - VSSOP package 3.0mm x 4.9mm
- Low Supply Current <1mA (max)
- Shutdown Current 1 μ A (Max)
- Versatile Shutdown Feature 10 μ s Turn-On
- Output Short Circuit Current 10mA
- Offset Voltage ± 5 mV (max)
- Gain-Bandwidth 1MHz
- Supply Voltage Range 2.7V-10V
- THD 0.18%
- Voltage Noise 36nV/ \sqrt{Hz}

APPLICATIONS

- Portable Communication (Voice, Data)
- Cellular Phone Power Amp Control Loop
- Buffer AMP
- Active Filters
- Battery Sense
- VCO Loop

DESCRIPTION

The LMC8101 is a Rail-to-Rail Input and Output high performance CMOS operational amplifier. The LMC8101 is ideal for low voltage (2.7V to 10V) applications requiring Rail-to-Rail inputs and output. The LMC8101 is supplied in the die sized DSBGA as well as the 8 pin VSSOP packages. The DSBGA package requires 75% less board space as compared to the SOT-23 package. The LMC8101 is an upgrade to the industry standard LMC7101.

The LMC8101 incorporates a simple user controlled methodology for shutdown. This allows ease of use while reducing the total supply current to 1nA typical. This extends battery life where power saving is mandated. The shutdown input threshold can be set relative to either V^+ or V^- using the SL pin (see [Application Notes](#) section for details).

Other enhancements include improved offset voltage limit, three times the output current drive and lower 1/f noise when compared to the industry standard LMC7101 Op Amp. This makes the LMC8101 ideal for use in many battery powered, wireless communication and Industrial applications.



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Connection Diagrams

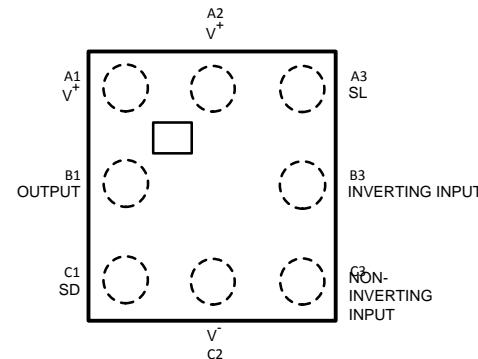
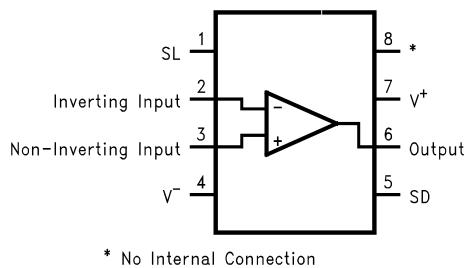


Figure 1. 8-Pin VSSOP Top View

Figure 2. DSBGA Top View



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

ESD Tolerance		2KV ⁽³⁾ 200V ⁽⁴⁾
V_{IN} differential		\pm Supply Voltage
Output Short Circuit Duration		See ⁽⁵⁾⁽⁶⁾
Supply Voltage ($V^+ - V^-$)		12V
Voltage at Input/Output pins		$V^+ +0.8V$, $V^- -0.8V$
Current at Input Pin		$\pm 10mA$
Current at Output Pin ⁽⁵⁾⁽⁶⁾		$\pm 80mA$
Current at Power Supply pins		$\pm 80mA$
Storage Temperature Range		-65°C to +150°C
Junction Temperature ⁽⁷⁾		+150°C
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human body model, 1.5kΩ in series with 100pF.
- (4) Machine Model, 0Ω in series with 200pF.
- (5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C. Output currents in excess of 40mA over long term may adversely affect reliability.
- (6) Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S < 6V$. Otherwise, extended period output short circuit may damage the device.
- (7) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings

Supply Voltage ($V^+ - V^-$)	2.7V to 10V	
Junction Temperature Range ⁽²⁾	-40°C to +85°C	
Package Thermal Resistance (θ_{JA}) ⁽²⁾	DSBGA	220°C/W
	VSSOP package 8 pin Surface Mount	230°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For ensured specifications and the test conditions, see the Electrical Characteristics.

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2.7V Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Limit ⁽²⁾	Units
V_{OS}	Input Offset Voltage		±0.70	±5 ±7	mV max
TCV_{OS}	Input Offset Voltage Average Drift		4		µV/°C
I_B	Input Bias Current	See ⁽³⁾	±1	±64	pA max
I_{OS}	Input Offset Current		0.5	32	pA max
$R_{in\ CM}$	Input Common Mode Resistance		10		GΩ
$C_{in\ CM}$	Input Common Mode Capacitance		10		pF
CMRR	Common Mode Rejection Ratio	0V <= V_{CM} <= 2.7V	78	60	dB min
		$V_S = 3\text{V}$ 0V <= V_{CM} <= 3V	78	64 60	
PSRR	Power Supply Rejection Ratio	$V_S = 2.7\text{V}$ to 3V	57	50 48	dB min
CMVR	Input Common-Mode Voltage Range	$V_S = 2.7\text{V}$ CMRR >= 50dB	0.0	0.0	V max
			3.0	2.7	V min
		$V_S = 3\text{V}$ CMRR >= 50dB	-0.2	-0.1	V max
			3.2	3.1	V min
A_{VOL}	Large Signal Voltage Gain	Sourcing $R_L = 2\text{k}\Omega$ to $V^+/2$ $V_O = 1.35\text{V}$ to 2.45V	3162	1000 562	V/V min
		Sinking $R_L = 2\text{k}\Omega$ to $V^+/2$ $V_O = 1.35\text{V}$ to 0.25V	3162	804 562	
		Sourcing $R_L = 10\text{k}\Omega$ to $V^+/2$ $V_O = 1.35\text{V}$ to 2.65V	4000	1778 1000	V/V min
		Sinking $R_L = 10\text{k}\Omega$ to $V^+/2$ $V_O = 1.35\text{V}$ to 0.05V	4000	1778 1000	
V_O	Output Swing High	$R_L = 2\text{k}\Omega$ to $V^+/2$ $V_{ID} = 100\text{mV}$	2.67	2.64 2.62	V min
		$R_L = 10\text{k}\Omega$ to $V^+/2$ $V_{ID} = 100\text{mV}$	2.69	2.68 2.67	V min
	Output Swing Low	$R_L = 2\text{k}\Omega$ to $V^+/2$ $V_{ID} = -100\text{mV}$	32	100 150	mV max
		$R_L = 10\text{k}\Omega$ to $V^+/2$ $V_{ID} = -100\text{mV}$	10	30 70	mV max

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) Positive current corresponds to current flowing into the device.

2.7V Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Limit ⁽²⁾	Units
I _{SC}	Output Short Circuit Current	Sourcing to $V^+/2$ $V_{\text{ID}} = 100\text{mV}^{(4)}$	20	14 6	mA min
		Sinking to $V^+/2$ $V_{\text{ID}} = -100\text{mV}^{(4)}$	10	5 4	mA min
I _S	Supply Current	No load, normal operation	0.70	1.0 1.2	mA max
		Shutdown mode	0.001	1	μA max
T _{on}	Shutdown Turn-on time	See ⁽⁵⁾	10	15	μs
T _{off}	Shutdown Turn-off time	See ⁽⁵⁾	1		μs
I _{in}	"SL" and "SD" Input Current ⁽⁶⁾		±1	±64	pA max
SR	Slew Rate ⁽⁷⁾	$A_V = +1$, $R_L = 10\text{k}\Omega$ to $V^+/2$ $V_I = 1\text{V}_{\text{PP}}$	1	0.8	V/μs min
f _u	Unity Gain-Bandwidth	$V_I = 10\text{mV}$, $R_L = 2\text{k}\Omega$ to $V^+/2$	750		KHz
GBW	Gain Bandwidth Product	$f = 100\text{KHz}$	1		MHz
e _n	Input-Referred Voltage Noise	$f = 10\text{KHz}$, $R_S = 50\Omega$	36		nV/√Hz
i _n	Input-Referred Current Noise	$f = 10\text{KHz}$	1.5		fA/√Hz
THD	Total Harmonic Distortion	$f = 1\text{KHz}$, $A_V = +1$, $V_O = 2.2\text{V}_{\text{pp}}$, $R_L = 600\Omega$ to $V^+/2$	0.18		%

- (4) Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S < 6\text{V}$. Otherwise, extended period output short circuit may damage the device.
- (5) Shutdown Turn-on and Turn-off times are defined as the time required for the output to reach 90% and 10%, respectively, of its final peak to peak swing when set for Rail to Rail output swing with a 100KHz sine wave, 2KΩ load, and $A_V = +10$.
- (6) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
- (7) Slew rate is the slower of the rising and falling slew rates.

±5V Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = -5\text{V}$, $V_{\text{CM}} = V_O = 0\text{V}$, and $R_L > 1\text{ M}\Omega$ to gnd.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Limit ⁽²⁾	Units
V _{OS}	Input Offset Voltage		±0.7	±5 ±7	mV max
TCV _{OS}	Input Offset Voltage Average Drift		4		μV/°C
I _B	Input Bias Current	See ⁽³⁾	±1	±64	pA max
I _{OS}	Input Offset Current		0.5	32	pA max
R _{in CM}	Input Common Mode Resistance		10		GΩ
C _{in CM}	Input Common Mode Capacitance		10		pF
CMRR	Common-Mode Rejection Ratio	$-5\text{V} \leq V_{\text{CM}} \leq 5\text{V}$	87	70 67	dB min
PSRR	Power Supply Rejection Ratio	$V_S = 5\text{V}$ to 10V	80	76 72	dB min
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	-5.3	-5.2 -5.0	V max
			5.3	5.2 5.0	V min

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) Positive current corresponds to current flowing into the device.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = -5\text{V}$, $V_{\text{CM}} = V_O = 0\text{V}$, and $R_L > 1\text{ M}\Omega$ to gnd.

Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Limit ⁽²⁾	Units
A _{VOL}	Large Signal Voltage Gain	Sourcing $R_L = 600\Omega$ $V_O = 0\text{V}$ to 4V	34.5	17.8 10	V/mV min
		Sinking $R_L = 600\Omega$ $V_O = 0\text{V}$ to -4V	34.5	17.8 3.16	
		Sourcing $R_L = 2\text{k}\Omega$ $V_O = 0\text{V}$ to 4.6V	138	31.6 17.8	V/mV min
		Sinking $R_L = 2\text{k}\Omega$ $V_O = 0\text{V}$ to -4.6V	138	31.6 10	
V _O	Output Swing High	$R_L = 600\Omega$ $V_{ID} = 100\text{mV}$	4.73	4.60 4.54	V min
		$R_L = 2\text{k}\Omega$ $V_{ID} = 100\text{mV}$	4.90	4.85 4.83	V min
	Output Swing Low	$R_L = 600\Omega$ $V_{ID} = -100\text{mV}$	-4.85	-4.75 -4.65	V max
		$R_L = 2\text{k}\Omega$ $V_{ID} = -100\text{mV}$	-4.95	4.90 -4.84	V max
I _{sc}	Output Short Circuit Current	Sourcing, $V_{ID} = 100\text{mV}$ ⁽⁴⁾⁽⁵⁾	49	30 25	mA min
		Sinking, $V_{ID} = -100\text{mV}$ ⁽⁴⁾⁽⁵⁾	90	60 52	mA min
I _s	Supply Current	No load, normal operation	1.1	1.7 1.9	mA max
		Shutdown mode	0.001	1	μA
T _{on}	Shutdown Turn-on time	See ⁽⁶⁾	10	15	μs
T _{off}	Shutdown Turn-off time	See ⁽⁶⁾	1		μs
I _{in}	"SL" and "SD" Input Current		±1	±64	pA max
SR	Slew Rate ⁽⁷⁾	$A_V = +10$, $R_L = 10\text{k}\Omega$, $V_O = 10\text{Vpp}$, $C_L = 1000\text{pF}$	1.2		V/μs
f _u	Unity Gain-Bandwidth	$V_I = 10\text{mV}$ $R_L = 2\text{k}\Omega$	840		KHz
GBW	Gain Bandwidth Product	$f = 10\text{KHz}$	1.3		MHz
e _n	Input-Referred Voltage Noise	$f = 10\text{KHz}$, $R_s = 50\Omega$	33		nV/√Hz
i _n	Input-Referred Current Noise	$f = 10\text{KHz}$	1.5		fA/√Hz
THD	Total Harmonic Distortion	$f = 10\text{KHz}$, $A_V = +1$, $V_O = 8\text{Vpp}$, $R_L = 600\Omega$	0.2		%

- (4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C . Output currents in excess of 40mA over long term may adversely affect reliability.
- (5) Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S < 6\text{V}$. Otherwise, extended period output short circuit may damage the device.
- (6) Shutdown Turn-on and Turn-off times are defined as the time required for the output to reach 90% and 10%, respectively, of its final peak to peak swing when set for Rail to Rail output swing with a 100KHz sine wave, 2KΩ load, and $A_V = +10$.
- (7) Slew rate is the slower of the rising and falling slew rates.

Typical Performance Characteristics

$V_S = 2.7V$, Single Supply, $V_{CM} = V^+/2$, $T_A = 25^\circ C$ unless specified

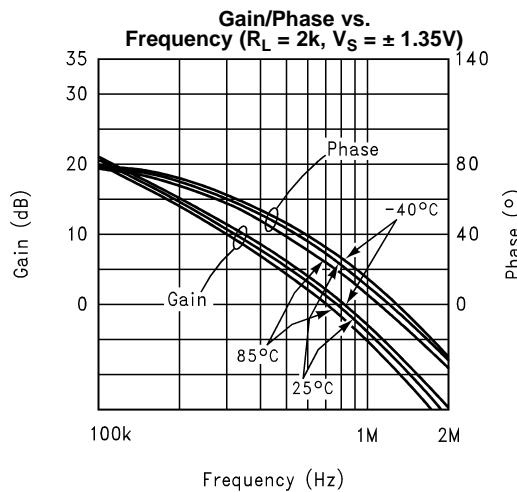


Figure 3.

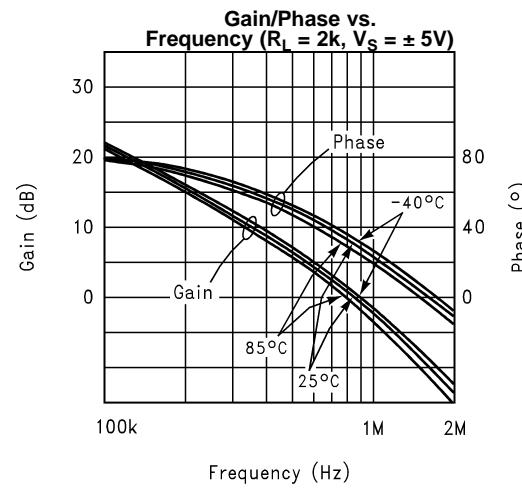


Figure 4.

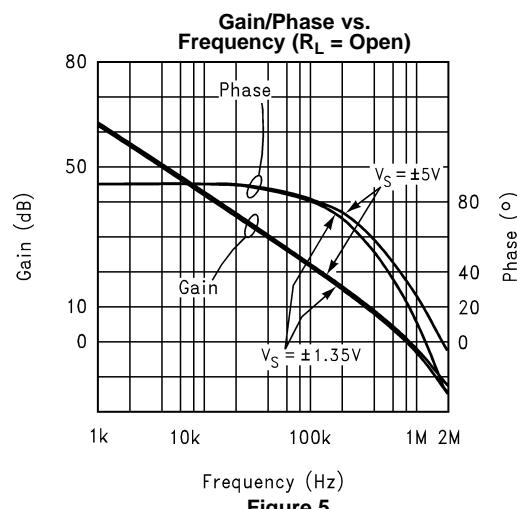


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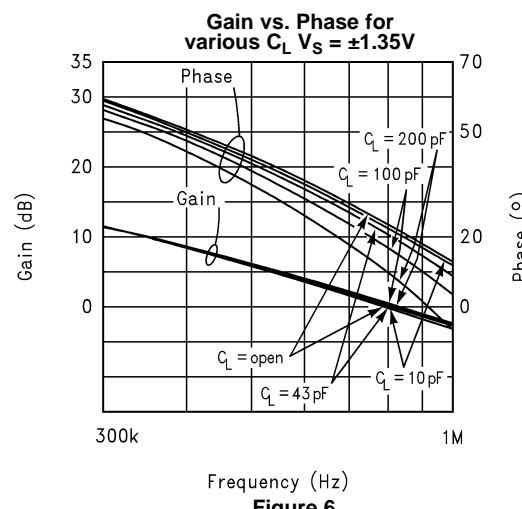


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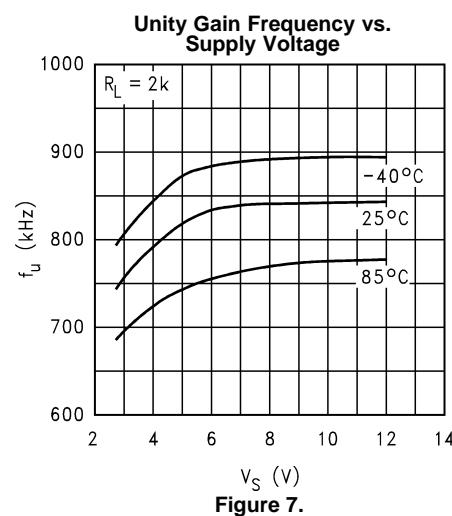


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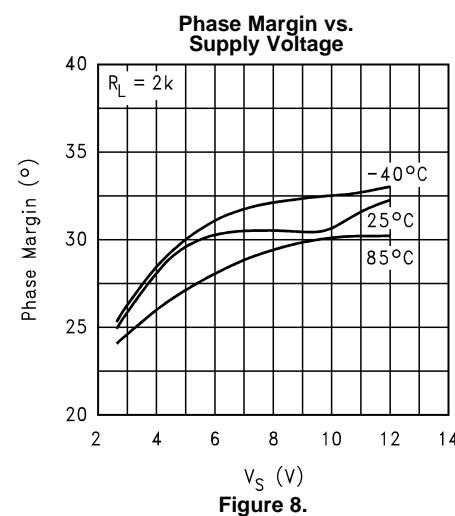


Figure 8.

Typical Performance Characteristics (continued)

$V_S = 2.7V$, Single Supply, $V_{CM} = V^+/2$, $T_A = 25^\circ C$ unless specified

Unity Gain Frequency and Phase Margin vs. Load

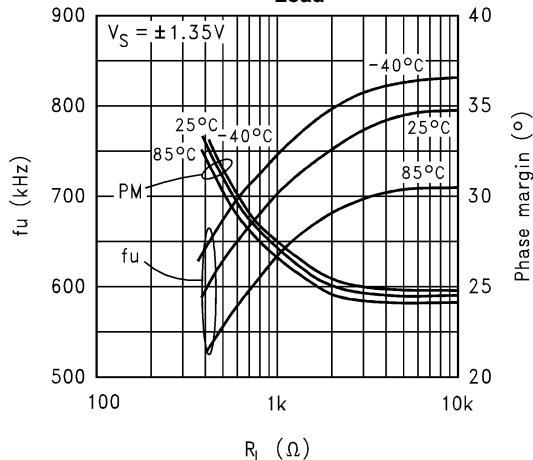


Figure 9.

Unity Gain Frequency and Phase Margin vs. Load

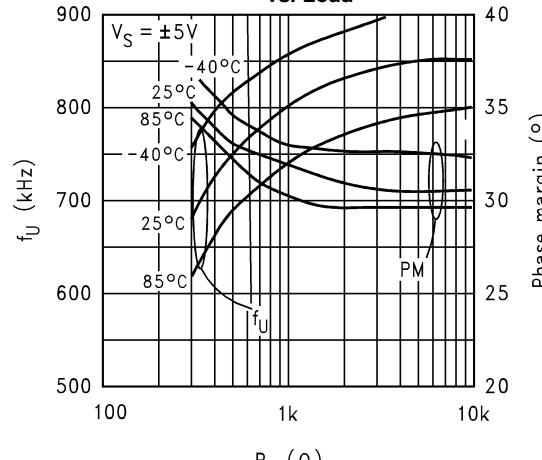


Figure 10.

PSRR vs. Frequency

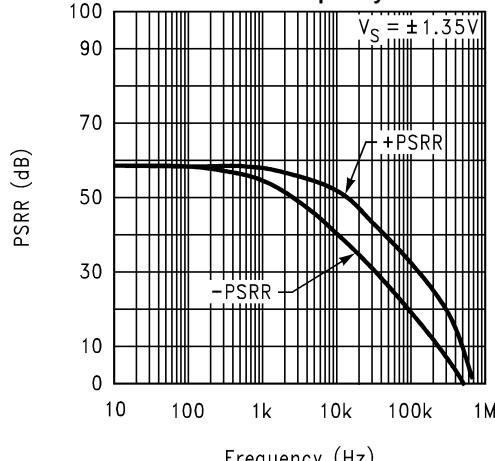


Figure 11.

PSRR vs. Frequency

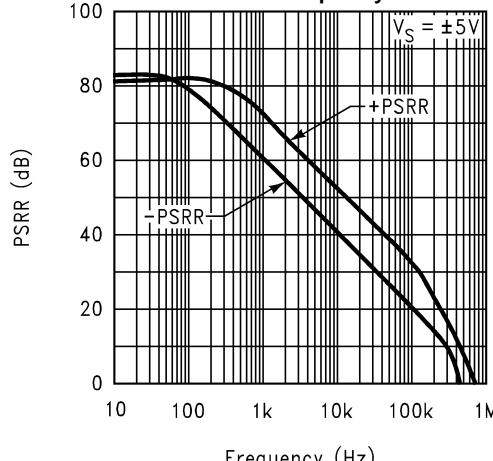


Figure 12.

CMRR vs. Frequency

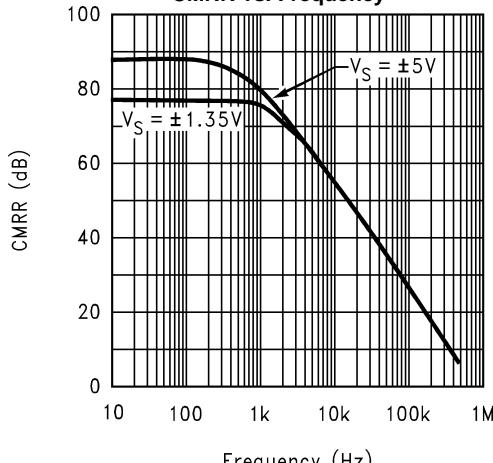


Figure 13.

Input Bias Current vs. Common Mode Voltage @ 85°C

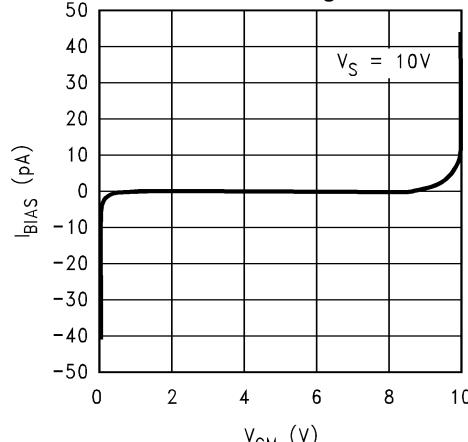


Figure 14.

Typical Performance Characteristics (continued)

$V_S = 2.7V$, Single Supply, $V_{CM} = V^+/2$, $T_A = 25^\circ C$ unless specified

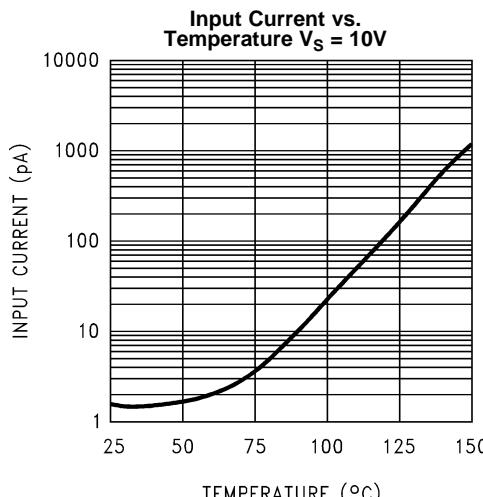


Figure 15.

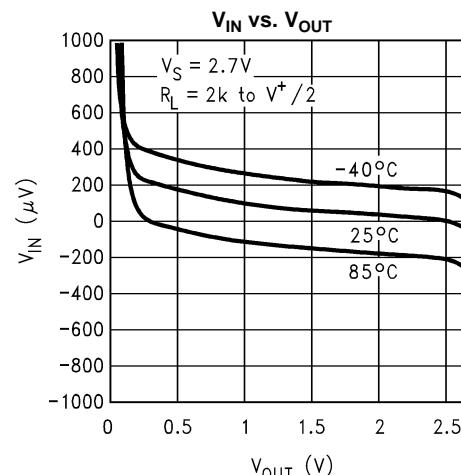


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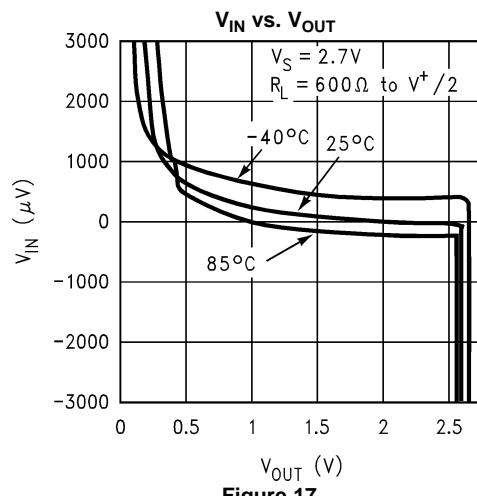


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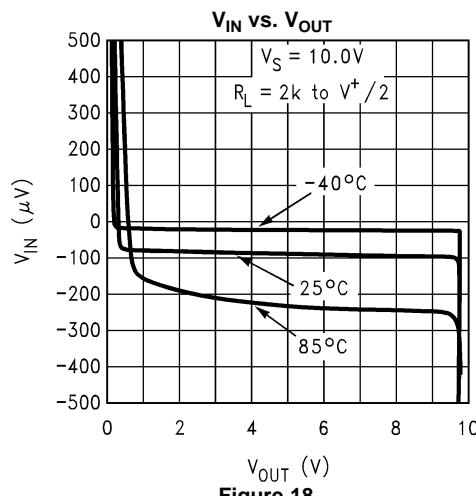


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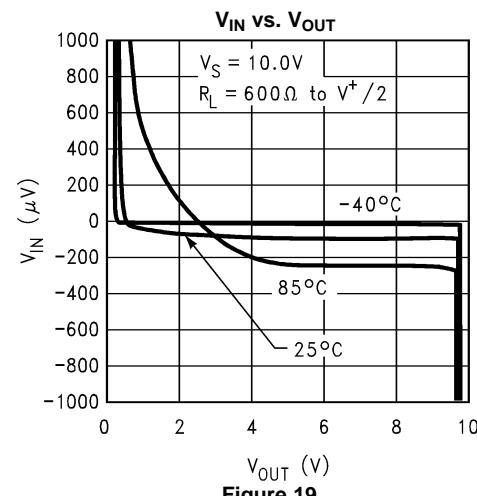


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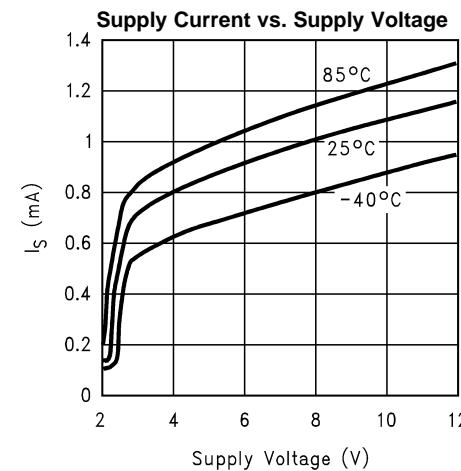


Figure 20.

Typical Performance Characteristics (continued)

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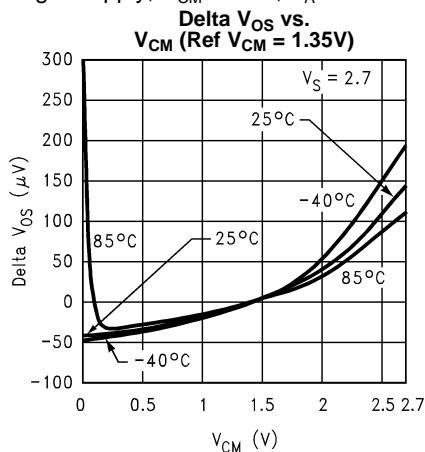


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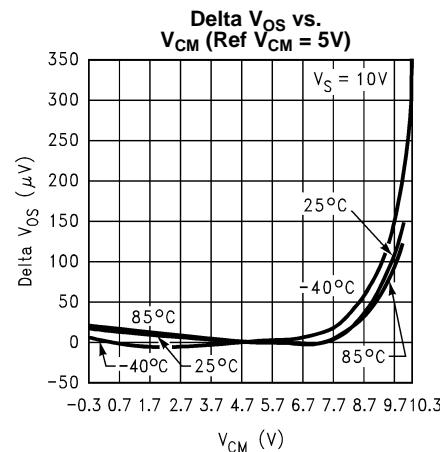


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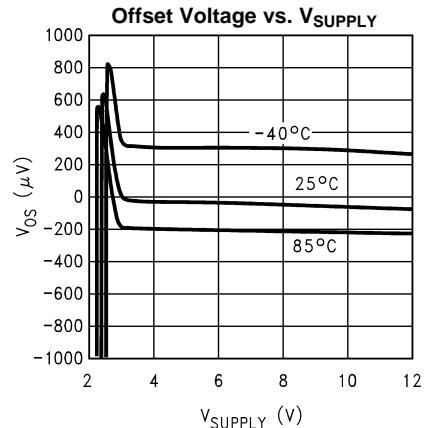


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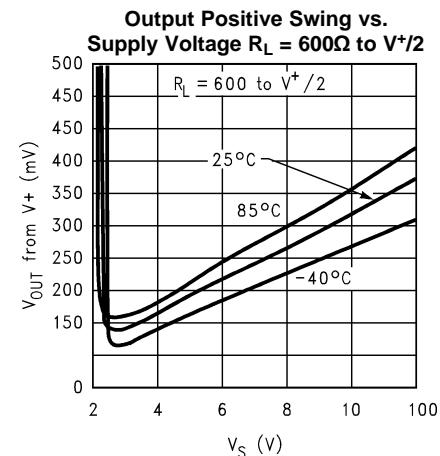


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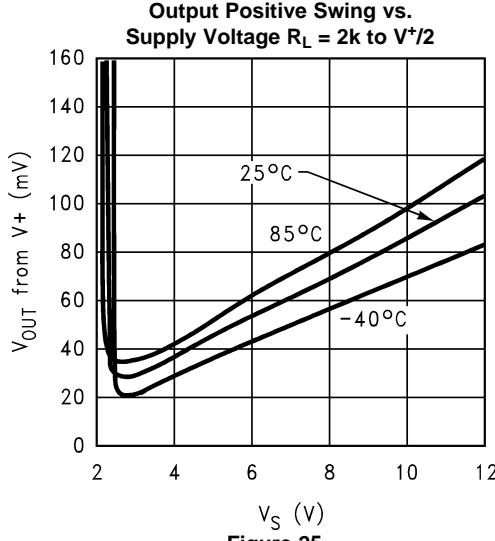


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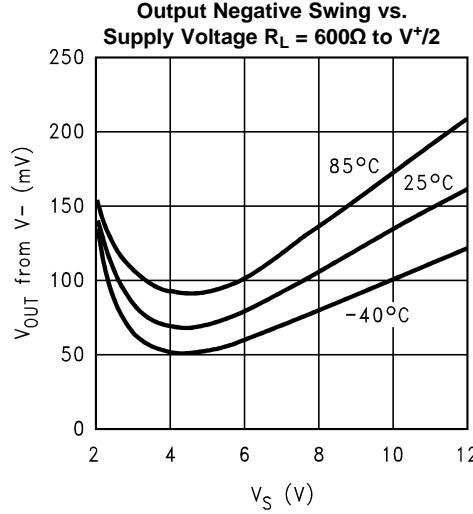


Figure 26.

Typical Performance Characteristics (continued)

$V_S = 2.7V$, Single Supply, $V_{CM} = V^+/2$, $T_A = 25^\circ C$ unless specified

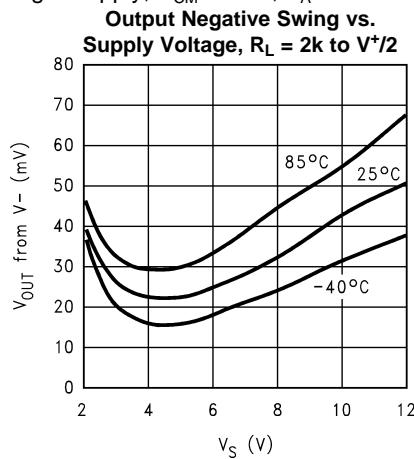


Figure 27.

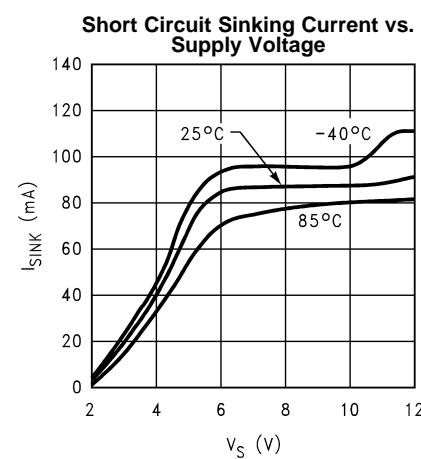


Figure 28.

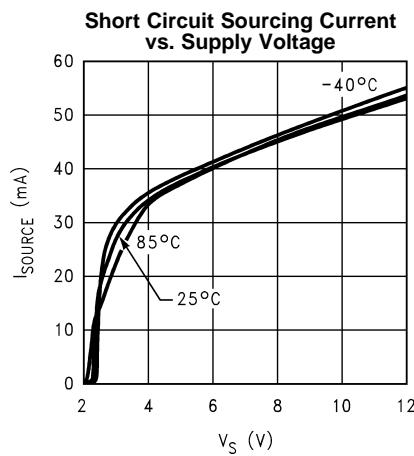


Figure 29.

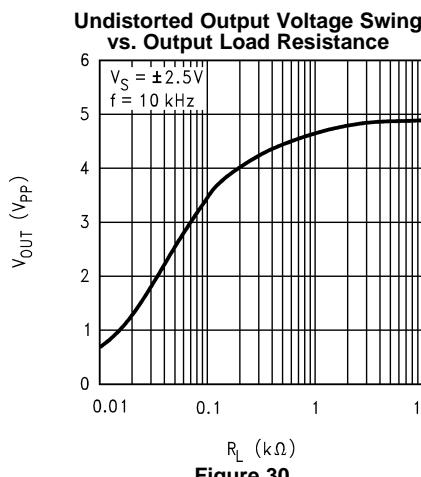


Figure 30.

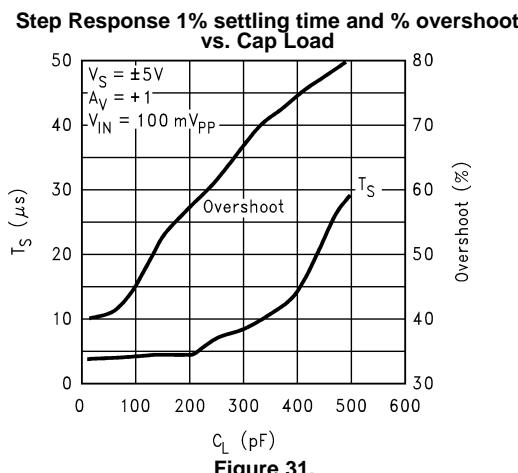


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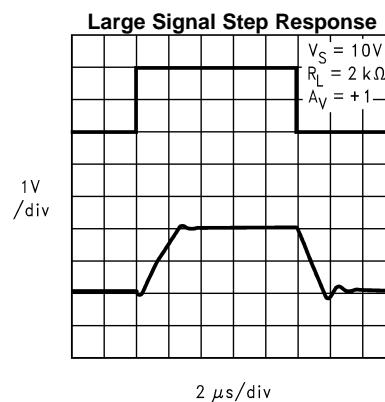


Figure 32.

Typical Performance Characteristics (continued)

$V_S = 2.7V$, Single Supply, $V_{CM} = V^+/2$, $T_A = 25^\circ C$ unless specified

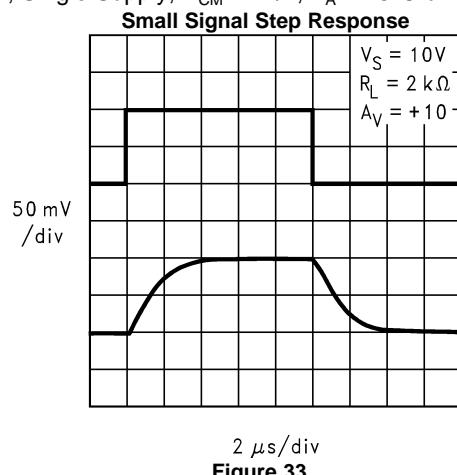


Figure 33.

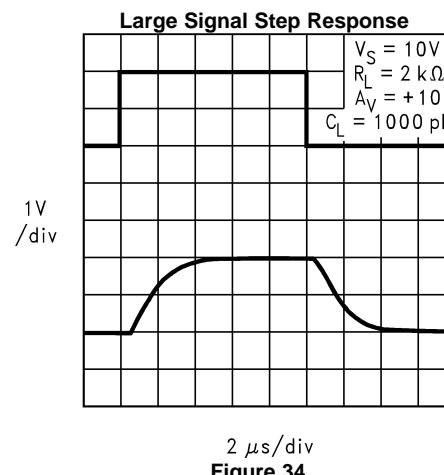


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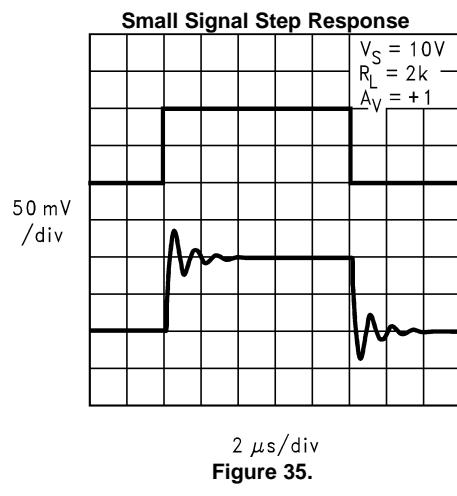


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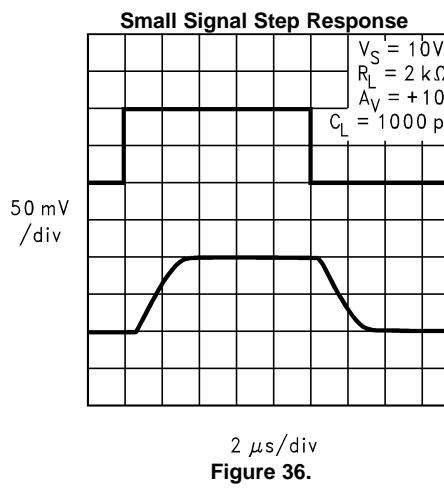


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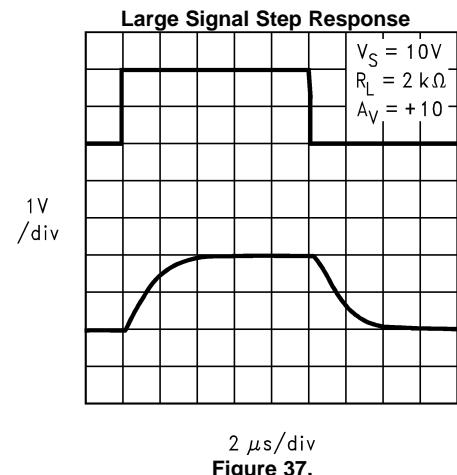


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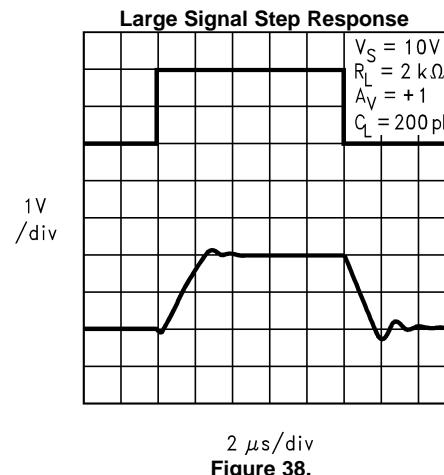


Figure 38.

Typical Performance Characteristics (continued)

$V_S = 2.7V$, Single Supply, $V_{CM} = V^+/2$, $T_A = 25^\circ C$ unless specified

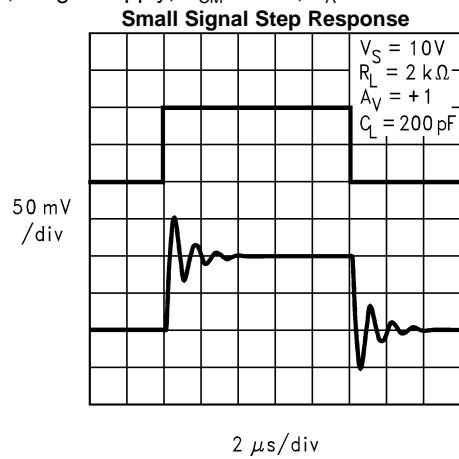


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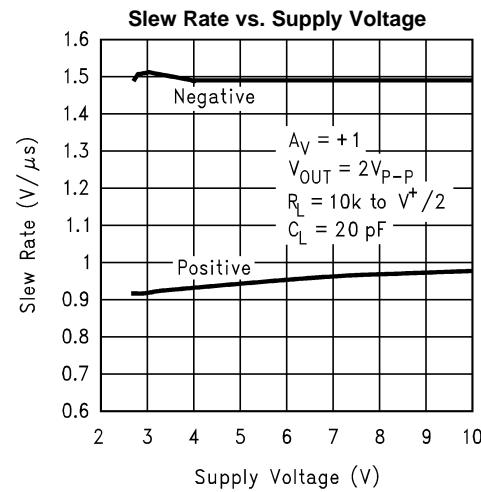


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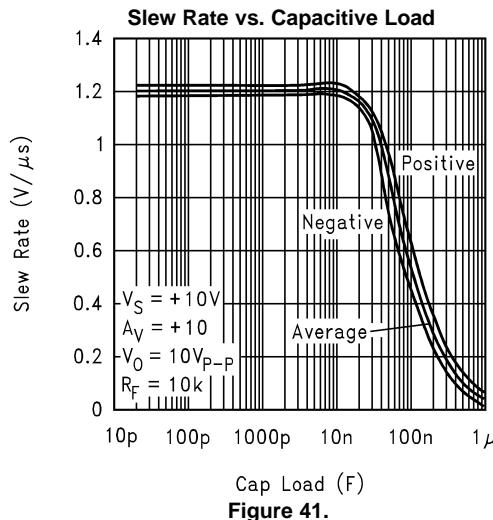


Figure 41.

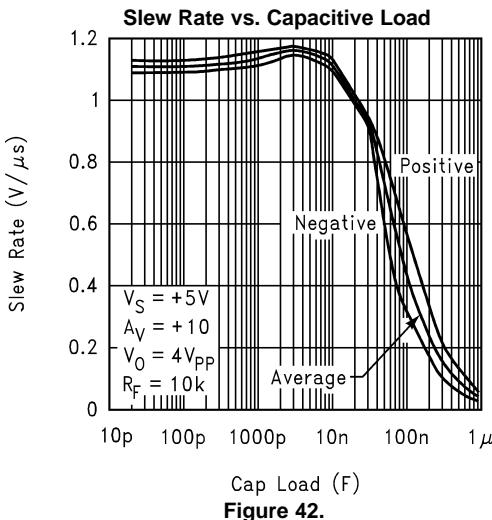


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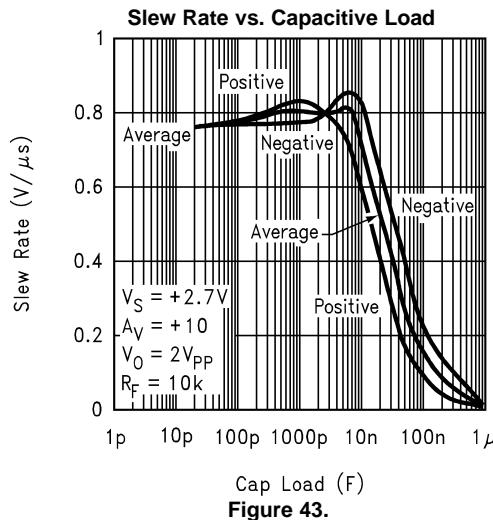


Figure 43.

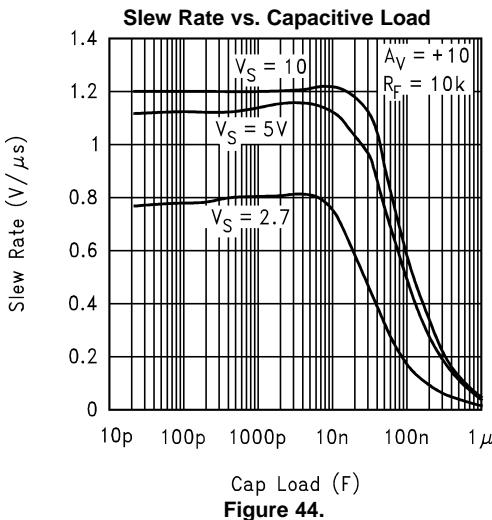


Figure 44.

Typical Performance Characteristics (continued)

$V_S = 2.7V$, Single Supply, $V_{CM} = V^+/2$, $T_A = 25^\circ C$ unless specified

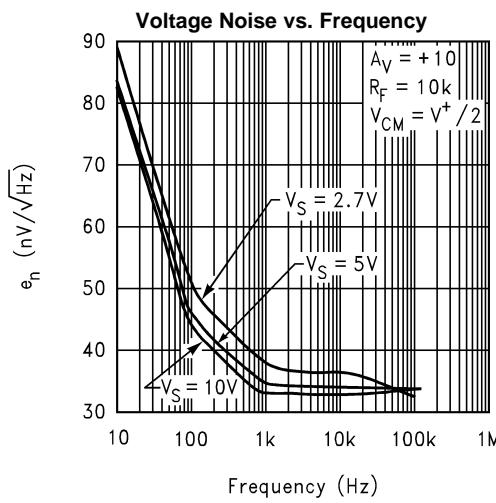


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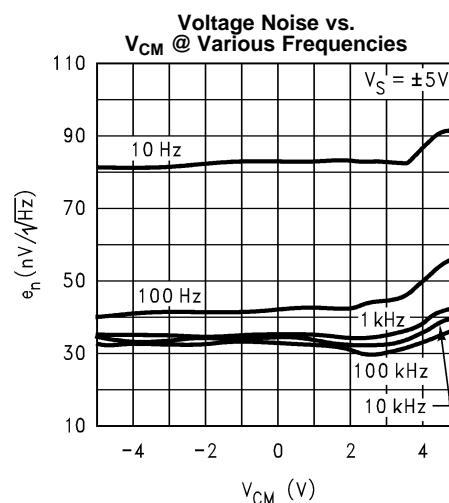


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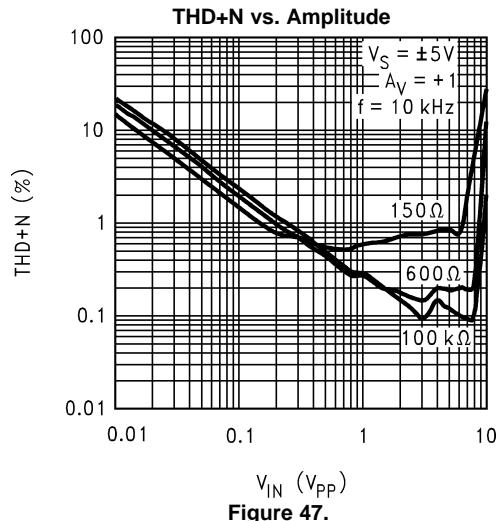


Figure 47.

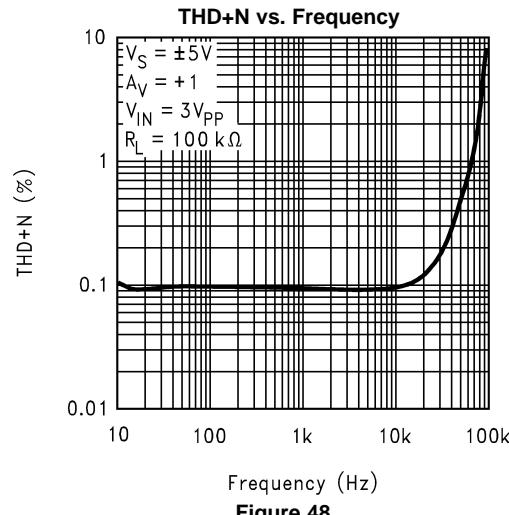


Figure 48.

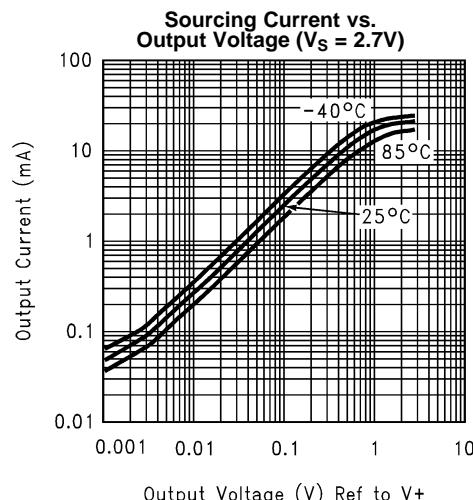


Figure 49.

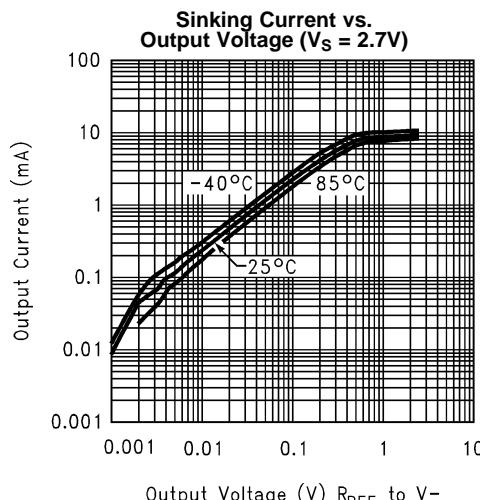
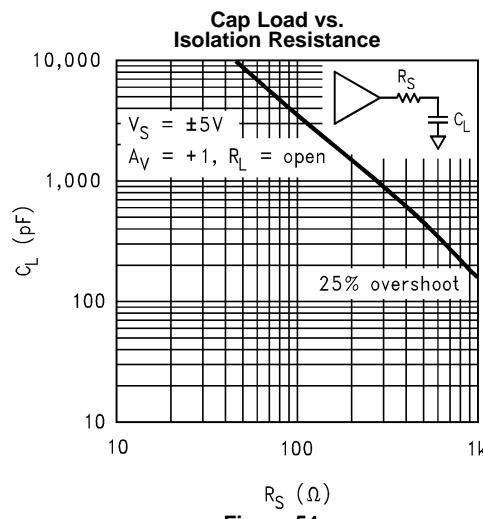
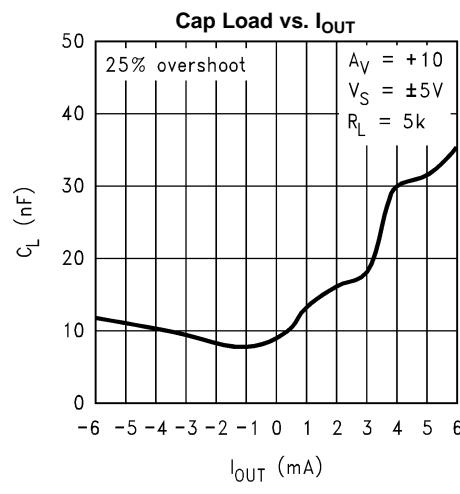
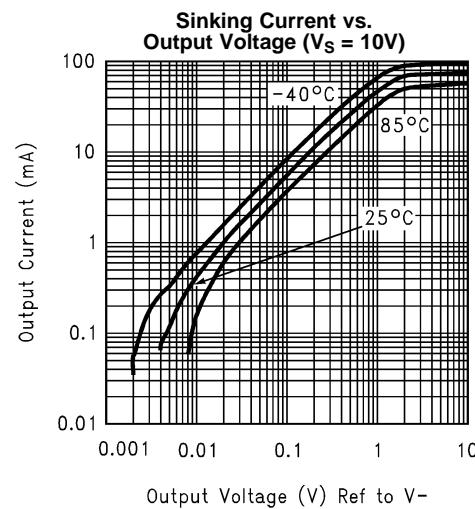
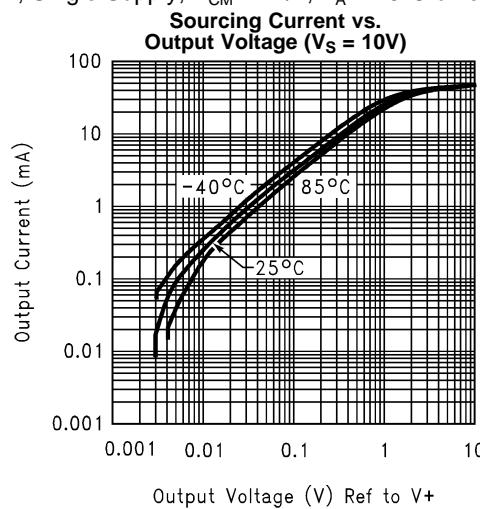


Figure 50.

Typical Performance Characteristics (continued)

$V_S = 2.7V$, Single Supply, $V_{CM} = V^+/2$, $T_A = 25^\circ C$ unless specified



APPLICATION NOTES

SHUTDOWN FEATURES

The LMC8101 is capable of being turned off in order to conserve power. Once in shutdown, the device supply current is drastically reduced (1 μ A maximum) and the output will be "Tri-stated".

The shutdown feature of the LMC8101 is designed for flexibility. The threshold level of the SD input can be referenced to either V^- or V^+ by setting the level on the SL input. When the SL input is connected to V^- , the SD threshold level is referenced to V^- and vice versa. This threshold will be about 1.5V from the supply tied to the SL pin. So, for this example, the device will be in shutdown as long as the SD pin voltage is within 1V of V^- . In order to ensure that the device would not "chatter" between active and shutdown states, hysteresis is built into the SD pin transition (see [Figure 55](#) for an illustration of this feature). The shutdown threshold and hysteresis level are independent of the supply voltage. [Figure 55](#) illustration applies equally well to the case when SL is tied to V^+ and the horizontal axis is referenced to V^+ instead. The SD pin should not be set within the voltage range from 1.1V to 1.9V of the selected supply voltage since this is a transition region and the device status will be undetermined.

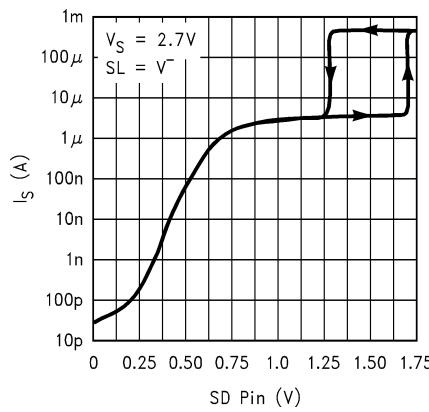


Figure 55. Supply Current vs. "SD" Voltage

[Table 1](#) summarizes the status of the device when the SL and SD pins are connected directly to V^- or V^+ :

Table 1. LMC8101 Status Summary

SL	SD	LMC8101 Status
V^-	V^-	Shutdown
V^-	V^+	Active
V^+	V^+	Shutdown
V^+	V^-	Active

In case shutdown operation is not needed, as can be seen above, the two pins SL and SD can simply be connected to opposite supply nodes to achieve "Active" operation. The SL and SD should always be tied to a node; if left unconnected, these high impedance inputs will float to an undetermined state and the device status will be undetermined as well.

With the device in shutdown, once "Active" operation is initiated, there will be a finite amount of time required before the device output is settled to its final value. This time is less than 15 μ s. In addition, there may be some output spike during this time while the device is transitioning into a fully operational state. Some applications may be sensitive to this output spike and proper precautions should be taken in order to ensure proper operation at all times.

TINY PACKAGE

The LMC8101 is available in the DSBGA package as well the 8 pin VSSOP package. The DSBGA package requires approximately 1/4 the board area of a SOT-23. This package is less than 1mm in height allowing it to be placed in absolute minimum height clearance areas such as cellular handsets, LCD panels, PCMCIA cards, etc. More information about the DSBGA package can be found at: <http://www.ti.com/packaing>.

CONVERSION BOARDS

In order to ease the evaluation of tiny packages such as the DSBGA, there is a conversion board (LMC8101CONV) available to board designers. This board converts a DSBGA device into an 8 pin DIP package (see [Figure 56](#)) for easier handling and evaluation. This board can be ordered from Texas Instruments by contacting <http://www.ti.com>.

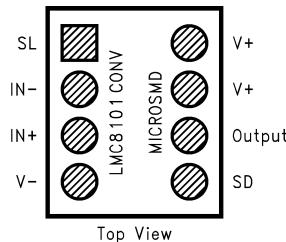


Figure 56. DSBGA Conversion Board pin-out

INCREASED OUTPUT CURRENT

Compared to the LMC7101, the LMC8101 has an improved output stage capable of up to three times larger output sourcing and sinking current. This improvement would allow a larger output voltage swing range compared to the LMC7101 when connected to relatively heavy loads. For lower supply voltages this is an added benefit since it increases the output swing range. For example, the LMC8101 can typically swing 2.5Vpp with 2mA sourcing and sinking output current ($V_s = 2.7V$) whereas the LMC7101 output swing would be limited to 1.9Vpp under the same conditions. Also, compared to the LMC7101 in the SOT-23 package, the LMC8101 can dissipate more power because both the VSSOP and the DSBGA packages have 40% better heat dissipation capability.

LOWER 1/f NOISE

The dominant input referred noise term for the LMC8101 is the input noise voltage. Input noise current for this device is of no practical significance unless the equivalent resistance it looks into is $5M\Omega$ or higher.

The LMC8101's low frequency noise is significantly lower than that of the LMC7101. For example, at 10Hz, the input referred spot noise voltage density is $85\text{ nV}\sqrt{\text{Hz}}$ as compared to about $200\text{nV}\sqrt{\text{Hz}}$ for the LMC7101. Over a frequency range of 0.1Hz to 100Hz, the total noise of the LMC8101 will be approximately 60% less than that of the LMC7101.

LOWER THD

When connected to heavier loads, the LMC8101 has lower THD compared to the LMC7101. For example, with 5V supply at 10KHz and 2Vpp swing ($A_v = -2$), the LMC8101 THD (0.2%) is 60% less than the LMC7101's. The LMC8101 THD can be kept below 0.1% with 3Vpp at the output for up to 10KHz (refer to the [Typical Performance Characteristics](#) plots).

IMPROVING THE CAP LOAD DRIVE CAPABILITY

This can be accomplished in several ways:

- Output resistive loading increase:

The Phase Margin increases with increasing load (refer to the [Typical Performance Characteristics](#) plots). When driving capacitive loads, stability can generally be improved by allowing some output current to flow through a load. For example, the cap load drive capability can be increased from 8200pF to 16000pF if the output load is increased from $5k\Omega$ to 600Ω ($A_v = +10$, 25% overshoot limit, 10V supply).

- Isolation resistor between output and cap load:

This resistor will isolate the feedback path (where excessive phase shift due to output capacitance can cause instability) from the capacitive load. With a 10V supply, a 100Ω isolation resistor allows unlimited capacitive load without oscillation compared to only 300pF without this resistor ($A_V = +1$).

- Higher supply voltage:

Operating the LMC8101 at higher supply voltages allows higher cap load tolerance. At 10V, the LMC8101's low supply voltage cap load limit of 300pF improves to about 600pF ($A_V = +1$).

- Closed loop gain increase:

As with all Op Amps, the capacitive load tolerance of the LMC8101 increases with increasing closed loop gain. In applications where the load is mostly capacitive and the resistive loading is light, stability increases when the LMC8101 is operated at a closed loop gain larger than +1.

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC8101MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A11	
LMC8101MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A11	Samples
LMC8101MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A11	Samples
LMC8101TP/NOPB	ACTIVE	DSBGA	YPB	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A08	Samples
LMC8101TPX/NOPB	ACTIVE	DSBGA	YPB	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A08	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



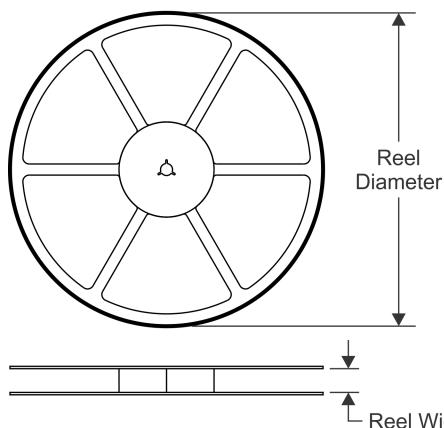
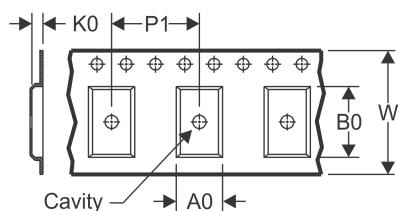
www.ti.com

PACKAGE OPTION ADDENDUM

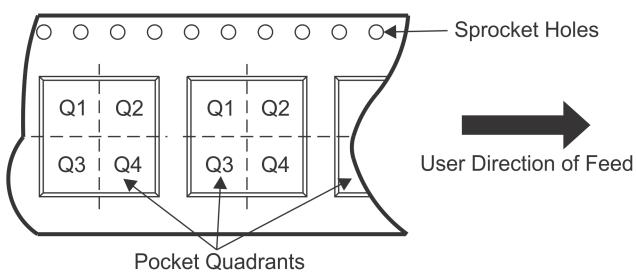
1-Nov-2013

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC8101MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC8101MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC8101MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC8101TP/NOPB	DSBGA	YPB	8	250	178.0	8.4	1.57	1.57	0.76	4.0	8.0	Q1
LMC8101TPX/NOPB	DSBGA	YPB	8	3000	178.0	8.4	1.57	1.57	0.76	4.0	8.0	Q1

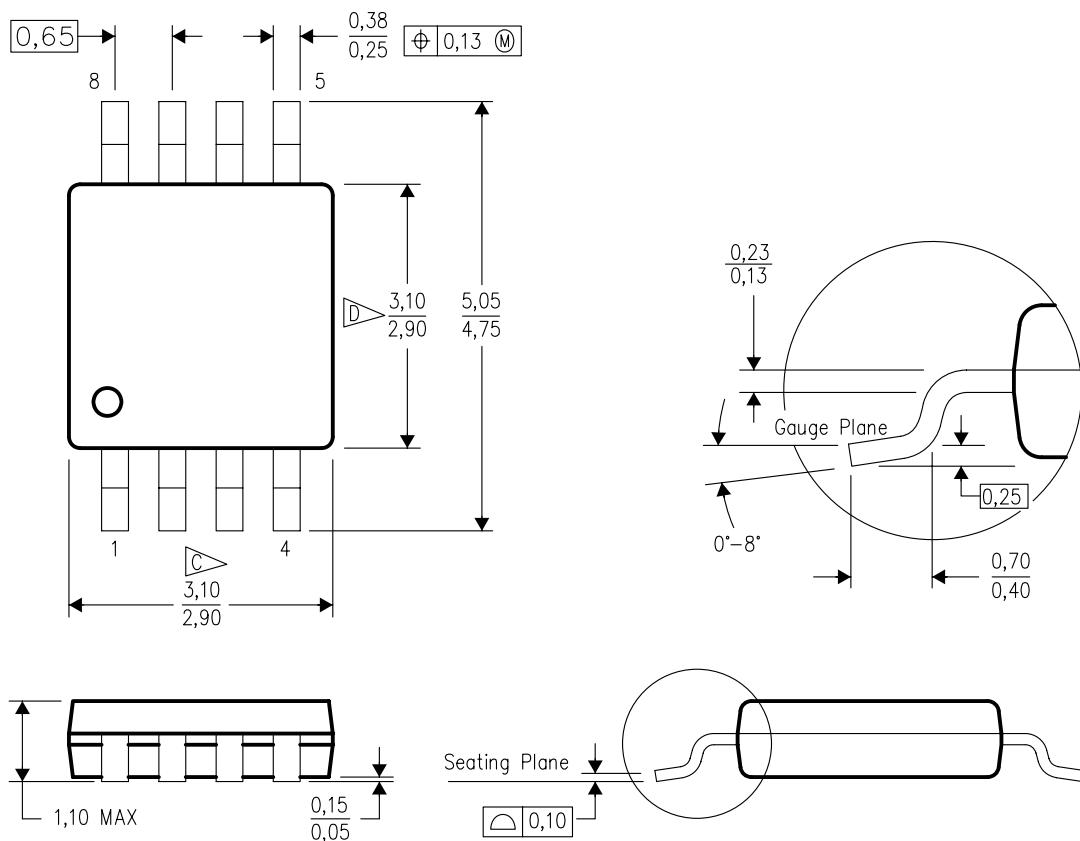
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC8101MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC8101MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC8101MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC8101TP/NOPB	DSBGA	YPB	8	250	210.0	185.0	35.0
LMC8101TPX/NOPB	DSBGA	YPB	8	3000	210.0	185.0	35.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

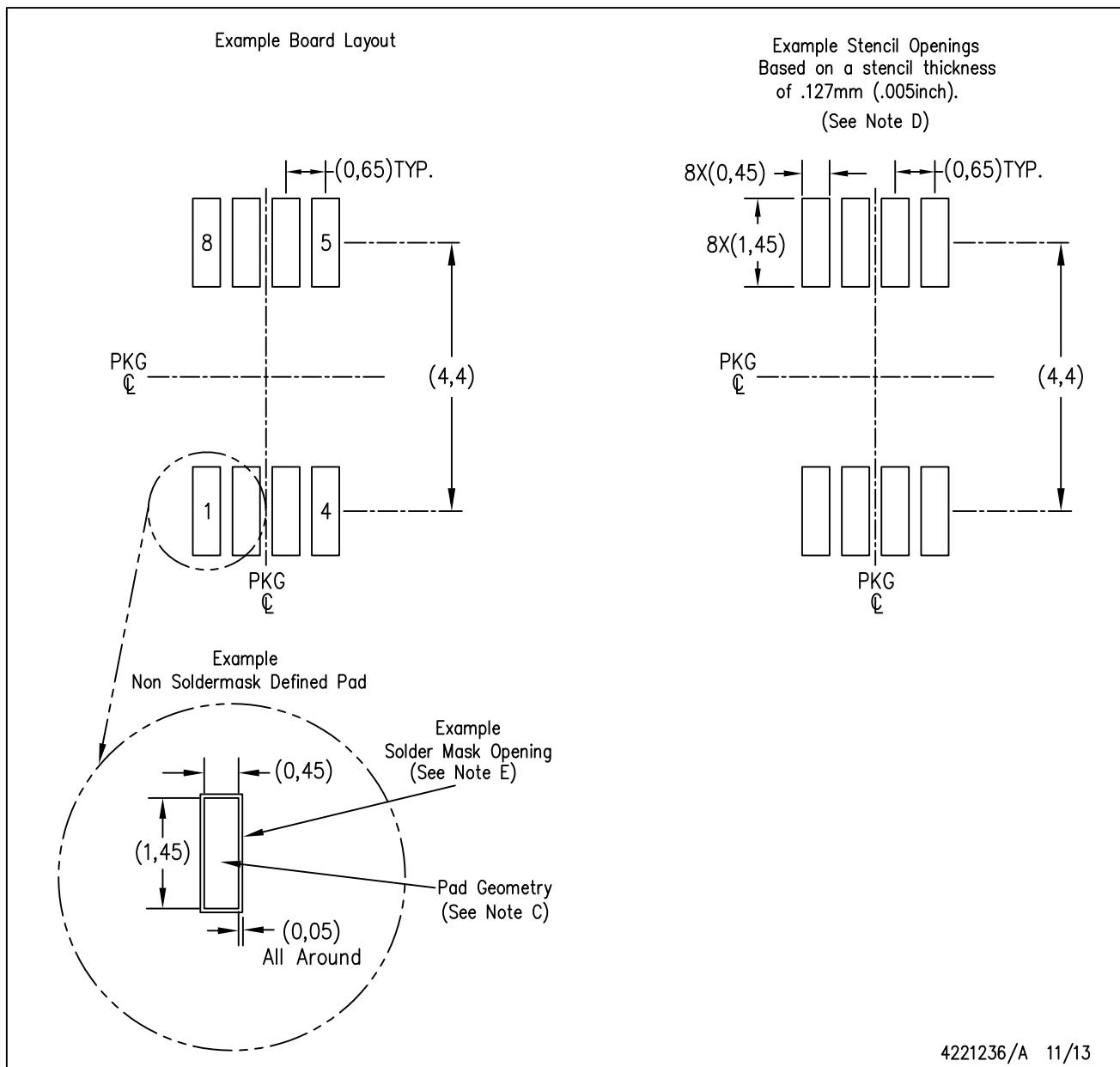
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

E. Falls within JEDEC MO-187 variation AA, except interlead flash.

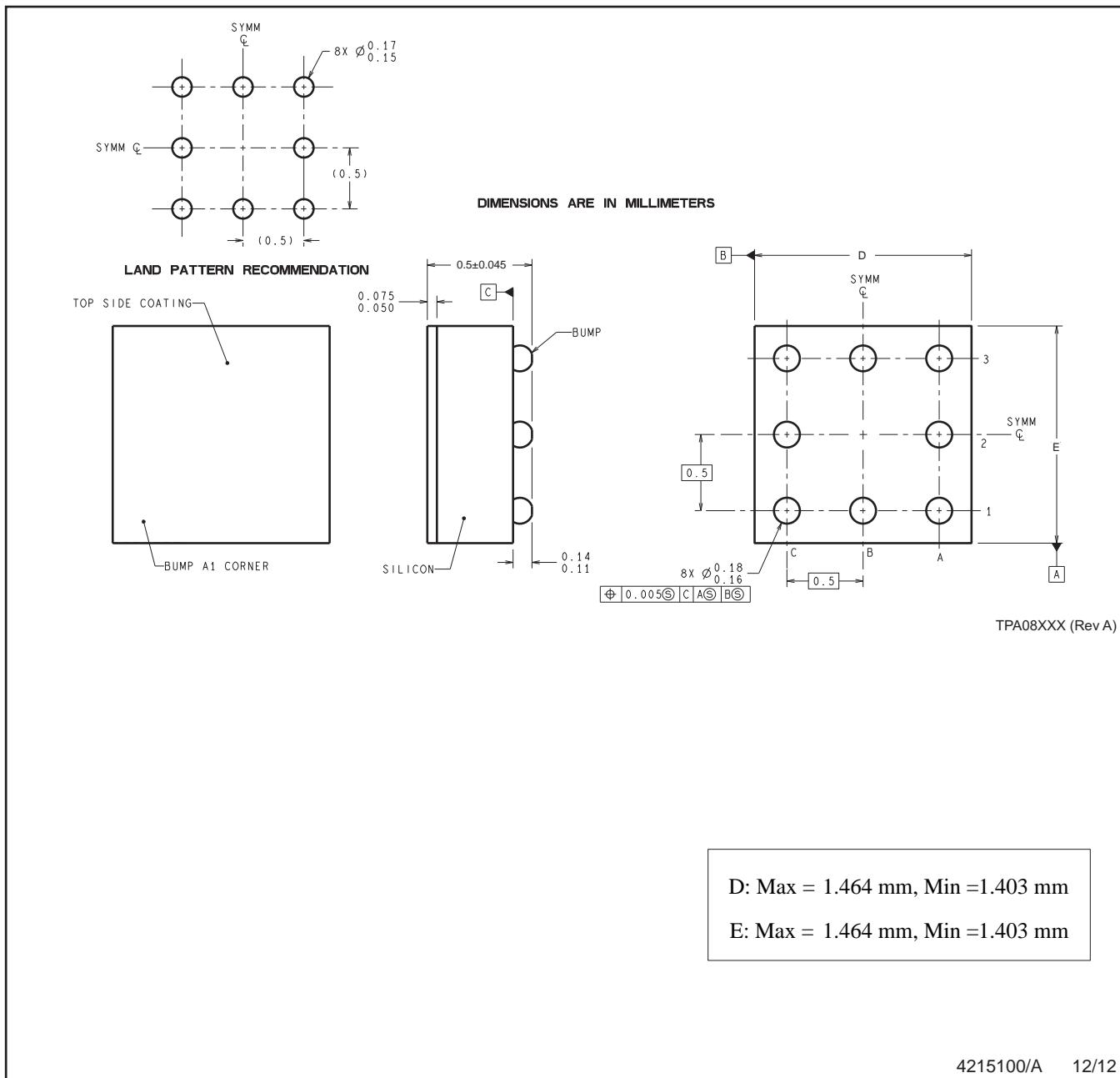
DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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