National Semiconductor

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LMH1983

3G/HD/SD Video Clock Generator with Audio Clock

General Description

The LMH1983 is a highly-integrated programmable audio/video (A/V) clock generator intended for broadcast and professional applications. It can replace multiple PLLs and VCXOs used in applications supporting SMPTE serial digital video (SDI) and digital audio AES3/EBU standards. It offers low-jitter reference clocks for any SDI transmitter to meet stringent output jitter specifications without additional clock cleaning circuits.

The LMH1983 features automatic input format detection, simple programming of multiple A/V output formats, genlock or digital free run modes, and override programmability of various automatic functions. The recognized input formats include HVF syncs for the major video standards, 27 MHz, 10 MHz, and 32/44.1/48/96 kHz audio word clocks.

The dual-stage PLL architecture integrates four PLLs with three on-chip VCOs. The first stage (PLL1) uses an external low-noise 27 MHz VCXO with narrow loop bandwidth to provide a clean reference clock for the next stage. The second stage (PLL2, 3, 4) consists of three parallel VCO PLLs for simultaneous generation of the major digital A/V clock fundamental rates, including 148.5 MHz, 148.5/1.001 MHz, and 98.304 MHz (4x 24.576 MHz). Each PLL can generate a clock and a timing pulse to indicate Top Of Frame (TOF).

When locked to reference, an internal 10-bit ADC will track the loop filter control voltage. When a loss of reference (LOR) occurs, the LMH1983 can be programmed to hold the control voltage to maintain output accuracy within ±0.5 ppm (typ.) of the previous reference. The LMH1983 can be configured to re-synchronize to a previous reference with glitch-less operation.

The LMH1983 is offered in a space-saving 6 mm x 6 mm 40-pin LLP package.

Features

- Four PLLs for simultaneous A/V clock generation
  - PLL1: 27 or 13.5 MHz
  - PLL2: 148.5 or 74.25 MHz
  - PLL3: 148.5/1.001 or 74.25/1.001 MHz
  - PLL4: 98.304 MHz / 2^X (X = 0 to 15)
- 3 x 2 Video clock crosspoint
- Flexible PLL bandwidth to optimize jitter performance and lock time
- Soft re-synchronization to new reference
- Digital holdover or free run on loss of reference
- Status flags for loss of reference, and loss of PLL lock
- 3.3V single supply operation
- I^2C interface with address select pin (3 states)

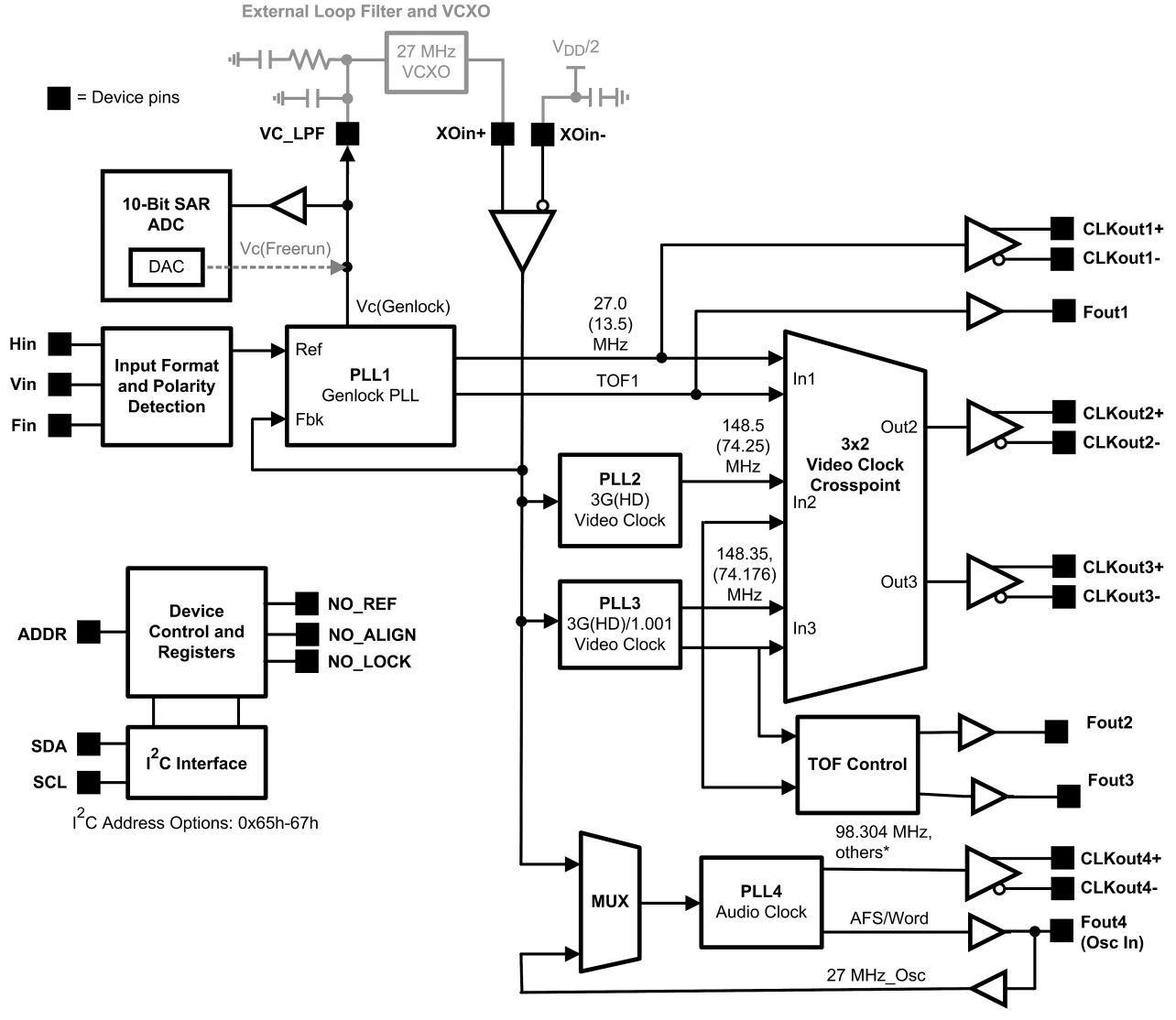
Applications

- Triple rate (3G/HD/SD) SDI SerDes
- FPGA reference clock generation/cleaning
- Audio embed/de-embed
- Video cameras
- Frame synchronizers (Genlock, DARS)
- A-D/D-A conversion, editing, processing cards
- Keyers and logo inserters
- Format/standards converters
- Video displays and projectors
- A/V test and measurement equipment

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
40-Pin LLP	LMH1983SQ		1k Units Tape and Reel	SQA40A
	LMH1983SQE		250 Units Tape and Reel	
	LMH1983SQX		2.5k Units Tape and Reel	

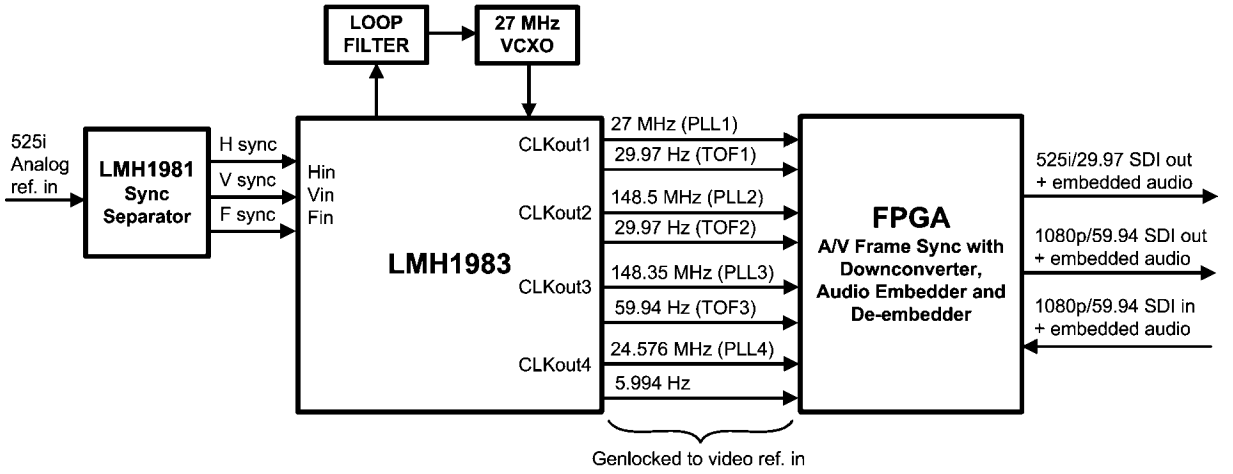
Functional Block Diagram



* Audio Clock PLL supports $98.304/2^{X}$ MHz, where X=0-15

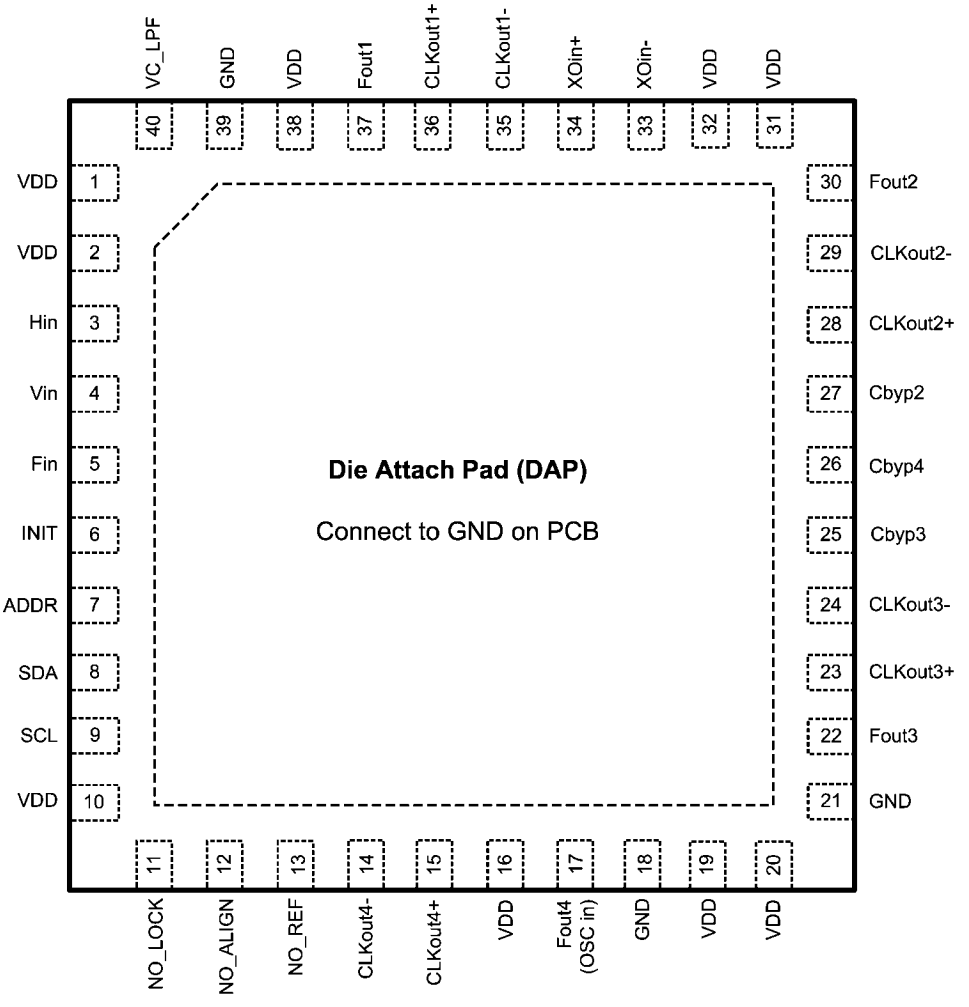
30085103

Typical Application Diagram



Video Genlock Timing Generation for A/V Frame Synchronizer

Connection Diagram



Top View
40-Pin LLP (SQA40A)

Pin Descriptions

Pin No.	Pin Name	I/O	Signal Level	Pin Description
–	DAP	–	GND	Die Attach Pad (Connect to ground on PCB)
1	VDD	–	Power	3.3V supply for PLL1
2	VDD	–	Power	3.3V supply for logic I/O
3	Hin	I	LVCMOS	Horizontal sync reference signal Auto polarity correction for HVF will be based off Hin polarity. Recognized clock inputs can be applied to Hin.
4	Vin	I	LVCMOS	Vertical sync reference signal
5	Fin	I	LVCMOS	Field sync (odd/even) reference signal
6	INIT	I	LVCMOS	Reset signal for audio-video phase alignment (rising edge triggered)
7	ADDR	I	LVCMOS	I²C address select Pin settings: – Tie low: 65h (7-bit slave address in hex) – Float: 66h – Tie high: 67h
8	SDA	I/O	I²C	I²C Data signal
9	SCL	I	I²C	I²C Clock signal
10	VDD	–	Power	3.3V supply for logic I/O
11	NO_LOCK	O	LVCMOS	Loss of lock status flag for PLLs 1-4 (active high)
12	NO_ALIGN	O	LVCMOST	Loss of alignment status flag for OUTs 1–4 (active high)
13	NO_REF	O	LVCMOS	Loss of reference status flag (active high)
14 15	CLKout4– CLKout4+	O	LVDS	Audio clock from PLL4 (fundamental rate is 98.304 MHz). The output is 24.576 MHz by default and is selectable via the host.
16	VDD	–	Power	3.3V supply for CLKout4
17	Fout4 (OSCin)	I/O	LVCMOS	Audio frame timing signal for OUT4 (active low.) Timing Generator fixed to PLL4 clock. The output is the audio-video-frame (AVF) pulse by default and is programmable via the host. **Optional** OSCin function can be used to apply a clean 27MHz external clock for PLL4 to generate an audio clock independent of the video input reference; this function must be enabled via the host.
18	GND	–	GND	Ground
19	VDD	–	Power	3.3V supply for PLL3 and PLL4
20	VDD	–	Power	3.3V supply for CLKout3
21	GND	–	GND	Ground
22	Fout3	O	LVCMOS	Video frame timing signal for OUT3 (active low). Timing generator assignable to PLL1, PLL2, or PLL3. OUT3 format is selectable via the host.
23 24	CLKout3+ CLKout3–	O	LVDS	Video clock from PLL1, PLL2, or PLL3 depending on output crosspoint mode. The output is 148.35 MHz by default and is selectable via the host.
25	Cbyp3	–	Analog	Bias bypass for on-chip LDO for PLL3 Connect to 1.0uF and 0.1uF bypass capacitors.
26	Cbyp4	–	Analog	Bias bypass for on-chip LDO for PLL4 Connect to 1.0uF and 0.1uF bypass capacitors.
27	Cbyp2	–	Analog	Bias bypass for on-chip LDO for PLL2 Connect to 1.0uF and 0.1uF bypass capacitors.

Pin No.	Pin Name	I/O	Signal Level	Pin Description
28 29	CLKout2+ CLKout2–	O	LVDS	Video clock from PLL1, PLL2, or PLL3 depending on output crosspoint mode. The output is 148.35 MHz by default and is selectable via the host.
30	Fout2	O	LVCMOS	Video clock from PLL1, PLL2, or PLL3 depending on output crosspoint mode. The output is 148.5 MHz by default and is selectable via the host.t
31	VDD	–	Power	3.3V supply for CLKout2
32	VDD	–	Power	3.3V supply for PLL2
33 34	XOin- XOin+	I	LVCMOS/LVDS	27 MHz VCXO clock signal for PLL1. – LVCMOS: Directly connect clock signal to XOin+ and bias XOin- to mid-supply with 0.1uF bypass capacitor. – LVDS: Directly connect LVDS clock signals to XOin+ and XOin-. **Note:**A TCXO or other clean 27 MHz oscillator can be applied for standalone clock generation using PLLs 2-4 (bypass PLL1).
35 36	CLKout1– CLKout1+	O	LVDS	Video clock from PLL1. The output is 27 MHz by default and is selectable via the host.
37	Fout1	O	LVCMOS	Reference frame timing signal for OUT1 (active Low) Timing generator fixed to PLL1 OUT1 Format follows the reference input format.
38	VDD	–	Power	3.3V supply for CLKout1
39	GND	–	GND	Ground
40	VC_LPF	O	Analog	Loop filter for PLL1 charge pump output with VCXO Voltage Control (VC) sensing. If freerun and holdover mode, PLL1 is disabled and an internal DAC outputs a control voltage to the VCXO.

Notes

1. The NO_LOCK status flag is derived from the Lock Status register bits (LOCK1-4) for each PLL. Each lock status bit can be masked from the NO_LOCK flag by setting their respective mask bits.
2. SDA and SCL pins each require a pull-up resistor of 4.7 kΩ to the VDD supply.
3. XOin must be driven by a 27 MHz clock in order to read or write registers via I^2C

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (*Note 2*)	
Human Body Model	2500V
Machine Model	250V
Charge-Device Model	750V
Supply Voltage, V_{DD}	3.6V
Input Voltage (any input)	−0.3V to V_{DD} +0.3V
Output Voltage (any output)	−0.3V to V_{DD} +0.3V
Storage Temperature Range	−65°C to +150°C
Junction Temperature, T_{JMAX}	150°C
Thermal Resistance (θ_{JA})	33°C/W
Soldering Information	
See product folder at www.national.com/mpf/LM/LMH1983.htm and further information at www.national.com/ms/MS-SOLDERING.pdf	

Operating Ratings

V_{DD}	3.3V ± 5%
Input Voltage	0V to V_{DD}
Temperature Range, T_A	-40°C to 85°C

Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_{DD} = 3.3V, R_{L_CLK} = 100Ω (CLKout differential load). **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (*Note 6*)	Typ (*Note 5*)	Max (*Note 6*)	Units
I_{DD}	Total Supply Current	Default register settings, no load on logic outputs.V_{DD} = 3.465V		170	212	mA
I_{DD}	Total Supply Current	PLL2, PLL3 and PLL4 disabled, no load on logic outputs.V_{DD} = 3.465V		60	100	mA
Reference Inputs (Hin, Vin, Fin)						
V_{IL}	Low Input Voltage	I_{IN} = ±10 µA	0		0.3 V_{DD}	V
V_{IH}	High Input Voltage	I_{IN} = ±10 µA	0.7 V_{DD}		V_{DD}	V
T_{AFD}	Auto-Format Detection Time	Time from when reference input first presented to when detected as indicated by NO_REF going low. Reference timing must be stable and accurate (no missing pulses).		2	4	input frames
OSCin Logic Inputs						
V_{IL}	Low Input Voltage	I_{IN} = ±10 µA	0		0.3 V_{DD}	V
V_{IH}	High Input Voltage	I_{IN} = ±10 µA	0.7 V_{DD}		V_{DD}	V
I²C Interface (SDA, SCL)						
V_{IL}	Low Input Voltage		0		0.3 V_{DD}	V
V_{IH}	High Input Voltage		0.7 V_{DD}		V_{DD}	V
I_{IN}	Input Current	V_{IN} between 0.1 V_{DD} and 0.9 V_{DD}	−10		+10	µA
I_{OL}	Low Output Sink Current	V_{OL} = 0V or 0.4V		3		mA
Status Flag Outputs (NO_REF, NO_ALIGN,NO_LOCK)						
V_{OL}	Low Output Voltage	I_{OUT} = +10 mA			0.4	V
V_{OH}	High Output Voltage	I_{OUT} = −10 mA	V_{DD} −0.4V			V
Frame Timing Outputs						
V_{OL}	Low Output Voltage	I_{OUT}=+10mA , Fout1, Fout2, Fout3			0.4	V
V_{OH}	High Output Voltage	I_{OUT}=-10mA Fout1, Fout2, Fout3	V_{DD}-0.4V			V
I_{OZ}	Output Shutdown Leakage Current	Output buffer shutdown, pin connected to V_{DD}or GND V_{DD}=3.465V		0.4	10	|µA|
t_R	Rise Time 20% to 80%	15 pF Load		1		ns
t_F	Fall Time 20% to 80%	15 pF load		1		ns

Symbol	Parameter	Conditions	Min (*Note 6*)	Typ (*Note 5*)	Max (*Note 6*)	Units
t_{D1}(*Note 8*)	Timing output delay time	TOF1 delay measured from the CLKout1 clock reset edge. Delay spec applies for all output clock and format supported by the output pair following output initialization. 15 pF load.		22		ns
t_{D2}	Timing output delay time	TOF2 delay measured from the CLKout2 clock reset edge. Delay spec applies for all output clock and format supported by the output pair following output initialization. 15 pF load.		2		ns
t_{D3}	Timing output delay time	TOF3 delay measured from the CLKout3 clock reset edge. Delay spec applies for all output clock and format supported by the output pair following output initialization. 15 pF load.		2		ns
t_{D4}	Timing output delay time	TOF4 delay measured from the CLKout4 clock reset edge. Delay spec applies for all output clock and format supported by the output pair following output initialization. 15 pF load.		22		ns

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Video and Audio Clock Outputs (CLKout1, CLKout2 and CLKout3)						
t_{DJ}	27 MHz TIE deterministic Jitter	Measured at CLKout1 all other CLKouts shutdown		250		fs
		Measured at CLKout1, other CLKouts output default PLL		250		fs
	148.5 MHz TIE deterministic Jitter	Measured at CLKout2 all other CLKouts shutdown		8		ps
		Measured at CLKout2, other CLKouts output default PLL		8		ps
	148.35 MHz TIE deterministic Jitter	Measured at CLKout3 all other CLKouts shutdown		4		ps
		Measured at CLKout3, other CLKouts output default PLL		4		ps
	24.576 MHz TIE deterministic Jitter	Measured at CLKout4 all other CLKouts shutdown		15		ps
		Measured at CLKout4, other CLKouts output default PLL		15		ps
t_{RJ}	27 MHz TIE random Output Jitter (Note 7)	Measured at CLKout1, other CLKouts shutdown		2.7		ps
		Measured at CLKout1, other CLKouts output default PLL		2.7		ps
	148.5 MHz TIE Random Output Jitter (Note 7)	Measured at CLKout2, other CLKouts shutdown		3.0		ps
		Measured at CLKout2, other CLKouts output default PLL		3.0		ps
	148.35 MHz TIE Random Output Jitter (Note 7)	Measured at CLKout3, other CLKouts shutdown		3.5		ps
		Measured at CLKout3, other CLKouts output default PLL		3.5		ps
	24.576 MHz TIE Random Output Jitter (Note 7)	Measured at CLKout4, other CLKouts shutdown		3.4		ps
		Measured at CLKout4, other CLKouts output default PLL		3.4		ps
T_D	Duty Cycle	Measured at 50% level of clock amplitude, any output clock		50		%
t_R	Rise Time 20% to 80%	15 pF load		400		ps
t_F	Fall Time 80% to 20%	15 pF load		400		ps
V_{OD}	Differential Signal Output Voltage	100Ω differential load, CLKout1, CLKout2 or CLKout3(Note 10)	247	350	454	mV
V_{OS}	Common Signal Output Voltage	100Ω differential load, CLKout1, CLKout2 or CLKout3(Note 10)	1.125	1.25	1.375	V
$\lvert V_{OD} \rvert$	|Change to V_{OD}| for Complementary Output States	100Ω differential load, CLKout1, CLKout2 or CLKout3(Note 10)			50	|mV|
$\lvert V_{OS} \rvert$	|Change to V_{OS}| for Complementary Output States	100Ω differential load, CLKout1, CLKout2 or CLKout3(Note 10)			50	|mV|
I_{OS}	Output Short Circuit Current	Differential clock output pins connected to GND for CLKout1, CLKout2 or CLKout3			24	|mA|
I_{OZ}	Output Shutdown Leakage Current	Output buffer in shutdown mode, differential clock output pins connected to V_{DD} or GND		1	10	|µA|

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
VCXO Input (XOin)						
f_{OFF}	Maximum Relative Frequency Offset between VCXO Input and H Input	Assumes H input jitter of ±15 ns		±150		ppm
V_{XOin_SE}	Single-ended Signal Input Voltage Range	Single-ended input buffer mode	0		V_{DD}	V
V_{XOin_DIFF}	Differential Signal Input Voltage Range	Differential input buffer mode, V_{CM} = 1.2V	247	350	454	mV
Digital Holdover and Free Run Specifications						
V_{VCout_RNG}	DAC Output Voltage Range	Digital Free Run Mode	0.5		V_{DD}-0.5 V	V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)

Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is PD = ($T_{J(MAX)}$ – T_A)/ θ_{JA}. All numbers apply for packages soldered directly onto a PC Board.

Note 4: Electrical Table values apply only for factory testing conditions at the temperature indicated. No guarantee of parametric performance is indicated in the electrical tables under conditions different than those tested.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using statistical analysis methods.

Note 7: The SD and HD clock output jitter is based on XO input clock with 20 ps peak-to-peak using a time interval error (TIE) jitter measurement. The typical TIE peak-to-peak jitter was measured on the LMH1983 evaluation bench board using TDSJIT3 jitter analysis software on a Tektronix DSA71604 oscilloscope and 1 GHz active differential probe.

TDSJIT3 Clock TIE Measurement Setup: 10^{-12} bit error rate (BER), >100K samples recorded using multiple acquisitions

Oscilloscope Setup: 20 mV/div vertical scale, 10 µs/div horizontal scale, and 25 GS/s sampling rate

Note 8: t_D for CLKoutX is measured from the positive clock edge of XOin to the positive clock edge of CLKoutX using 50% levels. The measurement is taken at the clock cycle where the input and output clocks are phase aligned.

Note 9: t_D for FoutX is measured from the positive clock edge of CLKout to the negative edge of FoutX at the 50% levels

Note 10: The differential output swing and common mode voltage may be adjusted via the I²C interface. Testing is done with a value of 03Eh loaded into register 0x3Ah

Supported Standards and Timing Formats

Table 1 lists the supported standard timing formats. The table includes the relevant parameters used to configure the LMH1983 for the input and output formats. Auto-detection of the input is supported for the formats listed in *Table 1*. The input format can also be manually programmed by the host via I²C if it's necessary to override the auto-detection feature.

TABLE 1. Supported Formats Lookup Table (LUT)

Format	INPUT TIMING / PLL1 PARAMETERS				OUTPUT TIMING (OUT1–4) PARAMETERS				
	Reference Divider	Feedback Divider	Phase Detector (PD) Frequency (kHz)	PD Periods per Frame Counter	PLL#	PLL Clock Frequency (MHz)	Total Clocks per Line Counter	Total Lines per Frame Counter	Frame Rate (Hz)
NTSC, 525i	1	1716	15.7343	525	1	27.0	1716	525	29.97
					2	148.5	9438		
PAL, 625i	1	1728	15.625	625	1	27.0	1728	625	25
					2	148.5	9504		
525p	1	858	31.4685	525	1	27.0	858	525	59.94
					2	148.5	4719		
625p	1	864	31.25	625	1	27.0	864	625	50
					2	148.5	4752		
720p/60	1	600	45.0	750	2	148.5	3300	750	60
720p/59.94	5	3003	8.99101	150	3	148.35	3300	750	59.94
720p/50	1	720	37.5	750	2	148.5	3960	750	50
720p/30	1	1200	22.5	750	2	148.5	6600	750	30
720p/29.97	5	6006	4.49550	150	3	148.35	6600	750	29.97
720p/25	1	1440	18.75	750	2	148.5	7920	750	25
720p/24	1	1500	18.0	750	2	148.5	8250	750	24
720p/23.98	2	3003	8.99101	375	3	148.35	8250	750	23.98
1080p/60	1	400	67.5	1125	2	148.5	2200	1125	60
1080p/59.94	5	2002	13.48651	225	3	148.35	2200	1125	59.94
1080p/50	1	480	56.25	1125	2	148.5	2640	1125	50
1080p(psF)/30	1	800	33.75	1125	2	148.5	4400	1125	30
1080p(psF)/29.97	5	4004	6.74326	225	3	148.35	4400	1125	29.97
1080p(psF)/25	1	960	28.125	1125	2	148.5	5280	1125	25
1080p(psF)/24	1	1000	27.0	1125	2	148.5	5500	1125	24
1080p(psF)/23.98	1	1001	26.9730	1125	3	148.35	5500	1125	23.98
1080i/60	1	800	33.75	1125	2	148.5	4400	1125	30
1080i/59.94	5	4004	6.74326	225	3	148.35	4400	1125	29.97
1080i/50	1	960	28.125	1125	2	148.5	5280	1125	25
48 kHz word clock	2	1125	24.0	1	4	98.304	2048	1	48000
96 kHz word clock	4	1125	24.0	1	4	98.304	1024	1	96000

Format	INPUT TIMING / PLL1 PARAMETERS				OUTPUT TIMING (OUT1–4) PARAMETERS				
	Reference Divider	Feedback Divider	Phase Detector (PD) Frequency (kHz)	PD Periods per Frame Counter	PLL#	PLL Clock Frequency (MHz)	Total Clocks per Line Counter	Total Lines per Frame Counter	Frame Rate (Hz)
27 MHz oscillator clock	1000	1000	27.000	1	Input only				
10 MHz GPS oscillator clock	600	1620	16.6666	1	Input only				

Auto Format Detection Codes

Format Code	Description	hsync period (in 27MHz clocks)	Interlaced/Progressive
0	480i/29.97	1716	I
1	576I25	1728	I
2	480P59.94	858	P
3	576P50	864	P
4	720P60	600	P
5	720P59.94	600.6	P
6	720P50	720	P
7	720P30	1200	P
8	720P27.97	1201.2	P
9	720P25	1440	P
10	720P24	1500	P
11	720P23.98	1501.5	P
12	1080P60	400	P
13	1080P59.94	400.4	P
14	1080P50	480	P
15	1080P30	800	P
16	1080P29.97	800.8	P
17	1080P25	960	P
18	1080P24	1000	P
19	1080P23.98	1001	P
20	1080I30	800	I
21	1080I29.97	800.8	I
22	1080I25	960	I
23	1080I24	1000	I
24	1080I23.98	1001	I
25	48KHz Audio	562.5	—
26	96KHz Audio	281.25	—
27	44.1KHz Audio	612.244898	—
28	32KHz Audio	843.75	—
29	27MHz HSYNC	1	—
30	10MHz HSYNC	2.7	—
31	User Defined	User Defined	User Defined
63	Unknown	All Others	

Register Descriptions

The following table provides details on the device's configuration registers.

Register Map

ADD	Name	Bits	Field	R/W	Default	Description
0x01	Device Status	7	Lock_Status	R	1	Returns lock status for all unmasked and enabled PLLs
		6	Align_Status	R	0	Returns the Align Status for all enabled TOFs
		5	Wrong_Format	R	1	Returns the falue of the wrong_format input port
		4	Holdover	R	0	Returns the value of the PLL Holdover Bit
		3:0	Reserved	R	0x0	Reserved
0x02	PLL Lock and Output Alignment Status	7:4	Lock_Detect	R	4hC	Lock_Detect[7] indicates the lock status of PLL4 Lock_Detect[6] indicates the lock status of PLL3 Lock_Detect[5] indicates the lock status of PLL2 Lock_Detect[4] indicates the lock status of PLL1 0=PLL Not Locked 1=PLL Locked
		3:0	Align_Detect	R	0	Align_Detect[3] indicates the lock status of TOF4 Align_Detect[2] indicates the lock status of TOF3 Align_Detect[1] indicates the lock status of TOF2 Align_Detect[0] indicates the lock status of TOF1 0=TOF Alignment not detected 1=TOF alignment detected
0x03	Revision ID	7:0		R	0xC0	Returns device revision code
0x04	Reserved					

ADD	Name	Bits	Field	R/W	Default	Description
0x05	Device Control	7	Soft_Reset	R/W	0	Writing a '1' will reset all registers to their default values. This bit is self-clearing and always returns '0' when read.
		6	Powerdown	R/W	0	Controls the power_down output port.
		5	EN_AFD	R/W	1	Enables Auto Format Detection (AFD). 0 = Auto Format Detect disabled 1 = Auto Format Detect enabled
		4:3	PLL1_Mode	R/W	0	Sets PLL1 operating mode: 00 = Force Free-run 01 = Genlock 10 = Force Holdover 11 = Reserved
		2	LOR Mode	R/W	1	Sets default mode of operation on Loss of Reference(LOR) condition: 0 = Holdover on LOR 1 = Free run on LOR
		1	Force_148	R/W	0	When this bit is set, it forces the PLL2 and PLL3 clock rates to 148.xx MHz regardless of chosen output format. Otherwise, the native clock rate of the chosen output format will be used. 0 = Uses the native clock rates 1 = Forces the 148.xx MHz clock rates
		0	GOE	R/W	1	Global Output Enable 0 = Disables all CLKout and Fout output buffers (Hi-Z) 1 = Enable active outputs
0x06	Input Polarity	7:4	RSVD		0	
		3	EN_AUTOPOL	R/W	1	Enables Auto Polarity Detection and Correction. The proper polarity needs to be set to synchronize the output timing signals to the leading edges of the H and V inputs. 0 = The polarities of HVF inputs are manually set by their respective polarity override registers. 1 = The polarity of the H input is auto-detected. The polarity correction applied to the H input will also be applied to V and F inputs.
		2	HIN_POL_OVR	R/W	0	Used to manually set the H input Polarity. 0=Active Low (Negative polarity) 1=Active High (Positive polarity)
		1	VIN_POL_OVR	R/W	0	Used to manually set the V input Polarity. 0=Active Low (Negative polarity) 1=Active High (Positive polarity)
		0	FIN_POL_OVR	R/W	0	Used to manually set the F input Polarity. 0=Active Low (Negative polarity) 1=Active High (Positive polarity)
0x07	Outut Mode — PLL2 Format	7:6	RSVD		00	Reserved
		5:0	PLL2_Format	R/W	0x0E	Sets the video format output timing for PLL2.
0x08	Output Mode — PLL3 Format	7:6	RSVD		00	Reserved
		5:0	PLL3_Format	R/W	0x0D	Sets the video format output timing for PLL2.

ADD	Name	Bits	Field	R/W	Default	Description
0x09	Output Mode —Misc	7:5	RSVD		0	
		4	AFS Mode	R/W	0	Sets the TOF4 output timing mode. 0 = Secondary Audio Clock Output (derived from PLL4 clock) 1 = Audio Frame Sync (derived from TOF1)
		3:0	XPT_Mode	R/W	0000	Sets the PLL/TOF crosspoint mode for Out2 and Out3. Refer to the crosspoint output selection table.
0x0A	Output Buffer Control	7:4	CLK_HIZ	R/W	0000	CLK_HIZ[3] sets CLKout4 output buffer mode. CLK_HIZ[2] sets CLKout3 output buffer mode. CLK_HIZ[1] sets CLKout2 output buffer mode. CLK_HIZ[0] sets CLKout1 output buffer mode. 0 = CLKoutx enabled 1 = CLKoutx Hi-Z
		3:0	FOUT_HIZ	R/W	0xF	FOUT_HIZ[3] sets Fout4 output buffer mode. FOUT_HIZ[2] sets Fout3 output buffer mode. FOUT_HIZ[1] sets Fout2 output buffer mode. FOUT_HIZ[0] sets Fout1 output buffer mode. 0 = Foutx enabled 1 = Foutx Hi-Z
0x0B	Output Frame Control — Offset1_MSB	7:5	RSVD	R/W	0	Reserved
		4:0	TOF1 Offset MSB	R/W	0x00	tof1_offset[12:0] sets number of lines to delay TOF1. TOF1_OFFSET_MSB[4:0] sets tof1_offset[12:8]
0x0C	Output Frame Control — Offset1_LSB	7:0	TOF1 Offset LSB	R/W	0x00	tof1_offset[12:0] sets number of lines to delay TOF1. TOF1_OFFSET_LSB[7:0] sets tof1_offset [7:0]
0x0D	Output Frame Control — Offset2_MSB	7:5	RSVD		0x00	Reserved
		4:0	TOF2 Offset MSB	R/W	0x00	tof2_offset[12:0] sets number of lines to delay TOF2 . TOF2_OFFSET_MSB[4:0] sets tof2_offset [12:8]
0x0E	Output Frame Control — Offset2_LSB	7:0	TOF2 Offset LSB	R/W	0x00	tof2_offset[12:0] sets number of lines to delay TOF2 . TOF2_OFFSET_LSB[7:0] sets tof2_offset [7:0
0x0F	Output Frame Control — Offset3_MSB	7:5	RSVD		0x0	Reserved
		4:0	TOF3 Offset MSB	R/W	0x00	tof3_offset[12:0] sets number of lines to delay TOF3 . TOF3_OFFSET_MSB[4:0] sets tof3_offset [12:8]
0x10	Output Frame Control — Offset3_LSB	7:0	TOF3 Offset LSB	R/W	0x00	tof3_offset[12:0] sets number of lines to delay TOF3. TOF3_OFFSET_LSB[7:0] sets tof2_offset [7:0

ADD	Name	Bits	Field	R/W	Default	Description
0x11	Alignment Control — TOF1	7:6	RSVD		00	
		5:4	TOF1_Align_Mode	R/W	11	00 = Auto-align when misaligned 01 = Reserved 10 = Always Align 11 = Never Align *When H_ONLY is 1, TOF1 align mode is forced to never align.
		3	TOF1_Sync_Near	R/W	1	This bit sets the PLL1/TOF1 output synchronization behavior when the same reference is reapplied following a momentary LOR condition and TOF1 is within 2 lines of the expected location. 0 = Clean synchronization- ensures the outputs drift smoothly back to frame alignment without excessive output phase disturbances 1 = Crash synchronization- achieves the fastest frame alignment through PLL/TOF counter resets, which can result in output phase disturbances
		2	TOF1_Sync_Far	R/W	0	This bit sets the PLL1/TOF1 output synchronization behavior when the same reference is reapplied following a momentary LOR condition and TOF1 is within 2 lines of the expected location. 0 = Clean synchronization- ensures the outputs drift smoothly back to frame alignment without excessive output phase disturbances 1 = Crash synchronization- achieves the fastest frame alignment through PLL/TOF counter resets, which can result in output phase disturbances
		1	TOF1_Sync_Slew	R/W	0	Sets the direction that TOF1 slews to achieve frame alignment when a new reference is applied and TOF1 is outside of 2 lines of the expected location. 0 = TOF1 lags by railing the VCXO input low 1 = TOF1 advances by railing the VCXO input high
		0	RSVD	R/W	0	Reserved

ADD	Name	Bits	Field	R/W	Default	Description
0x12	Alignment Control - TOF2	7:6	RSVD		00	
		5:4	TOF2_Align_Mode	R/W	11	00 = auto align when misaligned 01 = one shot manual align when writing TOF2_INIT=1 10 = always align 11 = never align
		3:1	RSVD		000	
		0	TOF2_INIT	R/W	0	Writing one to this bit while also writing TOF2_ALIGN_MODE = 3, will cause the tof2_init output to go high for at least one vframe period + one hsync period and not more than one vframe period + two hsync periods. The assertion of tof2_init must happen immediately (it cannot wait for hsync). If TOF2_ALIGN_MODE is being written to 3, this bit will have no effect. This bit is self-clearing and will always read zero.
0x13	Alignment Control — TOF3	7:6	RSVD		00	
		5:4	TOF3_Align_Mode	R/W	11	00 = auto align when misaligned 01 = one shot manual align when writing TOF3_INIT=1 10 = always align 11= never align
		3:1	RSVD		000	
		0	TOF3_INIT	R/W	0	Writing one to this bit while also writing TOF3_ALIGN_MODE != 3, will cause the tof3_init output to go high for at least one vframe period + one hsync period and not more than one vframe period + two hsync periods. The assertion of tof3_init must happen immediately (it cannot wait for hsync). If TOF3_ALIGN_MODE is being written to 3, this bit will have no effect. This bit is self-clearing and will always read zero.

ADD	Name	Bits	Field	R/W	Default	Description
0x14	Alignment Control — AFS	7:6	RSVD	R/W	00	Reserved
		5:4	AFS_Align_Mode	R/W	11	00 = auto align when misaligned 01 = one shot manual align. AFS_INIT_INPUT reg determines if done by pin (INIT) or register (AFS_INIT = 1) 10 = always align 11= never align
		3	AFS_Init_Input	R/W	0	0 = Rising edges on INIT (pin 6) trigger AFS one shot manual align. 1 = Writing '1' to AFS_INIT register triggers AFS one shot manual align.
		2:1	RSVD		00	
		0	AFS_INIT	R/W	0	Writing one to this bit while also writing AFS_ALIGN_MODE = 3 and AFS_INIT_INPUT=1, or providing a rising edge on the init input when AFS_ALIGN_MODE != 3 and AFS_INIT_INPUT=0, will cause the afs_init output to go high for at least one vframe period + one hsync period and not more than one vframe period + two hsync periods. The assertion of afs_init must happen immediately (it cannot wait for hsync). If AFS_ALIGN_MODE == 3, toggling the init input will have no effect. This bit is self-clearing and will always read zero.
0x15	Loss of Alignment Control	7:3	RSVD		0	
		2:0	LOA_Window	R/W	010	Number of 27MHz clocks between the TOF1 and VSYNC before Loss of Alignment is reported. If the code loaded in this register is n, then Loss of Alignment will be reported if the difference between TOF1 and VSYNC exceeds 2^n 27 MHz clock cycles
0x16	LOR Control — Holdover Sampled Voltage MSB	7:2	RSVD			
		1:0	VC_HOLD_MSB	R	10	The vc_hold[9:0] input signal changes rather slowly. For synchronization, it should be sampled on consecutive 27MHz clocks until two identical values are found. This value will be saved as vc_hold_sampled[9:0]. Whenever the VC_HOLD[9:8] register is read, vc_hold_sampled[9:8] is returned, and VC_HOLD[7:0] will memorize the current value of vc_hold_sampled[7:0] (to be read at a later time). This scheme allows a coherent 10-bit value to be read. Returns a synchronized snapshot of the vc_hold[9:8] (MSB)

ADD	Name	Bits	Field	R/W	Default	Description
0x17	LOR Control — Holdover Sampled Voltage LSB	7:0	VC_HOLD_LSB	R	NA	The vc_hold[9:0] input signal changes rather slowly. For synchronization, it should be sampled on consecutive 27MHz clocks until two identical values are found. This value will be saved as vc_hold_sampled[9:0]. Whenever the VC_HOLD[9:8] register is read, vc_hold_sampled[9:8] is returned, and VC_HOLD[7:0] will memorize the current value of vc_hold_sampled[7:0] (to be read at a later time). This scheme allows a coherent 10-bit value to be read. Returns a synchronized snapshot of the vc_hold[7:0] (LSB)
0x18	LOR Control Free Run Control Voltage MSB	7:2	RSVD			Reserved
		1:0	VC_Free_MSB	R/W	01	Freerun Control Volage (vc_free[9:0]) is the voltage asserted on VC_LPF pin in freerun mode. Writing will change the MSB (vc_free[9:8])
0x19	LOR Control — Free Run Control Voltage LSB	7:0	VC_Free_LSB	R/W	0xFF	Freerun Control Volage (vc_free[9:0]) is the voltage asserted on VC_LPF pin in freerun mode. Writing will change the LSB (vc_free[7:0])
0x1A	LOR Control — ADC & DAC Disable	7:2	RSVD			
		1	ADC_Disable	R/W	0	Directly controls the adc_disable output port. 0 = enable holdover ADC 1 = disable holdover ADC
		0	DAC_Disable	R/W	0	Directly controls the dac_disable output port. 0 = enable Freerun/Holdover DAC 1 = disable Freerun/Holdover DAC
0x1B	Loss of Reference Threshold	7	RSVD		0	
		6:4	HSYNC_Missing Threshold	R/W	00	Sets the threshold for number of additional clocks to wait before setting hsync_missing.
		3	RSVD		0	
		2:0	LOR_Threshold		001	Sets the number of hsync periods to wait before setting loss of reference. Since during blanking there can have up to 5 missing hsync pulses, this value is usually set to 6.
0x1C	Loss of Lock Threshold	7:5	RSVD		0	
		4:0	LOCK1_Threshold		10000	Sets the number of hsync periods to wait before setting loss of lock. Since during blanking there can have up to 5 missing hsync pulses, this value is usually set > 6..

ADD	Name	Bits	Field	R/W	Default	Description
0x1D	Mask Control — PLL Lock and Output Align	7	MASK_LOCK4	R/W	0	Setting this bit masks the PLL4 lock status in the global LOCK_STATUS bit.
		6	MASK_LOCK3	R/W	0	Setting this bit masks the PLL3 lock status in the global LOCK_STATUS bit.
		5	MASK_LOCK2	R/W	0	Setting this bit masks the PLL2 lock status in the global LOCK_STATUS bit.
		4	MASK_LOCK1	R/W	0	Setting this bit masks the PLL1 lock status in the global LOCK_STATUS bit.
		3	MASK_TOF4_ALIGN	R/W	0	Setting this bit masks the TOF4 align status in the global ALIGN_STATUS bit.
		2	MASK_TOF3_ALIGN	R/W	0	Setting this bit masks the TOF3 align status in the global ALIGN_STATUS bit.
		1	MASK_TOF2_ALIGN	R/W	0	Setting this bit masks the TOF2 align status in the global ALIGN_STATUS bit.
		0	MASK_TOF1_ALIGN	R/W	0	Setting this bit masks the TOF1 align status in the global ALIGN_STATUS bit.
0x1E	Reserved	7:0				Reserved
0x1F	Reserved	7:0				Reserved
0x20	Input Format	7:6	RSVD			
		5:0	Input Format		0x00	When Auto Format Detection is enabled (EN_AFD, address 0x05), this register is read-only and controlled automatically. When Auto Format Detection is disabled, this register is writable via I2C. All writes to this register (whether automatic or manual) will update all the LUT1 (Lookup Table 1), LUT2_2, and LUT2_3 output registers based on the value written here. Writing to any of the LUT1, LUT2_2, or LUT2_3 output registers will set this field to 6'd62 indicating that custom changes have been made.
0x21	Output Frame Lookup — Input VSync Code	7:4	RSVD			
		3:0	Input VSync Code	R/W	0011	Writes to this register update the vsync code which tells the device what the Input frame rate is.. There is a table which correlates the vsync codes to the actual frame rates. When Auto Format Detection is enabled (EN_AFD, address 5), this register is read-only, and is automatically loaded by the device.
0x22	Output Frame Lookup — PLL2 Vsync Code	7:4	RSVD			
		3:0	PLL2 Vsync Code	R/W	101	Whenever PLL2_FORMAT (address 7) is written, this field is updated with the appropriate vsync code. If any custom changes are made the device will set this field to 4'd14 to so indicate.
0x23	Output Frame Lookup — PLL3 Vsync Code	7:4	RSVD			
		3:0	PLL3 Vsync Code	R/W	110	Whenever PLL3_FORMAT (address 8) is written, this field is updated with the appropriate vsync code. If any custom changes are made the device will set this field to 4'd14 to so indicate.
0x24	Reserved					

ADD	Name	Bits	Field	R/W	Default	Description
0x25	PLL1 Advanced Control	7:5	RSVD			
		4	PLL1_DIV	R/W	0	0=Divide by 1 (Output is 27 MHz) 1=Divide by 2 (Output is 13.5 MHz)
		3	RSVD			
		2	PLL1 Input Mode	R/W	0	Directly controls the mode of the PLL1 input buffer 0=Single Ended 1=Differential
		1	RSVD		0	
		0	Fastlock		1	This bit enables ICP1_FAST (address 0x27) to be used during locking. 0= FastLock disabled 1=FastLock enabled
0x26	PLL1 Advanced Control FastLock Delay	7:4	RSVD			
		3:0	FastLock Delay	R/W	0000	Sets the amount of time that PLL1_Lock must be asserted before the PLL1 Charge pump current is reduced from the ICP1_Fast value to the ICP1 value. The time delay is speified in units of half seconds. Delay = FastlockDelay*0.5 Seconds. Valid values are from 0 to 10. Values from 11 to 15 are reserved.
0x27	PLL1 Advanced Control Fastlock CP Current	7:0	FastLock Charge Pump Current	R/W	0x1F	This field specifies the charge pump current to drive when FastLock is active
0x28	PLL1 Advanced Control Charge Pump Current	7:0	PLL1 Charge Pump Current	R/W	0x08	This field defines the charge pump current used when FastLock is not active.
0x29	PLL1 Advanced Control R Counter MSB	7:2	RSVD			
		1:0	MSB	R/W	0	The two LSBs of Register 0x29 along with the eight bits of Register 0x2A form a ten bit word which comprises the R divider for PLL1. This register is internally written based on the input format and when AutoFormatDetect is enabled, these registers are read only.
0x2A	PLL1 Advanced Control R Counter LSB	7:0	LSB	R/W	0x01	
0x2B	PLL1 Advanced Control N Counter MSB	7	RSVD			
		6:0	MSB	R/W	0x06	The 7 LSBs of Register 0x2B along with the eight bits of register 0x2C comprise the fifteen bit word which is used for the N divider of PLL1. These registers are internally controlled based on the input format detected and when AutoFormatDetect is enabled, these registers are read only.
0x2C	PLL1 Advanced Control N Counter LSB	7:0	LSB	R/W	0xB4	
0x2D	PLL1 Advanced Control Lock Step Size	7:5	RSVD			
		4:0	Lock Step Size	R/W	01000	See Applications section discussion on Lock Detect
0x2E	PLL2 Advanced Control Main	7:5	RSVD			
		4	PLL2_DIV	R/W	0	0=divide by 1 1=divide by 2
		3	PLL2_DISABLE	R/w	0	0=PLL_2 disable is determined by XPT_MODE (Address 0x09) 1=PLL2 is disabled
		2:0	RSVD			

ADD	Name	Bits	Field	R/W	Default	Description
0x2F	PLL2 Advanced Control Charge Pump Current	7:4	RSVD			
		3:0	ICP2	R/W	0010	Controls PLL2 Charge Pump Current
0x30	PLL2 Advanced Control VCO Range	7:0	VCO_RNG2	R/W	0x0C	Controls the VCO range
0x31	PLL3 Advanced Control Main	7:5	RSVD			
		4	PLL3_DIV	R/W	0	0=divide by 1 1=divide by 2
		3	ICP3	R/W	0	0=PLL_3 disable is determined by XPT_MODE (Address 0x09) 1=PLL3 is disabled
		2:0	RSVD			
0x32	PLL3 Advanced Control Charge Pump Current	7:4	RSVD			
		3:0	ICP3	R/W	011	Controls PLL3 Charge Pump Current
0x33	PLL3 Advanced Control VCO Range	7:0	VCO_RNG3	R/W	0x05	Controls the VCO range
0x34	PLL4 Advanced Control Main	7:4	PLL4_DIV	R/W	0010	Controls the PLL_4 output divider — PLL 4 is divided by 2^{PLL4_DIV}
		3	PLL4_Disable	R/W	0	0=PLL4 is enabled 1=PLL4 is disabled
		2	RSVD	r	0	
		1	IS125M	r/w	0	0=100MHz clock 1=125MHz clock
		0	PLL4_Mode	r/w	0	0=using 27MHz Clock 1=using external clock
0x35	PLL4 Advanced Control Charge Pump Current	7:4	RSVD	R	0	
		3:0	ICP4	R/W	1000	Controls PLL4 Charge Pump Current
0x36	PLL4 Advanced Control R counter	7	RSVD			
		6:0	DIV _R4	R/W	0x4B	Sets the R divider in PLL4
0x37	PLL4 Advanced Control N counter MSB	7:2	RSVD	R		
		1:0	DIV_N4_MSB	R/W	10	Two MSBs of the N divider in PLL4
0x38	PLL4 Advanced Control N counter LSB	7:0	DIV_N4_LSB	R/W	00	8 LSBs of the N divider in PLL4
0x39	PLL4 Advanced Control VCO Range	7:0			0x16	
0x3A	LVDS Control	7	LVDS Boost	R/W	0	Applies preemphasis to LVDS output
		6:4	LVDS_DIFF	R/W	100	Adjusts LVDS Differential output swing
		3:0	LVDS_CM	R/W	1001	Adjusts LVDS Common Mode output voltage
0x3B	TOF1 Adv Control LPF MSB	7:5	RSVD			
		4:0	TOF1_LPF_MSB	R/W	00010	5 MSBs of the TOF1 lines per Frame count. This is read-only and loaded automatically when Auto Format Detection is enabled

ADD	Name	Bits	Field	R/W	Default	Description
0x3C	TOF1 Advanced Control LPF_LSB	7:0	TOF1_LPF_LSB	R/W	0x0D	8 LSBs of the TOF1 lines per Frame count. This is read-only and loaded automatically when Auto Format Detection is enabled Together with register 0x3B this is a 13 bit number which number of lines per frame. TOF1 will be at a frequency of HSYNC divided by this value.
0x3D	TOF2 Advanced Control CPL MSB	7	RSVD			This 15 bit register gives the number of clock cycles per line to calculate TOF2. It is loaded automatically based on the format set with register 0x07
		6:0	TOF2_CPL_MSB		0x0A	
0x3E	TOF2 Advanced Control CPL LSB	7:0	TOF2_CPL_LSB		0x50	
0x3F	TOF2 Advanced Control LPF MSB	7:5	RSVD			This 13 bit register is loaded automatically based on the format selected via register 0x07. It sets the number of lines per frame for the selected format to set the TOF2 rate correctly
		4:0	TOF2_LPF_MSB	R/W	0x02	
0x40	TOF2 Advanced Control LPF_LSB	7:0	TOF2_LPF_LSB	R/W	0x65	
0x41	TOF2 Advanced Control Frame Reset MSB	7:5	RSVD			
		4:0	TOF2_RST_MSB		0x02	
0x42	TOF2 Advanced Control Frame Reset LSB	7:0	TOF2_RST_LSB		0x58	
0x43	TOF3 Advanced Control CPL_MSB	7	RSVD			This 15 bit register gives the number of clock cycles per line to calculate TOF3. It is loaded automatically based on the format set with register 0x08
		6:0	TOF3_CPL_MSB		0x08	
0x44	TOF3 Advanced Control CPL_LSB	7:0	TOF2_CPL_LSB		0x98	
0x45	TOF3 Advanced Control LPF_MSB	7:5	RSVD			This 13 bit register is loaded automatically based on the format selected via register 0x08. It sets the number of lines per frame for the selected format to set the TOF3 rate correctly
		4:0	TOF3_LPF_MSB		0x04	
0x46	TOF3 Advanced Control LPF_LSB	7:0	TOF3_LPF_LSB		0x65	
0x47	TOF3 Advanced Control Frame Reset MSB	7:5	RSVD			
		4:0	TOF3_RST_MSB		0x00	
0x48	TOF3 Advanced Control Frame Reset LSB	7:0	TOF3_RST_LSB		0x01	
0x49	TOF4 Advanced Control AFS	7:0	TOF4_AFS		0x05	
0x4A	TOF4 Advanced Control ACLK	7:4	RSVD			
		3:0	TOF4_ACLK		1011	
0x4B-0 x50	Reserved					

ADD	Name	Bits	Field	R/W	Default	Description
0x51	User Auto Format 27M High Value MSB	7:0	USR_27M_High_MSB	R/W	0x00	User format detect is determined by looking at the frequency of the HSYNC input. This frequency is measured by counting the number of 27MHz clock cycles that occur in 20 hsync periods. This 16 bit register lists the maximum number of 27MHz clock cycles in 20 Hsync periods that could be considered to meet the criteria for the User Format
0x52	User Auto Format 27M High Value LSB	7:0	USR_27M_High_LSB	R/W	0x00	
0x53	User Auto Format 27M Low Value MSB	7:0	USR_27M_Low_MSB	R/W	0x00	User format detect is determined by looking at the frequency of the HSYNC input. This frequency is measured by counting the number of 27MHz clock cycles that occur in 20 hsync periods. This 16 bit register lists the minimum number of 27MHz clock cycles in 20 Hsync periods that could be considered to meet the criteria for the User Format
0x54	User Auto Format 27M Low Value LSB	7:0	USR_27M_Low_LSB	R/W	0x00	
0x55	User Auto Format R divider MSB	7:2	RSVD			
		1:0	USR_DIV_R1_MSB		00	
0x56	User Auto Format R Divider LSB	7:0	USR_DIV_R1_LSB		0x00	
0x57	User Auto Format N Divider MSB	7	RSVD			
		6:0	USR_DIV_N1_MSB		0x00	
0x58	User Auto Format N Divider LSB	7:0	USR_DIV_N1_LSB		0x00	
0x59	User Auto Format Charge Pump Current	7:0	USR_ICP		0x00	
0x5A	User Auto Format LPF MSB	7:5	RSVD			
		4:0	USR_TOF_LPF_MSB		0x00	
0x5B	User Auto Format LPF LSB	7:0	USR_TOF_LPF_MSB		0x00	
0x5C	User Auto Format AFS	7:0	USR_TOF4		0x00	
0x5D	User Auto Format Misc	7	EN_USERMODE	R/W	0	Enables the Auto Format Detection User Mode 1= enabled 0= disabled
		6:5	RSVD			
		4	USR_IINTERLACED	R/W	0	Sets the INTERLACED value to output from LUT1 if the INPUT_FORMAT register is set to the user code. This bit also specifies the value that the Auto Format Detection must see on the interlaced signal to detect the user defined mode.
		3:0	USR_IN_VS_CODE	R/W	0000	Sets the INPUT_VS_CODE value to output from LUT1 if the INPUT_FORMAT registers is set to the user code.

Crosspoint Output Selection Table

Register 0x09 3:0	PLL2_disable(*Note 11*)	PLL3_Disable(*Note 11*)	OUT2 Source	OUT3 Source
0000	0	0	PLL2	PLL3
0001	1	1	PLL1	PLL1
0010	0	1	PLL2	PLL2
0011	1	0	PLL3	PLL3
0100	0	0	PLL3	PLL2
0101	1	0	PLL1	PLL3
0110	0	1	PLL2	PLL1
0111	0	1	PLL1	PLL2
1000	1	0	PLL3	PLL1
1001	Reserved	Reserved	Reserved	Reserved
1010	Reserved	Reserved	Reserved	Reserved
1011	Reserved	Reserved	Reserved	Reserved
1100	Reserved	Reserved	Reserved	Reserved
1101	Reserved	Reserved	Reserved	Reserved
1110	Reserved	Reserved	Reserved	Reserved
1111	Reserved	Reserved	Reserved	Reserved

Input VSync Codes

VSync Code	Frame Rate
0	23.98Hz
1	24 Hz
2	25 Hz
3	29.97 Hz
4	30 Hz
5	50 Hz
6	59.94 Hz
7	60 Hz

Note 11: PLL2_Disable and PLL3_Disable can be forced via register writes to the PLLx_DISABLE Registers independently of the status of the Crosspoint Mode bits.

Application Information

Functional Overview

The LMH1983 is an analog phase locked loop (PLL) clock generator that can output simultaneous clocks at any of a variety of video and audio rates, synchronized or "genlocked" to H sync and V sync input reference timing. The LMH1983 features an output Top of Frame (TOF) pulse generator for each of it's four channels, each with programmable timing that can also be synchronized to the reference frame. The clock generator uses a two-stage PLL architecture. The first stage is a VCXO-based PLL (PLL 1) that requires an external 27 MHz VCXO and loop filter. In Genlock mode, PLL 1 can phase lock the VCXO clock to the input reference. The use of a VCXO provides a low phase noise clock source even when the LMH1983 is configured with a low loop bandwidth, which is necessary to attenuate input timing jitter for minimum jitter transfer. The combination of the external VCXO, external loop filter, and programmable PLL parameters can provide flexibility for the system designer to optimize the loop bandwidth and loop response for the application. Depending on mode,

The second stage consists of three PLLs (PLL 2, 3, 4) with integrated VCOs and loop filters. These PLLs continually track the reference VCXO clock phase from PLL 1 regardless of the device mode. The PLL2 and PLL3 have pre-configured divider ratios to provide frequency multiplication or translation from the VCXO clock frequency to generate the two common HD clock rates (148.5 MHz and 148.35 MHz). PLL4 is pre-configured to generate an audio clock which defaults to a 24.576MHz output, although PLL4 has several registers which allow it to be reconfigured for a variety of applications.

The VCO PLLs use a high loop bandwidth to assure PLL stability, so the VCXO must provide a stable low-jitter clock reference to ensure optimal output jitter performance. Any unused clock or TOF output can be put in Hi-Z mode, which can be useful for reducing power dissipation as well as reducing jitter or phase noise on the active clock output. The TOF pulse can be programmed to indicate the start (top) of frame and even provide format cross-locking. The output format registers should be programmed to specify the output timing (output clocks and TOF pulse), the output timing offset relative to the reference, and the output initialization (alignment) to the reference frame. If unused, the TOF output can also be put in Hi-Z mode.

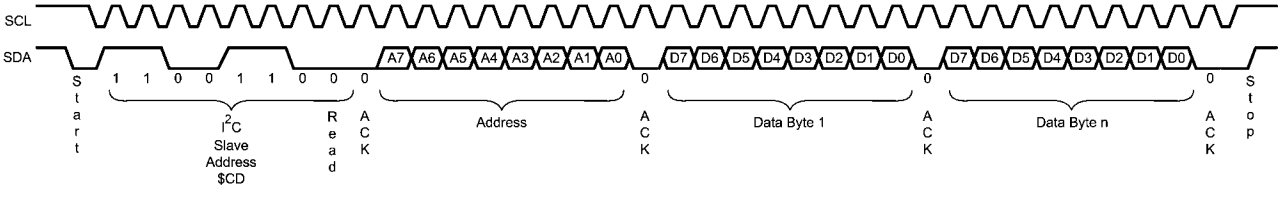
When a loss of reference occurs during genlock, PLL 1 can default to either Free run or Holdover operation. When free run is selected, the output frequency accuracy will be determined by the external bias on the free run control voltage input pin, VC_FREERUN. When Holdover is selected, the loop filter can hold the control voltage to maintain short-term output phase accuracy for a brief period in order to allow the application to select the secondary input reference and re-lock the outputs. These options in combination with proper PLL 1 loop response design can provide flexibility to manage output clock behavior during loss and re-acquisition of the reference. The reference status and PLL lock status flags can provide real-time status indication to the application system. The loss of reference and lock detection thresholds can also be configured.

I²C Interface Protocol

The protocol of the I²C interface begins with the start pulse, followed by a byte which consists of a seven-bit slave device address and a Read/Write bit as an LSB. The default address of the LMH1983 for write sequences is CCh (11001100) and for read addresses is CDh (11001101). The base address can be changed with the ADDR pin — with ADDR Open, the base address is 66h (which when left shifted becomes the CCh address), with ADDR connected to GND, the base address is 65h, and with ADDR connected to Vdd, the base address is 67h.

Write Sequence

The write sequence begins with a start condition, which consists of the master pulling SDA low, while SCL is high, next the slave address is sent, the address is made up of the 7 bit address, followed by the read/write bit, which for a write is (0). For the default base address of 66h, (1100110), the 0 is appended to the end, and the net address is CCh. Each byte sent after the address is followed by an ACK bit. When SCK is high, the master will release the SDA line, the slave pulls SDA low to acknowledge. Once the device address has been sent, the next byte sent is the register address following the register address and the ACK, the data byte is sent. When more than one data byte is sent, the address is automatically incremented so that the data is written into the next address location. Note in the Write Sequence Timing diagram that there is an ACK bit following each data byte.



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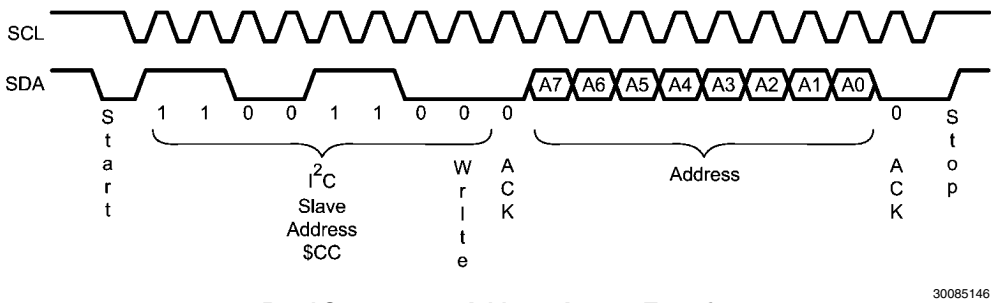
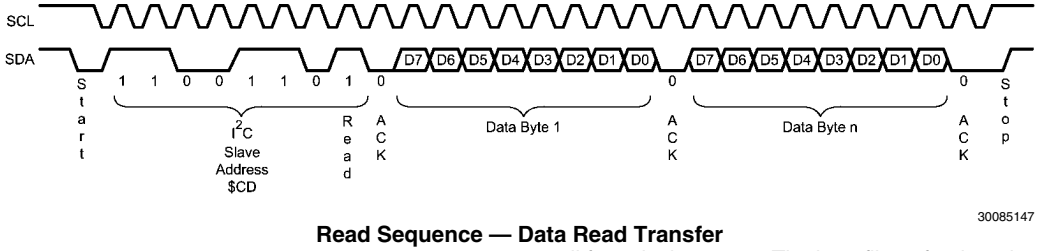
Write Sequence Timing diagram

Read Sequence

Read Sequences are made up of two I²C transfers. The first is the address access transfer, which consists of a write sequence that transfers only the address to be accessed. The second is the data read transfer which starts at the address indicated in the first transfer, and increments to the next address, continuing to read addresses until a stop condition is encountered. The address access transfer is shown in the timing diagram below, it consists of a start pulse, the slave device address including the read/write bit (a zero, indicating a write), and then its ACK bit. The next by7te is the address to be read, followed by the ACK bit, and the stop bit to indicate the end of the address access transfer. The subsequent read data transfer shown consists of the start pulse, the slave device address including the read/write bit (this time a ONE, indicating that the data is to be read) and the ACK bit. The next byte is the data read from the initial access address. After each data byte read, the address is incremented, so continuing to read from the device will provide the data in subsequent addresses. Each byte is separated from the previous byte by an ACK bit, and the end of the read sequence is indicated with a STOP bit.



Read Sequence — Address Access Transfer



Read Sequence — Data Read Transfer

Initialization

Under some circumstances, it is possible for an LMH1983 to power up in an anomalous state in which the output of PLL3, as seen on CLKout3 . A simple register write after power up will prevent the device from remaining in this state. Writing to register 0x09 with a 0x02, and then writing to register 0x09 with a 0x00 insures that the device will not exhibit the poor duty cycle performance on CLKout3

Reference detection

The default mode for the device is to use 'Auto Format Detect' in which the device determines the reference format from among those shown in the Auto Format Detection Code table, and sets up the internal configurations accordingly. There are 31 pre-defined formats, plus one format that the user can define which will be recognized. The way that the device recognizes a format is by making a measurement of the H_{IN} input frequency, and looking at the V_{IN} and F_{IN} inputs, to determine if the reference input format is an interlaced or progressive input. For some formats such as a 10MHz or 27MHz reference, if H_{IN} and V_{IN} are creating a spurious input, then the device will not properly recognize the reference input and it will not lock properly to the reference. Because of this, if H_{IN} has one of these 'special' signals on it, V_{IN} and F_{IN} should be muted.

Control of PLL1

PLL1 generates a 27 MHz reference that is used as the primary frequency reference for all of the other PLLs in the device. PLL1 has a dual loop architecture with the primary loop locking the external 27MHz VCXO to a harmonic of the H_{in} signal. In addition to this loop, there is a secondary loop which may be used in genlock operations, this second loop compares the phase of the TOF1 output signal from the LMH1983 to the F_{IN} signal. This second loop may override the primary loop in order to bring the frame alignment of the output signals into sync with the input reference. How to control this functionality is described in the section “TOF1 Alignment”

Since PLL2, PLL3 and PLL4 all have PLL1 as their input reference, the performance of PLL1 affects the performance of all four clock outputs. The loop filters for the other three PLLs are all internal, and the bandwidths are set significantly higher than that of PLL1, so all of the low frequency jitter characteristics of all four clock outputs are determined by the loop response of PLL1. Accordingly, special attention should be paid the PLL1's loop bandwidth and damping factor.

The loop response is primarily determined by the loop filter components and the loop gain. A passive second order loop filter consisting of R_S, C_S and C_P components can provide sufficient input jitter attenuation for most applications. In some cases, a higher order filter may be used to further shape the low frequency response of PLL1.

Several of these parameters are set by the device automatically, for example the charge pump current and the value of 'N'. When the input reference format changes, both N and the charge pump current are updated, N is changed to allow for lock to the new reference, and the charge pump current is adjusted to try to maintain constant loop bandwidth.

The primary locking mechanism for PLL1 is to lock the 27MHz output to a multiple of the H_{in} frequency, however there is a second loop in which the phase of TOF1 and V_{in} are compared, and depending upon the mode of the device, this loop can drive the VCXO control voltage to slew the output clocks into alignment.

PLL1 Loop Response Design Equations

The primary loop takes the reference applied to the Hin input, divides that by R (stored in registers 0x29 and 0x2A), and then compares it in phase and frequency to the output of the external VCXO divided by N (stored in registers 0x2B and 0x2C) The PFD then generates output pulses which are integrated via an external loop filter which drives the control voltage of the external VCXO (refer to PLL1 Block Diagram). Assuming a topology for the loop filter which is similar to that shown in the PLL1 block diagram, the bandwidth of the PLL is determined by:

$BW_{PLL1}=R_S x\ K_{VCO} x\ I_{CP1}/FB\_DIV$

Where

- R_S is the series resitor value in the external loop filter

- K_{VCO} is the nominal 27MHz VCXO gain in Hz/V. K_{VCO}=Pull_range*27 MHz/Vin_Range. For the VCXO used in the typical interface circuit (Mfgr: CTS, P/N 357LB3C027M0000): L_{VCO}=100ppm*27MHz/(3.0V-0.3V) =1000Hz/V
- I_{CP1} is the current from the PLL1 chargepump
- FB_DIV is the divide ratio of the PLL, which is set by the R and N register values, this will be equal to the number of 27MHz clock pulses in one H_{IN} period. For NTSC this value will be 1716

Under normal operation, several of these parameters are set by the device automatically, for example the charge pump current and the value of 'FB_DIV'. When the input reference format changes, both N and the charge pump current are updated, N is changed to allow for lock to the new reference, and the charge pump current is adjusted to try to maintain constant loop bandwidth.

It should be noted that this bandwidth calculation is an approximation, anddoes not take into account the effects of the damping factor or the second pole introduced by C_P.

At frequencies far above the —3dB loop bandwidth the closed-loop frequency response of PLL1 will roll off at about —40dB/decade, which is useful for attenuating input jitter at frequencies above the loop bandwidth. Near the —3dB corner frequency, the roll-off characteristic will depend on other factors, such as damping factor and filter order.

To prevent output jitter due to the modulation of the VCXO by the PLL's phase comparison frequency the bandwidth needs to meet the following criterion:

- BW (27MHz/FB_DIV)/20

PLL1s damping factor can be approximated by:

- $DF=(R_S/2)\sqrt{(I_{CP1}*C_S*K_{VCO}/FB\_DIV)}$

Where C_S is the value of the series capacitor (in Farads)

Typically, DF is targeted to be between $1/\sqrt{2}$ and 1 wigh will yield a good tradeoff between lock time and reference spur attenuation. DF is related to the phase margin, which is a measure of the PLL stability.

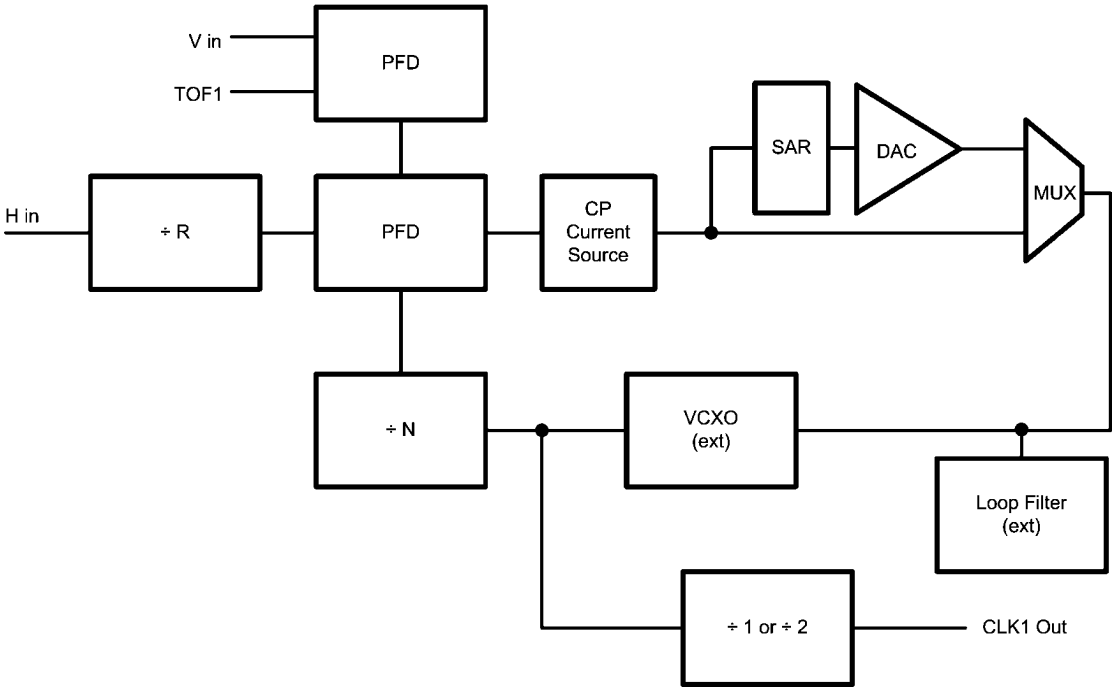
There is a second parallel capacitor, C_P which is needed to filter the reference spurs introduced by the PLL which may modulate the VCXO control voltage, leading to jitter. The following relationship should be used to determine C_P:

- $C_P \approx C_S/20$

The PLL loop gain, K can be calcuilated as:$K=I_{CP1}*K_{VCO}/FB\_DIV$

Therefore Bandwidth and Damping Factor can be expressed in terms of K:

- $BW=R_S*K$
- $DF=(R_S/2)*\sqrt{(C_S*K)}$



PLL1 Block Diagram

Loop Filter Capacitors

The most common types of capacitors used in many circuits today are Ferroelectric ceramic capacitors such as X7R, Y5V, X5R. Y5U, etc. These capacitors suffer from piezoelectric effects, which generate an electrical signal in response to mechanical vibration, stress and shock. This effect can adversely affect the jitter performance when presented to the control input to the VCXO. The easiest way to eliminate this effect is to use tantalum capacitors which do not exhibit the piezoelectric effect.

Lock Determination

There are four bits in register 2 that indicate the lock status of the four PLLs. Lock determination for PLL1 can be controlled through two registers:LockStepSize (register 0x2D) and the Loss of Lock Threshold Register. The LockStepSize register sets the amount of variation that is permitted on the VC_LPF pin while still considering the device to be locked. If the reference to the LMH1983 has a lot of jitter on it, then the device may be reluctant to declare lock if LockStepSize is set too low. The second register which controls the lock state declaration of PLL1 is Register 0x1C — Loss of Lock Threshold. This

register sets a number of cycles on the H_{IN} input that must be seen before loss of lock is declared. For some reference signals, there can be several missing H_{IN} pulses during vertical refresh, so it is suggested that this register be loaded with a value greater than 6. Pin 11, NO_LOCK, gives the lock status of the LMH1983. The status of the NO_LOCK pin can be read from register 0x01, and is a logical OR of the four individual NO_LOCK status bits of the four PLLs, and is masked by the bits in the PLL Lock mask (register 0x1D), and is also masked if an individual PLL is powered down.

Lock Time Considerations

The lock time of the LMH1983 is dominated by the lock time of PLL1 — The other PLLs have much higher loop bandwidths, and as a result lock much more quickly than does PLL1, therefore lock time considerations are all focussed on PLL1. The lock time for a PLL is dependent upon the loop bandwidth, the equation for which is listed above in the PLL1 Loop Response Design Equations section. The LMH1983 also allows a 'Fastlock' mode, in which the bandwidth is increased by increasing the charge pump current when the loop is unlocked, then at a time programmed by the user after lock is declared, $I_{CP1}$is throttled back to drop the bandwidth to the desired set point. The result is both fast lock time and very low residual jitter.

Another issue to watch when considering lock time is if you have enabled 'drift lock' as described in the section on TOF1 Alignment. If drift lock is enabled, and there is a significant difference in the phase of TOF1 relative to the F_{IN} signal. In this case, the VCXO is slewed to ramp the clock rate up or down until the two framing signal are brought into alignment. It is possible for this to take a long time (tens of seconds)

VCXO Selection Criteria

The recommended VCXO is CTS part number 357LB3C027M0000 which has an absolute pull range of ±50ppm and a temperature range of —20°C to +70°C. A VCXO with a smaller APR can provide better frequency stability, and slightly lower jitter, but the APR must be larger than the anticipated variation of the input frequency range.

Freerun, Locked and Holdover Modes

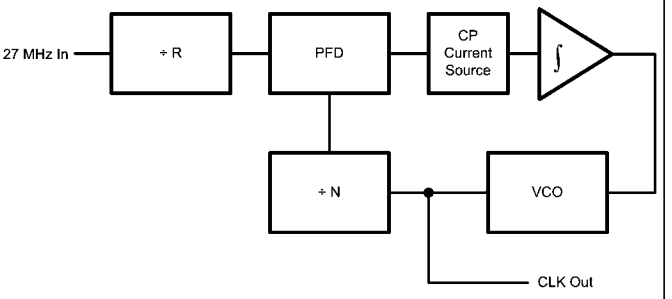
The LMH1983 primary PLL can operate in three different modes, selected via register 0x05h. In Freerun mode, H_{IN}, $V_{IN}$and F_{IN} are not used, and the VCXO control voltage is set by the contents of registers 0x15 and 0x16. By writing to these registers, the VCXO voltage can be trimmed up or down. the slave PLLs will remain locked to the primary PLL.

In Genlock mode, the VCXO control voltage is actively controlled to maintain lock between H_{IN} and the VCXO output frequency. In addition there is a second loop which may take over to assert a lock between TOF1 and F_{IN}. See the section on TOF1 alignment for more details.

The third mode is holdover mode. In the event that the reference is lost, there is an A/D — D/A pair which is able to take over for the PLL control loop, and hold the VCXO control voltage constant. For this to work properly, the device has to realize that it has lost it's reference shortly after the reference is indeed lost. Some sync separators, when the analog input is lost, will output random pulses from the H, V and F outputs, which can confuse the device, therefore if holdover mode is to be used in conjunction with an analog sync separator, it is best to gate the H, V, F signals with a signal which indicates if there is a valid reference input.

Control of PLL2 and PLL3

PLL2 and PLL3 have the least amount of flexibility of the four PLLs in the LMH1983. They are preprogrammed to run at 148.5MHz and 148.35MHz respectively. There is a ÷2 option available to allow the output to be 74.25MHz or 74.18MHz should these frequencies be required. The other controls available on these two PLLs are to disable them — disabling PLL2 or PLL3 can save significant amounts of power if that particular clock is not required.



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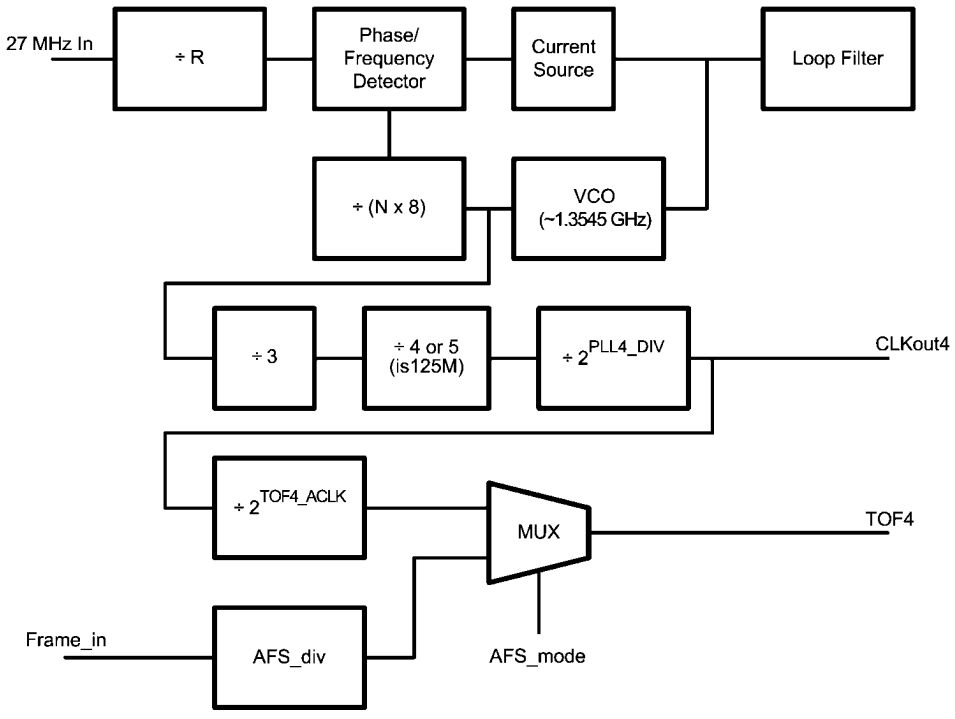
PLL2 / PLL3 Block Diagram

Control of PLL4

PLL4 is intended to generate a clock for audio use, but has a lot of versatility built into it. There is access to several registers which may be used to configure PLL4 to generate any of a broad selection of frequencies. The default state for PLL4 is to generate a 24.576MHz (48KHz x 512) on the output of CLK4, and a 5.996 Hz output from TOF4. This is done by taking CLK1 (27MHz), and dividing it by 75, resulting in a signal of 360 KHz, this is compared to the internal PLL4 VCO, which is nominally 1.2GHz, divided by 4096, which again yields 360KHz. This 1.2GHz output is divided by 12 to generate a 98.304MHz signal (48 KHz * 2048). Any power of two multiple of 48KHz can be generated by changing the contents of the PLL4_DIV component of register 0x34. Note that the divider here is in powers of 2, so the default value of 2, results in the 90.304MHz signal being divided by 2^2 or 4. PLL4_DIV is a 4 bit value, so values up to 15 may be programmed, resulting in a divide by 2^{15} or 32,768.

If audio clocks based on a 44.1KHz sampling clock are desired, then by changing the value of the is125M bit (in register 0x34) to a 1, then the divide ratio after the VCO changes from a 12 to a 15, which allows the PLL to lock to multiples of 44.1KHz while still keeping the VCO within it's permitted range. Clearly the contents of the R and N divide registers will have to be selected appropriately to generate the desired frequencies.

TOF4 has two different modes in which it can operate. When the AFS_mode bit (in register 0x09) is set to a 0, then TOF4 is derived by dividing down CLKout4 by a value of 2^{TOF4_ACLK} (register 0x4A). if the AFS_mode bit is set to a 1, then TOF4 is derived from TOF1 — divided by AFS_div (register 0x49). When AutoFormatDetect is true, then the AFS_div register is read only, and is internally set depending upon the format detected.



PLL4 Block Diagram

Clock Output Jitter

Several of the circuits which require video clocks, such as the embedded Serializers and Deserializers found in FPGAs are sensitive to jitter. In all real world applications, jitter has a random component, so it is best specified in statistical terms. The SMPTE serial standards (SMPTE 259M, SMPTE 292M and SMPTE 424M) use a frequency domain method of specifying jitter in which they refer to the peak-to-peak jitter of a signal after the jitter has been band pass filtered. Jitter at frequencies below 10Hz is ignored, and the jitter in a band from 10Hz to an intermediate frequency (1KHz for the 270Mbps standard, 100KHz for the 1.5Gbps and 3Gbps standards) is referred to as timing jitter, jitter from the intermediate frequency up to 1/10 of the serial rate is referred to as alignment jitter. The limits that the SMPTE standards place are peak-peak limits, but especially at the higher rates, random processes have a significant impact, and it is not possible to talk about peak to peak jitter without a corresponding confidence level. The methodology used to specify the jitter on the LMH1983 was to decompose the jitter into a deterministic component (t_{DJ}) plus a random component (t_{RJ}). This is the methodology used by the jitter analysis tools supported on high bandwidth oscilloscopes and timing analysis tools from the major instrumentation manufacturers.

To convert between RMS jitter and peak-to-peak jitter the Bit Error Rate (BER) must be specified. Without a known BER, since jitter is a random event, the peak-to-peak jitter will be dependent upon the observation time, and can be arbitrarily large. The equation which links peak to peak jitter to the RMS jitter is:

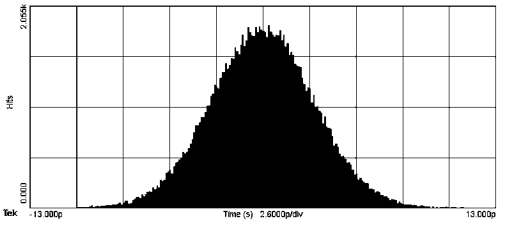
$$t_{P\text{-}P}=t_{DJ}+\alpha*t_{RJ}$$

Where α is determined by the BER according to the equation:

$$1/2\text{erfc}(\sqrt{2}*\alpha)=\text{BER}$$

The erfc function can be found in several mathematics references, and is also a function in both Excel and MATLAB. A fairly common BER used for these calculations is 10^{-12}, which can be used to find a value of 14 for α

Another common method for evaluating the jitter of a clock output is to look at the phase noise, as a function of frequency. Plots showing the phase noise for each of the four CLKout outputs can be found below



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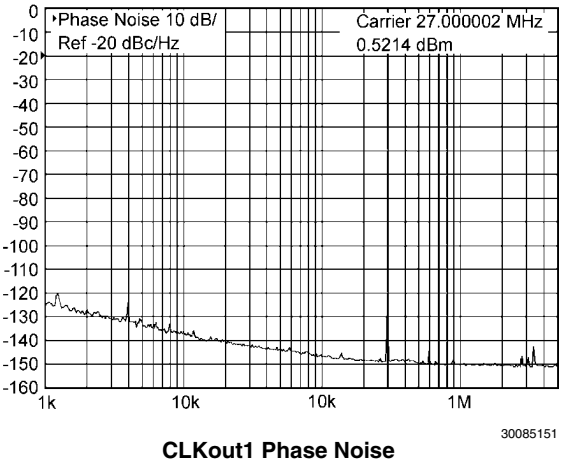
CLKout1 Jitter Histogram
Horizontal scale: 2.6ps/division



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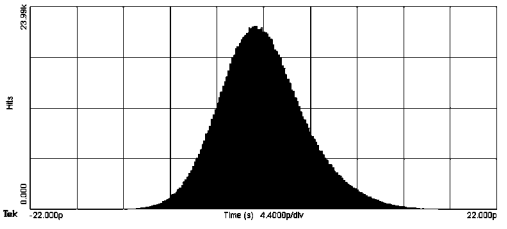
CLKout1 Phase Noise



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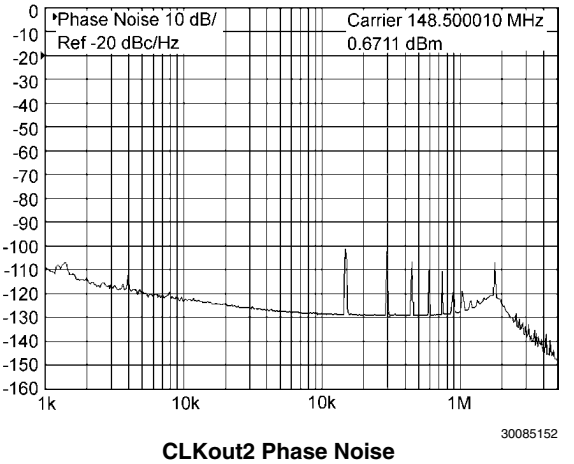
CLKout2 Jitter Histogram
Horizontal scale: 4.4ps/division



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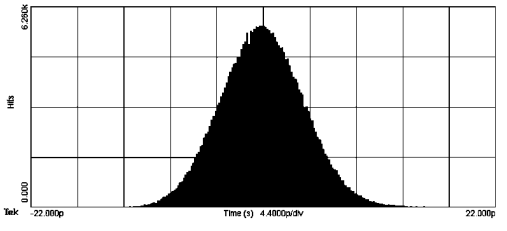
CLKout2 Phase Noise



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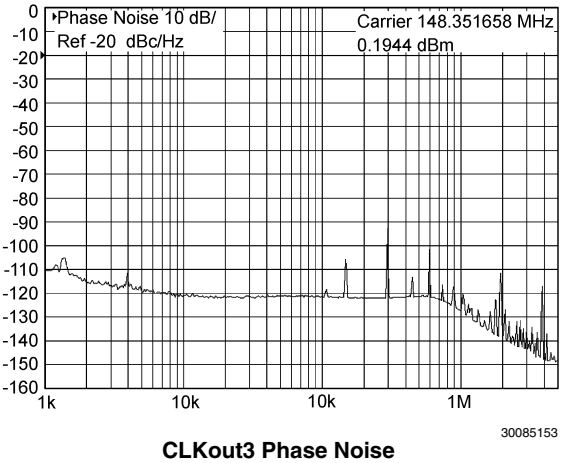
CLKout3 Jitter Histogram
Horizontal scale: 4.4ps/div



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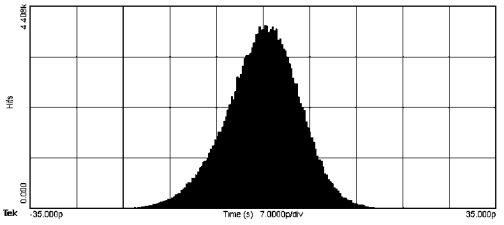
CLKout3 Phase Noise



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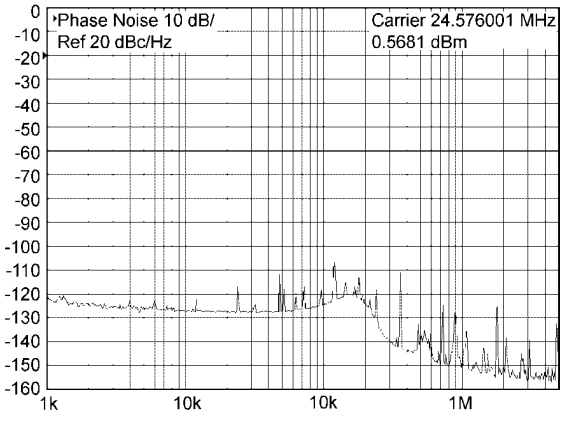
CLKout4 Jitter Histogram
Horizontal scale:7 ps/div



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CLKout4 Phase Noise

Output Driver Adjustments

The LVDS output drivers can be adjusted via the I²C interface to change the differential output voltage swing, the common mode voltage and to apply prepemphasis to the LVDS output

Register 0x3A MSB (bit 7) turns on the preemphasis which may be used to extend the reach between the LMH1983 and the load. It is recommended that the trace length be kept short, as longer traces have more opportunity to couple with hostile signals and degrade jitter performance.

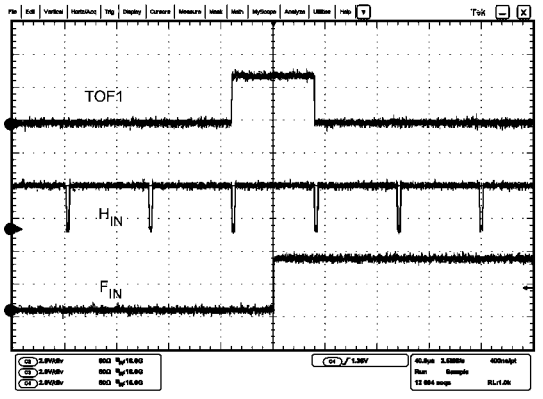
The differential output swing of CLKout pins is adjusted through bits [6:4] of register 0x3A a larger value loaded into this portion of the register will increase the output swing.

The common mode output voltage is also able to be adjusted via register 0x3A, using register bits [3:0]

TOF1 Alignment

Each of the four clock outputs has a corresponding Top Of Frame (TOF) output signal. The LMH1983 is programmed with a video format for each of the three video clocks, and the TOF signal will provide a digital indication of when the start of a new frame occurs for that particular format. As an example, if PLL1 is programmed with a video format corresponding to NTSC, CLK1 will be 27MHz, and TOF1 will output a pulse once per frame, or once every 900,900 clock cycles. The default state is for the LMH1983 to detect the input reference format, and to program this format as the output format for CLK1, so if the input reference is an NTSC reference, then TOF1 will default to a 27.97Hz signal.

If the H_{IN}, V_{IN},and F_{IN}inputs to the LMH1983 are coming from the LMH1981 Sync separator, then the rising edge of the F_{IN}input will come in the middle of a line (between H_{IN} pulses. The TOF pulse, if aligned, will be a pulse with a width of 1 H period, with transitions aligned with the leading edges of the H_{IN} pulses, and when set for a 0 offset, will be high during the H period in which the F_{IN} input transitions, as can be seed in the “TOF1 Timing” scope shot



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TOF1 Timing

The alignment between the incoming F_{IN} and the TOF1 output may be controlled in a number of ways. There are three different alignment modes in which TOF1 may operate, selected via register 0x11h. The default, powerup mode is for there to be no alignment, the other two options are to always force alignment to F_{IN}, and to force alignement to F_{IN} when they are misaligned. Misalignment can be defined by the user via register 0x15h where a window is defined which specifies the amount of mismatch that is permitted between F_{IN} and TOF1 while still considering them to be aligned. If the input reference signal has a significant amount of low frequency jitter or wander, it may be possible for the relative alignment between TOF1 and F_{IN} to move around since the TOF1 output will have it's jitter and wander attenuated by the PLL1 loop filter. If the align always mode is selected, this may lead to timing jumps on the output of CLKout1/TOF1 which would be undesirable.

Once the device decides that it needs to align TOF1 and F_{IN}, there are two ways that it can be done. Crash lock involves simply resetting the counter which keeps track of where the TOF1 output transition happens, and results in an instantaneous shift of TOF1 to align with F_{IN}. Drift lock involves using the second loop in PLL1, and skewing the VCXO to make the frequency of CLKout1 either speed up or slow down, slowly pulling TOF1 and F_{IN} into alignment. If a new reference is applied, which is not in alignment with TOF1, but the output is currently in use, it may be better to slew TOF1 into alignment rather than to cause a major disruption in the timing with a crash lock. The LMH1983 allows the user to select either crash lock, or drift lock under each of two different conditions, controllable via register 0x11h. If the difference in phase between TOF1 and $F_{in}$is small, and if the difference

between the two is large. Furthermore, if the difference is large, then the user has the opportunity to tell the device to achieve alignment either via advancing or retarding the phase of PLL1 in order to achieve alignment. Note that if the difference in alignment is large, to achieve alignment via drift lock may take a very long time (10s of seconds), during which time the output clock will not be phase locked to the input H_{IN}.

TOF2 and TOF3 Timing

Like with TOF1, each of the second and third channels has a video format associated with it. The format is determined by programming this into registers 0x07h and 0x08h respectively. Once the format is programmed, and the TOF outputs are enabled, a TOF pulse is generated at the appropriate rate for each of the outputs. There are four different alignment modes which may be selected for TOF2 and TOF3:

TOF2/TOF3 Alignment Modes

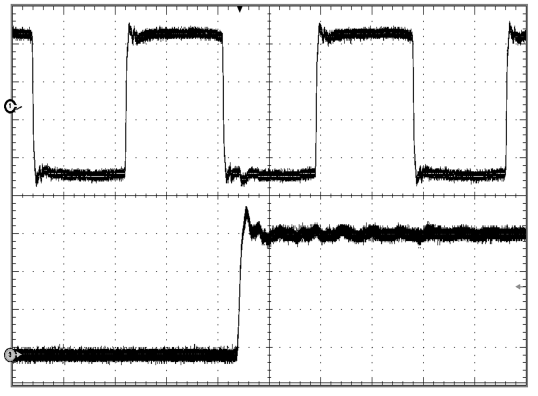
TOF2/TOF3 Alignment Mode	Description
0	Auto Align when misaligned
1	One shot manual align
2	always align
3	never align

TOF2 and TOF3 are generally aligned with TOF1. The alignment status bit will only be set if the frame rates are the same as one another. Another option for alignment is via software, where a but is written to the TOFX_INIT bit. For example, the LSB of register 0x12h is the TOF2_INIT bit. Writing a one to this bit, while also setting TOF2 alignment mode to anything other than 3, will cause TOF2 immediately reset it's phase. This bit is a self clearing bit, so reading it will always return a zero.

TOF4 Alignment Modes

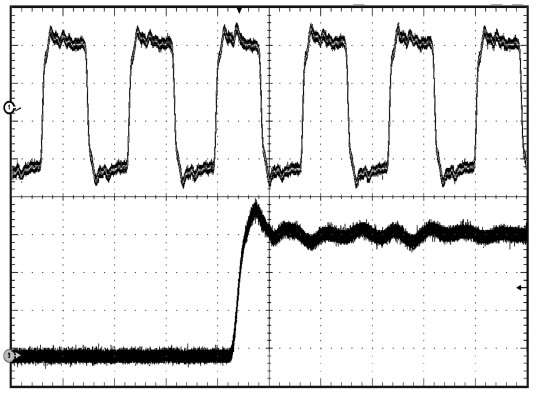
The fourth channel of the LMH1983 is most often used to generate an audio clock. The default base audio clock rate is 48KHz, and this sample clock is synchronous in phase with the video frame only once every 5 frames for 29.97 and 30Hz frame rate standards, or once every 10 frames for 60Hz and 59.94 Hz systems. The LMH1983 can generate a TOF4 pulse which will happen at this rate, allowing audio frames to be synchronized with the video frames.

TOF4 may be aligned either to TOF1, or to the F_{IN} input. Additionally, there is an external INIT input which can be used to set the TOF4 alignment.



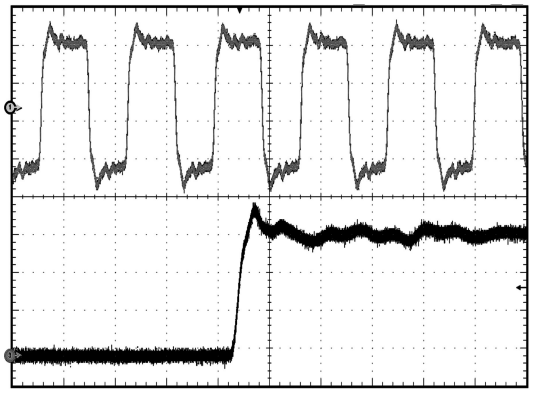
30085160

TOF1 Timing
Top Trace CLKout1, Bottom Trace TOF1
10ns/div. Top 200mV/div, Bottom 1V/div



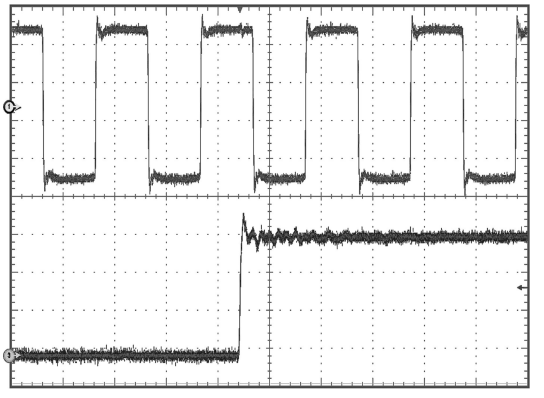
30085161

TOF2 Timing
Top Trace CLKout2, Bottom Trace TOF2
4ns/div, Top 200mV/div, Bottom 1V/div



30085162

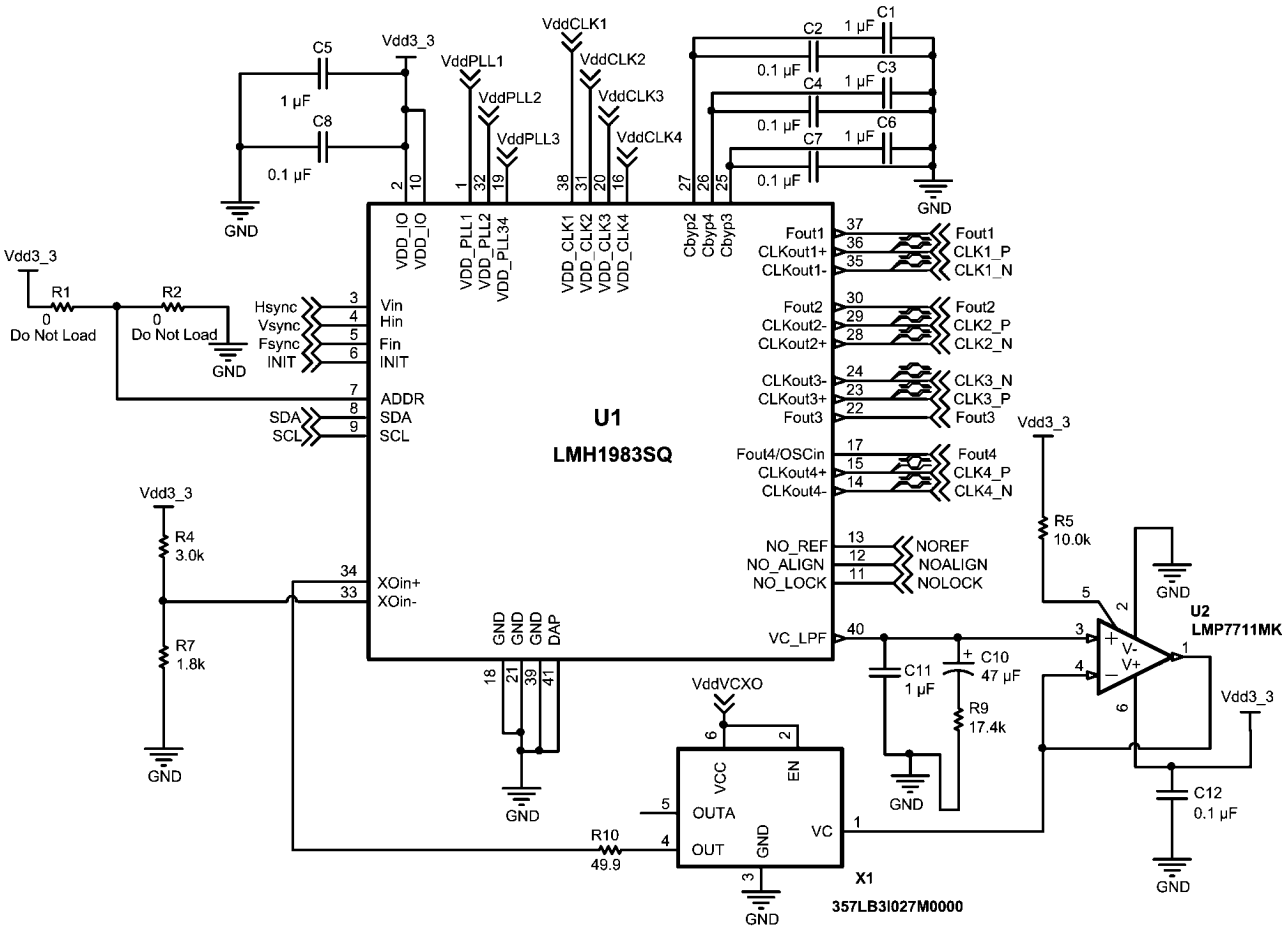
TOF3 Timing
Top Trace CLKout3, Bottom Trace TOF3
4ns/div, Top 200mV/div, Bottom 1V/div



30085163

TOF4 Timing
Top Trace CLKout4, Bottom Trace TOF4
10ns/div, Top 200mV/div, Bottom 1V/div

Typical Interface Circuit



LMH1983 Typical Interface Circuit

A typical application circuit for the LMH1983 is shown in the Typical Interface Circuit. The key areas to consider on this circuit are the loop filter — which consists of R_S,C_S and C_P and the LM7711 Operational amplifier which buffers the loop filter output prior to driving the control voltage input of the VCXO. Care must be taken in the component selection for the loop filter components (see the loop filter discussion above). The CLKout outputs are differential, LVDS signals, and should be treated as differential signals. These signals may be layed out as fully differential lines, in which the characteristic impedance between the two lines is nominally 100Ω. Alternately, loosely coupled lines may be used, in which case the characteristic impedance of each line should be 50Ω referenced to GND. In either case, care should be taken to match the lengths of the traces as closely as possible. Trace length mismatches on a differential line will add to the jitter seen on that line. Jitter is also added to the clock outputs if other signals are allowed to interfere with the signal traces, therefore, to the greatest extent possibly, the clock traces should be isolated from other signals, especially avoiding long parallel runs. In places where a hostile signal must cross a sensitive clock signal, it should be routed such that it crosses as closely as possible to a 90° crossing.

One potential source of jitter on a multiple clock system such as the LMH1983 is interference between the four PLLs on the chip. To help reduce this effect, internally on the LMH1983 each PLL is run from a separate power supply, and each supply has its own internal regulator. These regulators each require their own external bypass — this can be seen in the typical interface circuit with the capacitors C_A, C_B

An I²C bus is also connected from the control system to the LMH1983. The LMH1983 will have one of three I²C addresses, selected by the state of the ADDR pin, which may be tied high, tied low or left open. Depending on the configuration of the control bus, it may require a pull-up resistor on the SDA and SCK pins.

PCB Design Do's and Don'ts

DO Whenever possible dedicate an entire layer to each power supply. This will reduce the inductance in the supply plane.

DO use surface mount components whenever possible

DO place bypass capactors and filter components as close as possible to each power pin

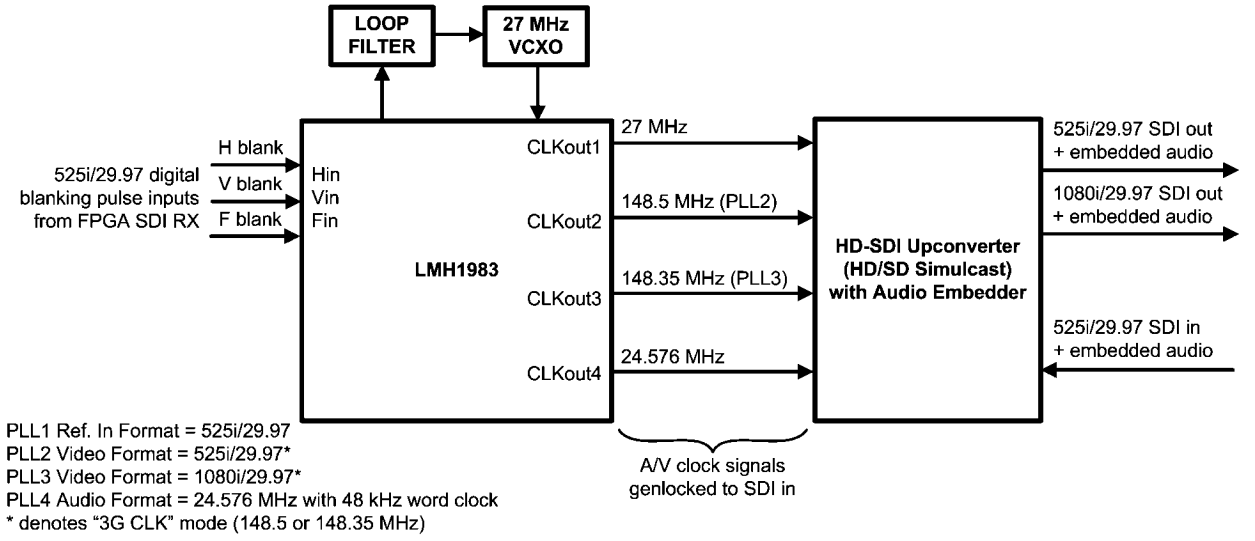
DO place the loop filter components, including the buffer amplifier, and VCXO as close as possible to the LMH1983

DON'T allow discontinuities in the ground planes-return currents follow the path of least resistance, for high frequency signals this will be the path of least inductance.

DO make sure to match the trace lengths of all differential traces.

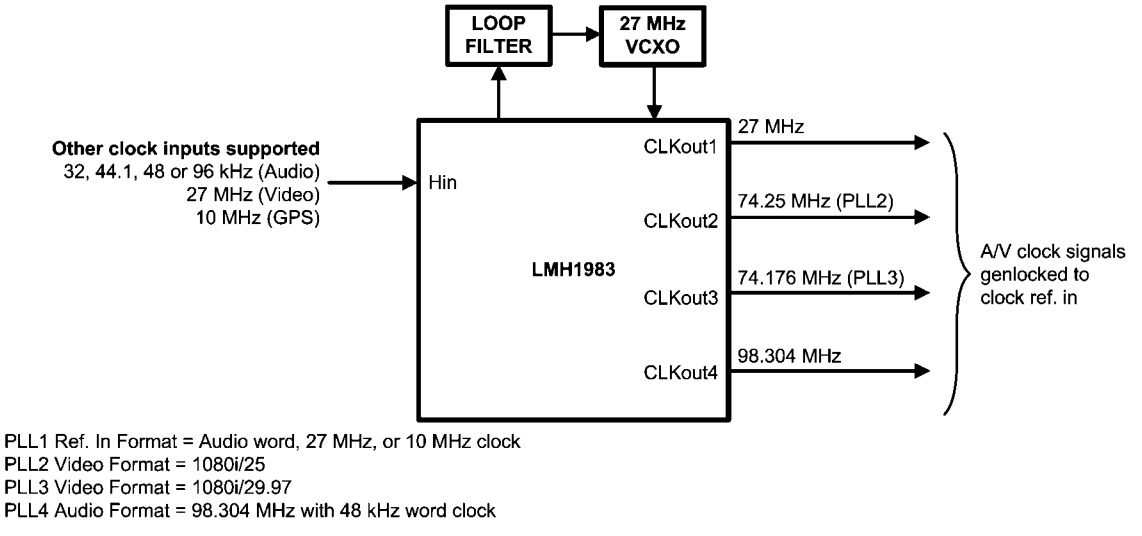
DO remember that VIAs have significant inductance — when using a via to connect to a power supply or ground layer, two in parallel will reduce the inductance over a singe VIA.

DO connect the pad on the bottom of the package to a solid ground connection. This contact is used as a major ground connection as well as providing a thermal conduit which helps to maintain a constant die temperature.



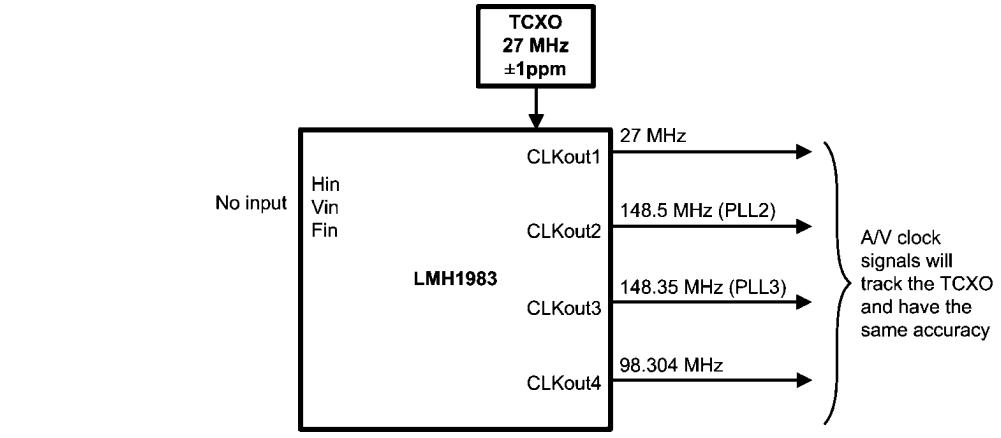
30085140

3G, 3G/1.001, and Audio Clock Generation for SD to HD SDI Upconversion with audio embed/disembed



30085141

A/V Clock Generation using a Recognized Clock-based Input reference

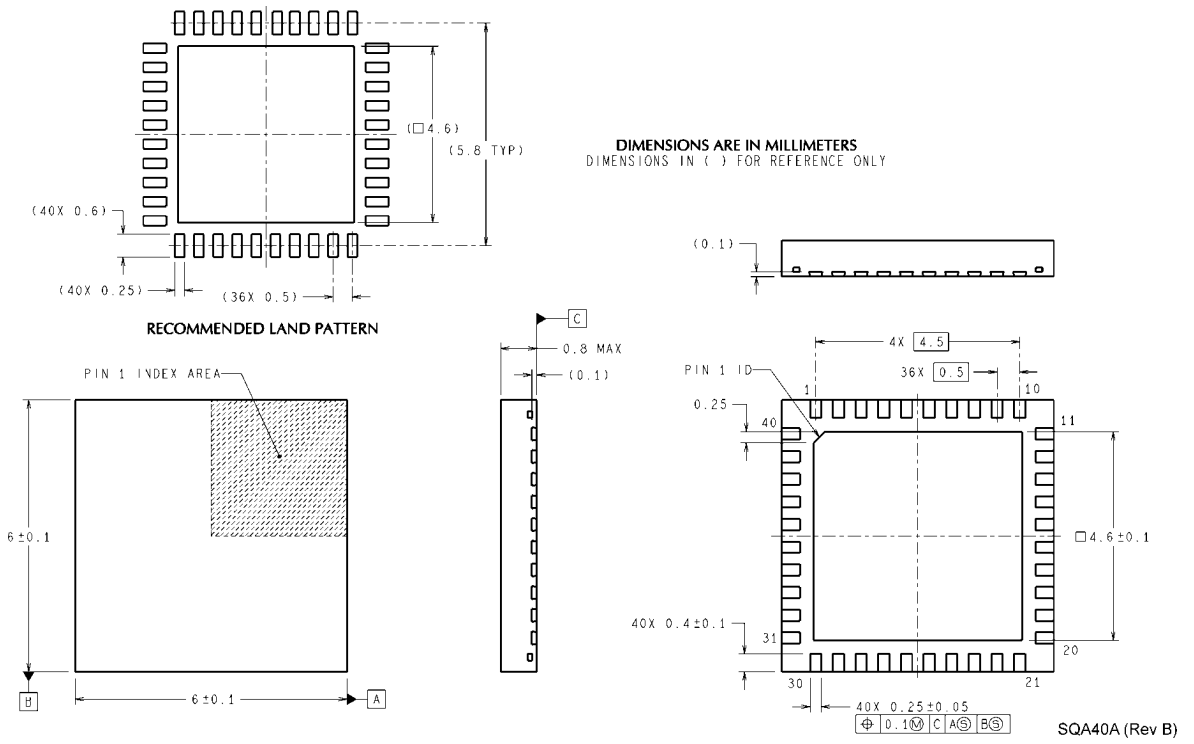


PLL1 Mode = Free run
PLL2 Video Format = 1080p/50
PLL3 Video Format = 1080p/59.94
PLL4 Audio Format = 98.304 MHz with 48 kHz word clock

30085143

High-Precision, Stable A/V clock generation using a 27MHz TCXO Reference

Physical Dimensions inches (millimeters) unless otherwise noted



40-Pin LLP
NS Package Number SQA40A

Notes

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LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
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