

GENERAL-PURPOSE LOW-VOLTAGE COMPARATORS

FEATURES

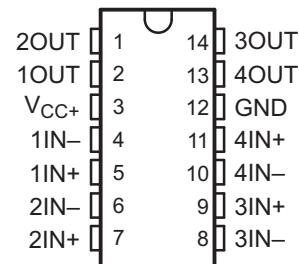
- **2.7-V and 5-V Performance**
- **Low Supply Current**
 - LMV331 . . . 130 μ A Typ
 - LMV393 . . . 210 μ A Typ
 - LMV339 . . . 410 μ A Typ
- **Input Common-Mode Voltage Range Includes Ground**
- **Low Output Saturation Voltage 200 mV Typical**
- **Open-Collector Output for Maximum Flexibility**

DESCRIPTION/ ORDERING INFORMATION

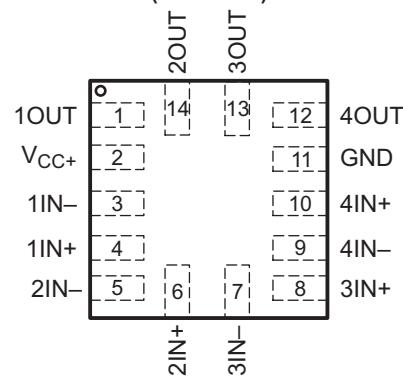
The LMV393 and LMV339 devices are low-voltage (2.7 V to 5.5 V) versions of the dual and quad comparators, LM393 and LM339, which operate from 5 V to 30 V. The LMV331 is the single-comparator version.

The LMV331, LMV339, and LMV393 are the most cost-effective solutions for applications where low-voltage operation, low power, space saving, and price are the primary specifications in circuit design for portable consumer products. These devices offer specifications that meet or exceed the familiar LM339 and LM393 devices at a fraction of the supply current.

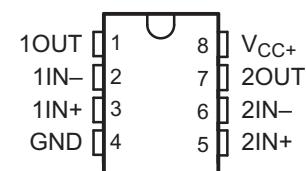
**LMV339 . . . D OR PW PACKAGE
(TOP VIEW)**



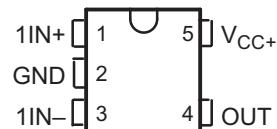
**LMV339 . . . RUC PACKAGE
(TOP VIEW)**



**LMV393 . . . D, DDU, DGK OR PW PACKAGE
(TOP VIEW)**



**LMV331 . . . DBV OR DCK PACKAGE
(TOP VIEW)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

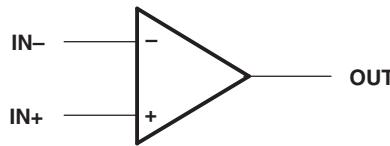
T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER		TOP-SIDE MARKING ⁽³⁾
–40°C to 85°C	Single	SC-70 – DCK	Reel of 3000	LMV331IDCKR	R2_
			Reel of 250	LMV331IDCKT	
	SOT23-5 – DBV	Reel of 3000	LMV331IDBVR	R1I_	
			Reel of 250	LMV331IDBVT	
	Dual	MSOP/VSSOP – DGK	Reel of 2500	LMV338IDGKR	R9_
		SOIC – D	Tube of 75	LMV393ID	MV393I
			Reel of 2500	LMV393IDR	
		TSSOP – PW	Tube of 90	LMV393IPW	MV393I
			Reel of 2000	LMV393IPWR	
	Quad	VSSOP – DDU	Reel of 3000	LMV393IDDUR	RABR
		SOIC – D	Tube of 50	LMV339ID	LM339I
			Reel of 2500	LMV339IDR	
		TSSOP – PW	Tube of 150	LMV339IPW	MV339I
			Reel of 2000	LMV339IPWR	
		μQFN – RUC	Reel of 3000	LMV339IRUCR	RT

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

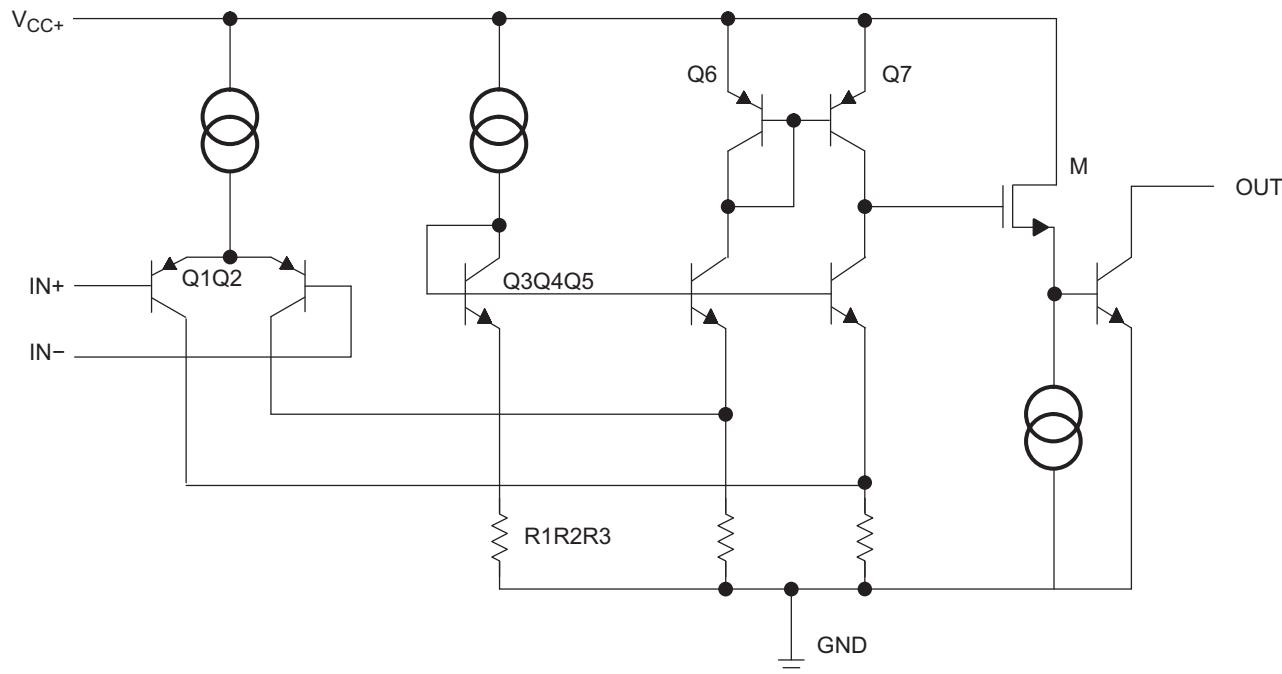
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) DBV/DCK/DGK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

SYMBOL (EACH COMPARATOR)



LMV324 SIMPLIFIED SCHEMATIC



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽²⁾			5.5	V
V_{ID}	Differential input voltage ⁽³⁾			± 5.5	V
V_I	Input voltage range (either input)		0	5.5	V
	Duration of output short circuit (one amplifier) to ground ⁽⁴⁾	At or below $T_A = 25^\circ\text{C}$, $V_{CC} \leq 5.5 \text{ V}$		Unlimited	
θ_{JA}	Package thermal impedance ^{(5) (6)}	D package	8 pin	97	°C/W
			14 pin	86	
		DBV package		206	
		DCK package		252	
		DDU package		TBD	
		RUC package		TBD	
		DGK package		172	
		PW package	8 pin	149	
			14 pin	113	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
- (5) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage (single-supply operation)		2.7	5.5	V
V_{OUT}	Output voltage			$V_{CC} + 0.3$	V
T_A	Operating free-air temperature	I temperature	-40	85	°C

Electrical Characteristics

$V_{CC+} = 2.7$ V, GND = 0 V, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	25°C		1.7	7	mV
α_{VIO}	Average temperature coefficient of input offset voltage	–40°C to 85°C		5		$\mu\text{V}/^\circ\text{C}$
I_{IB}	Input bias current	25°C		15	250	nA
		–40°C to 85°C		400		
I_{IO}	Input offset current	25°C		5	50	nA
		–40°C to 85°C		150		
I_O	Output current (sinking)	$V_O \leq 1.5$ V	25°C	5	23	mA
	Output Leakage Current	25°C		0.003		μA
		–40°C to 85°C		1		
V_{ICR}	Common-mode input voltage range	25°C		–0.1 to 2		V
V_{SAT}	Saturation voltage	$I_O \leq 1.5$ mA	25°C	200		mV
I_{CC}	LMV331	25°C		40	100	μA
	LMV393 (both comparators)	25°C		70	140	
	LMV339 (all four comparators)	25°C		140	200	

Switching Characteristics

$T_A = 25^\circ\text{C}$, $V_{CC+} = 2.7$ V, $R_L = 5.1$ k Ω , GND = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
t_{PHL}	Propagation delay high to low level output switching Input overdrive = 10 mV	1000	ns
	Input overdrive = 100 mV	350	
t_{PLH}	Propagation delay low to high level output switching Input overdrive = 10 mV	500	ns
	Input overdrive = 100 mV	400	

Electrical Characteristics

$V_{CC+} = 5 \text{ V}$, $\text{GND} = 0 \text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage		25°C		1.7	7	mV
		–40°C to 85°C			9	
α_{VIO} Average temperature coefficient of input offset voltage		25°C		5		$\mu\text{V}/^\circ\text{C}$
I_{IB} Input bias current		25°C		25	250	nA
		–40°C to 85°C			400	
I_{IO} Input offset current		25°C		2	50	nA
		–40°C to 85°C			150	
I_O Output current (sinking)	$V_O \leq 1.5 \text{ V}$	25°C	10	84		mA
Output Leakage Current		25°C		0.003		μA
		–40°C to 85°C			1	
V_{ICR} Common-mode input voltage range		25°C		–0.1 to 4.2		V
A_{VD} Large-signal differential voltage gain		25°C	20	50		V/mV
V_{SAT} Saturation voltage	$I_O \leq 4 \text{ mA}$	25°C		200	400	mV
		–40°C to 85°C			700	
I_{CC} Supply current	LMV331	25°C		60	120	μA
		–40°C to 85°C			150	
	LMV393 (both comparators)	25°C		100	200	
		–40°C to 85°C			250	
	LMV339 (all four comparators)	25°C		170	300	
		–40°C to 85°C			350	

Switching Characteristics

$T_A = 25^\circ\text{C}$, $V_{CC+} = 5 \text{ V}$, $R_L = 5.1 \text{ k}\Omega$, $\text{GND} = 0 \text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
t_{PHL} Propagation delay high to low level output switching	Input overdrive = 10 mV	600	ns
	Input overdrive = 100 mV	200	
t_{PLH} Propagation delay low to high level output switching	Input overdrive = 10 mV	450	ns
	Input overdrive = 100 mV	300	

REVISION HISTORY

Changes from Revision M (November 2005) to Revision N	Page
• Changed document format from Quicksilver to DocZone.	1
• Added RUC package pin out and RUC package ordering information.	1

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
LMV331IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV331IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV331IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV331IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV331IDBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV331IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV331IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV331IDCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV331IDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV331IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV331IDCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV331IDCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV339ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV339IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV339IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV339IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV339IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
LMV339IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV339IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV339IPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV339IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV339IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV339IPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV339IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV339IRUCR	ACTIVE	QFN	RUC	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IDDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IDDURE4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IDDURG4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
LMV393IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV393IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

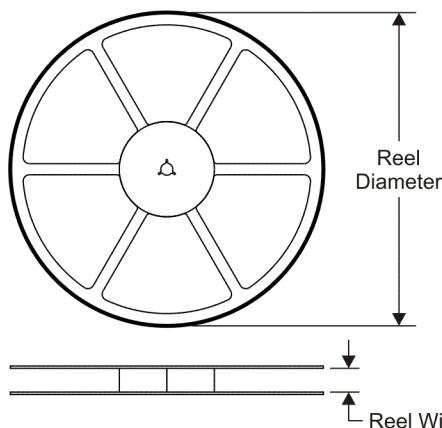
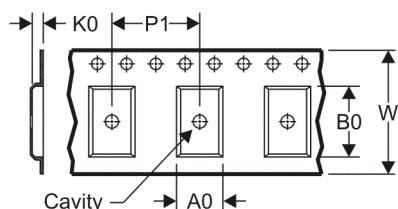
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV331, LMV393 :

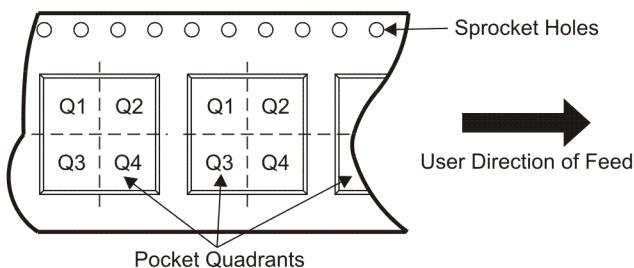
- Automotive: [LMV331-Q1](#), [LMV393-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV331IDBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
LMV331IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV331IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV331IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV331IDCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
LMV331IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV331IDCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
LMV339IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV339IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV339IRUCR	QFN	RUC	14	3000	180.0	8.4	2.3	2.3	0.55	4.0	8.0	Q2
LMV393IDDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LMV393IDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV393IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV393IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

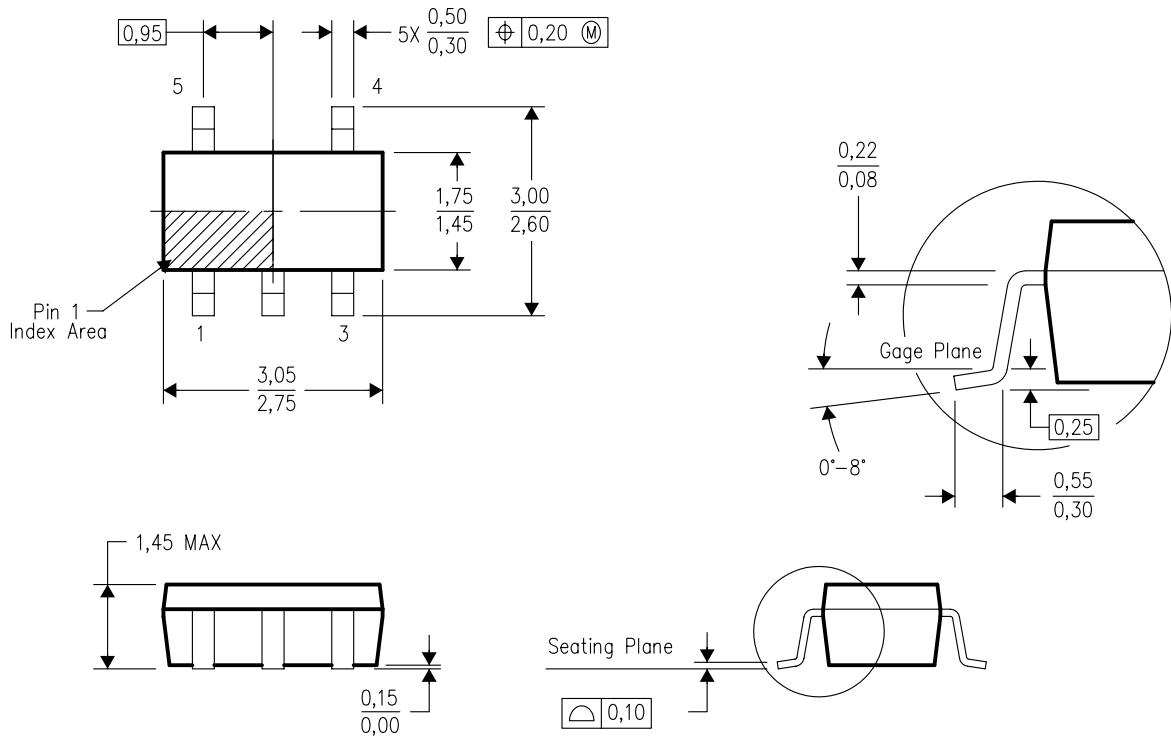
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV331IDBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
LMV331IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LMV331IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LMV331IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LMV331IDCKR	SC70	DCK	5	3000	205.0	200.0	33.0
LMV331IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
LMV331IDCKT	SC70	DCK	5	250	205.0	200.0	33.0
LMV339IDR	SOIC	D	14	2500	346.0	346.0	33.0
LMV339IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
LMV339IRUCR	QFN	RUC	14	3000	202.0	201.0	28.0
LMV393IDDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
LMV393IDGKR	MSOP	DGK	8	2500	358.0	335.0	35.0
LMV393IDR	SOIC	D	8	2500	340.5	338.1	20.6
LMV393IPWR	TSSOP	PW	8	2000	346.0	346.0	29.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/K 03/2006

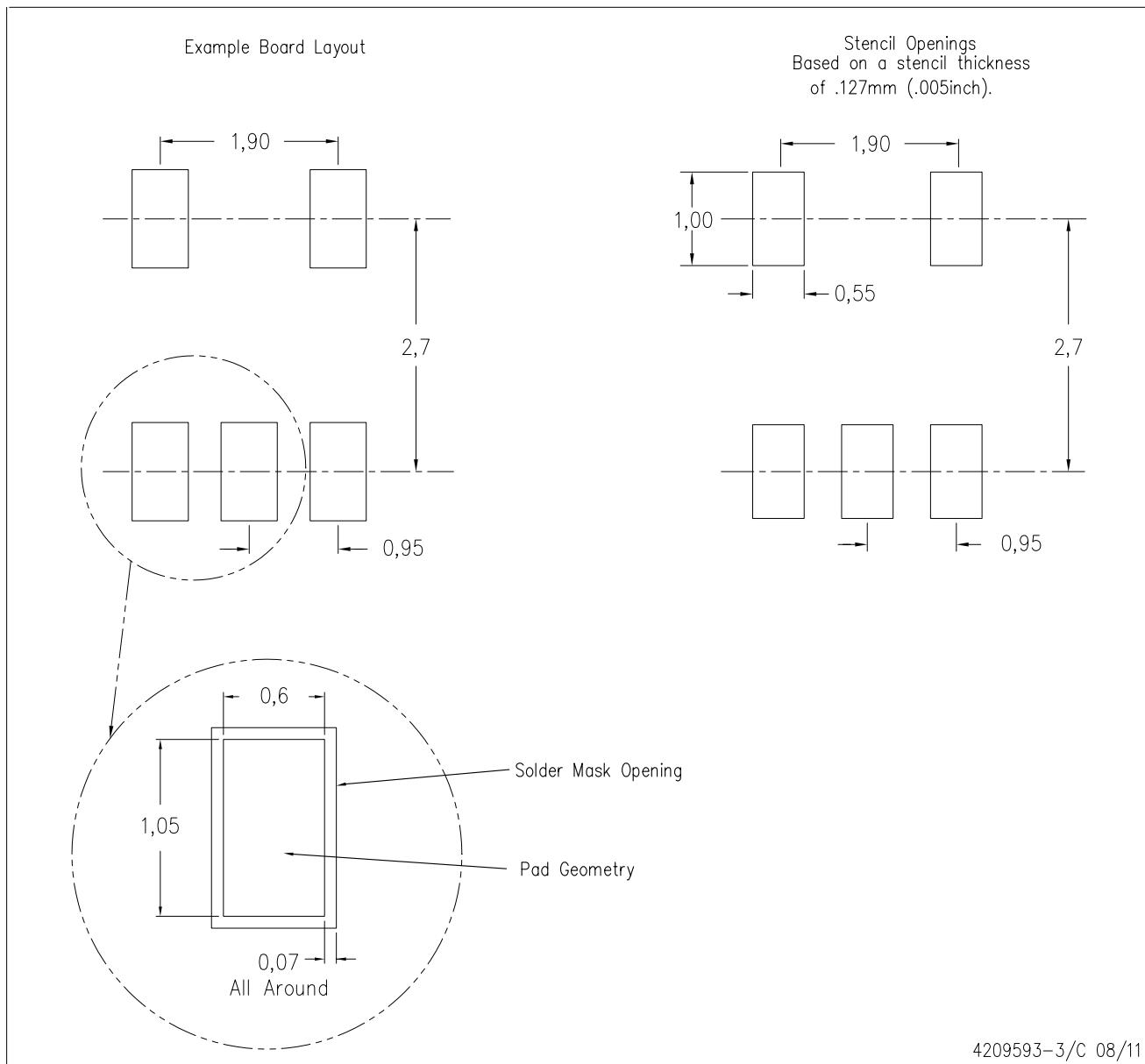
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0,15 per side.
- Falls within JEDEC MO-178 Variation AA.

LAND PATTERN DATA

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE

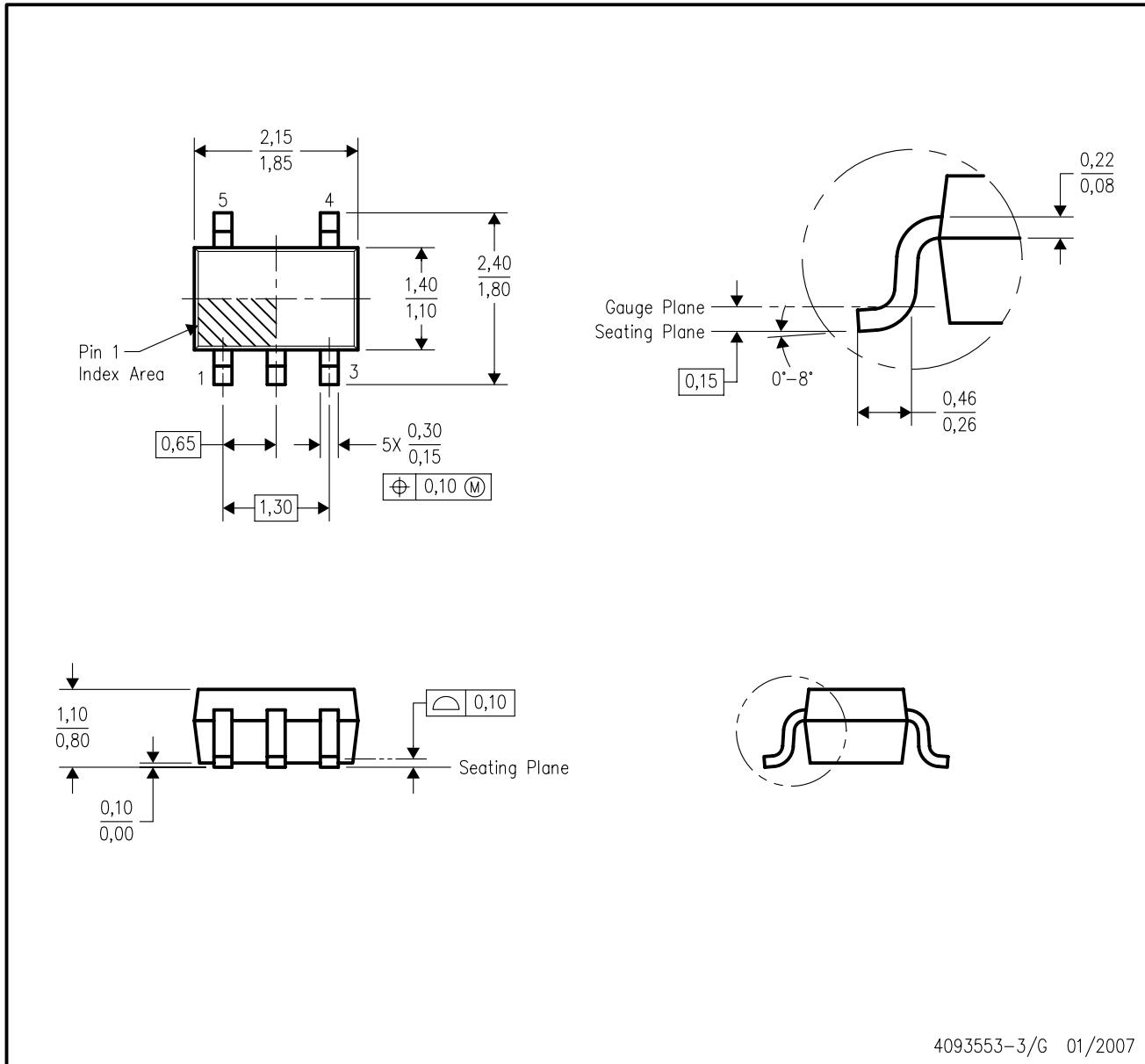


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES:

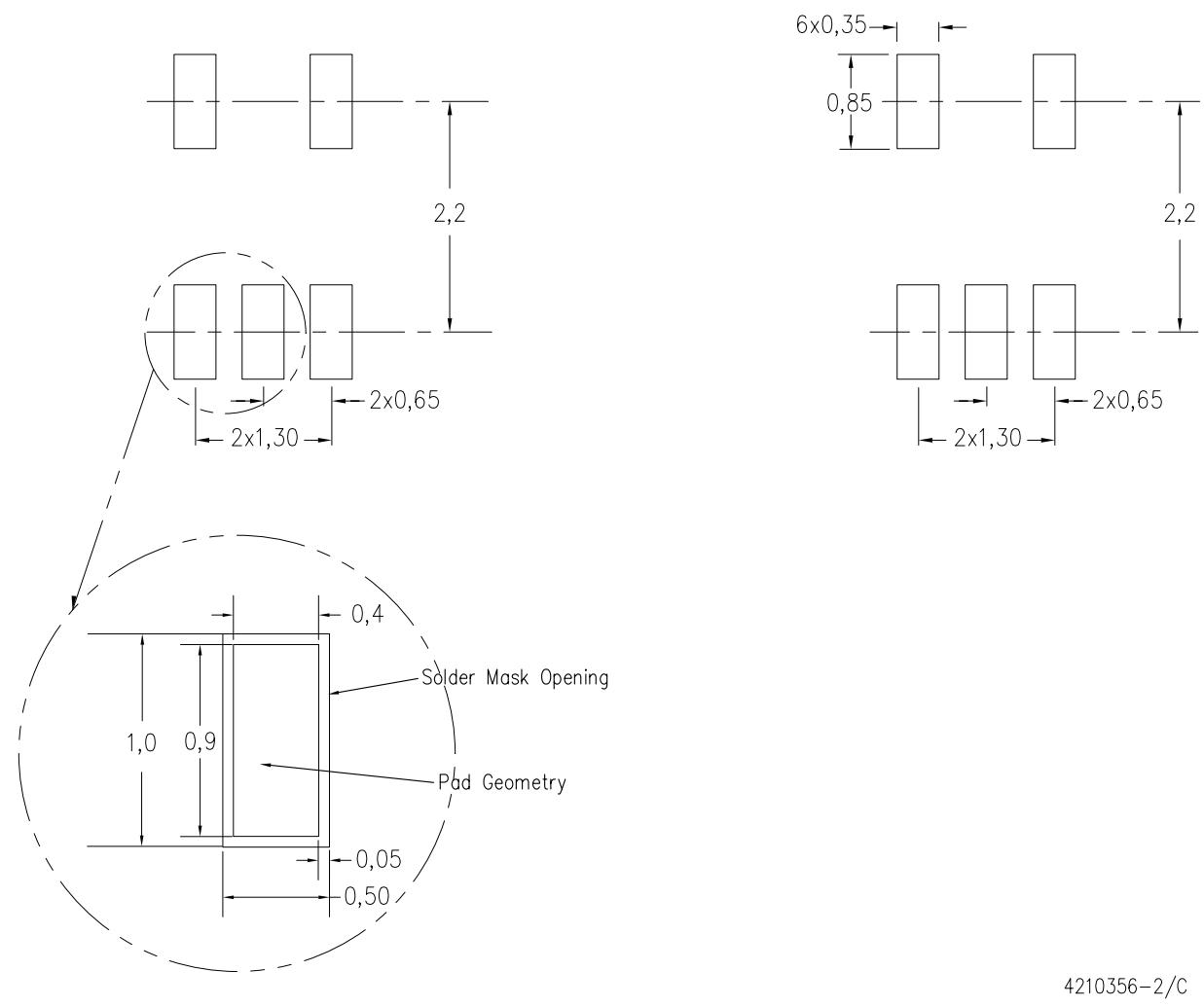
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

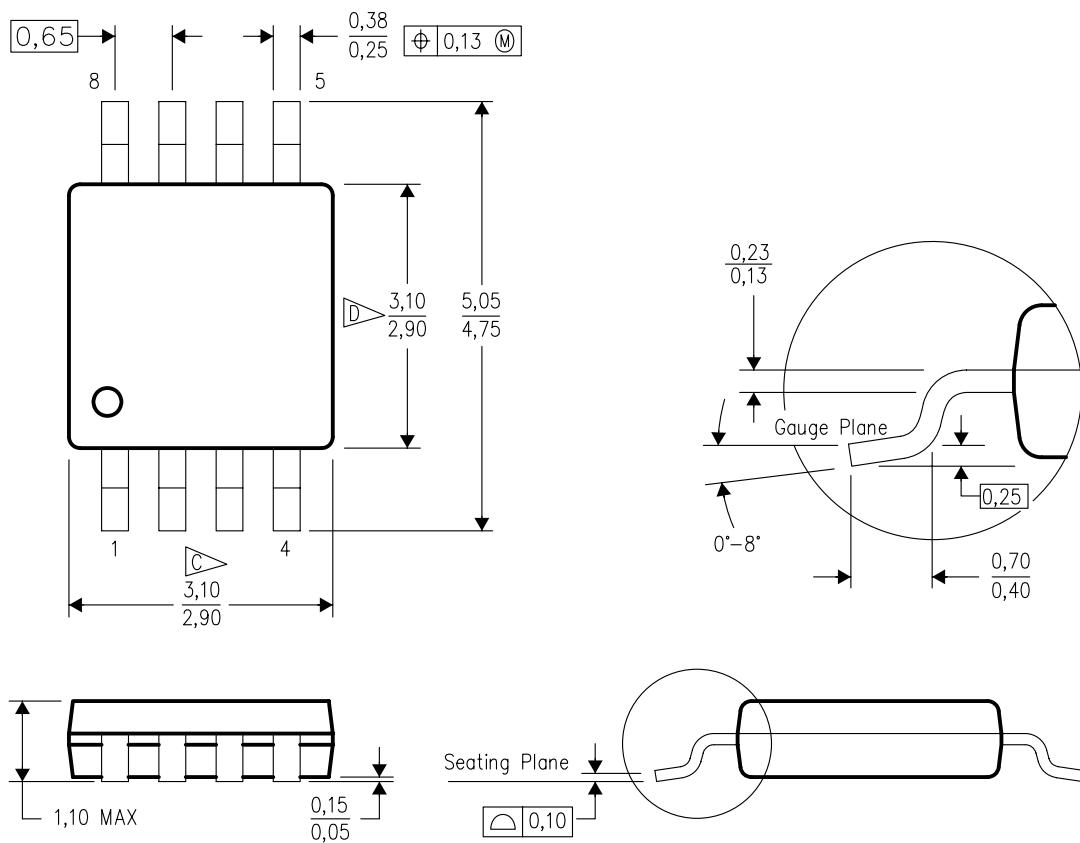


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

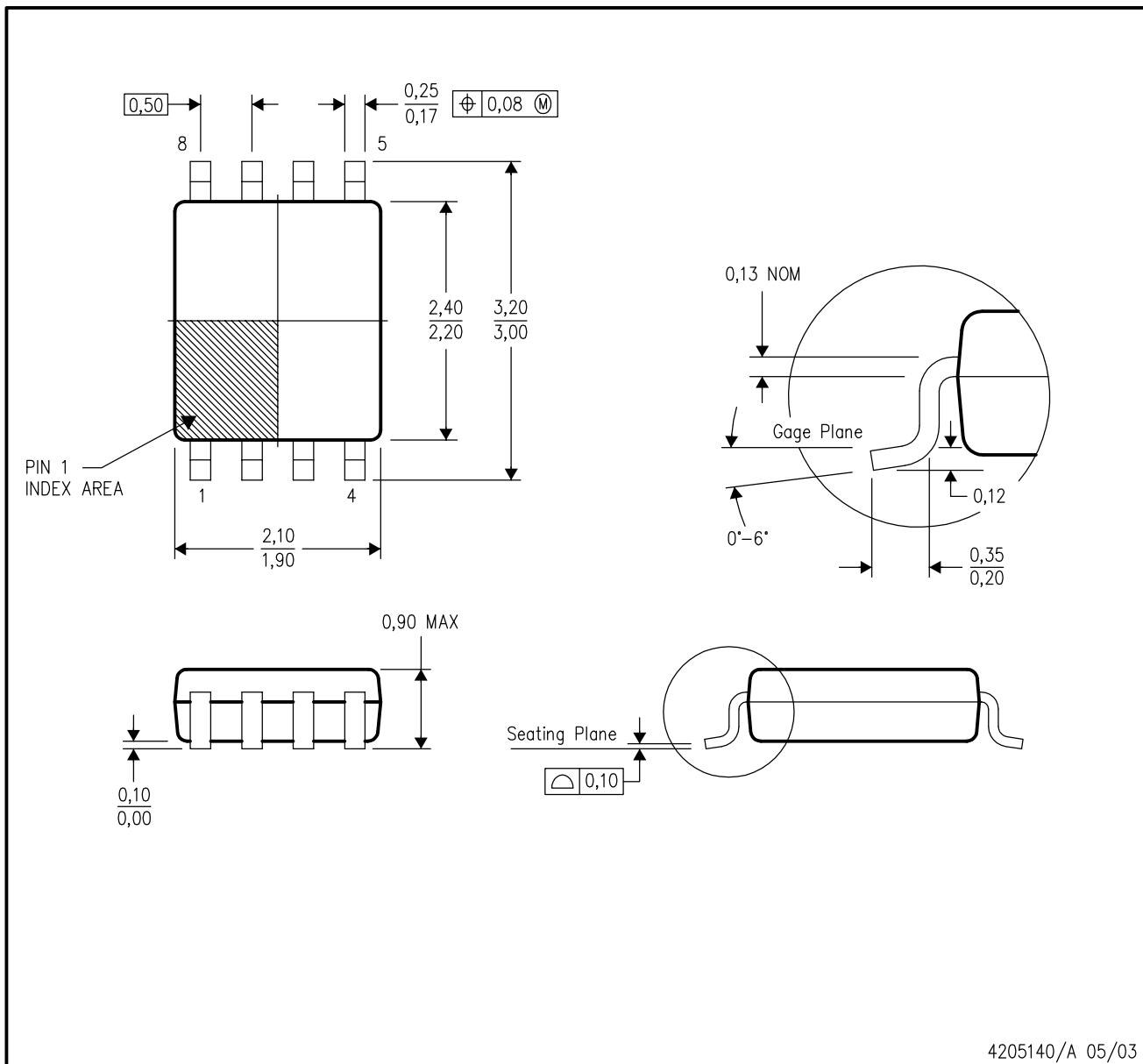
 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

 Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DDU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



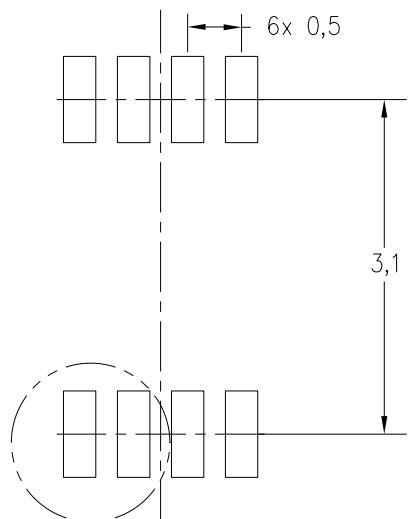
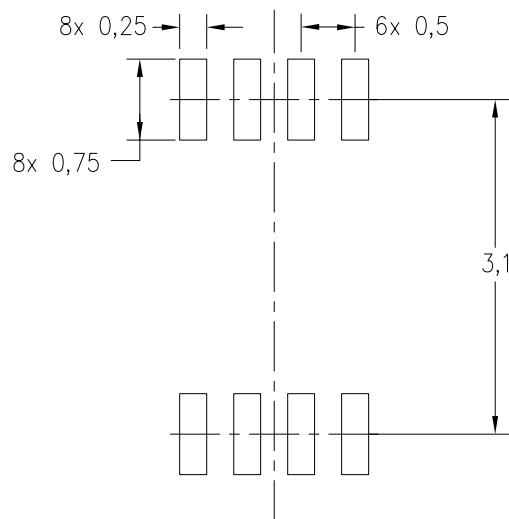
4205140/A 05/03

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion.
- Falls within JEDEC MO-187 variation CA.

DDU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE UP)

Example Board Layout
(Note C,E)Example Stencil Design
(Note D)

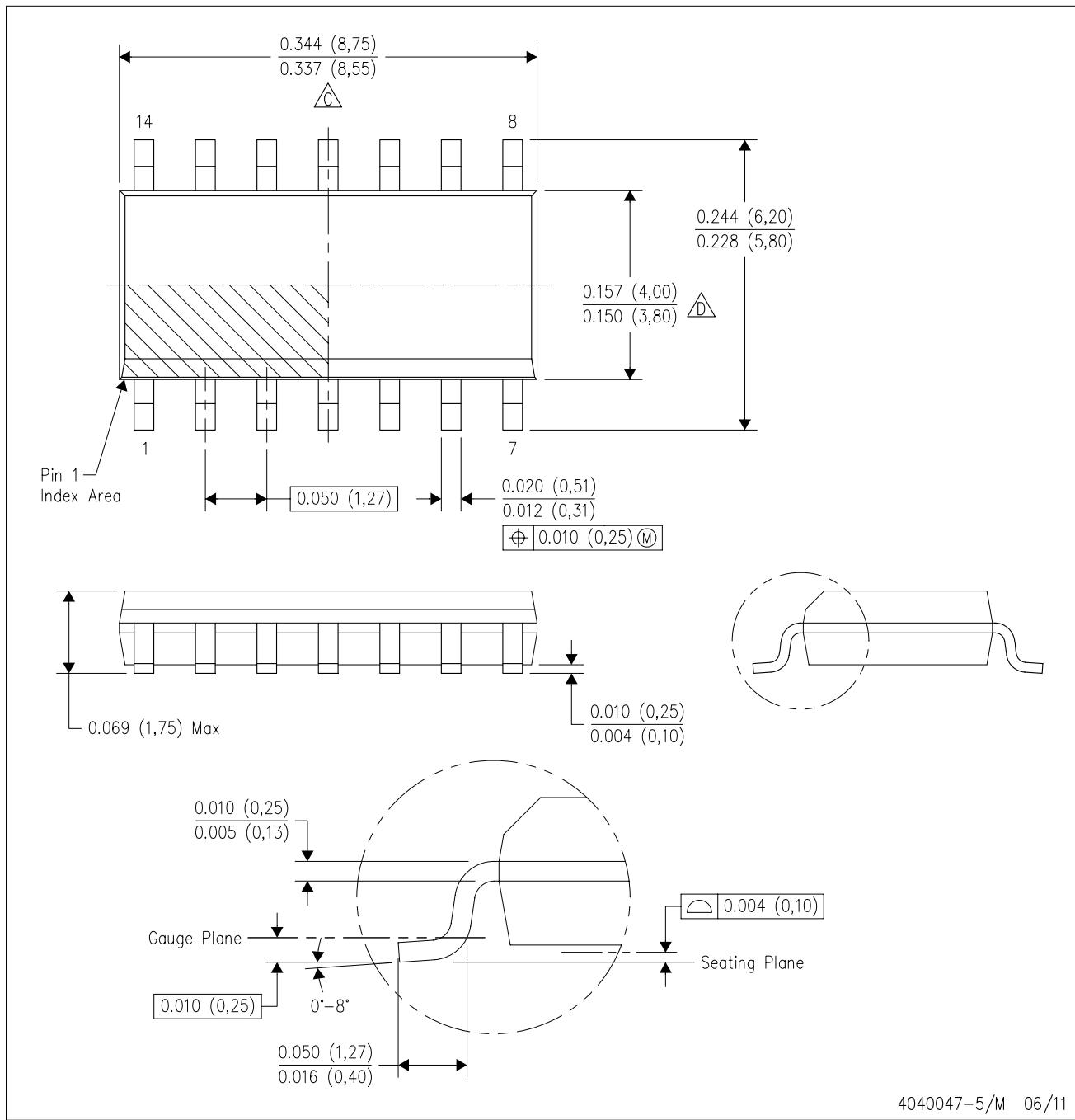
4211035/A 05/10

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

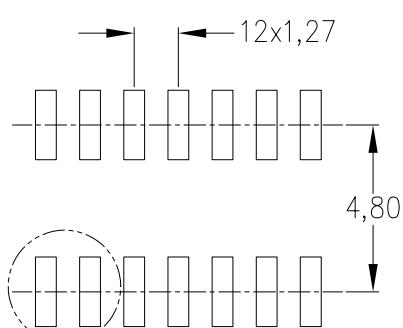
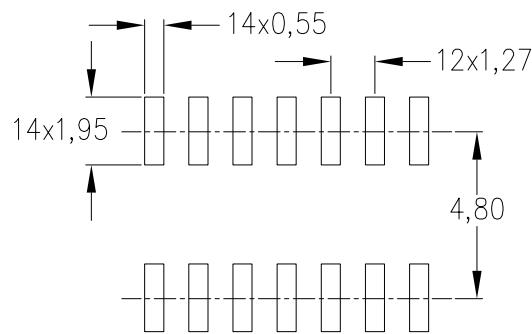
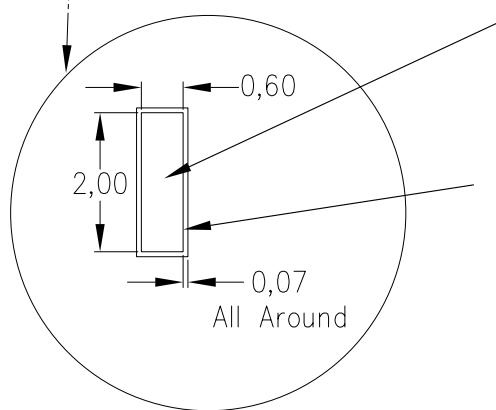
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

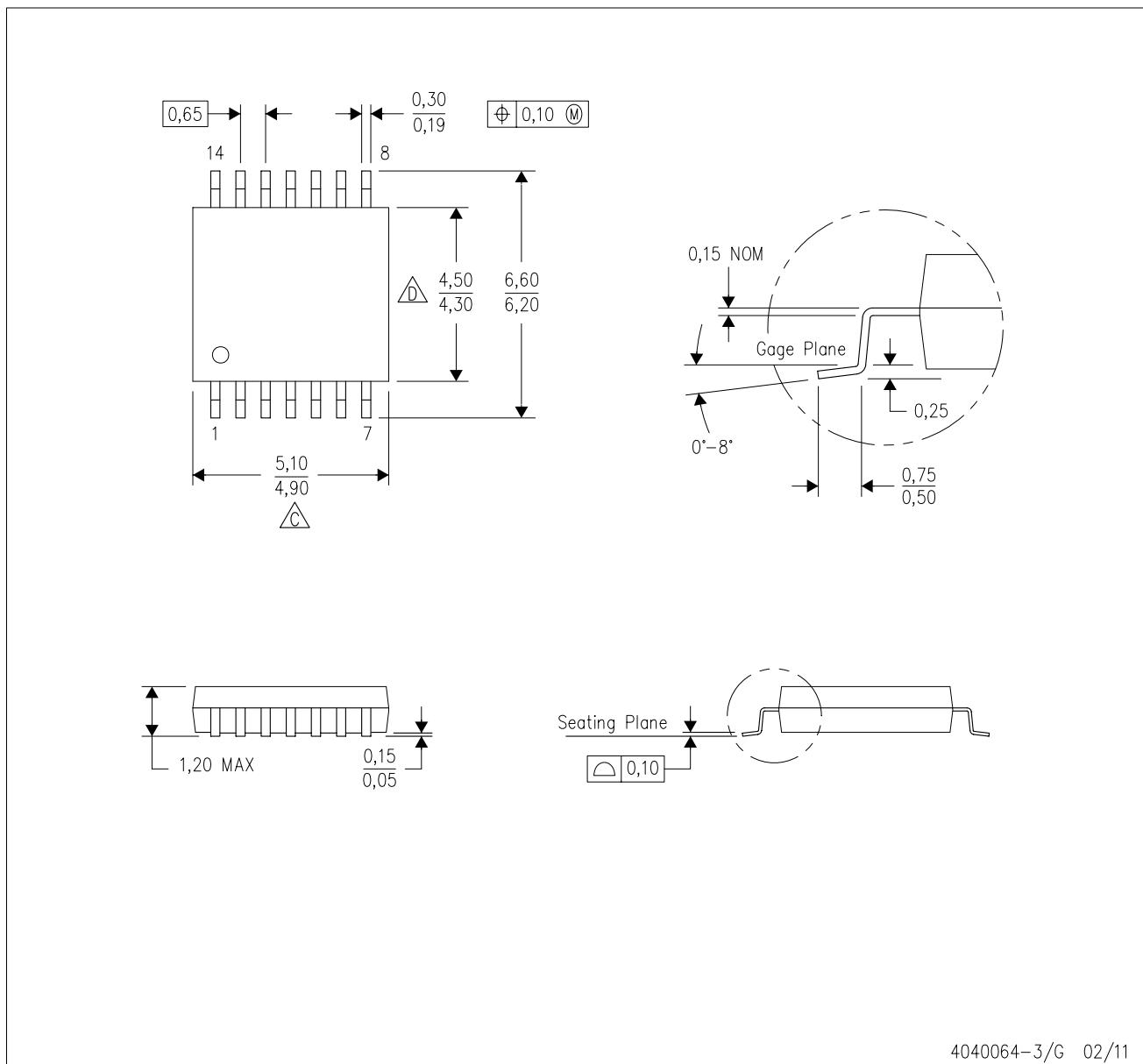
4211283-3/D 06/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

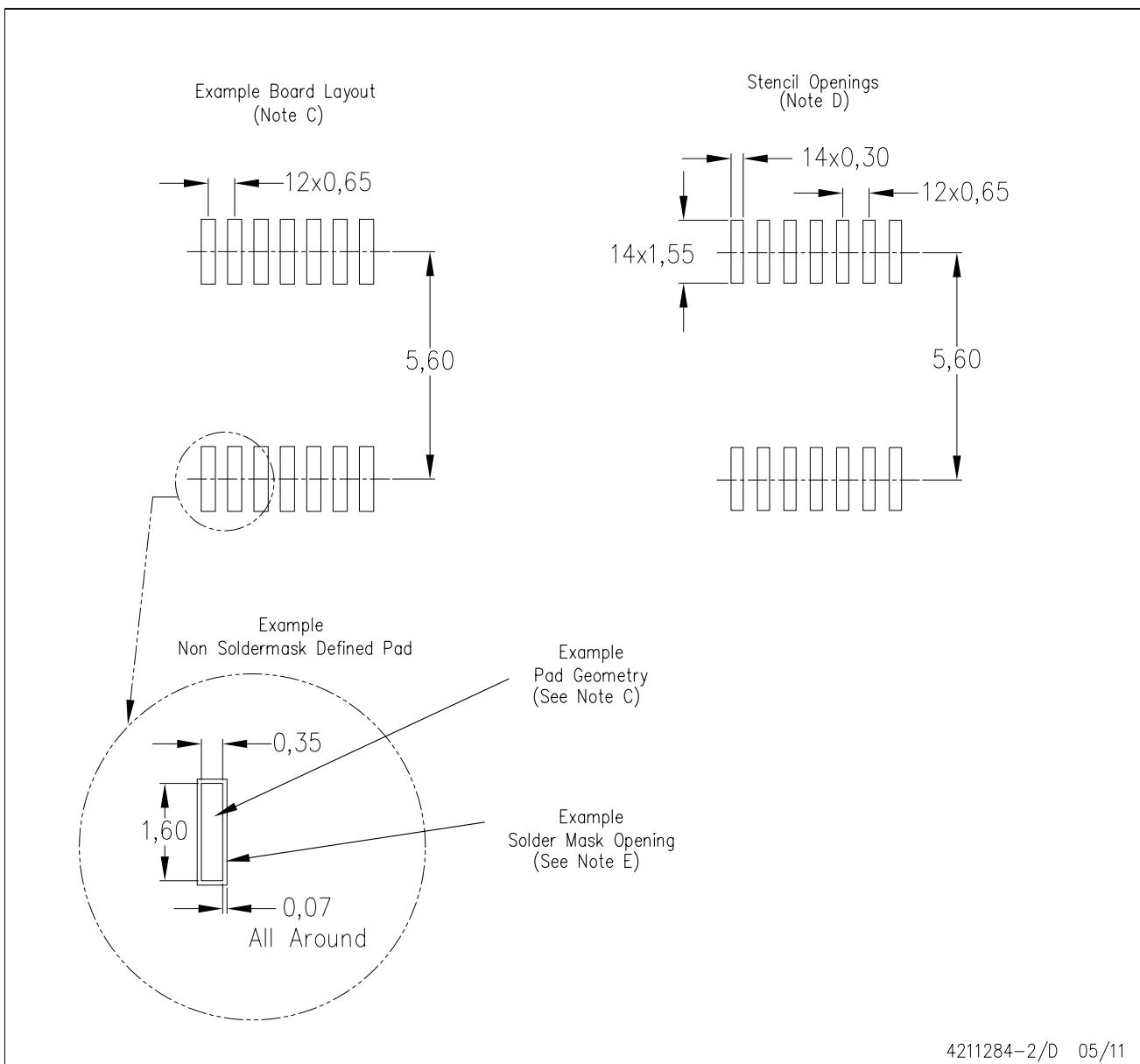
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



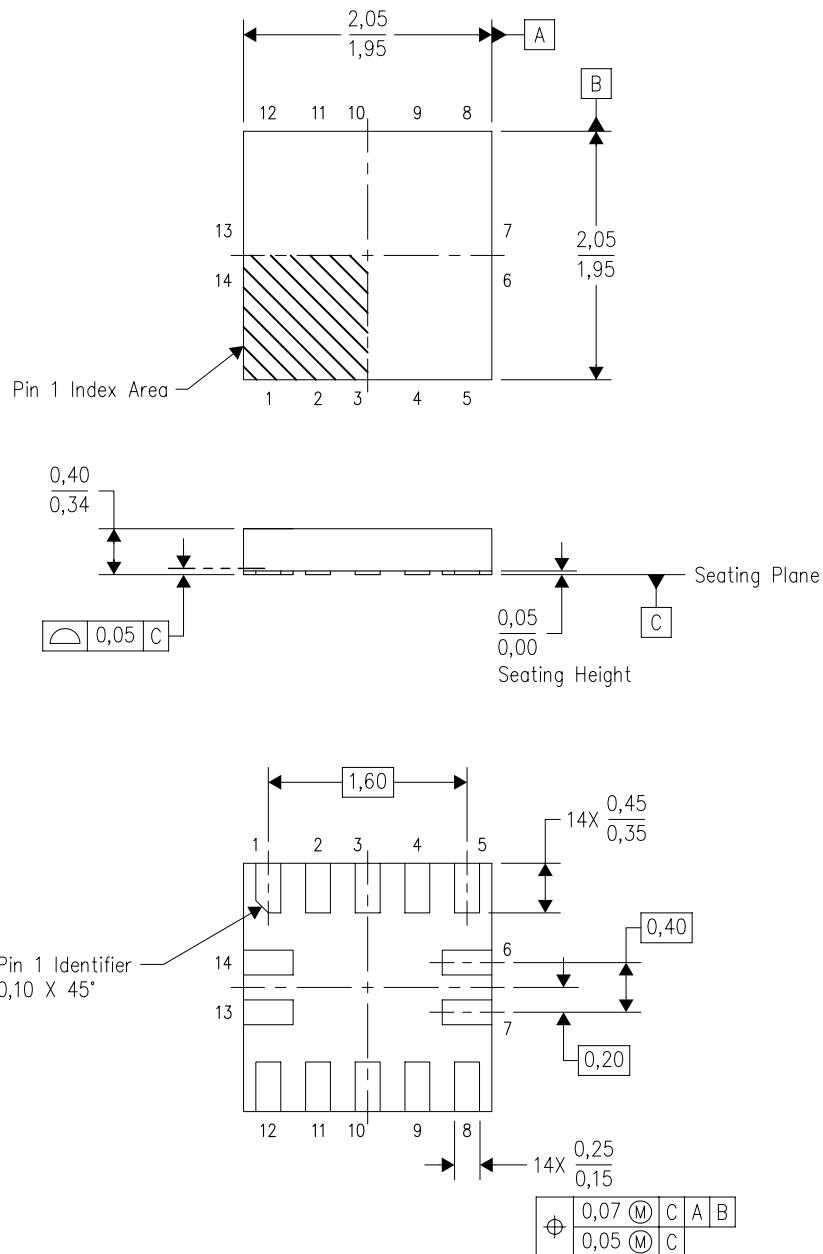
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

RUC (S-PX2QFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

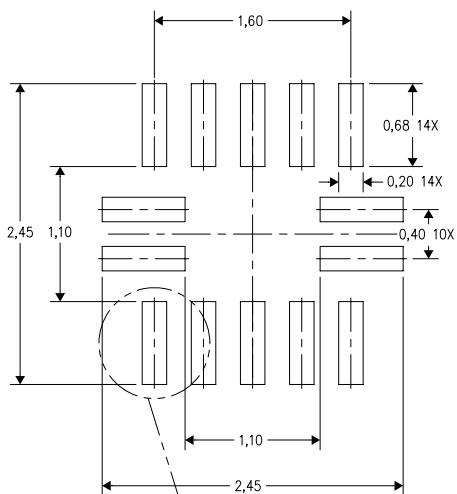
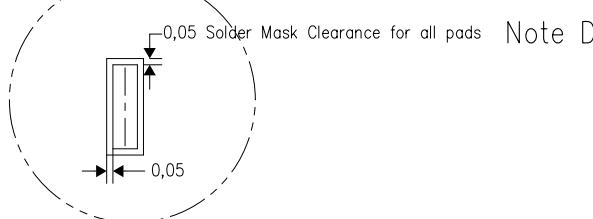
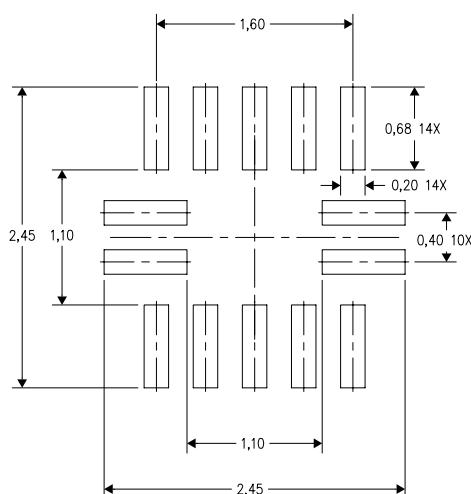
4208447/C 08/2008

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-lead) package configuration.
D. This package complies to JEDEC MO-288 variation X2GFE.

RUC (S-PX2QFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

Example Board Layout

Example Stencil Design
(Note E)

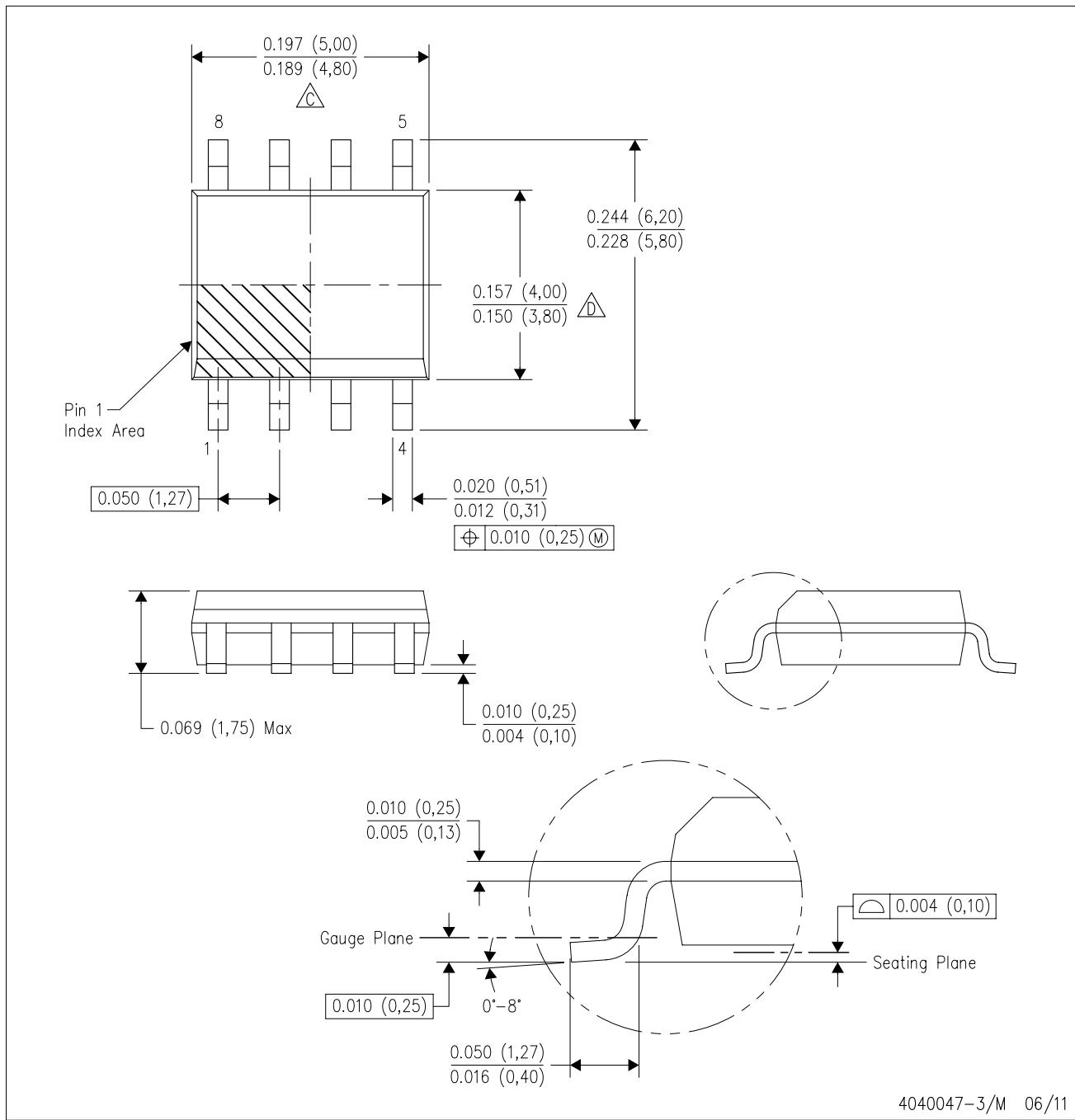
4211124/A 06/10

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Side aperture dimensions over-print land for acceptable area ratio > 0.66 . Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

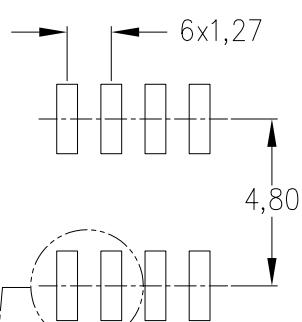
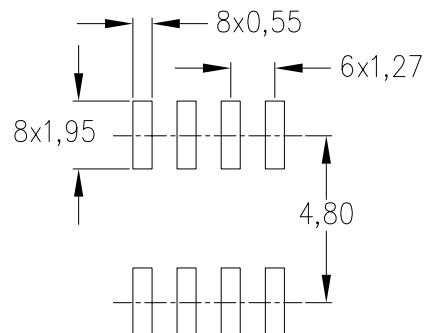
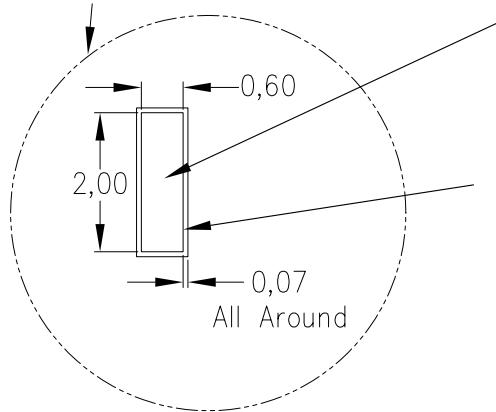
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

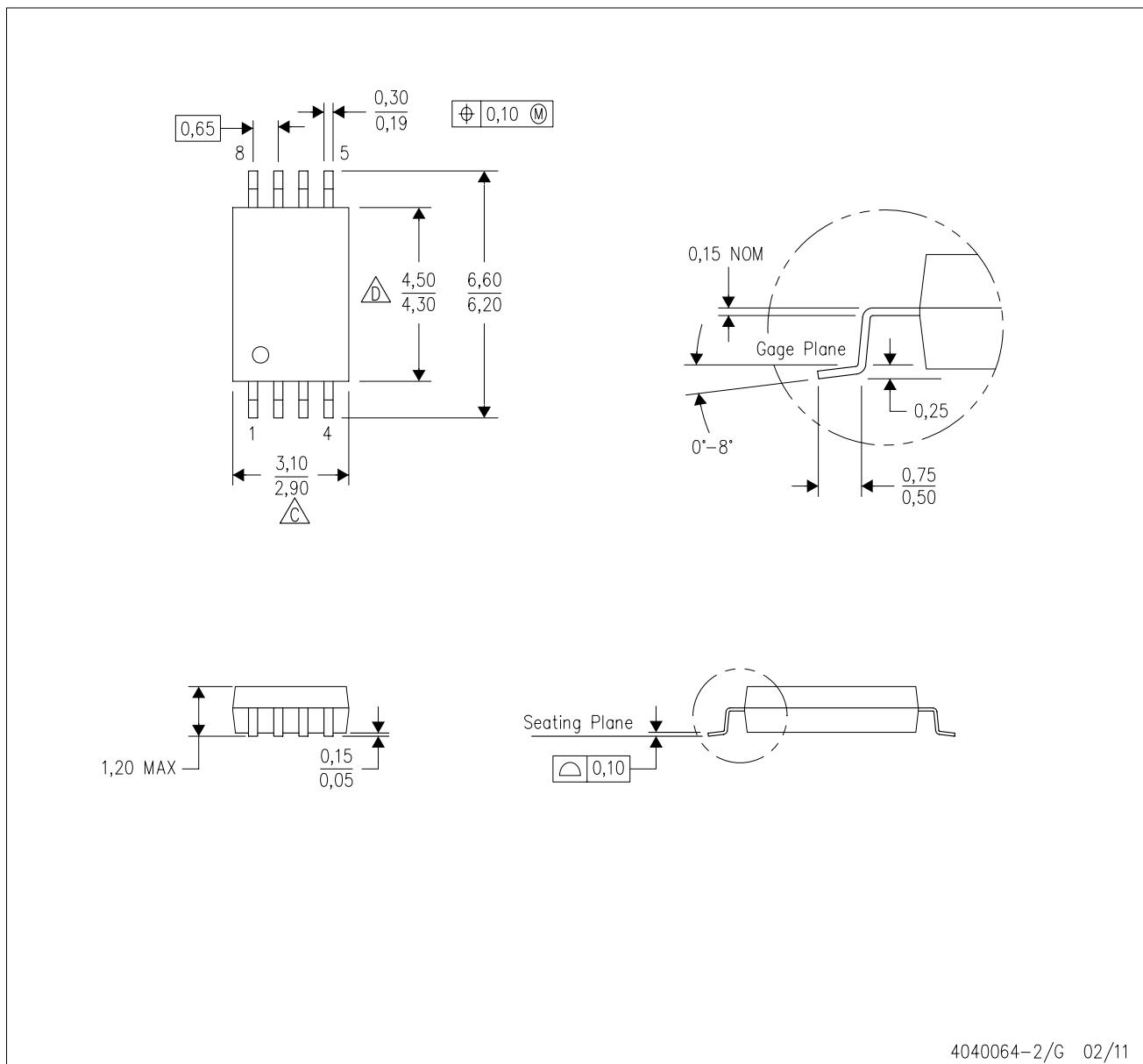
4211283-2/D 06/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

 D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

4040064-2/G 02/11

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