LMV341-N/LMV342-N/LMV344-N Single with Shutdown/Dual/Quad General Purpose, 2.7V, Rail-to-Rail Output, 125°C, Operational Amplifiers

Check for Samples: LMV341-N, LMV342-N, LMV344-N

FEATURES

(Typical 2.7V Supply Values; Unless Otherwise Noted)

- **Ensured 2.7V and 5V Specifications**
- **Input Referred Voltage Noise (@ 10kHz) 29nV/$\sqrt{Hz}$**
- **Supply Current (per Amplifier) 100µA**
- **Gain Bandwidth Product 1.0MHz**
- **Slew Rate 1.0V/µs**
- **Shutdown Current (LMV341-N) 45pA**
- **Turn-On Time from Shutdown (LMV341-N) 5µs**
- **Input Bias Current 20fA**

APPLICATIONS

- **Cordless/Cellular Phones**
- **Laptops**
- **PDAs**
- **PCMCIA/Audio**
- **Portable/Battery-Powered Electronic Equipment**
- **Supply Current Monitoring**
- **Battery Monitoring**
- **Buffer**
- **Filter**
- **Driver**

DESCRIPTION

The LMV341-N/LMV342-N/LMV344-N are single, dual, and quad low voltage, low power Operational Amplifiers. They are designed specifically for low voltage portable applications. Other important product characteristics are low input bias current, rail-to-rail output, and wide temperature range.

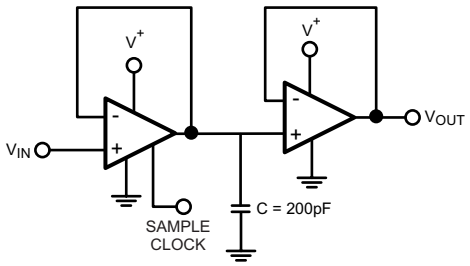
The patented class AB turnaround stage significantly reduces the noise at higher frequencies, power consumption, and offset voltage. The PMOS input stage provides the user with ultra-low input bias current of 20fA (typical) and high input impedance.

The industrial-plus temperature range of −40°C to 125°C allows the LMV341-N/LMV342-N/LMV344-N to accommodate a broad range of extended environment applications. LMV341-N expands Texas Instrument's Silicon Dust amplifier portfolio offering enhancements in size, speed, and power savings. The LMV341-N/LMV342-N/LMV344-N are specified to operate over the voltage range of 2.7V to 5.5V and all have rail-to-rail output.

The LMV341-N offers a shutdown pin that can be used to disable the device. Once in shutdown mode, the supply current is reduced to 45pA (typical). The LMV341-N/LMV342-N/LMV344-N have 29nV Voltage Noise at 10KHz, 1MHz GBW, 1.0V/µs Slew Rate, 0.25mVos, and 0.1µA shutdown current (LMV341-N.)

The LMV341-N is offered in the tiny 6-Pin SC70 package, the LMV342-N in space saving 8-Pin VSSOP and SOIC, and the LMV344-N in 14-Pin TSSOP and SOIC. These small package amplifiers offer an ideal solution for applications requiring minimum PC board footprint. Applications with area constrained PC board requirements include portable electronics such as cellular handsets and PDAs.

Sample and Hold Circuit



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Machine Model	200V
	Human Body Model	2000V
Differential Input Voltage		± Supply Voltage
Supply Voltage (V^+ -V^-)		6.0V
Output Short Circuit to V^+		See(4)
Output Short Circuit to V^-		See(5)
Storage Temperature Range		−65°C to 150°C
Junction Temperature(6)		150°C
Mounting Temperature	Infrared or Convection Reflow (20 sec.)	235°C
	Wave Soldering Lead Temperature (10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) Shorting output to V^+ will adversely affect reliability.
(5) Shorting output to V^- will adversely affect reliability.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings(1)

Supply Voltage		2.7V to 5.5V
Temperature Range		−40°C to 125°C
Thermal Resistance (θ_{JA})	6-Pin SC70	414°C/W
	8-Pin SOIC	190°C/W
	8-Pin VSSOP	235°C/W
	14-Pin TSSOP	155°C/W
	14-Pin SOIC	145°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

2.7V DC Electrical Characteristics(1)

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	LMV341-N		0.25	4 **4.5**	mV
		LMV342-N/LMV344-N		0.55	5 **5.5**	
TCV_{OS}	Input Offset Voltage Average Drift			1.7		µV/°C
I_B	Input Bias Current			0.02	120 **250**	pA
I_{OS}	Input Offset Current			6.6		fA
I_S	Supply Current	Per Amplifier		100	170 **230**	µA
		Shutdown Mode, V_{SD} = 0V (LMV341-N)		45pA	1µA **1.5µA**	
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.7V 0V ≤ V_{CM} ≤ 1.6V	56 **50**	80		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V	65 **60**	82		dB
V_{CM}	Input Common Mode Voltage	For CMRR ≥ 50dB	0	−0.2 to 1.9 (Range)	1.7	V
A_V	Large Signal Voltage Gain	R_L = 10kΩ to 1.35V	78 **70**	113		dB
		R_L = 2kΩ to 1.35V	72 **64**	103		
V_O	Output Swing	R_L = 2kΩ to 1.35V		24	60 **95**	mV
			60 **95**	26		
		R_L = 10kΩ to 1.35V		5.0	30 **40**	
			30 **40**	5.3		
I_O	Output Short Circuit Current	Sourcing LMV341-N/LMV342-N	20	32		mA
		Sourcing LMV344-N	18	24		
		Sinking	15	24		
t_{on}	Turn-on Time from Shutdown	(LMV341-N)		5		µs
V_{SD}	Shutdown Pin Voltage Range	ON Mode (LMV341-N)		1.7 to 2.7	2.4 to 2.7	V
		Shutdown Mode (LMV341-N)		0 to 1	0 to 0.8	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

2.7V AC Electrical Characteristics(1)

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
SR	Slew Rate	R_L = 10kΩ(4)		1.0		V/µs
GBW	Gain Bandwidth Product	R_L = 100kΩ, C_L = 200pF		1.0		MHz
Φ_m	Phase Margin	R_L = 100kΩ		72		deg
G_m	Gain Margin	R_L = 100kΩ		20		dB
e_n	Input-Referred Voltage Noise	f = 1kHz		40		nV/√Hz
i_n	Input-Referred Current Noise	f = 1kHz		0.001		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = $1V_{PP}$		0.017		%

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with $2V_{PP}$ step input. Number specified is the slower of the positive and negative slew rates.

5V DC Electrical Characteristics(1)

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	LMV341-N		0.025	4 **4.5**	mV
		LMV342-N/LMV344-N		0.70	5 **5.5**	
TCV_{OS}	Input Offset Voltage Average Drift			1.9		µV/°C
I_B	Input Bias Current			0.02	200 **375**	pA
I_{OS}	Input Offset Current			6.6		fA
I_S	Supply Current	Per Amplifier		107	200 **260**	µA
		Shutdown Mode, V_{SD} = 0V (LMV341-N)		0.033	1 **1.5**	µA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4.0V 0V ≤ V_{CM} ≤ 3.9V	56 **50**	86		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V	65 **60**	82		dB
V_{CM}	Input Common Mode Voltage	For CMRR ≥ 50dB	0	−0.2 to 4.2 (Range)	4	V
A_V	Large Signal Voltage Gain(4)	R_L = 10kΩ to 2.5V	78 **70**	116		dB
		R_L = 2kΩ to 2.5V	72 **64**	107		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) R_L is connected to mid-supply. The output voltage is GND + 0.2V ≤ V_O ≤ V^+ −0.2V

5V DC Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
V_O	Output Swing	R_L = 2kΩ to 2.5V		32	60 **95**	mV
			60 **95**	34		
		R_L = 10kΩ to 2.5V		7	30 **40**	mV
			30 **40**	7		
I_O	Output Short Circuit Current	Sourcing	85	113		mA
		Sinking	50	75		
t_{on}	Turn-on Time from Shutdown	(LMV341-N)		5		µs
V_{SD}	Shutdown Pin Voltage Range	ON Mode (LMV341-N)		3.1 to 5	4.5 to 5.0	V
		Shutdown Mode (LMV341-N)		0 to 1	0 to 0.8	

5V AC Electrical Characteristics[1]

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
SR	Slew Rate	R_L = 10kΩ [4]		1.0		V/µs
GBW	Gain-Bandwidth Product	R_L = 10kΩ, C_L = 200pF		1.0		MHz
Φ_m	Phase Margin	R_L = 100kΩ		70		deg
G_m	Gain Margin	R_L = 100kΩ		20		dB
e_n	Input-Referred Voltage Noise	f = 1kHz		39		nV/√Hz
i_n	Input-Referred Current Noise	f = 1kHz		0.001		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = 1V_{PP}		0.012		%

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with 2V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

Connection Diagram

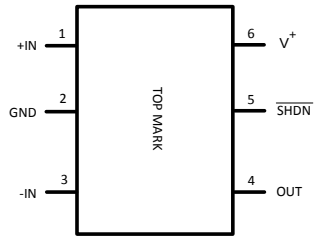


Figure 1. 6-Pin SC70
Top View

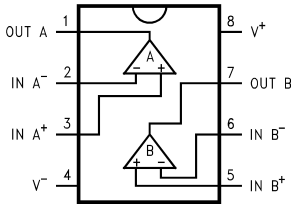


Figure 2. 8-Pin VSSOP/SOIC
Package Number DGK/D
Top View

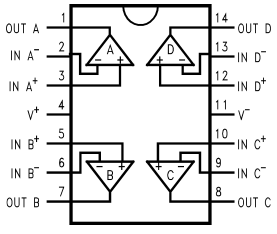


Figure 3. 14-Pin TSSOP/SOIC
Package Number PW/D
Top View

Typical Performance Characteristics

Supply Current vs. Supply Voltage (LMV341-N)

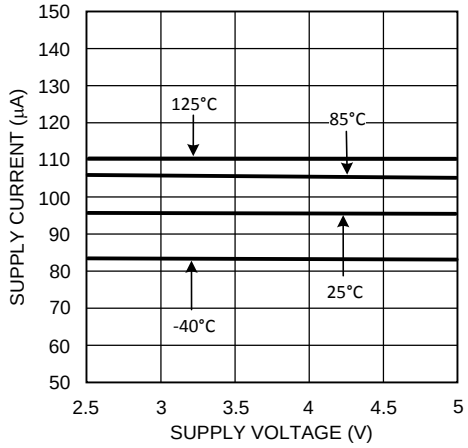


Figure 4.

Input Current vs. Temperature

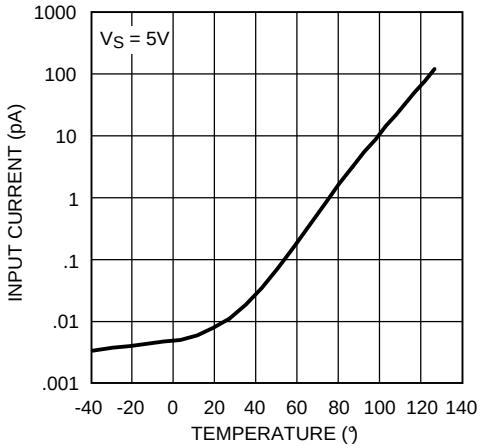


Figure 5.

Output Voltage Swing vs. Supply Voltage

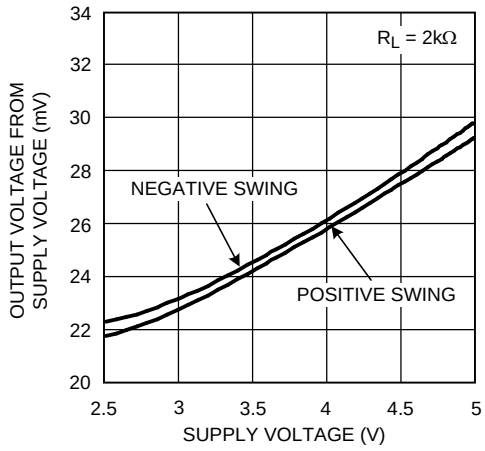


Figure 6.

Output Voltage Swing vs. Supply Voltage

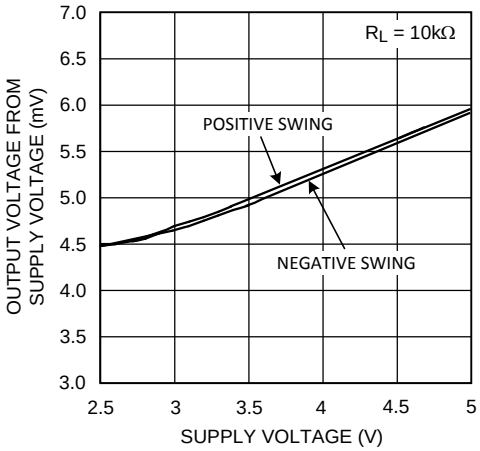


Figure 7.

I_{SOURCE} vs. V_{OUT}

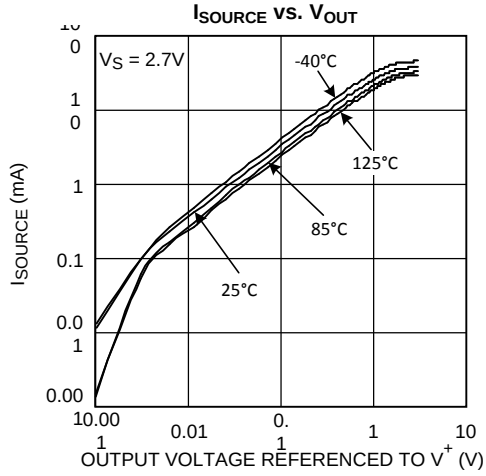


Figure 8.

I_{SOURCE} vs. V_{OUT}

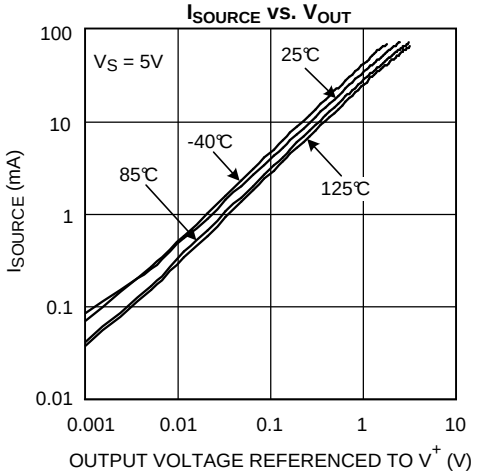


Figure 9.

Typical Performance Characteristics (continued)

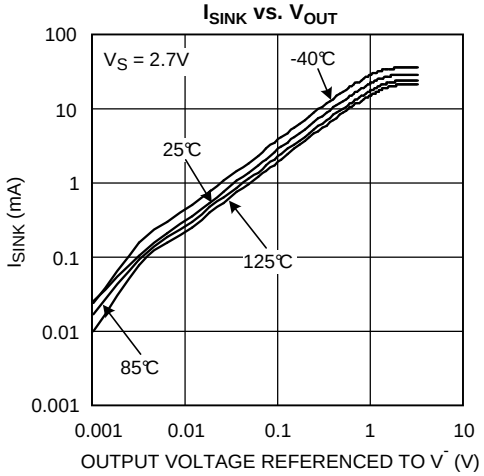


Figure 10.

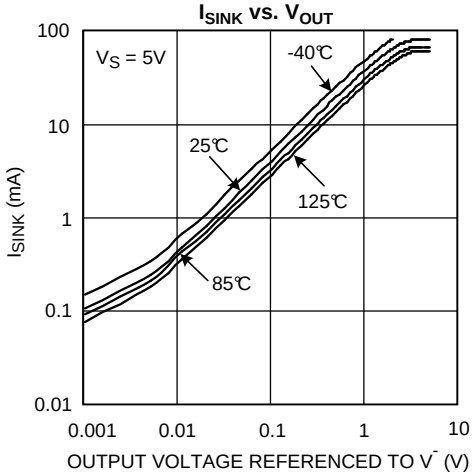


Figure 11.

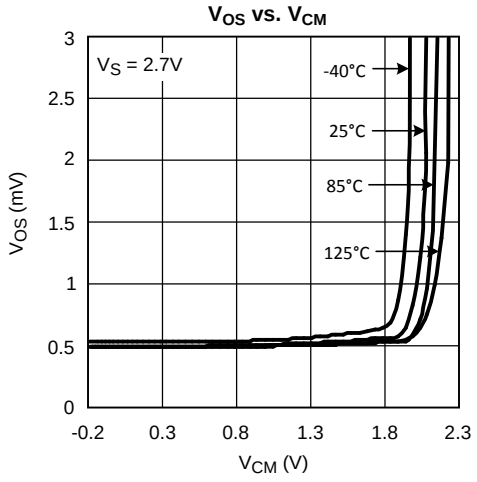


Figure 12.

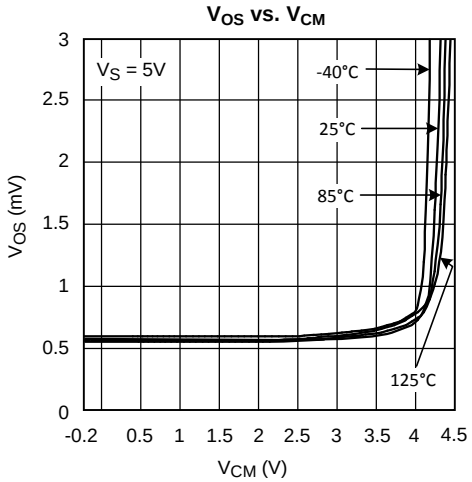


Figure 13.

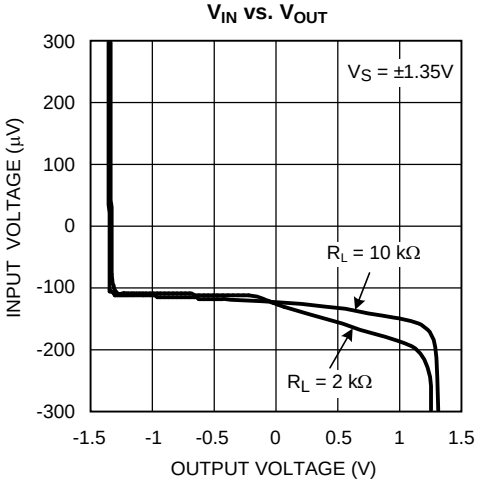


Figure 14.

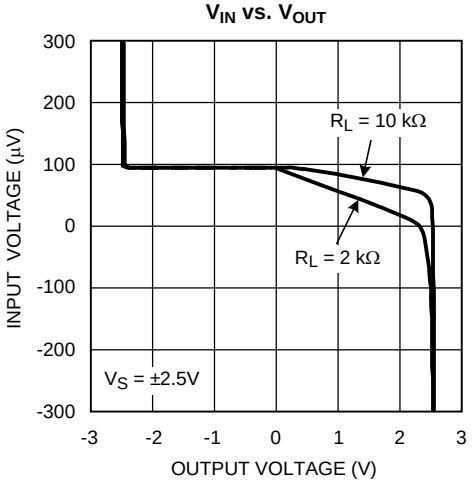


Figure 15.

Typical Performance Characteristics (continued)

CMRR vs. Frequency

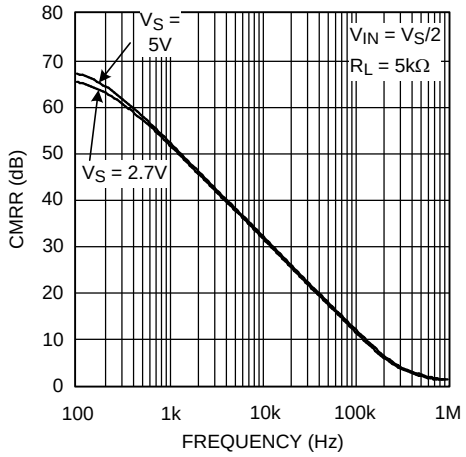


Figure 16.

PSRR vs. Frequency

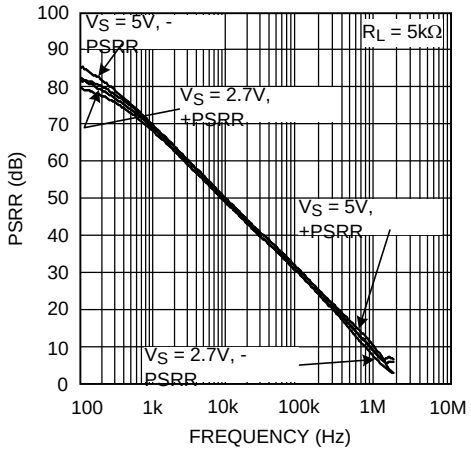


Figure 17.

Input Voltage Noise vs. frequency

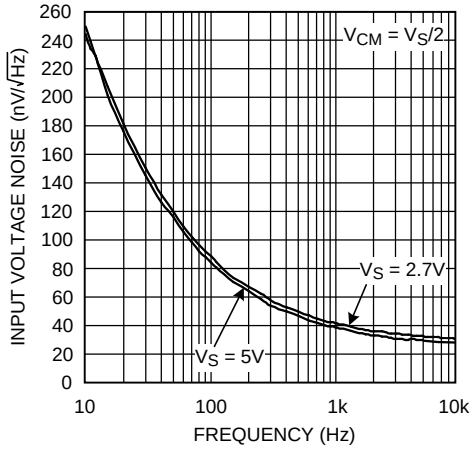


Figure 18.

Slew Rate vs. V_{SUPPLY}

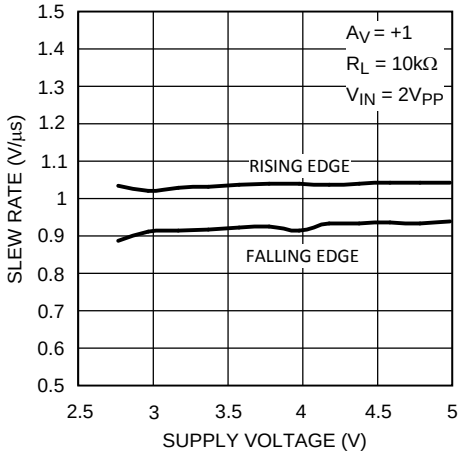


Figure 19.

Slew Rate vs. Temperature

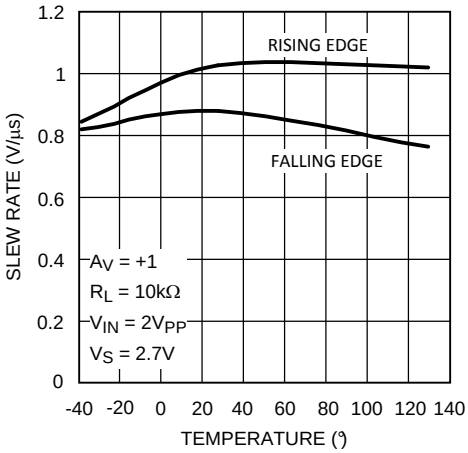


Figure 20.

Slew Rate vs. Temperature

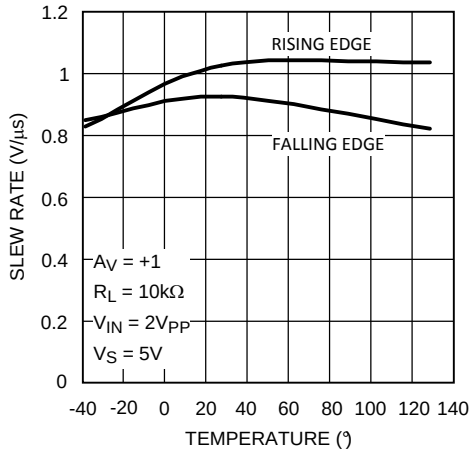


Figure 21.

Typical Performance Characteristics (continued)

THD+N vs. Frequency

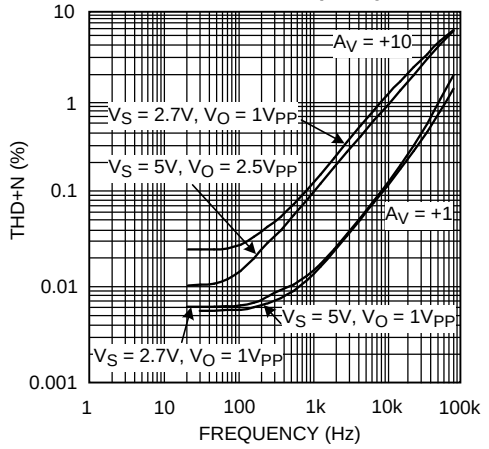


Figure 22.

THD+N vs. V_{OUT}

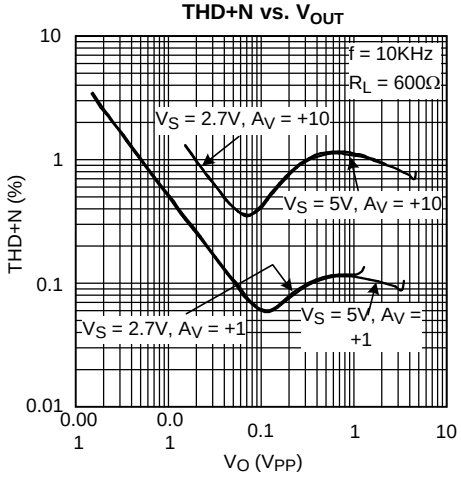


Figure 23.

Open Loop Frequency Over Temperature

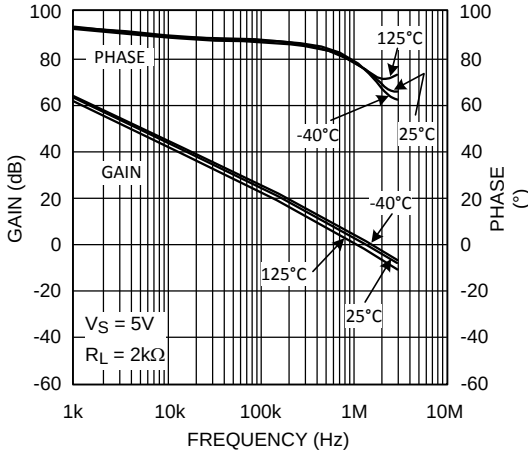


Figure 24.

Open Loop Frequency Response

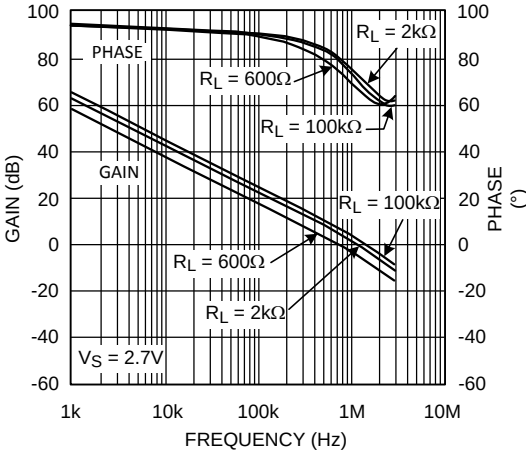


Figure 25.

Open Loop Frequency Response

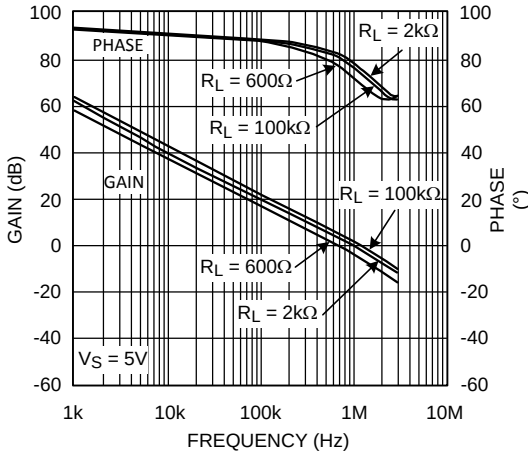


Figure 26.

Gain and Phase vs. C_L

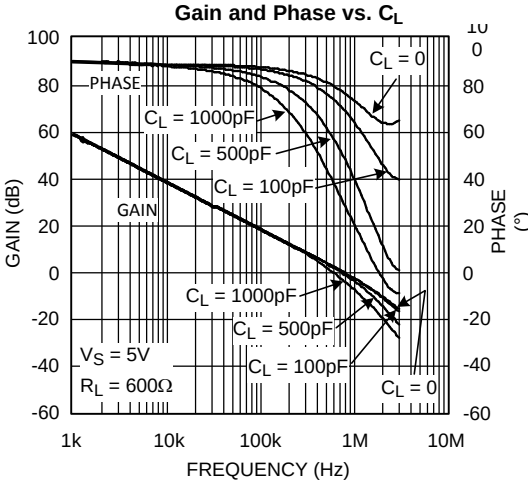


Figure 27.

Typical Performance Characteristics (continued)

Gain and Phase vs. C_L

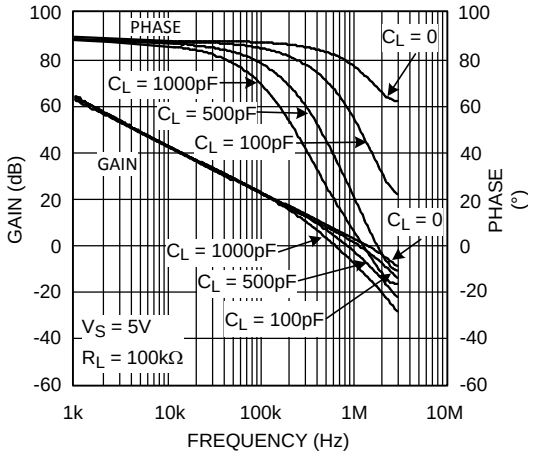


Figure 28.

Stability vs. Capacitive Load

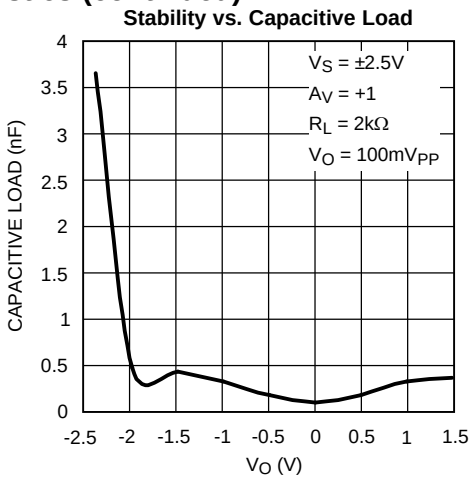


Figure 29.

Stability vs. Capacitive Load

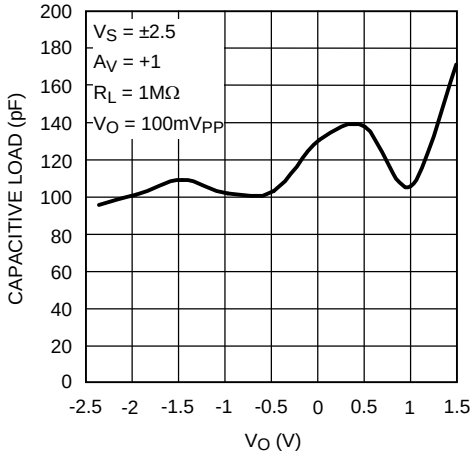


Figure 30.

Non-Inverting Small Signal Pulse Response

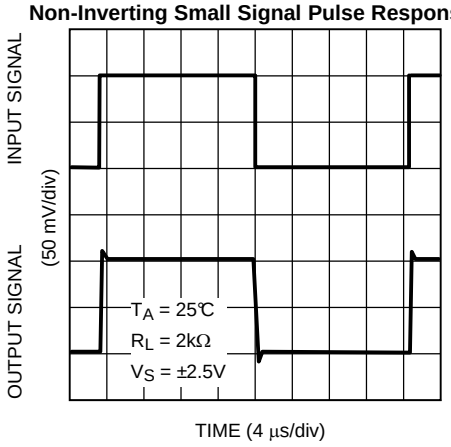


Figure 31.

Non-Inverting Large Signal Pulse Response

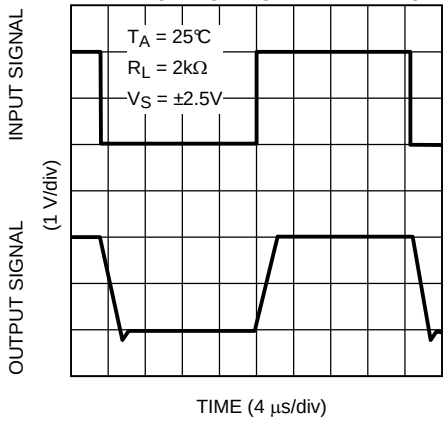


Figure 32.

Non-Inverting Small Signal Pulse Response

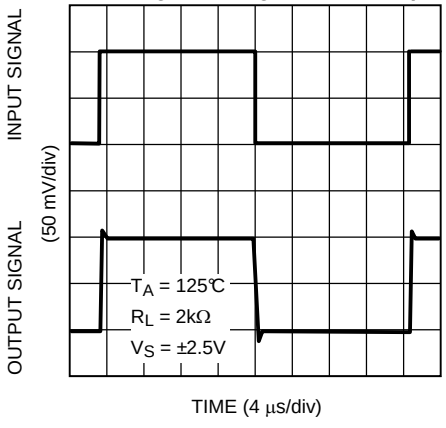


Figure 33.

Typical Performance Characteristics (continued)

Non-Inverting Large Signal Pulse Response

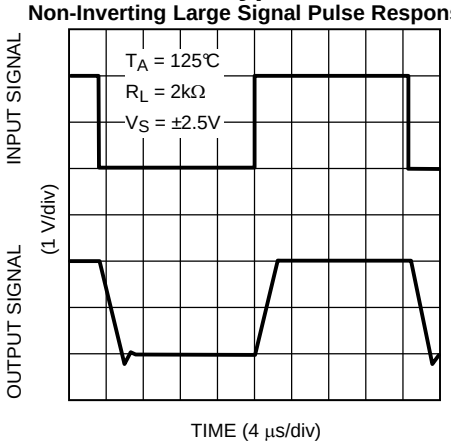


Figure 34.

Non-Inverting Small Signal Pulse Response

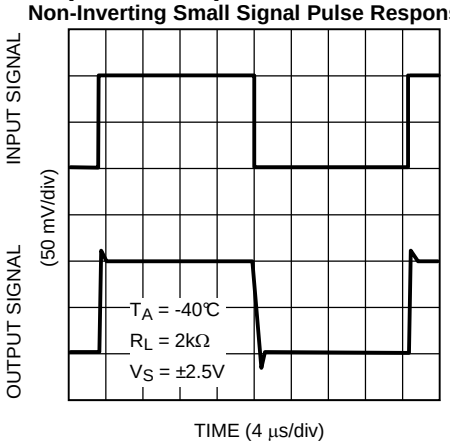


Figure 35.

Non-Inverting Large Signal Pulse Response

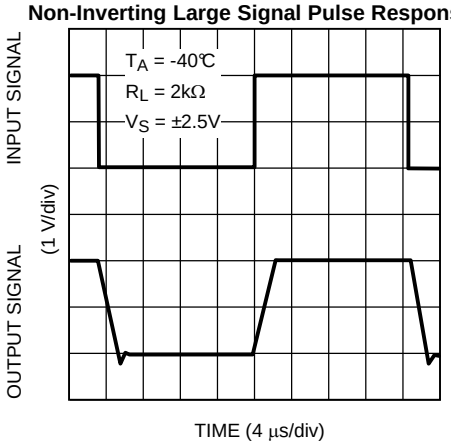


Figure 36.

Inverting Small Signal Pulse Response

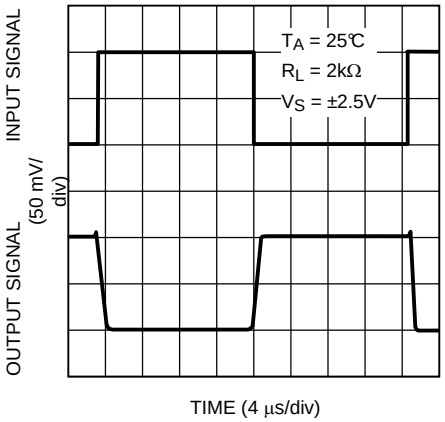


Figure 37.

Inverting Large Signal Pulse Response

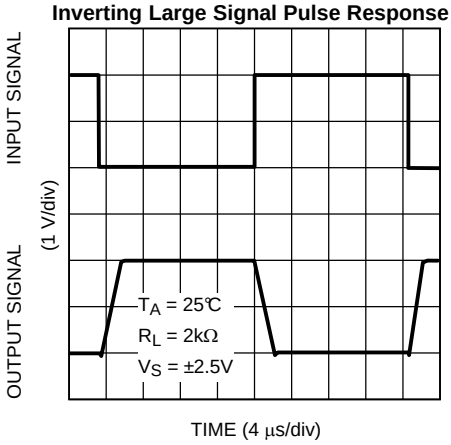


Figure 38.

Inverting Small Signal Pulse Response

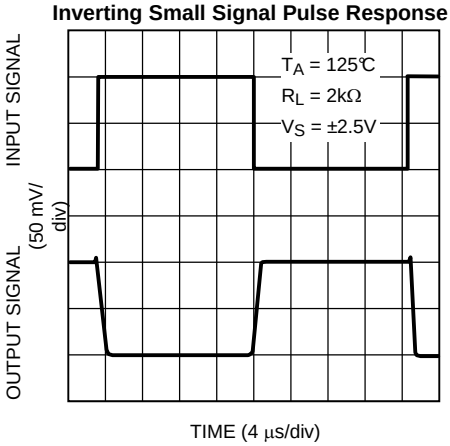


Figure 39.

Typical Performance Characteristics (continued)

Inverting Large Signal Pulse Response

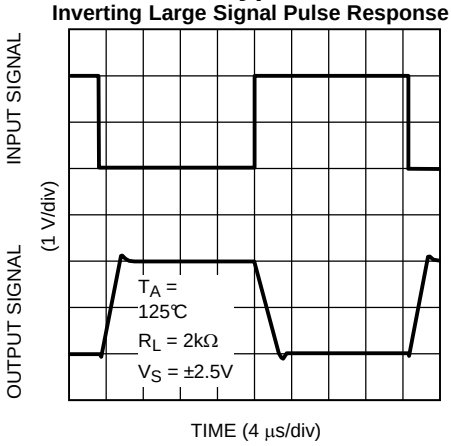


Figure 40.

Inverting Small Signal Pulse Response

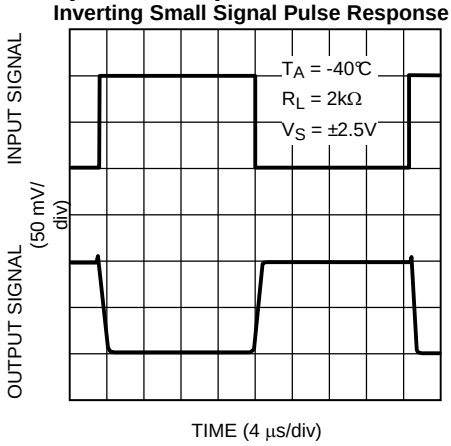


Figure 41.

Inverting Large Signal Pulse Response

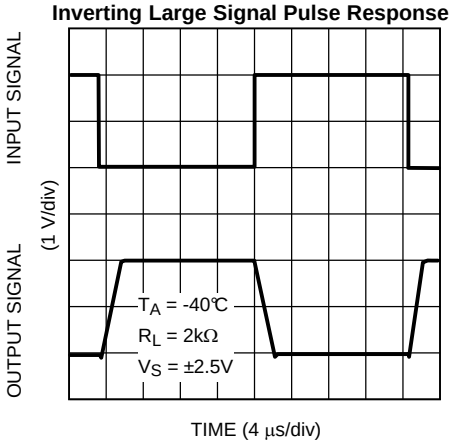


Figure 42.

Crosstalk Rejection vs. Frequency

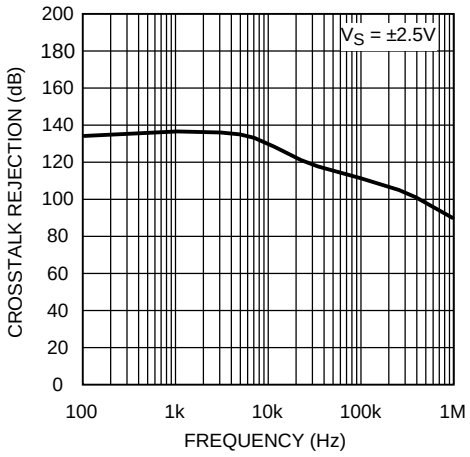


Figure 43.

APPLICATION SECTION

LMV341-N/LMV342-N/LMV344-N

The LMV341-N/LMV342-N/LMV344-N family of amplifiers features low voltage, low power, and rail-to-rail output operational amplifiers designed for low voltage portable applications. The family is designed using all CMOS technology. This results in an ultra low input bias current. The LMV341-N has a shutdown option, which can be used in portable devices to increase battery life.

A simplified schematic of the LMV341-N/LMV342-N/LMV344-N family of amplifiers is shown in Figure 44. The PMOS input differential pair allows the input to include ground. The output of this differential pair is connected to the Class AB turnaround stage. This Class AB turnaround has a lower quiescent current, compared to regular turnaround stages. This results in lower offset, noise, and power dissipation, while slew rate equals that of a conventional turnaround stage. The output of the Class AB turnaround stage provides gate voltage to the complementary common-source transistors at the output stage. These transistors enable the device to have rail-to-rail output.

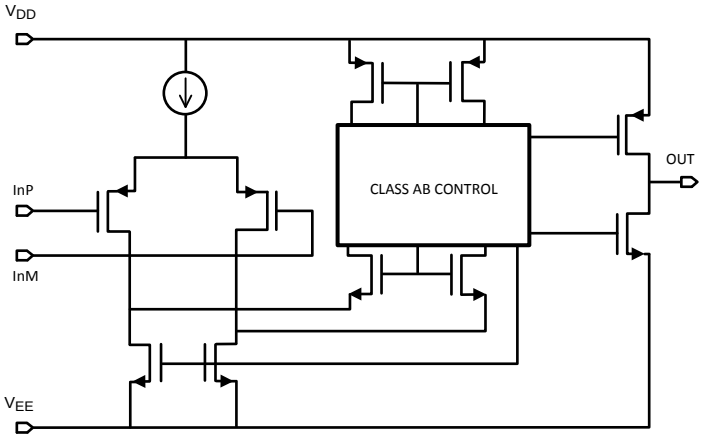


Figure 44. Simplified Schematic

Class AB Turnaround Stage Amplifier

This patented folded cascode stage has a combined class AB amplifier stage, which replaces the conventional folded cascode stage. Therefore, the class AB folded cascode stage runs at a much lower quiescent current compared to conventional folded cascode stages. This results in significantly smaller offset and noise contributions. The reduced offset and noise contributions in turn reduce the offset voltage level and the voltage noise level at the input of the LMV341-N/LMV342-N/LMV344-N. Also the lower quiescent current results in a high open-loop gain for the amplifier. The lower quiescent current does not affect the slew rate of the amplifier nor its ability to handle the total current swing coming from the input stage.

The input voltage noise of the device at low frequencies, below 1kHz, is slightly higher than devices with a BJT input stage; However the PMOS input stage results in a much lower input bias current and the input voltage noise drops at frequencies above 1kHz.

Sample and Hold Circuit

The lower input bias current of the LMV341-N results in a very high input impedance. The output impedance when the device is in shutdown mode is quite high. These high impedances, along with the ability of the shutdown pin to be derived from a separate power source, make LMV341-N a good choice for sample and hold circuits. The sample clock should be connected to the shutdown pin of the amplifier to rapidly turn the device on or off.

Figure 45 shows the schematic of a simple sample and hold circuit. When the sample clock is high the first amplifier is in normal operation mode and the second amplifier acts as a buffer. The capacitor, which appears as a load on the first amplifier, will be charging at this time. The voltage across the capacitor is that of the non-inverting input of the first amplifier since it is connected as a voltage-follower. When the sample clock is low the first amplifier is shut off, bringing the output impedance to a high value. The high impedance of this output, along with the very high impedance on the input of the second amplifier, prevents the capacitor from discharging. There is very little voltage droop while the first amplifier is in shutdown mode. The second amplifier, which is still in normal operation mode and is connected as a voltage follower, also provides the voltage sampled on the capacitor at its output.

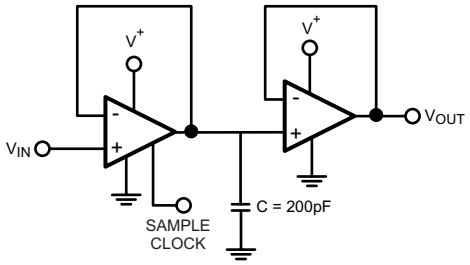


Figure 45. Sample and Hold Circuit

Shutdown Feature

The LMV341-N is capable of being turned off in order to conserve power and increase battery life in portable devices. Once in shutdown mode the supply current is drastically reduced, 1µA maximum, and the output will be "tri-stated."

The device will be disabled when the shutdown pin voltage is pulled low. The shutdown pin should never be left unconnected. Leaving the pin floating will result in an undefined operation mode and the device may oscillate between shutdown and active modes.

The LMV341-N typically turns on 2.8µs after the shutdown voltage is pulled high. The device turns off in less than 400ns after shutdown voltage is pulled low. Figure 46 and Figure 47 show the turn-on and turn-off time of the LMV341-N, respectively. In order to reduce the effect of the capacitance added to the circuit by the scope probe, in the turn-off time circuit a resistive load of 600Ω is added. Figure 48 and Figure 49 show the test circuits used to obtain the two plots.

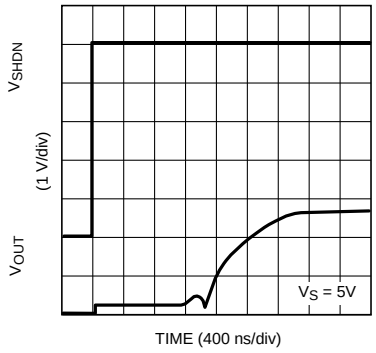


Figure 46. Turn-on Time

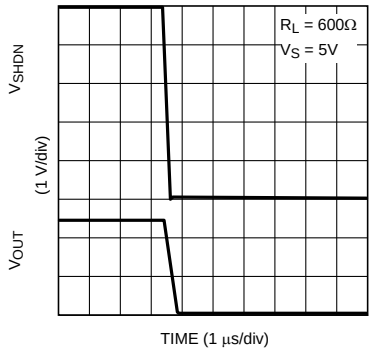


Figure 47. Turn-off Time

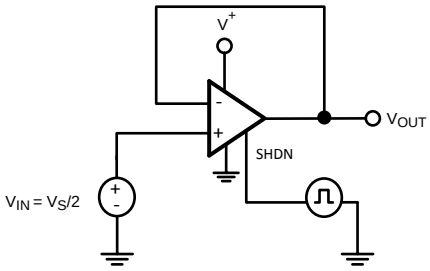


Figure 48. Turn-on Time

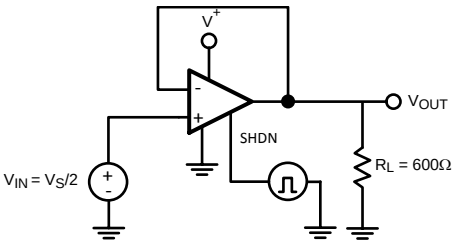


Figure 49. Turn-off Time

Low Input Bias Current

The LMV341-N/LMV342-N/LMV344-N Amplifiers have a PMOS input stage. As a result, they will have a much lower input bias current than devices with BJT input stages. This feature makes these devices ideal for sensor circuits. A typical curve of the input bias current of the LMV341-N is shown in Figure 50.

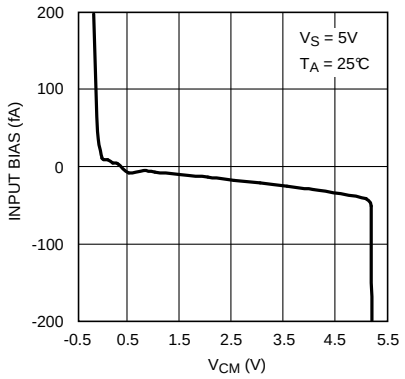


Figure 50. Input Bias Current vs. V_{CM}

REVISION HISTORY

Changes from Revision F (March 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV341MG/NOPB	ACTIVE	SC70	DCK	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A78	Samples
LMV341MGX/NOPB	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A78	Samples
LMV342MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV34 2MA	Samples
LMV342MAX	NRND	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	LMV34 2MA	
LMV342MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV34 2MA	Samples
LMV342MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A82A	Samples
LMV342MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A82A	Samples
LMV344MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV344MA	Samples
LMV344MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV344MA	Samples
LMV344MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LMV34 4MT	Samples
LMV344MTX	NRND	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	LMV34 4MT	
LMV344MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LMV34 4MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

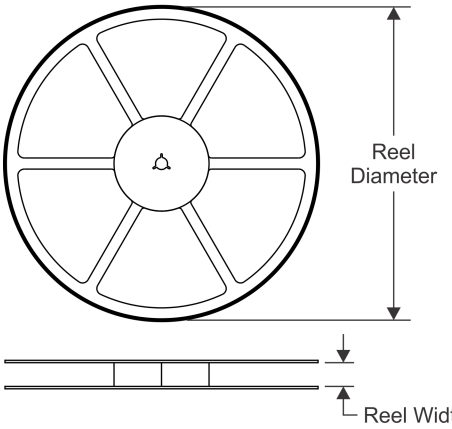
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

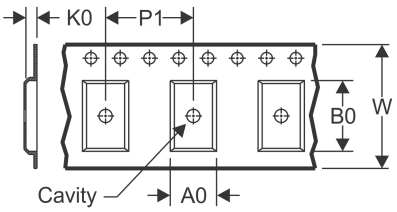
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

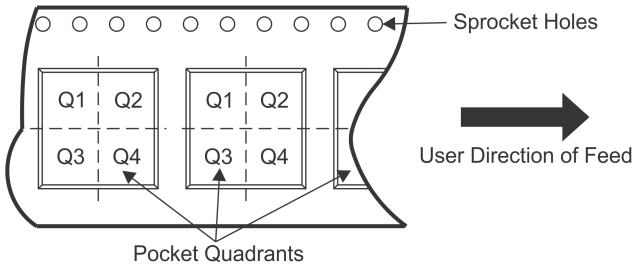


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

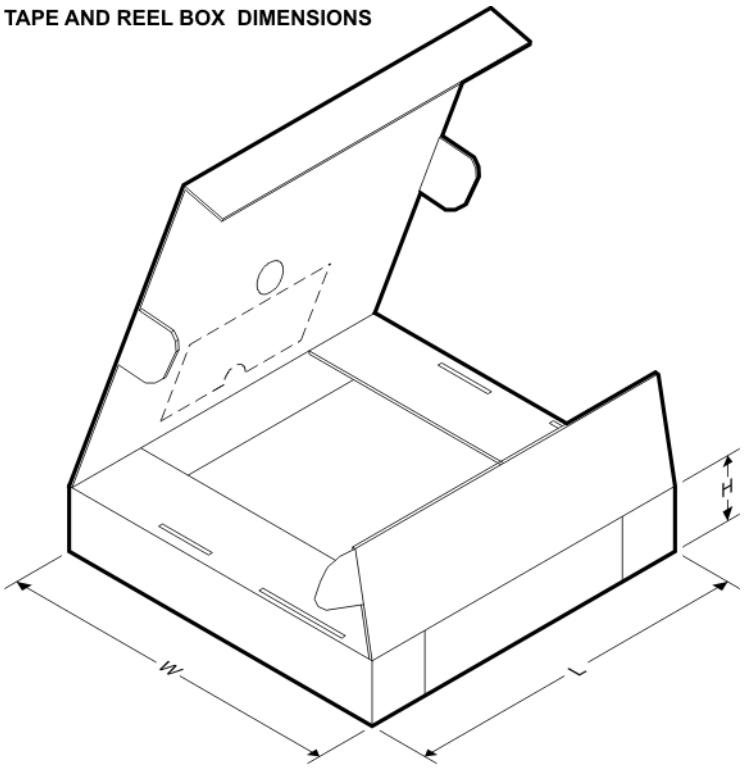
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV341MG/NOPB	SC70	DCK	6	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV341MGX/NOPB	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV342MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV342MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV342MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV344MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV344MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

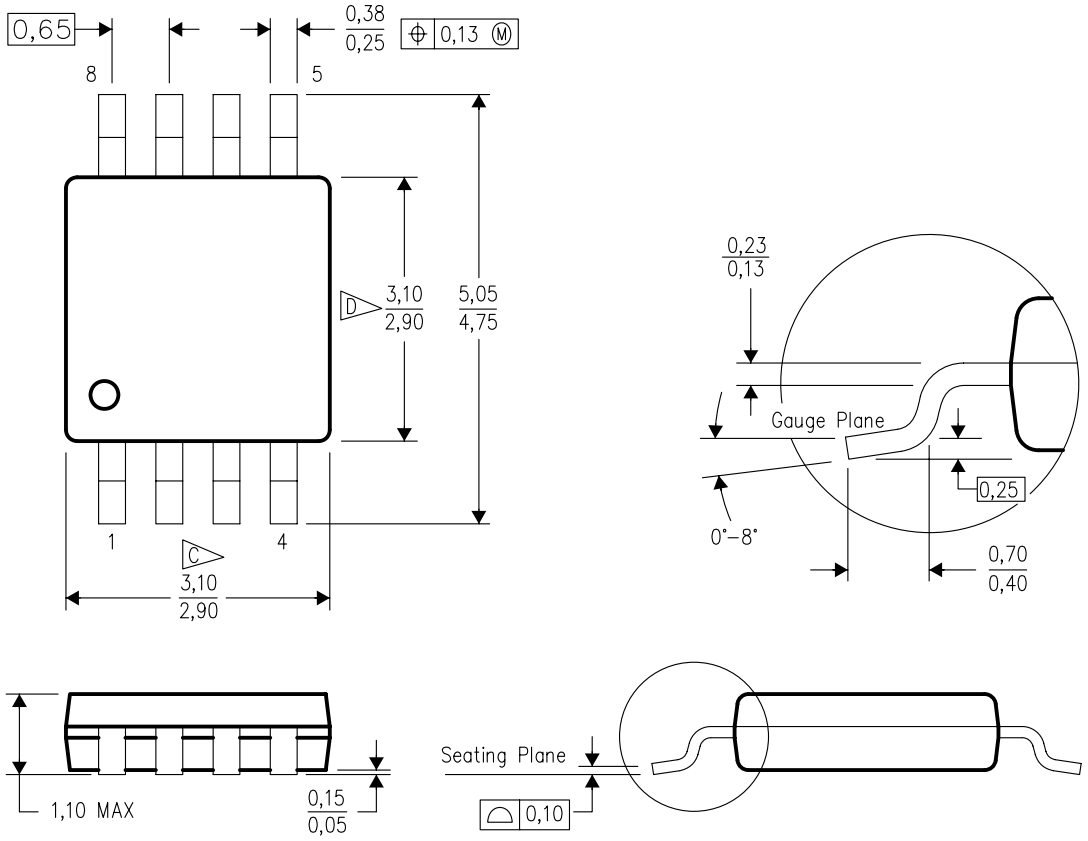
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV341MG/NOPB	SC70	DCK	6	1000	210.0	185.0	35.0
LMV341MGX/NOPB	SC70	DCK	6	3000	210.0	185.0	35.0
LMV342MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV342MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV342MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV344MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMV344MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

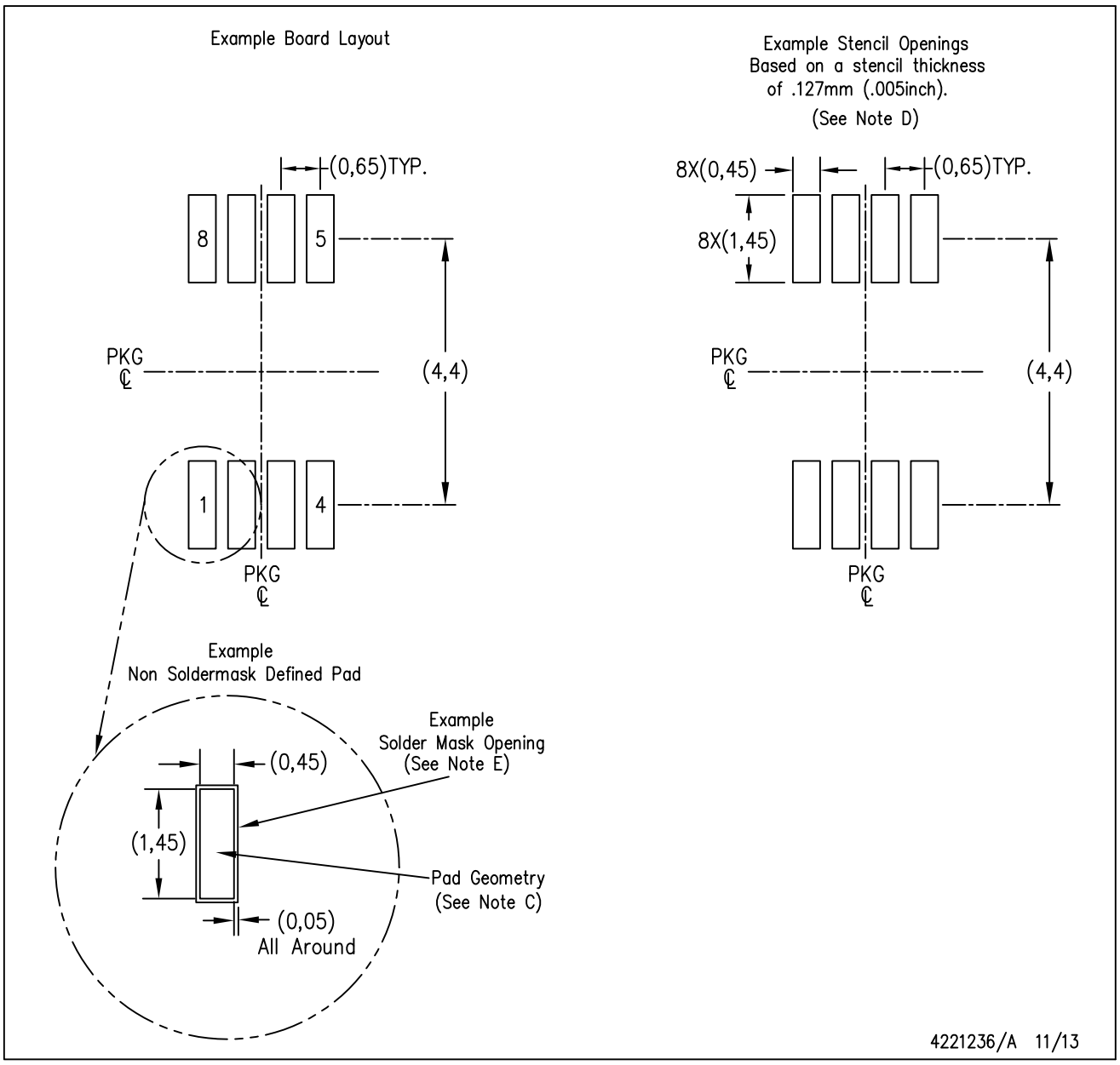
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

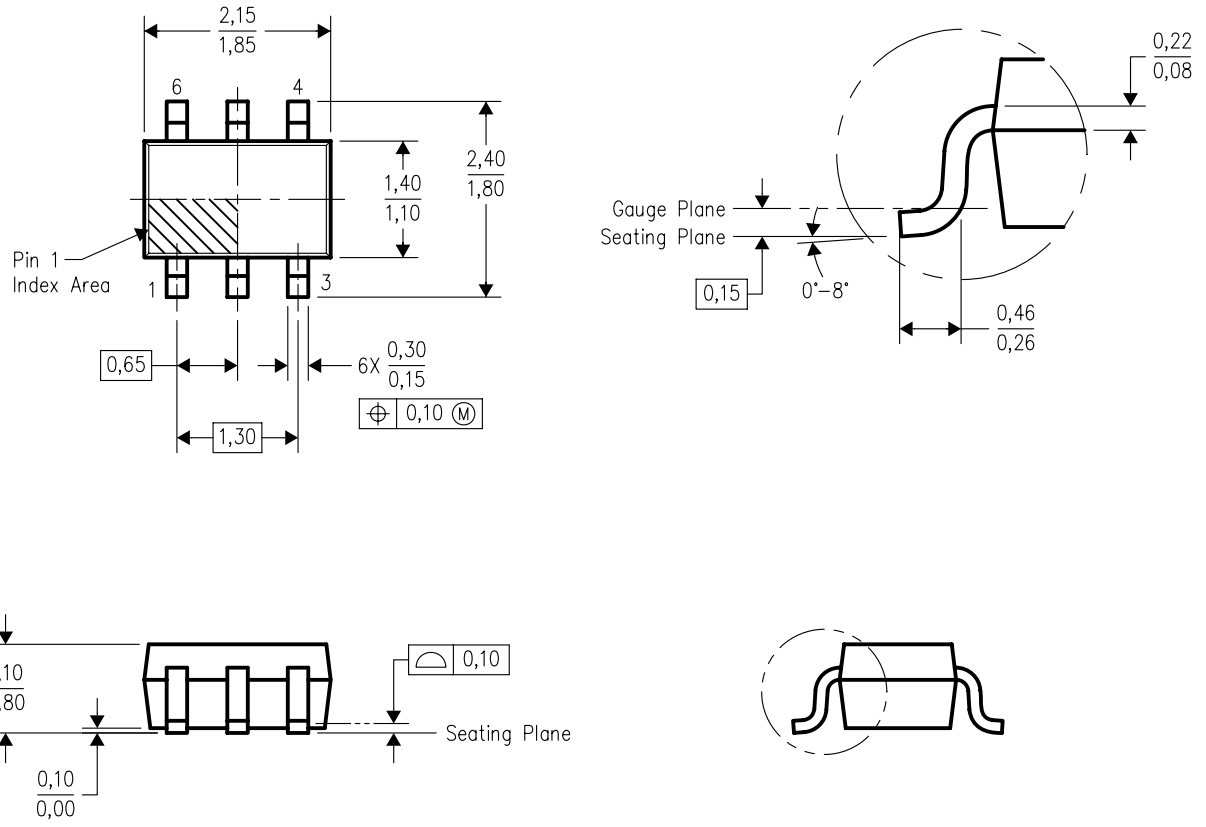
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

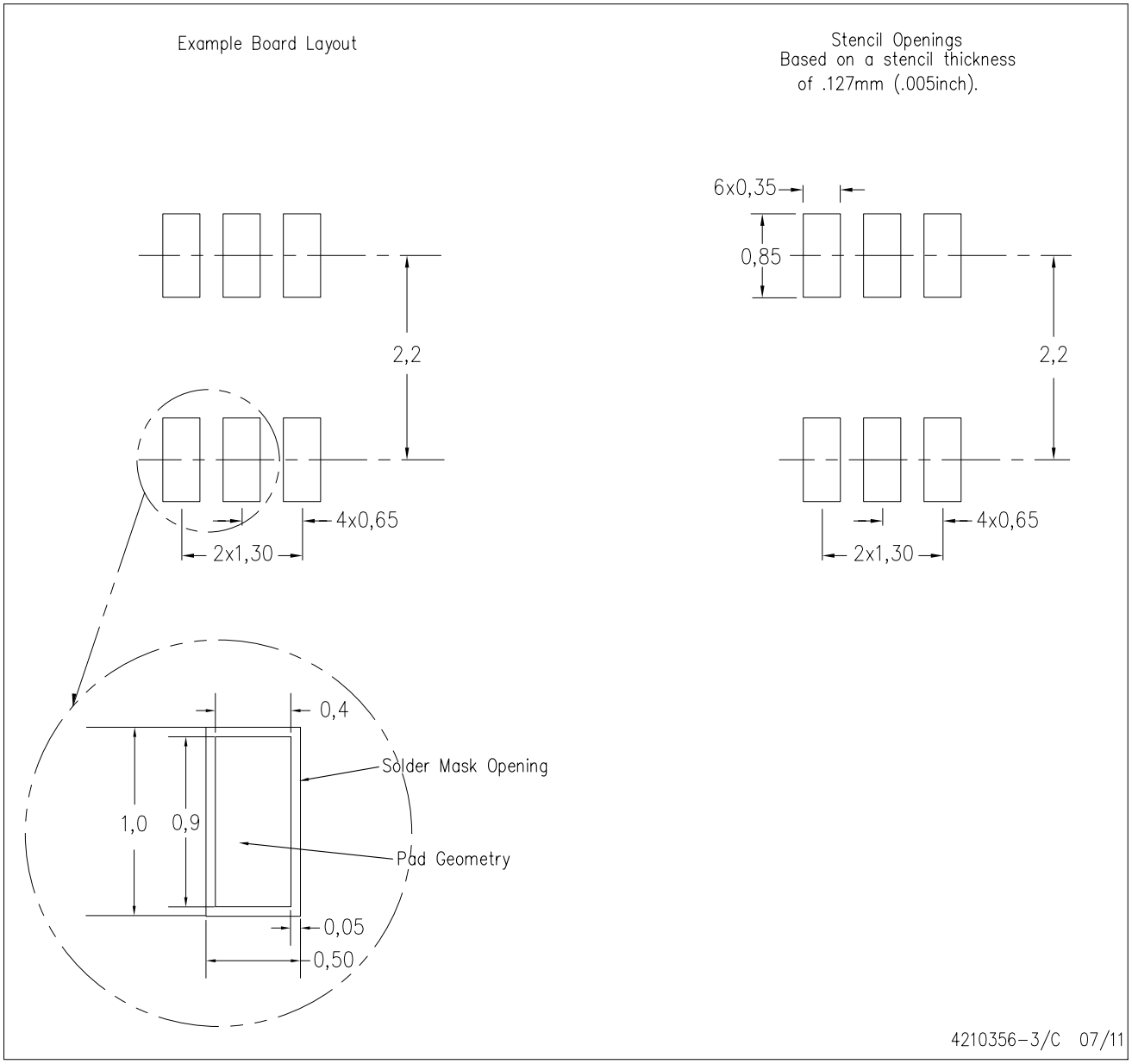
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

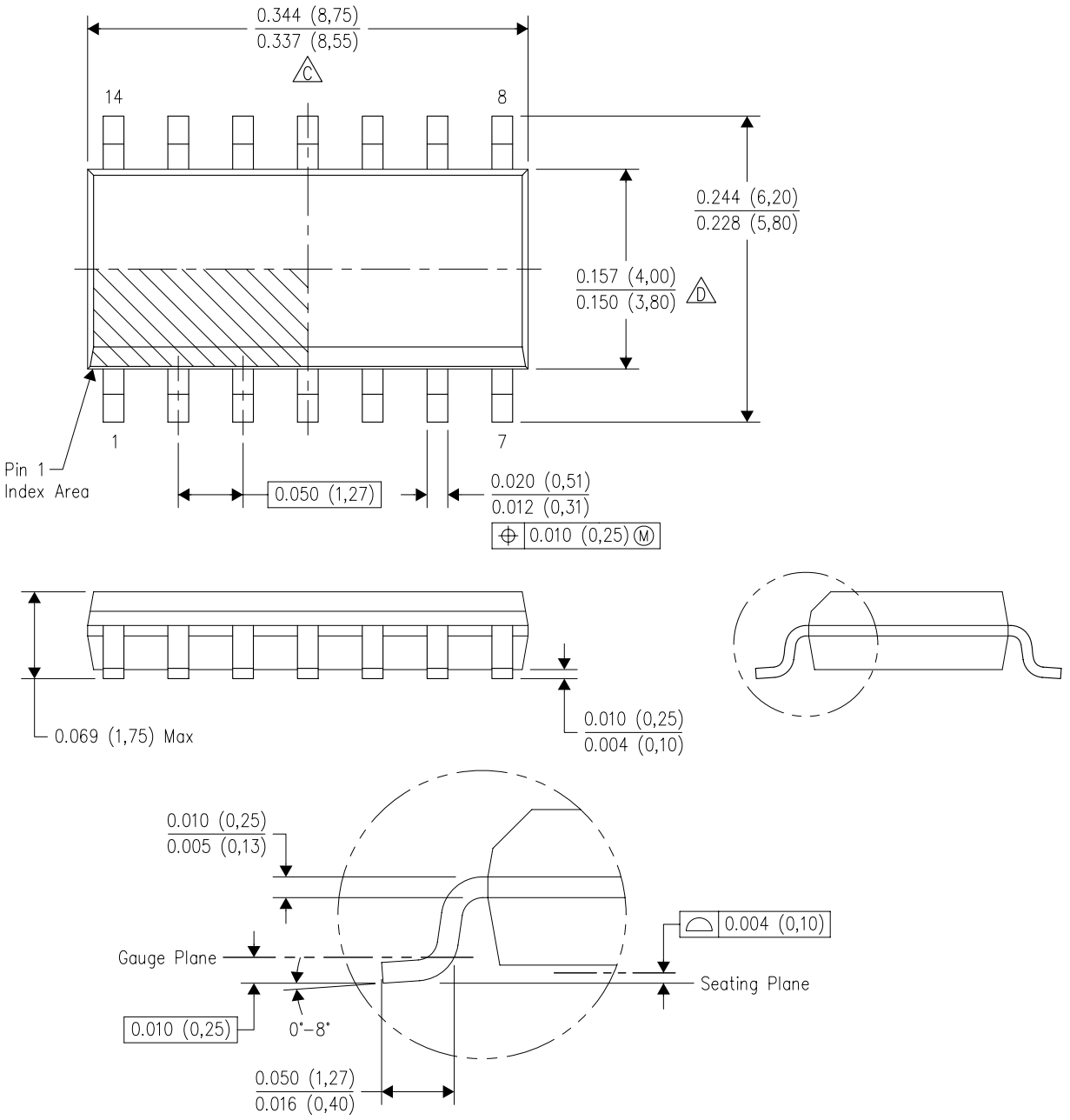
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

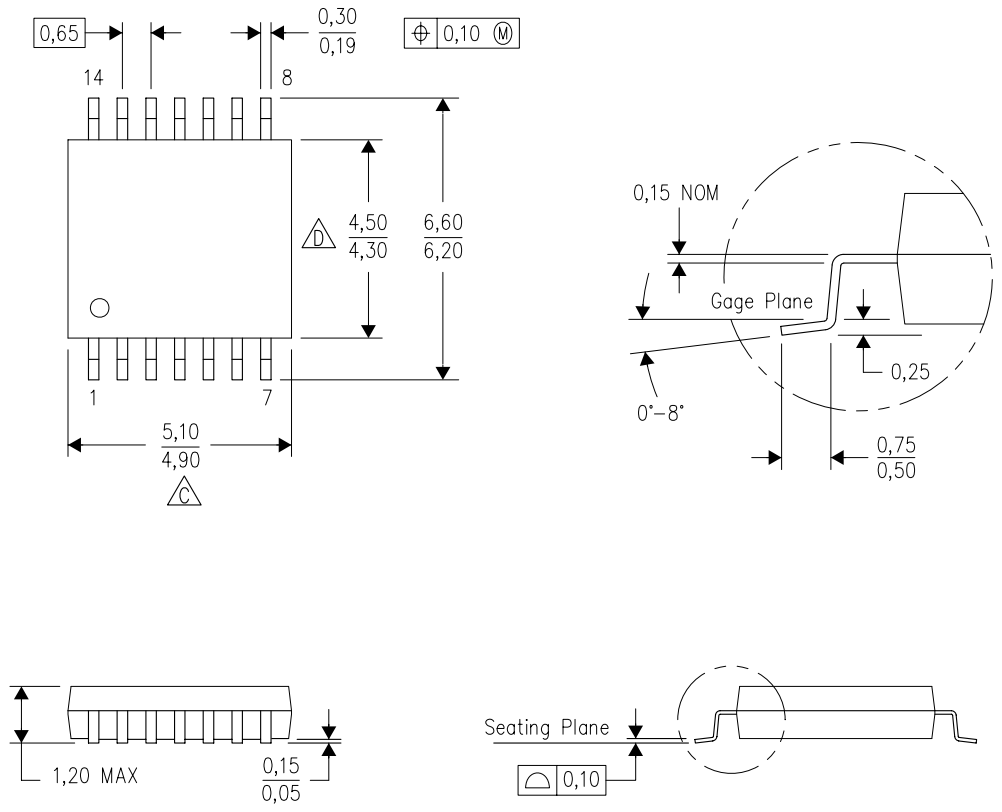
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

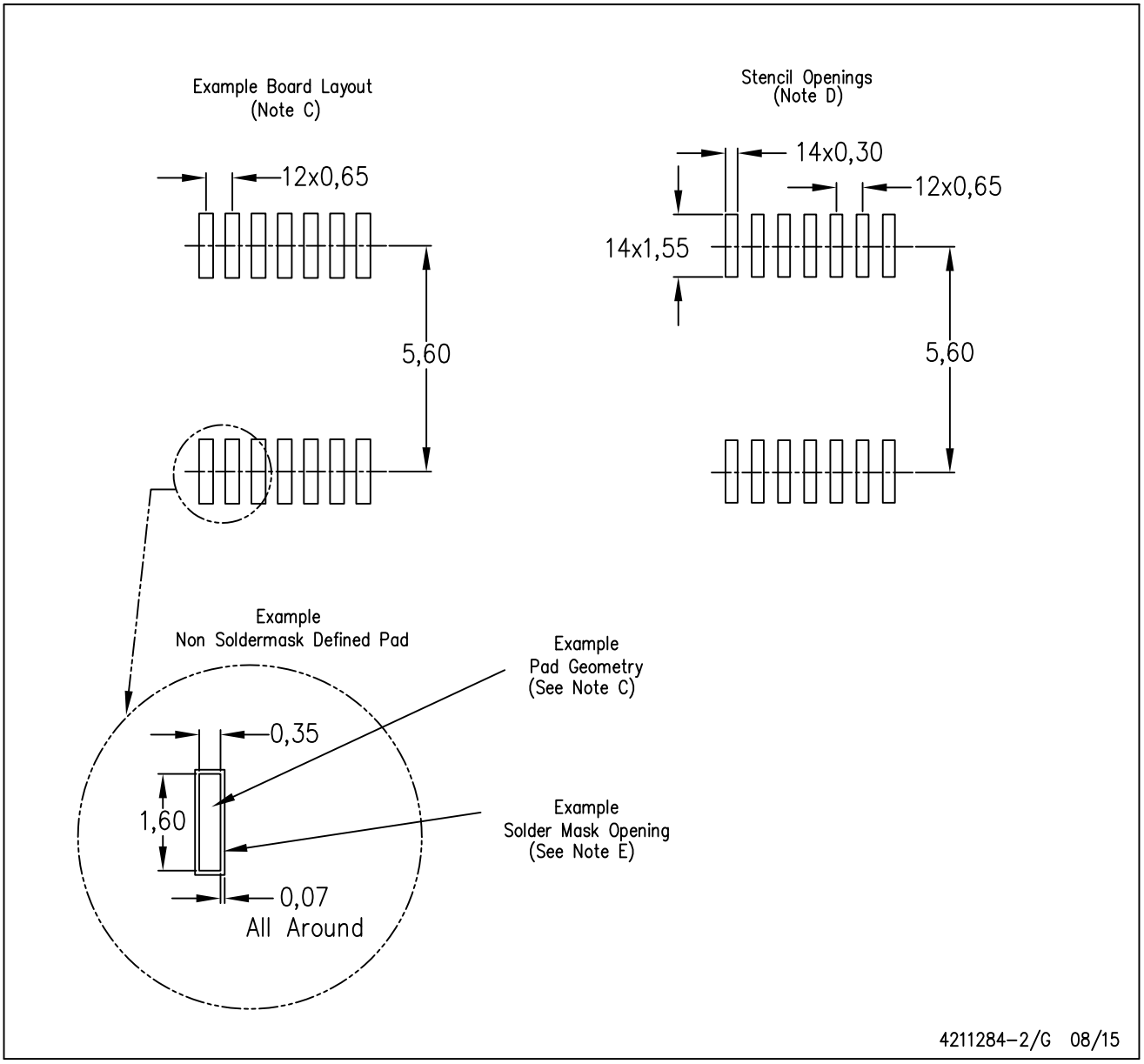
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

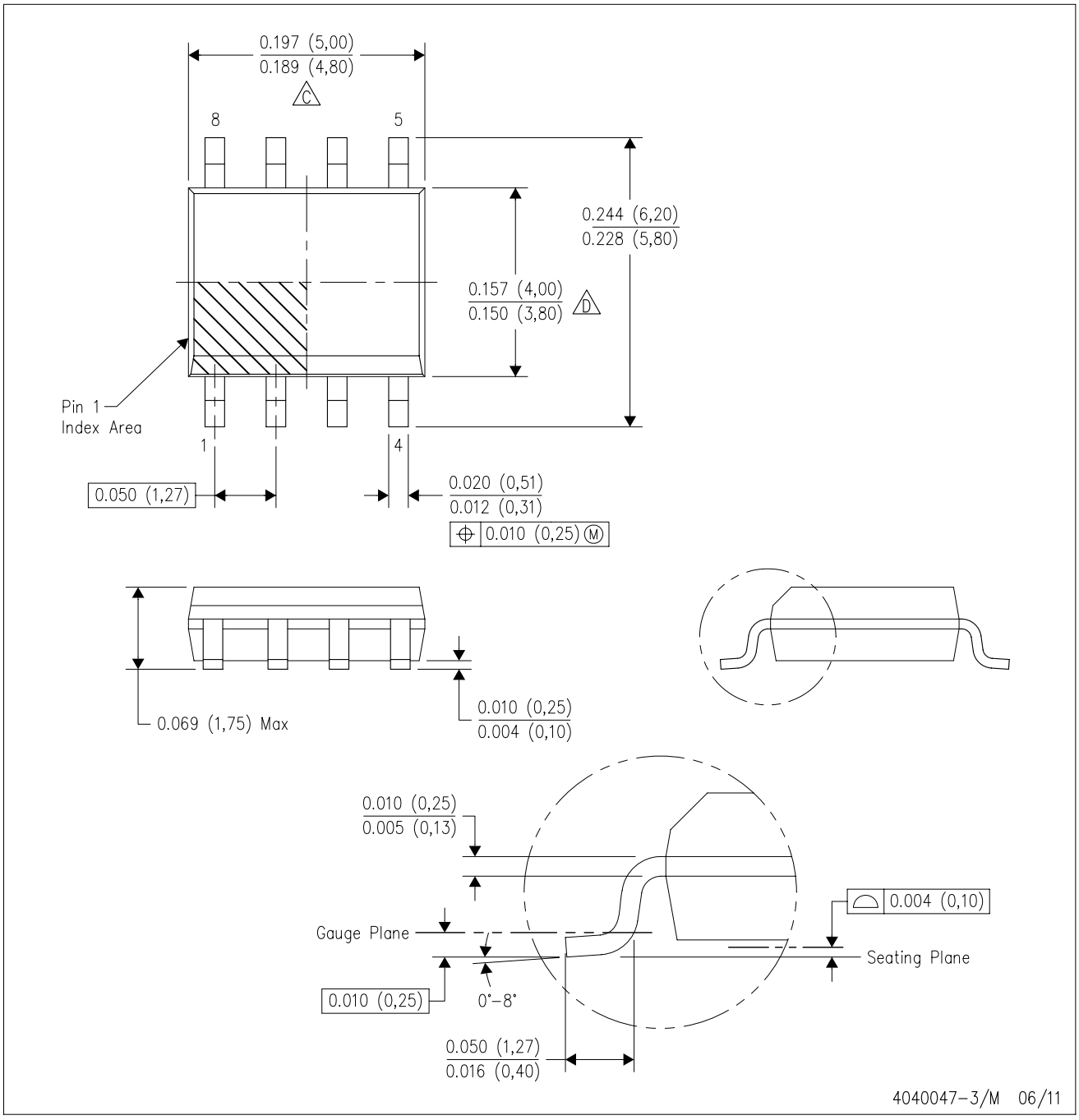
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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