

## LMX2330U/LMX2331U/LMX2332U PLLatinum™ Ultra Low Power Dual Frequency Synthesizer for RF Personal Communications

LMX2330U 2.5 GHz/600 MHz LMX2331U 2.0 GHz/600 MHz LMX2332U 1.2 GHz/600 MHz

#### **General Description**

The LMX233xU devices are high performance frequency synthesizers with integrated dual modulus prescalers. The LMX233xU devices are designed for use as RF and IF local oscillators for dual conversion radio transceivers.

A 32/33 or a 64/65 prescale ratio can be selected for the 2.5 GHz LMX2330U RF synthesizer. A 64/65 or a 128/129 prescale ratio can be selected for both the LMX2331U and LMX2332U RF synthesizers. The IF circuitry contains an 8/9 or a 16/17 prescaler. Using a proprietary digital phase locked loop technique, the LMX233xU devices generate very stable, low noise control signals for RF and IF voltage controlled oscillators. Both the RF and IF synthesizers include a two-level programmable charge pump. The RF synthesizer has dedicated Fastlock circuitry.

Serial data is transferred to the devices via a three-wire interface (Data, LE, Clock). Supply voltages from 2.7V to 5.5V are supported. The LMX233xU family features ultra low current consumption:

LMX2330U (2.5 GHz)—3.3 mA, LMX2331U (2.0 GHz)—2.9 mA, LMX2332U (1.2 GHz)—2.5 mA at 3.0V.

The LMX233xU devices are available in 20-Pin TSSOP and 24-Pin CSP surface mount plastic packages.

#### **Features**

- Ultra Low Current Consumption
- Upgrade and Compatible to LMX233xL Family
- 2.7V to 5.5V Operation
- Selectable Synchronous or Asynchronous Powerdown Mode:

 $I_{CC-PWDN} = 1 \mu A typical$ 

■ Selectable Dual Modulus Prescaler:

LMX2330U RF: 32/33 or 64/65 LMX2331U RF: 64/65 or 128/129 LMX2332U RF: 64/65 or 128/129 LMX2330U/31U/32U IF: 8/9 or 16/17

- Selectable Charge Pump TRI-STATE® Mode
- Programmable Charge Pump Current Levels RF and IF: 0.95 or 3.8 mA
- Selectable Fastlock<sup>™</sup> Mode for the RF Synthesizer
- Push-Pull Analog Lock Detect Output
- Available in 20-Pin TSSOP and 24-Pin Chip Scale Package (CSP)

#### **Applications**

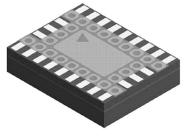
- Mobile Handsets (GSM, GPRS, W-CDMA, CDMA, PCS, AMPS, PDC, DCS)
- Cordless Handsets (DECT, DCT)
- Wireless Data
- Cable TV Tuners

#### Thin Shrink Small Outline Package (MTC20)



10136680

#### Chip Scale Package (SLB24A)



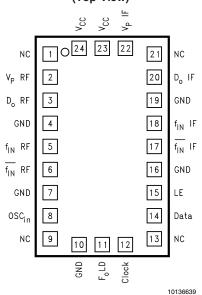
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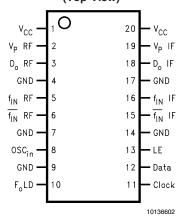
#### **Functional Block Diagram** 15-BIT IF N COUNTER $f_{\mathsf{IN}}$ IF IF PRESCALER PHASE CHARGE PUMP DETECTOR IF LOCK DETECT 15-BIT IF R COUNTER MUX **>\** F<sub>o</sub>LD osc<sub>in</sub> RF LOCK DETECT 15-BIT RF R COUNTER PHASE DETECTOR CHARGE **∳** D₀ RF $\frac{f_{\mathsf{IN}}}{f_{\mathsf{IN}}} \; \frac{\mathsf{RF}}{\mathsf{RF}}$ RF PRESCALER 18-BIT RF PUMP N COUNTER MICROWIRE INTERFACE Clock 🕻 FASTLOCK Data C LMX2330U/LMX2331U/LMX2332U GND GND GND GND GND 10136601

#### **Connection Diagrams**

#### Chip Scale Package (SLB) (Top View)



#### Thin Shrink Small Outline Package (TM) (Top View)



#### **Pin Descriptions**

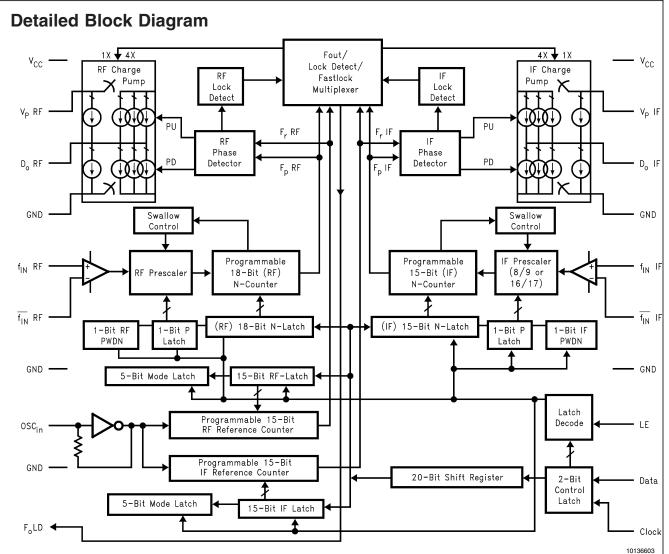
Pin Name	Pin No. 24-Pin CSP	Pin No. 20-Pin TSSOP	1/0	Description
V <sub>CC</sub>	24	1	_	Power supply bias for the RF PLL analog and digital circuits. V <sub>CC</sub> may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
V <sub>P</sub> RF	2	2	_	RF PLL charge pump power supply. Must be ≥ V <sub>CC</sub> .
D <sub>o</sub> RF	3	3	0	RF PLL charge pump output. The output is connected to the external loop filter, which drives the input of the VCO.
GND	4	4	_	Ground for the RF PLL digital circuitry.
f <sub>IN</sub> RF	5	5	I	RF PLL prescaler input. Small signal input from the VCO.
f <sub>IN</sub> RF	6	6	I	RF PLL prescaler complementary input. For single ended operation, this pin should be AC grounded. The LMX233xU RF PLL can be driven differentially when the bypass capacitor is omitted.
GND	7	7	_	Ground for the RF PLL analog circuitry.
OSC <sub>in</sub>	8	8	I	Reference oscillator input. The input has an approximate $V_{\rm CC}/2$ threshold and can be driven from an external CMOS or TTL logic gate.
GND	10	9	_	Ground for the IF PLL digital circuits, MICROWIRE™, F <sub>o</sub> LD, and oscillator circuits.
F₀LD	11	10	0	Programmable multiplexed output pin. Functions as a general purpose CMOS TRI-STATE output, RF/IF PLL push-pull analog lock detect output, N and R divider output or Fastlock output, which connects a parallel resistor to the external loop filter.
Clock	12	11	I	MICROWIRE Clock input. High impedance CMOS input. Data is clocked into the 22-bit shift register on the rising edge of Clock.
Data	14	12	I	MICROWIRE Data input. High impedance CMOS input. Binary serial data. The MSB of Data is shifted in first. The last two bits are the control bits.
LE	15	13	I	MICROWIRE Latch Enable input. High impedance CMOS input. When LE transitions HIGH, Data stored in the shift register is loaded into one of 4 internal control registers.
GND	16	14	_	Ground for the IF PLL analog circuitry.

#### Pin Descriptions (Continued)

Pin Name	Pin No. 24-Pin CSP	Pin No. 20-Pin TSSOP	I/O	Description
f <sub>IN</sub> IF	17	15	ı	IF PLL prescaler complementary input. For single ended operation, this pin
				should be AC grounded. The LMX233xU IF PLL can be driven differentially
				when the bypass capacitor is omitted.
f <sub>IN</sub> IF	18	16	I	IF PLL prescaler input. Small signal input from the VCO.
GND	19	17	_	Ground for the IF PLL digital circuitry, MICROWIRE, FoLD, and oscillator
				circuits.
D <sub>o</sub> IF	20	18	0	IF PLL charge pump output. The output is connected to the external loop
				filter, which drives the input of the VCO.
V <sub>P</sub> IF	22	19	_	IF PLL charge pump power supply. Must be $\geq V_{CC}$ .
V <sub>CC</sub>	23	20	_	Power supply bias for the IF PLL analog and digital circuits, MICROWIRE,
				F <sub>o</sub> LD, and oscillator circuits. V <sub>CC</sub> may range from 2.7V to 5.5V. Bypass
				capacitors should be placed as close as possible to this pin and be
				connected directly to the ground plane.
NC	1, 9, 13, 21	X		No connect.

#### **Ordering Information**

Model	Temperature Range	Package Description	Packing	NS Package Number
LMX2330USLBX	-40°C to +85°C	Chip Scale Package (CSP) Tape and Reel	2500 Units Per Reel	SLB24A
LMX2330UTM	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	73 Units Per Rail	MTC20
LMX2330UTMX	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP) Tape and Reel	2500 Units Per Reel	MTC20
LMX2331USLBX	-40°C to +85°C	Chip Scale Package (CSP) Tape and Reel	2500 Units Per Reel	SLB24A
LMX2331UTM	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	73 Units Per Rail	MTC20
LMX2331UTMX	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP) Tape and Reel	2500 Units Per Reel	MTC20
LMX2332USLBX	-40°C to +85°C	Chip Scale Package (CSP) Tape and Reel	2500 Units Per Reel	SLB24A
LMX2332UTM	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	73 Units Per Rail	MTC20
LMX2332UTMX	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP) Tape and Reel	2500 Units Per Reel	MTC20



#### Notes:

- 1. A 64/65 or 128/129 prescaler ratio can be selected for the LMX2331U and LMX2332U RF synthesizers. A 32/33 or 64/65 prescaler ratio can be selected for the LMX2330U RF synthesizer.
- 2. V<sub>CC</sub> supplies power to the RF and IF prescalers, RF and IF feedback dividers, RF and IF reference dividers, RF and IF phase detectors, the OSC<sub>in</sub> buffer, MICROWIRE, and F<sub>o</sub>LD circuitry.
- 3.  $V_P$  RF and  $V_P$  IF supply power to the charge pumps. They can be run separately as long as  $V_P$  RF  $\geq$   $V_{CC}$  and  $V_P$  IF  $\geq$   $V_{CC}$

#### Absolute Maximum Ratings (Notes 1,

2, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage

 $V_{\text{CC}}$  to GND -0.3V to +6.5V-0.3V to +6.5VV<sub>P</sub> RF to GND V<sub>P</sub> IF to GND -0.3V to +6.5V

Voltage on any pin to GND (V<sub>I</sub>)  $V_1$  must be < +6.5V-0.3V to  $V_{\rm CC}$ +0.3V -65°C to +150°C Storage Temperature Range (T<sub>S</sub>) Lead Temperature (solder 4 s) (T<sub>L</sub>) +260°C TSSOP  $\theta_{\mathsf{JA}}$  Thermal Impedance 114.5°C/W  $\text{CSP } \theta_{\text{JA}} \text{ Thermal Impedance}$ 112°C/W

#### **Recommended Operating** Conditions (Note 1)

Power Supply Voltage

 $V_{\text{CC}}$  to GND +2.7V to +5.5V V<sub>P</sub> RF to GND  $V_{\rm CC}$  to +5.5V  $V_{\rm CC}$  to +5.5V V<sub>P</sub> IF to GND Operating Temperature (T<sub>A</sub>) -40°C to +85°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, refer to the Electrical Characteristics section. The guaranteed specifications apply only for the conditions listed.

Note 2: This device is a high performance RF integrated circuit with an ESD rating <2 kV and is ESD sensitive. Handling and assembly of this device should only be done at ESD protected work stations.

Note 3: GND = 0V

#### **Electrical Characteristics**

 $V_{CC} = V_P RF = V_P IF = 3.0V, -40^{\circ}C \le T_A \le +85^{\circ}C$ , unless otherwise specified

Symbol	Parame	tor	Conditions		Value		Units
Зуппоп	Parame		Conditions	Min	Тур	Max	Office
I <sub>CC</sub> PARAM	ETERS						
$I_{CC_{RF + IF}}$	Power Supply	LMX2330U	Clock, Data and LE = GND		3.3	4.3	mA
	Current, RF + IF Synthesizers	LMX2331U	OSC <sub>in</sub> = GND PWDN RF Bit = 0		2.9	3.8	mA
		LMX2332U	PWDN IF Bit = 0		2.5	3.3	mA
I <sub>CCRF</sub>	Power Supply	LMX2330U	Clock, Data and LE = GND		2.3	3.0	mA
	Current, RF Synthesizer Only	LMX2331U	OSC <sub>in</sub> = GND PWDN RF Bit = 0		1.9	2.5	mA
		LMX2332U	PWDN IF Bit = 1		1.5	2.0	mA
I <sub>CCIF</sub>	Power Supply Current, IF Synthesizer Only	LMX233xU	Clock, Data and LE = GND OSC <sub>in</sub> = GND PWDN RF Bit = 1 PWDN IF Bit = 0		1.0	1.3	mA
I <sub>CC-PWDN</sub>	Powerdown Current	LMX233xU	Clock, Data and LE = GND OSC <sub>in</sub> = GND PWDN RF Bit = 1 PWDN IF Bit = 1		1.0	10.0	μА
RF SYNTHE	SIZER PARAMETERS		•			•	
f <sub>IN</sub> RF	RF Operating	LMX2330U		500		2500	MHz
	Frequency	LMX2331U		200		2000	MHz
		LMX2332U		100		1200	MHz
N <sub>RF</sub>	RF N Divider Range		Prescaler = 32/33 (Note 4)	96		65631	
			Prescaler = 64/65 (Note 4)	192		131135	
			Prescaler = 128/129 (Note 4)	384		262143	
R <sub>RF</sub>	RF R Divider Range			3		32767	
$F_{\phi RF}$	RF Phase Detector Fi	requency				10	MHz

**Electrical Characteristics** (Continued)  $V_{CC} = V_P \ RF = V_P \ IF = 3.0V, \ -40 \ C \le T_A \le +85 \ C, \ unless otherwise specified$ 

Cumbal	Dava		Conditions		Value		l lmita
Symbol	Para	meter	Conditions	Min	Тур	Max	Units
RF SYNTHE	SIZER PARAMETE	RS					
Pf <sub>IN</sub> RF	RF Input Sensitivity	/	$2.7V \le V_{CC} \le 3.0V$	-15		0	dBm
			(Note 5)				
			$3.0 < V_{CC} \le 5.5V$	-10		0	dBm
			(Note 5)				
ID <sub>o</sub> RF	RF Charge Pump	Output Source	$VD_o$ RF = $V_P$ RF/2		-0.95		mA
SOURCE	Current		ID <sub>o</sub> RF Bit = 0				
			(Note 6)				
			$VD_o RF = V_P RF/2$		-3.80		mA
			ID <sub>o</sub> RF Bit = 1				
			(Note 6)				
ID₀ RF	RF Charge Pump	Output Sink Current	$VD_o RF = V_P RF/2$		0.95		mA
SINK			ID <sub>o</sub> RF Bit = 0				
			(Note 6)				
			$VD_o RF = V_P RF/2$		3.80		mA
			ID <sub>o</sub> RF Bit = 1				
			(Note 6)				
$ID_oRF$	RF Charge Pump	Output TRI-STATE	$0.5V \le VD_o RF \le V_P RF - 0.5V$	-2.5		2.5	nA
TRI-STATE	Current		(Note 6)				
ID₀ RF		Output Sink Current	VD <sub>o</sub> RF = V <sub>P</sub> RF/2		3	10	%
SINK	Vs Charge Pump (	Output Source	$T_A = +25^{\circ}C$				
Vs	Current Mismatch		(Note 7)				
ID₀ RF							
SOURCE	RF Charge Pump Output Current						
ID <sub>o</sub> RF	RF Charge Pump Output Current Magnitude Variation Vs Charge Pump		$0.5V \le VD_o RF \le V_P RF - 0.5V$		10	15	%
Vs	_	n Vs Charge Pump	$T_A = +25^{\circ}C$				
VD <sub>o</sub> RF	Output Voltage		(Note 7)				-
ID <sub>o</sub> RF	RF Charge Pump	•	$VD_o RF = V_P RF/2$		10		%
Vs	Magnitude Variatio	n vs remperature	(Note 7)				
T <sub>A</sub>	SIZER PARAMETERS						
	SIZER PARAMETERS  IF Operating LMX2330U		T	45	T	000	T N 41 1-
f <sub>IN</sub> IF	' '			45		600	MHz
	Frequency LMX2331U			45		600	MHz
	LMX2332U			45		600	MHz
$N_{IF}$	IF N Divider Range		Prescaler = 8/9	24		16391	
			(Note 4)				-
			Prescaler = 16/17	48		32767	
	 		(Note 4)			00===	-
R <sub>IF</sub>	IF R Divider Range			3		32767	
$F_{\phiIF}$	IF Phase Detector	Frequency				10	MHz
Pf <sub>IN</sub> IF	IF Input Sensitivity		$2.7V \le V_{CC} \le 5.5V$	-10		0	dBm
			(Note 5)				

**Electrical Characteristics** (Continued)  $V_{CC} = V_P \; RF = V_P \; IF = 3.0V, \; -40^{\circ}C \leq T_A \leq +85^{\circ}C, \; unless \; otherwise \; specified$ 

Symbol	Parameter	Conditions		Value	,	Units
		Conditions	Min	Тур	Max	Omio
	SIZER PARAMETERS					
ID <sub>o</sub> IF	IF Charge Pump Output Source	$VD_o$ IF = $V_P$ IF/2		-0.95		mA
SOURCE	Current	$ID_o$ IF Bit = 0				
		(Note 6)				
		$VD_o$ IF = $V_P$ IF/2		-3.80		mA
		ID <sub>o</sub> IF Bit = 1				
ID IE	15.01	(Note 6)		0.05	-	-
ID <sub>o</sub> IF	IF Charge Pump Output Sink Current	$VD_o$ IF = $V_P$ IF/2		0.95		mA
SINK		ID <sub>o</sub> IF Bit = 0 (Note 6)				
		$VD_{O}$ IF = $V_{P}$ IF/2		2.00		m A
		$ VD_0 $ IF $= V_P$ IF/2 $ ID_0 $ IF Bit $= 1$		3.80		mA
		(Note 6)				
ID <sub>o</sub> IF	IF Charge Pump Output TRI-STATE	$0.5V \le VD_0 \text{ IF } \le V_P \text{ IF } - 0.5V$	-2.5		2.5	nA
TRI-STATE	Current	(Note 6)	-2.5		2.5	IIA
ID <sub>o</sub> IF	IF Charge Pump Output Sink Current	$VD_o$ IF = $V_P$ IF/2		3	10	%
SINK	Vs Charge Pump Output Source	$T_A = +25^{\circ}C$		3	10	70
Vs	Current Mismatch	(Note 7)				
ID <sub>o</sub> IF	Current Wishlaton	(Note 7)				
SOURCE						
ID <sub>o</sub> IF	IF Charge Pump Output Current	$0.5V \le VD_o \text{ IF} \le V_P \text{ IF} - 0.5V$		10	15	%
Vs	Magnitude Variation Vs Charge Pump	$T_A = +25^{\circ}C$				,,,
VD <sub>o</sub> IF	Output Voltage	(Note 7)				
ID <sub>o</sub> IF	IF Charge Pump Output Current	VD <sub>o</sub> IF = V <sub>P</sub> IF/2		10		%
Vs	Magnitude Variation Vs Temperature	(Note 7)				
$T_A$						
	R PARAMETERS		'		,	
Fosc	Oscillator Operating Frequency		2		40	MHz
V <sub>osc</sub>	Oscillator Sensitivity	(Note 8)	0.5		V <sub>cc</sub>	V <sub>PP</sub>
l <sub>osc</sub>	Oscillator Input Current	$V_{OSC} = V_{CC} = 5.5V$			100	μΑ
		$V_{OSC} = 0V, V_{CC} = 5.5V$	-100			μΑ
DIGITAL IN	TERFACE (Data, LE, Clock, F <sub>o</sub> LD)					
V <sub>IH</sub>	High-Level Input Voltage		0.8 V <sub>CC</sub>			V
V <sub>IL</sub>	Low-Level Input Voltage				0.2 V <sub>CC</sub>	V
I <sub>IH</sub>	High-Level Input Current	$V_{IH} = V_{CC} = 5.5V$	-1.0		1.0	μA
I <sub>IL</sub>	Low-Level Input Current	$V_{IL} = 0V, V_{CC} = 5.5V$	-1.0		1.0	μA
V <sub>OH</sub>	High-Level Output Voltage	I <sub>OH</sub> = -500 μA	V <sub>CC</sub> -			V
			0.4			
V <sub>OL</sub>	Low-Level Output Voltage	I <sub>OL</sub> = 500 μA			0.4	V
MICROWIRE	INTERFACE					
t <sub>cs</sub>	Data to Clock Set Up Time	(Note 9)	50			ns
t <sub>CH</sub>	Data to Clock Hold Time	(Note 9)	10			ns
t <sub>CWH</sub>	Clock Pulse Width HIGH	(Note 9)	50			ns
t <sub>CWL</sub>	Clock Pulse Width LOW	(Note 9)	50			ns
	<u> </u>	+			+	+
t <sub>ES</sub>	Clock to Load Enable Set Up Time	(Note 9)	50			ns

**Electrical Characteristics** (Continued)  $V_{CC} = V_P \; RF = V_P \; IF = 3.0V, \; -40^{\circ}C \leq T_A \leq +85^{\circ}C, \; unless \; otherwise \; specified$ 

Cumbal	Davamat		Conditions		Value		I I mit m
Symbol	Paramet	er	Conditions	Min	Тур	Max	Units
PHASE NO	ISE CHARACTERISTICS	3		•			
L <sub>N</sub> (f) RF	RF Synthesizer Norma	lized Phase	TCXO Reference Source		-212.0		dBc/
	Noise Contribution		ID <sub>o</sub> RF Bit = 1				Hz
	(Note 10)						
L(f) RF	RF Synthesizer Single	LMX2330U	$f_{IN}$ RF = 2450 MHz		-77.24		dBc/
	Side Band Phase		f = 1 kHz Offset				Hz
	Noise Measured		$F_{\phi RF} = 200 \text{ kHz}$				
			Loop Bandwidth = 7.5 kHz				
			N = 12250				
			F <sub>OSC</sub> = 10 MHz				
			$V_{OSC} = 0.632 V_{PP}$				
			ID <sub>o</sub> RF Bit = 1				
			PWDN IF Bit = 1				
			$T_A = +25^{\circ}C$				
			(Note 11)				
		LMX2331U	f <sub>IN</sub> RF = 1960 MHz		-79.18		dBc/
			f = 1 kHz Offset				Hz
			$F_{\phi RF} = 200 \text{ kHz}$				
			Loop Bandwidth = 15 kHz				
			N = 9800				
			F <sub>OSC</sub> = 10 MHz				
			$V_{OSC} = 0.632 V_{PP}$				
			ID <sub>o</sub> RF Bit = 1				
			PWDN IF Bit = 1				
			$T_A = +25^{\circ}C$				
			(Note 11)				
		LMX2332U	$f_{IN} RF = 900 MHz$		-85.94		dBc/
			f = 1 kHz Offset				Hz
			$F_{\phi RF} = 200 \text{ kHz}$				
			Loop Bandwidth = 12 kHz				
			N = 4500				
			F <sub>OSC</sub> = 10 MHz				
			$V_{OSC} = 0.632 V_{PP}$				
			ID <sub>o</sub> RF Bit = 1				
			PWDN IF Bit = 1				
			$T_A = +25^{\circ}C$				
			(Note 11)				

#### **Electrical Characteristics** (Continued)

 $V_{CC} = V_P RF = V_P IF = 3.0V, -40^{\circ}C \le T_A \le +85^{\circ}C$ , unless otherwise specified

Cumbal	Davamat	<b>.</b>	Conditions		Value		Unite
Symbol	Paramet	ier	Conditions	Min	Тур	Max	Units
PHASE NOI	SE CHARACTERISTICS	S					
L <sub>N</sub> (f) IF	IF Synthesizer Normal	ized Phase	TCXO Reference Source		-212.0		dBc/
	Noise Contribution		ID <sub>o</sub> IF Bit = 1				Hz
	(Note 10)						
L(f) IF	IF Synthesizer Single	LMX233xU	f <sub>IN</sub> IF = 200 MHz		-99.00		dBc/
	Side Band Phase		f = 1 kHz Offset				Hz
	Noise Measured		$F_{\phi IF} = 200 \text{ kHz}$				
			Loop Bandwidth = 18 kHz				
			N = 1000				
			F <sub>OSC</sub> = 10 MHz				
			$V_{OSC} = 0.632 V_{PP}$				
			ID <sub>o</sub> IF Bit = 1				
			PWDN RF Bit = 1				
			$T_A = +25^{\circ}C$				
			(Note 11)				

**Note 4:** Some of the values in this range are illegal divide ratios (B < A). To obtain continuous legal division, the Minimum Divide Ratio must be calculated. Use N  $\geq$  P \* (P-1), where P is the value of the prescaler selected.

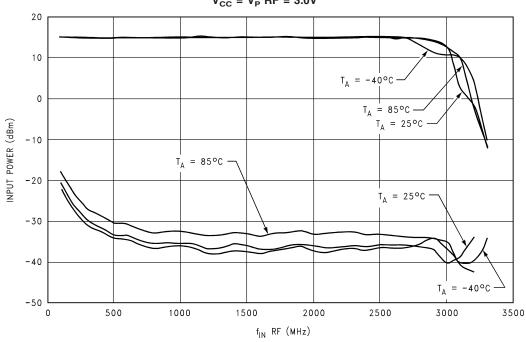
- Note 5: Refer to the LMX233xU f<sub>IN</sub> Sensitivity Test Setup section
- Note 6: Refer to the LMX233xU Charge Pump Test Setup section
- Note 7: Refer to the Charge Pump Current Specification Definitions for details on how these measurements are made.
- Note 8: Refer to the LMX233xU OSC<sub>in</sub> Sensitivity Test Setup section
- Note 9: Refer to the LMX233xU Serial Data Input Timing section

Note 10: Normalized Phase Noise Contribution is defined as :  $L_N(f) = L(f) - 20 \log (N) - 10 \log (F_{\phi})$ , where L(f) is defined as the single side band phase noise measured at an offset frequency, f, in a 1 Hz bandwidth. The offset frequency, f, must be chosen sufficiently smaller than the PLL's loop bandwidth, yet large enough to avoid substantial phase noise contribution from the reference source. N is the value selected for the feedback divider and  $F_{\phi}$  is the RF/IF phase detector comparison frequency.

Note 11: The synthesizer phase noise is measured with the LMX2330TMEB/LMX2330SLBEB Evaluation boards and the HP8566B Spectrum Analyzer.

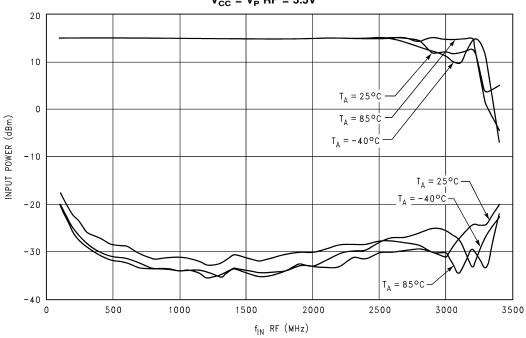
## **Typical Performance Characteristics Sensitivity**





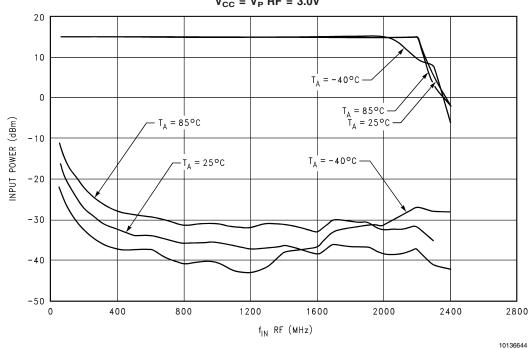
10136642

### LMX2330U f<sub>IN</sub> RF Input Power Vs Frequency $V_{CC} = V_P$ RF = 5.5V

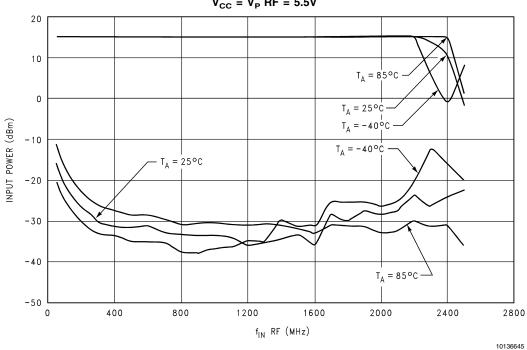


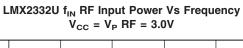
10136643

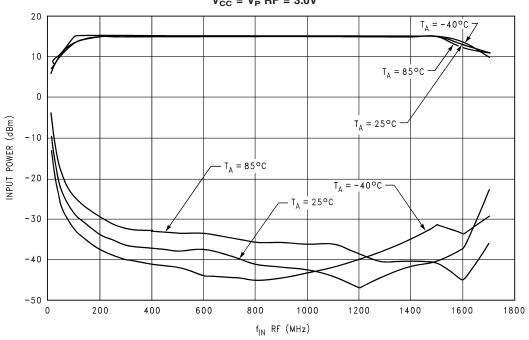




### LMX2331U $f_{IN}$ RF Input Power Vs Frequency $V_{CC}$ = $V_P$ RF = 5.5V

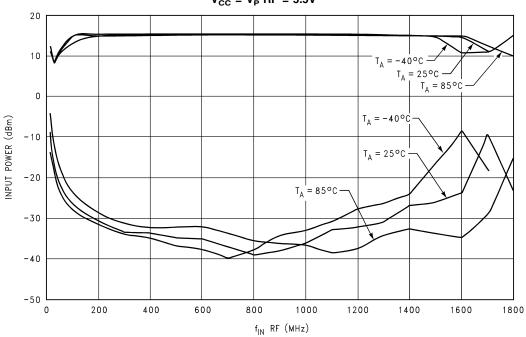




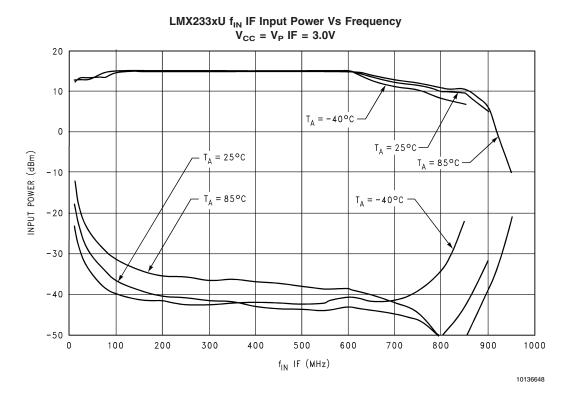


10136646

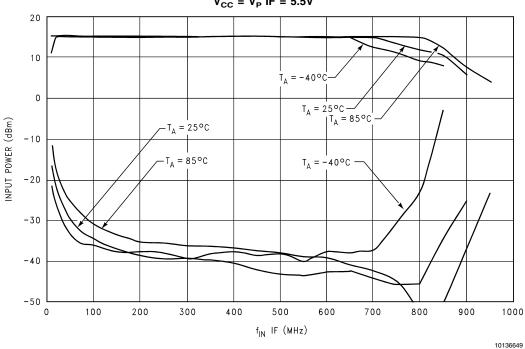
## LMX2332U $f_{IN}$ RF Input Power Vs Frequency $V_{CC}$ = $V_{P}$ RF = 5.5V

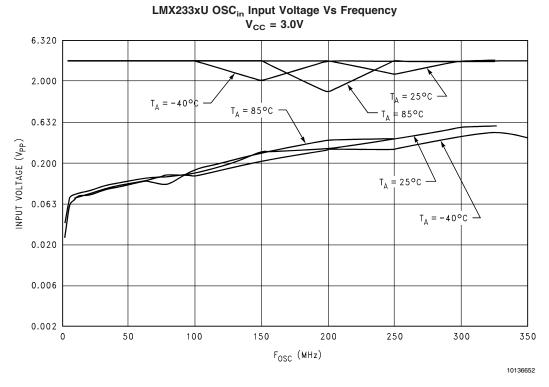


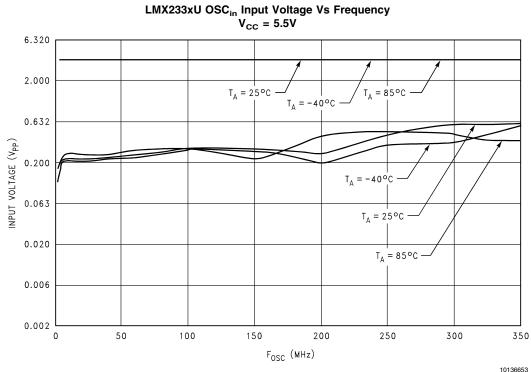
10136647



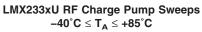
### LMX233xU $f_{IN}$ IF Input Power Vs Frequency $V_{CC} = V_P$ IF = 5.5V

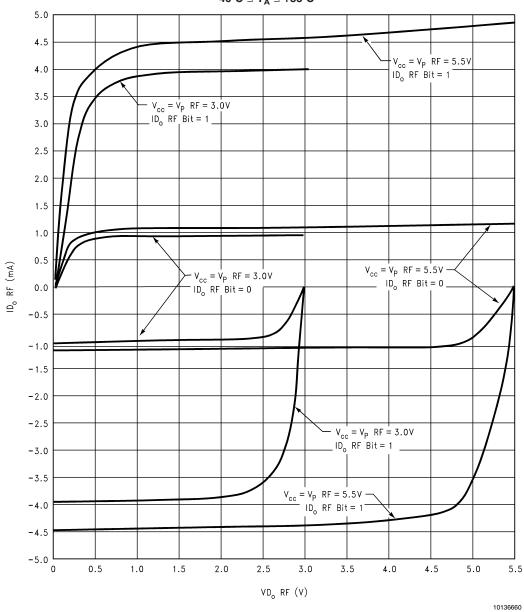




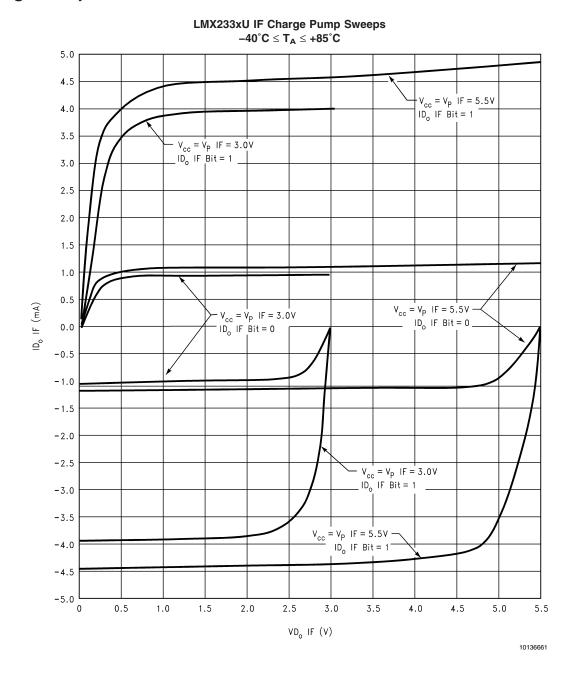


## **Typical Performance Characteristics Charge Pump**





## Typical Performance Characteristics Charge Pump (Continued)

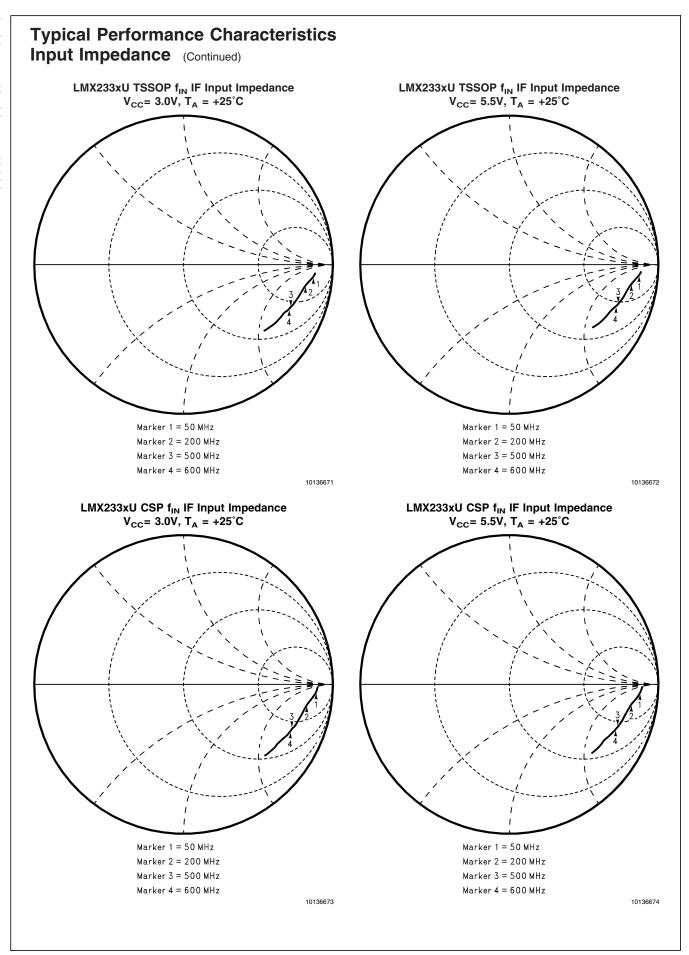


## **Typical Performance Characteristics Input Impedance** LMX233xU TSSOP $f_{IN}$ RF Input Impedance $V_{CC}$ = 3.0V, $T_{A}$ = +25°C LMX233xU TSSOP $f_{IN}$ RF Input Impedance $V_{CC}$ = 5.5V, $T_A$ = +25°C Marker 1 = 900 MHz Marker 1 = 900 MHz Marker 2 = 1800 MHz Marker 2 = 1800 MHz Marker 3 = 1900 MHz Marker 3 = 1900 MHz Marker 4 = 2500 MHz Marker 4 = 2500 MHz 10136667 LMX233xU CSP $f_{IN}$ RF Input Impedance $V_{CC}$ = 3.0V, $T_A$ = +25°C LMX233xU CSP $f_{IN}$ RF Input Impedance $V_{CC}$ = 5.5V, $T_A$ = +25°C Marker 1 = 900 MHz Marker 1 = 900 MHz Marker 2 = 1800 MHz Marker 2 = 1800 MHz Marker 3 = 1900 MHz Marker 3 = 1900 MHz Marker 4 = 2500 MHz Marker 4 = 2500 MHz 10136668 10136669

LMX233xU TSSOP and LMX233xU CSP f<sub>IN</sub> RF Input Impedance Table

				LM)	X233xU TSSOP Zf <sub>IN</sub> RF	SSOP	Zf <sub>IN</sub> RF							5	LMX233xU CSP	1	Zf <sub>IN</sub> RF			
		V <sub>CC</sub> = V <sub>F</sub>	, RF = 3.0	$V_{CC} = V_P RF = 3.0V (T_A = 25)$	(2)		V <sub>CC</sub> = V <sub>P</sub> RF	RF = 5.5V	V (TA = 25°C)	(၃)	>	V <sub>CC</sub> = V <sub>P</sub>	RF = 3.0V	V (TA = 25°C)	(2)		V <sub>CC</sub> = V <sub>P</sub>	P RF = 5.5V	5V (T <sub>A</sub> = 25°C)	(S)
f <sub>in</sub> RF (MHz)	딥	77	Zfin RF (D)	Zfin RF (\O)	IZf <sub>in</sub> RFI (Ω)	드	7	æ Zfin RF (Ω)	%, Zf <sub>in</sub> RF (Ω)	IZf <sub>in</sub> RFI (Ω)	드	7	Zfin RF (D)	% Zf <sub>in</sub> RF (Ω)	IZf <sub>in</sub> RFI (Ω)	드	7	25 Zfin RF (D)	<i>γ,</i> Zf <sub>in</sub> RF (Ω)	IZf <sub>liv</sub> RFI (Ω)
100	0.862	0.862 -6.23	439.774	439.774 -319.866	543.798	0.862	-6.07	448.230	-318.841	550.064	0.864	-6.44	431.004	-330.013	542.838	0.864	-6.30	438.240	-327.814	547.281
200	0.834	-9.30	0.834 -9.30 307.614 -272.274	-272.274	410.803 0.834		-9.00	316.479 -271.581		417.031	0.836	-9.88	291.252	291.252  -277.923	402.577	0.836	-9.57	300.190	-277.552	408.838
300	0.820	-12.11	0.820 -12.11 237.700 -249.291	-249.291	344.452	0.821	-11.66	247.264	-251.098	352.406	0.821	-13.24	215.318	-248.361	328.702	0.821	-12.76	224.624	-249.637	335.819
400	0.808	-15.25	0.808 -15.25 185.048 -227.171	-227.171	293.001	0.808	-14.61	0.808 -14.61 194.668 -229.054	-229.054	300.601	0.808 -16.88	16.88	163.190 -219.893	-219.893	273.832		0.808 -16.24	171.345	-222.518	280.844
200	0.796	-18.51	0.796 -18.51 147.785 -203.923	-203.923	251.843	0.796	-17.66	156.935	251.843 0.796 -17.66 156.935 -207.313 260.014	260.014	0.793	20.90	126.193	0.793 -20.90 126.193 -191.939	229.707 0.794 -20.00 133.885	0.794	-20.00	133.885	-196.200	237.528
009	0.781	-21.81	0.781 -21.81 122.091 -181.461	-181.461	218.710		-20.70	0.782 -20.70 130.906 -185.850	-185.850	227.325	0.775 -24.82		102.956	-168.026	197.060	0.777	0.777 -23.70	109.531	-172.887	204.663
700	0.765	-24.72	0.765 -24.72 106.107 -163.758	-163.758	195.129	0.767	-23.45	113.780	195.129 0.767 -23.45 113.780 -168.514 203.329		0.749 -28.29		90.820	-146.582	-146.582 172.437 0.752 -27.02	0.752	-27.02	96.279	-151.333	179.363
800	0.760	-28.35	0.760 -28.35 87.984 -150.524	-150.524	174.352	0.762	-26.97	94.255	-155.481 181.819		0.742	-31.22	79.737	-136.782	158.327	0.746	0.746 -29.85	84.470	-141.473	164.772
900	0.747	-32.60	73.777	0.747 -32.60 73.777 -134.500	153.406 0.750 -30.95	0.750	-30.95		79.270 -139.668 160.596	160.596	0.739 -36.04		64.577	-123.951	139.764		0.742 -34.37	900.69	-128.610	145.954
1000	0.732	-36.68	0.732 -36.68 64.122 -120.908	-120.908	136.859 0.735 -34.73	0.735	-34.73	69.215	69.215 -126.104 143.851		0.719 -41.44	- 1	55.019	-108.415	-108.415 121.577 0.723 -39.46	0.723	-39.46	58.684	-113.123	127.439
1100	0.717	0.717 -41.25	55.780	55.780 -108.398	121.908	0.720	0.720 -39.12	60.041	-113.215	128.151	0.694	-47.27	48.056	-94.403	105.931	0.698	0.698 -45.08	51.159	-98.547	111.035
1200	0.698	-46.24	0.698 -46.24 49.180	-96.605	108.403	0.702	0.702 -43.84	52.848	-101.254 114.216	114.216	0.669 -53.59	53.59	42.269	-82.401	92.610	0.674	-51.01	45.061	-86.388	97.434
1300		-51.43	0.678 -51.43 43.982	-86.291	96.853	0.683	0.683 -48.77	47.173	-90.676	102.212	0.641 -60.42	- 1	37.856	-71.653	81.039	0.647	0.647 -57.50	40.230	-75.400	85.461
1400	0.663	0.663 -56.68	39.397	-77.901	87.296	0.667	0.667 -53.71	42.317	-82.070	92.337	0.610 -68.33	68.33	34.108	-61.481	70.308	0.613	0.613 -64.90	36.477	-64.872	74.424
1500		-62.08	0.649 -62.08 35.566	-70.500	78.963		0.653 -58.74	38.281	-74.569	83.821	0.577 -77.01	- 1	31.049	-52.388	60.898	0.581	0.581 -73.18	33.064	-55.554	64.649
1600	0.630	0.630 -67.58	32.912	-63.544	71.562	0.634	-63.96	35.335	-67.423	76.121	0.539	-84.86	29.732	-44.952	53.895	0.543	-80.36	31.654	-48.119	57.597
1700	$\overline{}$	-72.22	0.608 -72.22 31.565	-57.996	66.030	0.614	0.614 -68.51	33.590	-61.632	70.191	0.477	27.97	0.477 -27.97 100.359	-58.171	115.999		0.487 -84.99	33.106	-42.105	53.562
1800	0.596	-75.66	1800 0.596 -75.66 30.440 -54.462	-54.462	62.392	0.601	0.601 -71.81	32.358	-57.943	66.366	0.455	89.90	32.829	-37.624	49.933	0.468	0.468 -85.87	33.886	-40.554	52.847
1900	$\overline{}$	-80.06	0.598 -80.06 27.915	-51.164	58.284	0.602	0.602 -76.22	29.678	-54.335	61.912	0.493	87.34	29.357	-38.214	48.189	0.500	0.500 -88.90	29.576	-39.369	49.241
2000	$\overline{}$	-85.31	0.607 -85.31 24.914	-47.651	53.771	0.607	0.607 -81.32	26.675	-50.603	57.203	0.520 79.89	79.89	25.120	-35.225	43.264	0.521	84.05	26.396	-37.576	45.921
2100	0.612	89.24	0.612 89.24 22.502	-43.994	49.414	0.611	0.611 -86.42	21.612	45.064	47.292	0.529 70.97	70.97	22.177	-30.771	37.930	0.525	0.525 75.52	23.556	-33.043	40.580
2200		0.605 84.09	21.289	-40.358	45.629	0.602	88.61	22.901	-43.251	48.940	0.531	61.99	20.155	-26.331	33.159	0.524	66.93	21.544	-28.595	35.802
2300	$\overline{}$	0.594 78.44	20.367	-36.566	41.855	0.589	83.13	21.961	-39.298	45.018	0.533	52.71	18.533	-21.975	28.747	0.525	57.61	19.706	-24.119	31.146
2400	0.590	72.27	2400 0.590 72.27 19.111	-32.907	38.054	0.584	0.584 77.11	20.598	-35.536	41.074	0.550 43.18	43.18	16.578	-17.883	24.385	0.537	0.537 47.69	17.671	-19.749	26.501
2500		0.586 67.24	18.297	-30.064	35.194	0.576 72.09	72.09	19.792	-32.516	38.066	0.583 34.44		14.340	-14.328	20.272	0.566	0.566 38.69	15.416	-16.055	22.257

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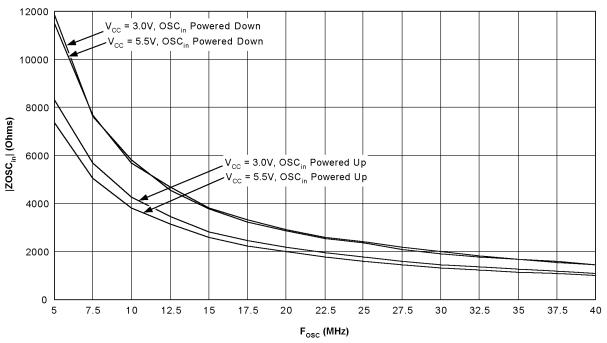


LMX233xU TSSOP and LMX233xU CSP fin IF Input Impedance Table

Canal Form   Can	LMX233XU TSSOP Zf <sub>IN</sub> IF V <sub>CC</sub> = V <sub>P</sub> IF = 3.0V (T <sub>A</sub> = 25°C) V <sub>CC</sub> = V	33×U TSS	33×U TSS	33×U TSS	SSOP Zf	🔚 ˈo	NF = V <sub>P</sub>  F =	IF = 5.5V	5.5V (T <sub>A</sub> = 25°C)	ွ		V <sub>CC</sub> = V	= V <sub>P</sub> IF = 3.0V	3.0V (T <sub>A</sub> = 25°C)	LMX233xU CSP 5°C)	CSP 2	Zf <sub>IN</sub> IF	/ <sub>P</sub> IF = 5.5	'fin IF V <sub>CC</sub> = Vp IF = 5.5V (T <sub>A</sub> = 25°C)	
86 - 3.81         630.568 - 340.996         716.864         0.899 - 1.69         716.2408         0.899 - 1.69         722.583         907.340         0.899 - 1.67         737 - 239.188           773 - 5.18         511.352 - 338.259         613.107         0.891 - 3.44         683.12 - 354.024         769.408         0.891 - 3.43         692.599 - 3.49.036           161 - 6.24         4.38.666 - 318.001         518.001         541.805         0.889 - 4.98         555.334 - 360.736         645.533         0.889 - 4.85         543.907         357.167           152 - 7.10         391.644 - 287.162         485.86 - 7.26         388.975 - 319.049         508.695 - 7.98         562.00 - 303.914           337 - 7.10         391.644 - 287.684         430.020         0.865 - 8.18         346.599 - 339.296         569.840         0.886 - 6.06         454.188         377.65         377.66         645.53         0.886 - 7.07         397.015 - 317.892         377.66         645.53         0.886 - 7.07         397.016 - 317.892         377.66         685.00 - 7.98         685.00 - 7.98         685.00 - 818         346.50         986.040         986.86 - 7.07         397.015 - 317.892         377.016         377.66         377.66         377.66         377.66         377.66         377.66         377.66         377.66         377.017 <th><math display="block">\begin{array}{c ccccccccccccccccccccccccccccccccccc</math></th> <th>26 /m   Zf<sub>IN</sub>   E Zf<sub>IN</sub>   E Zf<sub>IN</sub>   E (Ω)</th> <th>2fin IF (Ω)</th> <th>Z Z</th> <th>E (E</th> <th>` <u></u></th> <th>,</th> <th>Zfin IF</th> <th>2/m Zfin IF (Ω)</th> <th>IZf<sub>in</sub>IFI (Ω)</th> <th>1</th> <th>7</th> <th>Zfin IF (Ω)</th> <th>24 / 24 / 24 / 24 / 24 / 24 / 24 / 24 /</th> <th>Zf<sub>IN</sub> IFI (Ω)</th> <th>드</th> <th>7</th> <th>Zfin IF</th> <th>/m Zf<sub>IN</sub> IF (Ω)</th> <th>Zf<sub>IN</sub> IFI (Ω)</th>	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	26 /m   Zf <sub>IN</sub>   E Zf <sub>IN</sub>   E Zf <sub>IN</sub>   E (Ω)	2fin IF (Ω)	Z Z	E (E	` <u></u>	,	Zfin IF	2/m Zfin IF (Ω)	IZf <sub>in</sub> IFI (Ω)	1	7	Zfin IF (Ω)	24 / 24 / 24 / 24 / 24 / 24 / 24 / 24 /	Zf <sub>IN</sub> IFI (Ω)	드	7	Zfin IF	/m Zf <sub>IN</sub> IF (Ω)	Zf <sub>IN</sub> IFI (Ω)
0.852 - 5.18 511.352 - 338.259 613.107 0.891 - 3.44 683.122 - 354.024 769.408 0.891 - 3.33 692.599 3-49.036 775.577 650.739 0.861 - 6.24 436.666 - 318.001 541.805 0.868 - 6.23 445.399 3-392.995 559.840 0.868 - 6.06 454.188 - 337.263 565.715 0.844 - 7.90 356.461 - 287.182 493.650 0.868 - 6.23 445.399 3-392.995 559.840 0.868 - 6.06 454.188 - 337.263 565.715 0.844 - 7.90 356.461 - 287.182 455.056 0.868 - 7.25 388.975 3-19.049 503.065 0.868 - 7.07 397.015 - 317.892 508.603 0.837 - 8.57 330.546 - 275.058 1-30.020 0.850 - 3.18 348.16 - 303.517 462.229 0.850 - 7.98 356.200 - 303.914 468.233 0.832 - 3.22 306.296 - 257.480 40.8913 0.834 - 10.77 267.263 2.91.646 430.360 0.844 - 8.84 324.033 - 291.128 455.606 0.832 - 3.05 296 - 257.480 1.054 2.00.200 0.830 - 10.77 267.263 2.27.027 382.740 1.055 0.859 - 11.24 257.659 - 257.4417 371.482 0.834 - 10.77 267.263 2.27.027 382.740 0.839 - 11.24 257.657 - 247.511 354.299 0.830 - 11.55 247.027 382.740 0.839 - 11.24 257.657 - 247.511 354.299 0.830 - 11.55 247.027 382.740 0.839 - 11.24 257.657 - 247.511 354.299 0.830 - 11.55 247.027 382.740 0.829 - 11.24 257.657 - 247.511 354.299 0.830 - 11.55 247.027 382.740 0.839 - 11.24 257.657 - 247.511 354.299 0.830 - 11.55 247.027 382.740 0.839 - 11.24 256.102 - 256.244 30.849 0.839 - 11.25 247.027 382.740 0.839 - 11.24 256.102 - 257.80 382.740 0.839 - 11.25 247.857 382.740 0.839 - 11.24 257.857 382.740 0.839 - 11.25 247.857 382.740 0.839 - 11.25 247.857 382.740 0.839 - 11.25 247.857 382.740 0.839 - 11.24 256.857 382.740 0.839 - 11.25 247.857 382.740 0.839 - 11.25 247.857 382.740 0.839 1.12.23 0.839 1.12.23 183.858 2.234 2.234 2.2455 2.2399 2.244.57 382.849 0.830 1.14.44 198.121 - 224.662 2.234 0.830 1.12.24 2.234 2.2455 2.234 2.2455 2.224.557 3.20316 0.234 2.2455 2.245	0.884 -3.93 621.523 -345.924 711.305 0.8	621.523 -345.924 711.30	-345.924 711.30	711.30	S.	83	-	30.568	340.995	716.864	0.899		874.934	-242.583	907.940	0.899	-1.67	874.127	-239.189	906.261
0.852	0.873 -5.30 503.424 -340.786 607.923	503.424 -340.786 607.923	-340.786 607.923	607.923		0.873								-354.024		0.891	-3.33	692.599	-349.036	775.577
0.882         -7.10         391.664         -300.482         493.650         0.888         -6.23         445.399         -339.295         559.840         0.888         -6.06         454.188         -377.283         565.715         -300.482         -7.20         386.41         -287.182         457.753         0.889         -7.29         0.888         -7.20         386.41         -287.182         457.753         0.889         -7.20         0.860         -7.29         366.200         -303.914         468.233         0.889         -2.20         -303.914         468.233         0.889         -2.20         <	0.861   -6.42   429.629   -319.996   535.704   0.8	429.629 -319.996 535.704	-319.996 535.704	535.704	_	9	6.24 4	38.666		541.805	0.880		535.334	-360.736	645.533	0.879	-4.85		-357.157	650.739
0.82         -7.90         366.461         -287.182         457.753         0.869         -7.96         0.860         -7.98         366.200         -303.914         468.233           0.82         -8.57         330.546         -275.088         430.020         0.860         -8.18         348.616         -303.517         462.29         0.860         -7.98         366.200         -303.914         468.233           0.82         -8.2         306.264         -28.14         408.813         0.843         -9.07         316.481         -291.646         408.66         0.884         -10.45         276.02         -282.345         410.254           0.82         -10.64         270.659         -264.417         371.462         0.884         -10.47         267.102         327.402         382.340         0.880         -10.45         276.02         -276.02         276.02         -276.02         -286.345         40.666         0.889         -9.06         28.34         40.666         0.889         -9.06         28.34         40.666         0.889         -9.06         28.34         40.666         0.889         -9.06         27.83         282.342         40.4666         0.889         -9.06         28.34         40.666         0.889 <th< td=""><td>0.851 -7.27 384.494 -301.186 488.414</td><td>384.494 -301.186 488.414</td><td>-301.186 488.414</td><td>488.414</td><td></td><td></td><td></td><td>91.664 -</td><td>_</td><td>493.650</td><td>0.868</td><td><math>\overline{}</math></td><td>445.309</td><td>-339.295</td><td>559.840</td><td>0.868</td><td></td><td>454.188</td><td>-337.263</td><td>565.715</td></th<>	0.851 -7.27 384.494 -301.186 488.414	384.494 -301.186 488.414	-301.186 488.414	488.414				91.664 -	_	493.650	0.868	$\overline{}$	445.309	-339.295	559.840	0.868		454.188	-337.263	565.715
0.827         -9.22         306.266         -275.068         430.020         0.880         -8.18         349.616         -303.517         462.229         0.880         -7.98         366.200         -303.914         468.233           0.827         -9.22         309.266         -267.480         408.913         0.841         -20.7         316.481         -291.666         10.893         -9.66         27.640         -282.345         410.254           0.827         -9.95         288.264         -260.187         31.462         0.883         -10.77         267.263         -27.027         382.780         0.834         -10.46         27.666         0.883         -9.66         27.607         22.346         40.254         382.780         388.034         40.254         382.780         0.883         -10.46         267.705         382.780         0.883         -10.47         267.705         344.532         0.883         -10.250         228.671         267.705         344.532         0.883         -10.26         228.671         267.705         344.532         0.882         -12.50         228.671         226.705         344.532         0.882         -12.50         228.671         226.705         344.532         0.826         -12.28         388.719	0.844 -8.11 349.099 -288.744 453.038 0.8	349.099  -288.744   453.038	-288.744 453.038	453.038		44	7.90	56.461	287.182	457.753	0.858		388.975	-319.049	503.085	0.858		397.015	-317.892	508.603
0.822 - 9.22         309.206 - 267.400         408.913 0 0.834 - 9.07         316.481 - 291.646         409.606 0 0.839 - 9.66         297.640         282.345         410.254           0.822 - 4.95 2 288.264 - 260.187 388.322 0 0.838 - 9.93 2 289.893 - 282.342         404.666 0 0.839 - 9.66         297.640         282.345         410.254           0.823 - 10.64 270.659 2 254.417 371.462 0 0.834 - 10.77 2 67.263 2 74.027         382.780 0 0.834 - 10.45 27.662         274.027 382.780         0.834 - 10.45 27.672 2 73.085 380.03         388.034 0 0.834 - 10.45 27.624 3 880.03         388.034 0 0.834 - 10.45 27.624 3 880.03         388.034 0 0.834 - 10.45 27.624 3 880.03         388.034 0 0.834 - 10.45 27.624 3 880.03         388.034 0 0.834 - 10.45 27.627 2 73.085 380.03         388.034 0 0.834 - 10.45 27.627 2 72.020         388.034 0 0.826 - 12.03 2 74.027 3 82.030         388.034 0 0.826 - 12.03 2 74.027 3 82.030         388.034 0 0.826 - 12.03 2 74.027 3 82.030         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 2 880.03         388.034 0 0.826 - 12.250 8 80.03         388.034 0 0.826 - 12.250 8 80.03         388.034	0.837   -8.85   322.082   -276.707   424.622   0.8	322.082 -276.707 424.622	-276.707 424.622	424.622		37		30.546		430.020	0.850		348.616	-303.517	462.229	0.850	-7.98	356.200	-303.914	468.233
0.823         -9.95         288.264         -260.187         388.322         0.838         -9.93         289.893         -282.342         40.4666         0.839         -9.66         297.640         -282.345         410.254           0.823         -10.64         270.659         -254.417         371.462         0.834         -10.77         267.263         -274.027         382.780         0.834         -10.45         275.672         -273.085         388.034           0.818         -11.38         253.507         -247.511         354.299         0.830         -11.63         247.024         -265.175         362.407         0.829         -11.24         256.102         -265.264         368.034           0.815         -12.14         237.587         -241.965         339.109         0.826         -12.50         226.287         362.30         0.822         -13.38         212.305         -260.287         368.03         -13.223         368.93         -14.23         188.231         -242.453         313.176         0.829         -14.63         182.74         -257.00         368.93         -242.453         313.176         0.829         -14.23         388.034         -282.845         -282.845         388.134         -282.845         388.134         -	0.832 -9.54 300.314 -268.356 402.745 0.832	300.314 -268.356 402.745	-268.356 402.745	402.745			9.22	09.296	267.480	408.913	0.843		316.481	-291.646	430.369	0.844	-8.84	324.033		435.606
0.823         -10.64         270.669         -254.417         371.462         0.834         -10.77         267.263         -274.027         382.780         0.834         -10.45         275.672         -273.085         388.034           0.818         -11.38         253.507         -247.511         354.299         0.830         -11.63         247.024         -265.175         362.407         0.829         -11.24         256.102         -265.264         368.719           0.815         -12.13         253.507         -247.511         354.299         0.830         -11.63         247.024         -265.176         344.532         0.826         -12.08         257.803         256.264         368.719           0.815         -12.14         237.587         -241.965         329.109         0.826-12.50         228.671         -257.705         344.532         0.826         -12.90         221.471         -251.212         334.899           0.807         -13.62         132.223         0.819-14.23         198.231         -242.453         313.176         0.816         -13.60         0.816-15.21         188.231         -242.453         313.176         0.816         -13.63         222.445         313.176         0.816         -13.60         221.471	0.827   -10.29   279.576   -260.995   382.467	279.576  -260.995   382.467	-260.995 382.467	382.467			9.95	88.264 -	260.187	388.322	0.838		289.893	-282.342	404.666	0.839	-9.66			410.254
1.818         -1.1.38         255.507         -247.511         354.299         0.830         -11.63         247.024         -265.175         362.407         0.829         -11.24         256.264         265.175         362.407         0.829         -11.24         256.262         257.803         256.264         368.719         360.652           1.815         -12.14         237.587         -241.965         339.109         0.826         -12.50         237.603         -257.879         350.652           1.811         -12.84         224.277         -236.738         326.106         0.823         -13.28         212.305         -250.287         328.033         0.822         -12.90         221.471         -251.212         334.839           1.807         -13.62         10.927         -230.202         312.223         0.819         -14.23         198.231         -24.433         31.776         0.826         -13.73         206.868         -24.557         320.316           1.807         -14.44         198.121         -224.602         299.497         0.812-16.09         172.186         -227.189         285.066         0.815-16.48         180.755         -229.880         292.435           1.804         -15.20         187.411         -2	0.823 -11.04 261.205 -254.758 364.870 0				0	.823	10.64 2	- 659.02			0.834	10.77	267.263		382.780	0.834	-10.45		-273.085	388.034
1.815         1.2.14         237.587         -241.965         339.109         0.826         -12.50         228.671         -257.705         344.532         0.826         -12.08         237.603         -257.879         350.652           1.811         -12.84         224.277         -236.738         326.106         0.823         -13.38         212.305         -250.287         328.203         0.822         -12.90         221.471         -251.212         334.899           1.807         -13.62         210.927         -230.202         312.223         0.819         -14.23         198.231         -242.453         313.176         0.819         -13.73         206.868         -244.557         320.316           1.807         -13.62         210.927         -230.202         312.223         0.819         -14.23         198.231         -24.453         313.176         0.819         -13.73         206.868         -244.557         320.316           1.807         -14.44         198.121         -229.89         0.812         -16.09         172.185         -227.189         285.066         0.812         -16.69         -227.189         285.066         0.812         -16.38         180.084         -244.357         -227.89         287.38         -227.89	0.819 -11.80 244.399 -248.227 348.350 0.8	244.399 -248.227 348.350 0	-248.227 348.350 0	348.350	0	.818	11.38 2	- 23.507		354.299	0.830	11.63	247.024	-265.175	362.407	0.829	-11.24		-265.264	368.719
0.807         -12.84         224.277         -236.738         326.106         0.823         -13.36         226.287         328.203         0.822         -12.90         221.471         -251.212         334.899           0.807         -13.62         210.927         -230.202         312.223         0.819         -14.23         198.231         -242.453         313.176         0.819         -13.73         206.868         -244.557         320.316           0.804         -14.44         198.121         -224.602         299.497         0.816         -15.21         183.656         -234.712         298.025         0.815         -14.63         305.740         -236.735         305.274           0.804         -15.20         172.18         172.186         -227.186         285.066         0.812         -16.03         172.186         -227.189         285.066         0.812         -16.03         172.186         -227.189         285.066         0.812         -16.03         172.186         -227.189         285.066         0.812         -16.03         172.186         -227.189         285.066         0.812         -16.03         172.186         -227.189         285.066         0.812         -16.89         141.126         -203.252         203.26         1	0.814 -12.58 228.964 -241.239 332.597					0.815 -	12.14 2	- 282.78	241.965	339.109	0.826	12.50			344.532	0.826	-12.08		-257.879	350.652
0.807         -13.62         210.927         -230.202         312.223         0.819         -14.23         198.231         -242.455         313.176         0.819         -13.73         206.868         -244.557         320.316           0.804         -14.44         198.121         -224.602         299.497         0.816         -15.21         183.656         -234.712         298.025         0.815         -14.63         192.740         -236.735         305.274           0.801         -15.20         187.401         -219.200         288.388         0.812         -16.09         172.185         -227.189         285.066         0.812         -15.48         180.755         -229.880         292.433           0.797         -16.02         176.91         -212.21         160.959         -220.345         272.873         0.808         -16.36         192.740         -236.735         305.274           0.794         -16.02         176.91         176.02         160.959         -220.345         272.873         0.808         -16.36         170.02         188.242         272.873         188.81         180.755         222.889         280.085           0.794         -16.81         167.89         171.26         -206.449         250.075	12 -13.36 214.910 -236.082 319.251	214.910 -236.082 319.251	-236.082 319.251	319.251		0.811	12.84 2	24.277	236.738	326.106	0.823 -	13.38	212.305	-250.287	328.203	0.822	-12.90	221.471	-251.212	334.899
0.804         -1.4.44         198.121         -224.602         299.497         0.816         -15.21         183.656         -234.712         298.025         0.815         -14.63         192.740         -236.735         305.274           0.801         -15.20         187.401         -219.200         288.388         0.812         -16.09         172.185         -227.189         285.066         0.812         -15.48         180.755         -229.880         292.433           0.797         -16.02         176.91         -210.25         220.345         272.873         0.808         -16.36         169.600         -222.898         280.085           0.794         -16.81         167.586         -208.198         267.267         0.805         -17.99         150.694         -213.253         261.124         0.805         -18.10         260.249         250.075         0.805         -17.29         141.126         -206.449         250.075         0.805         -18.43         141.126         -206.449         250.075         0.802         -18.16         149.611         -210.221         258.249         250.046         250.046         250.046         250.046         250.046         250.046         250.046         250.046         250.046         250.046	0.807 -14.18 201.728 -228.591 304.874 0.807 -13.62	201.728 -228.591 304.874	-228.591 304.874	304.874		0.807				312.223	0.819	14.23	198.231	-242.453	313.176	0.819	-13.73		-244.557	320.316
0.801 - 15.20         187.401 - 219.200         288.388         0.812 - 16.09         172.185 - 227.189         285.066         0.812 - 15.48         180.755 - 229.880         292.433           0.797 - 16.02         176.917 - 213.413         277.208         0.809 - 17.02         160.959 - 220.345         272.873         0.808 - 16.36         169.600 - 222.898         280.085           0.794 - 16.81         167.586 - 208.198         267.267         0.805 - 17.29         150.694 - 213.253         261.124         0.805 - 17.28         158.914 - 216.102         268.242           0.794 - 16.81         167.586 - 208.198         267.267         0.805 - 17.89         141.126 - 206.449         250.075         0.802 - 18.16         149.11 - 210.221         258.024           0.787 - 18.43         150.871 - 197.426         248.474         0.799 - 19.92         132.835 - 200.384         240.414         0.799 - 19.09         140.765 - 20.90         250.00         251.86 - 193.96         230.851         0.796 - 20.09         140.00         251.89         140.416         197.69         197.69         297.39         197.69         197.89         197.89         197.89         197.69         197.69         197.89         197.89         197.89         197.89         197.89         197.89         197.89         197.89         197.89	04 -14.98 189.889 -223.629 293.373	189.889 -223.629 293.373	-223.629 293.373	293.373		0.804 -	14.44	98.121	224.602	299.497	0.816	15.21	183.656	-234.712	298.025	0.815	-14.63	192.740	-236.735	305.274
0.794 - 16.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         176.02         186.04         -216.12         0.805 - 17.28         158.914         -216.10         268.242           0.791 - 17.67         158.301 - 202.585         257.09         0.802 - 18.98         141.126         -206.449         250.075         0.802 - 18.16         149.611         -210.221         258.024           0.787 - 18.43         150.871         197.426         248.474         0.799 - 19.92         132.835         200.384         240.414         0.799 - 19.09         140.765         -204.004         247.856           0.783 - 19.20         144.065         -192.240         240.231         0.796 - 20.90         125.186         -193.96         230.081         0.795 - 20.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         197.09         1	01 -15.85 178.372 -217.315 281.144	178.372 -217.315 281.144	-217.315 281.144	281.144	-	0.801 -	15.20	87.401 -	219.200	288.388	0.812	16.09	172.185	-227.189	285.066	0.812	-15.48	180.755		292.433
0.794 - 16.81         167.586         -208.198         267.267         0.805 - 17.99         150.694         -213.253         261.124         0.805 - 17.28         158.914         -216.102         268.242           0.791 - 17.67         158.301         -202.585         257.099         0.802 - 18.98         141.126         -206.449         250.075         0.802 - 18.16         149.611         -210.221         258.024           0.787 - 18.43         150.871 - 197.426         248.474         0.799 - 19.92         132.835         -200.384         240.414         0.799 - 19.09         140.765         -204.004         247.856           0.783 - 19.20         144.065         -192.240         240.231         0.796 - 20.90         125.186 - 193.960         230.851         0.796 - 20.03         132.797         -197.693         238.154           0.780 - 19.97         137.814 - 187.051         232.338         0.793 - 21.39         118.197         -187.808         221.906         0.792 - 20.97         125.698         -191.502         229.070           0.776 - 20.75         131.867 - 182.250         224.954         0.789 - 22.86         102.18.671         -185.881         -195.90         0.785 - 22.86         10.395 - 22.86         10.785 - 22.85         133.154         -180.132         130.753 <td< td=""><td>0.797 -16.72 167.895 -211.342 269.915 0.7</td><td>167.895 -211.342 269.915</td><td>-211.342 269.915</td><td>269.915</td><td></td><td>0.797 -</td><td>16.02</td><td>76.917</td><td>213.413</td><td>277.208</td><td>0.809</td><td>17.02</td><td>160.959</td><td>-220.345</td><td>272.873</td><td>0.808</td><td>-16.36</td><td>169.600</td><td>-222.898</td><td>280.085</td></td<>	0.797 -16.72 167.895 -211.342 269.915 0.7	167.895 -211.342 269.915	-211.342 269.915	269.915		0.797 -	16.02	76.917	213.413	277.208	0.809	17.02	160.959	-220.345	272.873	0.808	-16.36	169.600	-222.898	280.085
0.781 - 17.67         158.301         -202.585         257.099         0.802 - 18.98         141.126         -206.449         250.075         0.802 - 18.16         149.611         -210.221         258.024           0.787 - 18.43         150.871 - 197.426         248.474         0.799 - 19.92         132.835         -200.384         240.414         0.799 - 19.09         140.765         -204.004         247.856           0.783 - 19.20         144.065         -192.240         240.231         0.796 - 20.90         125.186         -193.960         230.851         0.796 - 20.03         132.797         -197.693         238.154           0.776 - 19.97         137.814         -187.051         232.338         0.793 - 21.89         118.197         -187.808         221.906         0.792 - 20.97         125.698         -191.502         229.070           0.776 - 20.75         131.867         -182.250         224.954         0.789 - 22.85         112.161         -181.851         213.658         0.789 - 21.92         118.871         -185.881         220.640           0.771 - 21.53         126.693         -175.916         0.785 - 22.86         106.393         -175.910         205.61         0.786 - 22.86         133.154         -180.132         212.723	0.794 -17.57 158.542 -205.691 259.700 0.7	158.542 -205.691 259.700	-205.691 259.700	259.700			16.81	- 985.79	208.198	267.267	0.805	17.99	150.694	-213.253	261.124	0.805	-17.28		-216.102	268.242
0.783         -19.20         140.05         -19.240         240.414         0.799         -19.09         -19.09         -19.09         -19.09         -19.09         -19.09         -19.09         -19.09         -19.09         -19.09         -19.09         -20.386         -20.0386         -20.0387         0.796         -20.09         125.186         -193.960         230.851         0.796         -20.09         125.186         -193.960         230.851         0.796         -20.09         125.186         -197.808         221.906         0.792         -20.097         125.698         -191.502         229.070           0.776         -20.75         131.867         -182.250         224.954         0.789         -22.86         112.161         -181.851         213.658         0.789         -21.92         118.871         -185.881         220.640           0.771         -21.53         126.693         -175.06         0.785         -23.86         106.393         -175.910         205.581         0.785         -22.86         106.393         -175.910         205.581         0.785         -22.86         131.15         -185.801         -186.132         -186.132         -186.132         -186.132         -186.132         -186.132         -186.132         -186.132	0.790 -18.41 150.375 -199.750 250.026	150.375 -199.750 250.026	-199.750 250.026	250.026	-	0.791 -	17.67	58.301	202.585	257.099	0.802	18.98	141.126	-206.449	250.075	0.802	-18.16	149.611	-210.221	258.024
0.783         19.20         144.065         192.240         240.231         0.796         -20.39         125.186         -193.960         230.851         0.796         -20.99         125.186         -193.960         230.851         0.796         -20.07         125.698         -197.693         238.154           0.776         -20.75         131.867         -182.250         224.954         0.789         -22.85         112.161         -181.851         213.658         0.789         -21.92         118.871         -185.881         220.640           0.771         -21.53         126.693         -176.796         277.66         0.785         -23.86         106.393         -175.910         205.681         0.786         -22.286         133.154         -180.132         212.723	0.787 -19.24 142.803 -194.502 241.295 0.7	142.803 -194.502 241.295	-194.502 241.295	241.295		0.787	18.43	50.871	197.426	248.474	0.799	19.92	132.835	-200.384	240.414	0.799	-19.09	140.765	-204.004	247.856
0.776 -20.75   131.867   -182.250   224.954   0.789   -22.85   112.161   -181.851   213.658   0.789   -21.92   118.871   -185.881   220.640   0.771   -21.53   126.693   -176.798   217.506   0.785   -23.86   106.393   -175.910   205.581   0.785   -22.85   113.154   -180.132   212.723	0.783 -20.10 135.793 -188.890 232.635 0.7	135.793 -188.890 232.63	-188.890 232.63	232.63	10		19.20		192.240	240.231	0.796	20.90	125.186	-193.960	230.851	0.796	-20.03	132.797	-197.693	238.154
0.776   -20.75   131.867   -182.250   224.954   0.789   -22.85   112.161   -181.851   213.658   0.789   -21.92   118.871   -185.881   220.640   0.771   -21.53   126.693   -176.798   217.506   0.785   -23.86   106.393   -175.910   205.581   0.785   -22.85   113.154   -180.132   212.723	0.779 -20.93 129.745 -183.353 224.616 0.7	129.745 -183.353 224.610	-183.353 224.610	224.61	(0)		19.97	37.814	187.051	232.338	0.793	21.89	118.197	-187.808	221.906	0.792	-20.97	125.698		229.070
0.771  -21.53   126.693  -176.798   217.506   0.785  -23.86   106.393  -175.910   205.581   0.785  -22.85   113.154  -180.132   212.723	0.775 -21.73 124.298 -178.182 217.253 0.776 -20.75	124.298 -178.182 217.25	-178.182 217.25	217.25	8	0.776			182.250			22.85	112.161	-181.851	213.658	0.789	-21.92	118.871	-185.881	220.640
	70  -22.59   119.110  -172.763   209.843	119.110 -172.763 209.843	-172.763 209.843	209.843		0.771	21.53 1	26.693	176.798	217.506	0.785	23.86	106.393	-175.910	205.581	0.785	-22.85	113.154	-180.132	212.723

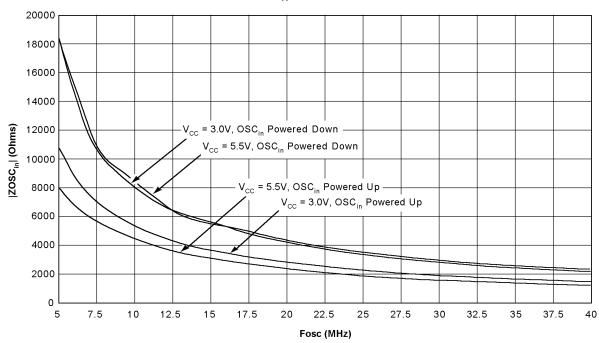
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#### LMX233xU TSSOP $OSC_{in}$ Input Impedance Vs Frequency $T_A = +25^{\circ}C$



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#### LMX233xU CSP OSC<sub>in</sub> Input Impedance Vs Frequency $T_A = +25^{\circ}C$

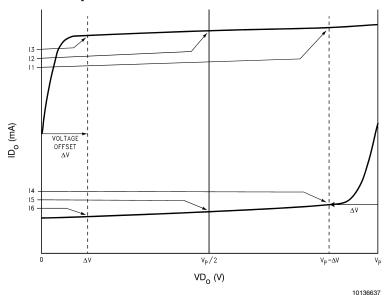


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LMX233xU TSSOP and LMX233xU CSP OSC<sub>in</sub> Input Impedance Table

			<u>`</u> {	25	88	ဥ္သ	191	43	13	74	2	8	8	8	8	8	78	42	929
		FER	, IZOSC <sub>in</sub> (Ω)	-18073.24 18544.50	0 10756.	0 8854.6	2 6313.3	8 5729.4	4985.007 4994.613	7 4356.1	3 3939.4	-3506.895 3511.232	8 3217.4	-2934.223 2938.443	9 2784.9	-2600.472 2603.500	-2419.904 2424.228	3 2307.9	10136678
	ဥ	OSC <sub>in</sub> BUFFER POWERED DOWN	Im ZOSC <sub>in</sub> (Ω)	-18073.2	-10602.9	-8800.59	-6248.93	-5712.78	-4985.00	4345.59	-3935.87	-3506.89	-3213.47	-2934.22	-2780.46	-2600.47	-2419.90	-2302.91	
	V <sub>cc</sub> = 5.5V (T <sub>A</sub> = 25°C)	POW	Re ZOSC <sub>m</sub> (Ω)	4154.104	2626.329 4998.105 5646.119 1812.311 -10602.90 10756.68	976.808 -8800.590 8854.633	899.697 -6248.932 6313.367	436.542 -5712.788 5729.443	309.618	303.378 -4345.597 4356.174	168.163 -3935.873 3939.464	174.460	159.273 -3213.478 3217.422	157.424	157.389 -2780.469 2784.920	125.530	144.727	273.323 -1199.918 1230.654 152.283 -2302.913 2307.942	
	= 5.5V	뚭음	IZOSC <sub>In</sub> I	8056.318	5646.119	4512.261	3663.045	3098.519	2697.692	2384.315	2098.100	1912.986	1756.195	1608.182	1498.818	1390.840	1305.774	1230.654	
ڻ اڻ	δ,	OSC, BUFFER POWERED UP	Im ZOSC <sub>in</sub> (Ω)	-6544.007	4998.105	1625.723 -4209.219 4512.261	1182.342 -3466.982 3663.045	856.006  -2977.931   3098.519	-2605.886 2697.692	554.417 -2318.961 2384.315	485.437 -2041.170 2098.100	-1865.270 1912.986	379.086 -1714.793 1756.195	357.340 -1567.979 1608.182	332.065 -1461.571 1498.818	-1358.120 1390.840	-1274.370 1305.774	-1199.918	
SOZ ds:		OSC	Re ZOSC <sub>in</sub> (Ω)	4698.960	2626.329	1625.723	1182.342	856.006	697.781	554.417	485.437	424.599	379.086	357.340	332.065	299.913	284.654	273.323	
LMX233xU CSP ZOSCin		N.N.	IZOSC <sub>II</sub> I	18544.50	10325.74	3418.499		5675.536	4809.039	1246.948	3782.429	3406.648	3120.763	2843.557	2667.608	2473.011	2334.664		
LMX	6	OSC <sub>in</sub> BUFFER POWERED DOWN	Im ZOSC <sub>in</sub> (Ω)	-18073.24	10205.48	8350.651	-6341.105 6382.730	-5658.273 5675.536	4799.917 4809.039	4242.475	-3777.847 3782.429	-3402.400 3406.648	-3114.867 3120.763	-2837.317 2843.557	2664.486	-2471.170 2473.011	-2331.694 2334.664	-2182.473 2183.987	
	= 3.0V (T <sub>A</sub> = 25°C)	POWE	Re ZOSC <sub>in</sub> (Ω)	4154.104	571.331 -	066.661 ⊣	727.756	442.319	296.061	194.872 -4242.475 4246.948	186.123	170.072	191.739	188.280 -:	129.014  -2664.486  2667.608	95.424	117.732	81.318	
	= 3.0V (	e: •	ZOSC <sub>in</sub> l	10809.27	6920.146 1571.331 -10205.48 10325.74	432.335		3663.861	3232.825							675.961		481.260	
	8	OSC,, BUFFER POWERED UP	Im ZOSCin (Ω)	9526.374	544.475	170.920 5	245.537 4	-3558.426	-3158.030	-2791.912 2847.441	-2512.522 2551.129	-2261.024 2304.307	-2060.013 2092.491	-1893.442 1926.747	776.540 1	-1648.356 1675.961	-1549.601 1578.377	454.298	
		osc Pov	Re ZOSC <sub>in</sub> (Ω)	5107.688 -6	249.061 -6	664.886 -	1048.750 4245.537 4373.153	872.629 -3	691.377 -3	559.597 -2	442.147 -2	444.524 -2	367.245 -2	356.692 -1	348.916 -1776.540 1810.480	302.932 -1	300.020	81.334 -1	
		a ×	IZOSC <sub>in</sub> l (Ω)	504.282 5	692.910	5680.388 1664.886 -5170.920 5432.335 1066.661 -8350.651 8418.499	4669.295	3803.003	3311.570		2610.449	2389.913	2162.832	1985.928	1813.090	1690.365	1591.854	471.004	
		OSC <sub>in</sub> BUFFER POWERED DOWN	Im ZOSC <sub>in</sub> []	-11436.600 11504.282	-7675.309 7692.910 2249.061 -6544.475	-5659.675 5	-4665.169	-3799.626	-3305.741	-2917.281 2918.215	-2608.411 2	-2388.967	-2161.702	-1984.769	-1812.700	-1689.748	-1591.439	-1470.482 1471.004 281.334 -1454.298 1481.260	
	= 5.5V (T <sub>A</sub> = 25°C)	OSC	Re ZOSC <sub>in</sub> 2 (Ω)	1246.071 -1	520.098 -7	484.656 -5	196.239 -4	160.236 -3	196.400 -3	73.816 -2	103.131 -2	67.246 -2	69.923 -2	67.843 -1	37.610 -1	45.646 -1	36.346 -1	39.180	
	= 5.5V (	æ a	ZOSC <sub>in</sub>   Z	7342.982 12	5023.579 5	673 3826.886 4	845 3126.584	243 2570.238	2214.372	267 1987.347 7	101 1754.310 1	814 1598.857 6	713 1444.646 6	929 1322.520 6	403 1219.482 3	429 1137.399 4	461 1070.066 3	990.631	
ڻ ت	8	BUFFER ERED UP	Im ZOSC <sub>in</sub> iZ (Ω)	.525	.053				584									54	
LMX233xU TSSOP ZOSC <sub>in</sub>		OSC <sub>in</sub> B POWER	Re ZOSC <sub>in</sub> Z (Ω)	32.878 -67	67.479	39.926 -37	544.280 -3078	-3761.566 3765.044 416.644 -2536	309.867 -2192	227.640 -1974	-2543.330 2545.222 214.873 -1741.	169.812 -1589	160.401 -1435	-1926.889 1928.604 141.501 -1314	21.612 -12	-1662.230 1662.666 116.385 -1131.	109.381 -1064.	90.267 -9	
3×U TSS		~ Z	ZOSC <sub>IN</sub> Z	366.234 28	45.994 12	99.207		65.044			45.222 2		- 1	28.604	51.443	62.666		39.919	
LMX23		OSC <sub>in</sub> BUFFER POWERED DOWN	Im ZOSC <sub>in</sub>    Z(	25.209 118	40.322 76	93.060 57	47.094 45	61.566 37	-3203.351 3206.467	-2879.931 2880.631	43.330 25	-2340.221 2341.923	-2106.253 2107.405	26.889 19	50.824 17	52.230 16	-1547.816 1548.263	39.460 14	
	, = 25°C)	OSC <sub>II</sub> POWER	Re ZOSC <sub>in</sub> ZC (Ω)	985.863 -11825.209 11866.234 2832.878 -6774	1202.389 -5538.197 5667.218 294.460 -7640.322 7645.994 1267.479 4861	791.970 -4218.658 4292.353 266.942 -5793.060 5799.207 739.926 -3754	527.664 -3418.978 3459.456 197.874 -4547.094 4551.397	161.801 -376		63.505 -287	98.108 -25	89.270 -23	69.675 -210	81.310 -192	46.548 -1750.824 1751.443 121.612 -1213.	38.046 -166	37.202 -154	36.351 -1439.460 1439.919 100.267 -985.	
	V <sub>cc</sub> = 3.0V (T <sub>A</sub> = 25°C)		IZOSC <sub>in</sub> ] ZO (Ω)		7.218 294	2.353 266	9.456 197	8.794 161	0.085 141			- 1				- 1		5.296 36.	
	νς:	OSC <sub>in</sub> BUFFER POWERED UP	Im ZOSC <sub>in</sub>  ZO (Ω)	2291.113 -8000.376 8321.972	8.197 566	8.658 429	8.978 345	343.020 -2817.993 2838.794	316.446 -2439.647 2460.085 141.326	228.526 -2179.146 2191.096	211.659 -1932.535 1944.091	163.618 -1762.903 1770.480	163.733 -1589.620 1598.030	148.446 -1463.071 1470.583	130.683 -1340.206 1346.562	126.059 -1255.034 1261.349	115.848 -1178.954 1184.632	108.280 -1089.931 1095.296	
		OSC <sub>II</sub> POWE	Re ZOSC <sub>n</sub> (Ω)	1.113 -800	2.389 -553	970 -421	.664 -341	.020 -281	446 -243	526 -217	.659 -193	618 -176	733 -158	446 -146	.683 -134	.059 -125	.848	280 -108	
			Fosc ZO:	5.0 2291	7.5 1202	10.0	12.5 527	15.0 343	17.5 316	20.0	22.5 211	25.0 163	27.5 163	30.0 148	32.5 130	35.0 126	37.5 115.	40.0	

#### **Charge Pump Current Specification Definitions**



I1 = Charge Pump Sink Current at  $VD_0 = V_P - \Delta V$ 

I2 = Charge Pump Sink Current at  $VD_0 = V_P/2$ 

I3 = Charge Pump Sink Current at  $VD_0 = \Delta V$ 

I4 = Charge Pump Source Current at  $VD_0 = V_P - \Delta V$ 

I5 = Charge Pump Source Current at VD<sub>0</sub> = V<sub>P</sub>/2

I6 = Charge Pump Source Current at  $VD_0 = \Delta V$ 

 $\Delta V = Voltage$  offset from the positive and negative rails. Dependent on the VCO tuning range relative to  $V_{CC}$  and GND. Typical values are between 0.5V and 1.0V.

 $V_P$  refers to either  $V_P$  RF or  $V_P$  IF

 $\mathrm{VD_{o}}$  refers to either  $\mathrm{VD_{o}}$  RF or  $\mathrm{VD_{o}}$  IF

 ${\rm ID_0}$  refers to either  ${\rm ID_0}$  RF or  ${\rm ID_0}$  IF

#### Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage

$$ID_{o} Vs VD_{o} = \frac{(|11| - |13|)}{(|11| + |13|)} \times 100\%$$
$$= \frac{(|14| - |16|)}{(|14| + |16|)} \times 100\%$$

#### Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch

$$ID_o$$
 SINK Vs  $ID_o$  SOURCE = 
$$\frac{|I2| - |I5|}{\frac{1}{2}(|I2| + |I5|)} \times 100\%$$

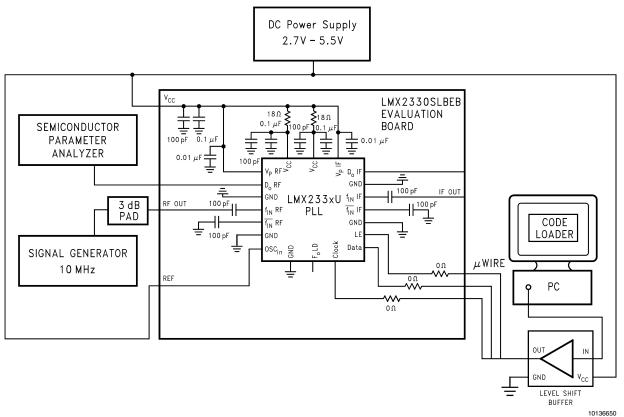
#### **Charge Pump Output Current Magnitude Variation Vs Temperature**

$$ID_{o} \text{ Vs } T_{A} = \frac{|I_{2}||_{T_{A}} - |I_{2}||_{T_{A} = 25^{\circ}C}}{|I_{2}||_{T_{A} = 25^{\circ}C}} \times 100\%$$

$$= \frac{|I_{5}||_{T_{A}} - |I_{5}||_{T_{A} = 25^{\circ}C}}{|I_{5}||_{T_{A} = 25^{\circ}C}} \times 100\%$$

#### **Test Setups**

#### LMX233xU Charge Pump Test Setup



The block diagram above illustrates the setup required to measure the LMX233xU device's RF charge pump sink current. The same setup is used for a LMX2330TMEB Evaluation Board. The IF charge pump measurement setup is similar to the RF charge pump measurement setup. The purpose of this test is to assess the functionality of the RF charge pump.

This setup uses an open loop configuration. A power supply is connected to  $V_{\rm cc}$  and swept from 2.7V to 5.5V. By means of a signal generator, a 10 MHz signal is typically applied to the  $f_{\rm IN}$  RF pin. The signal is one of two inputs to the phase detector. The 3 dB pad provides a 50  $\Omega$  match between the PLL and the signal generator. The OSC $_{\rm in}$  pin is tied to  $V_{\rm cc}$ . This establishes the other input to the phase detector. Alternatively, this input can be tied directly to the ground plane. With the  $D_{\rm o}$  RF pin connected to a Semiconductor Parameter Analyzer in this way, the sink, source, and TRI-STATE currents can be measured by simply toggling the **Phase Detector Polarity** and **Charge Pump State** states in Code Loader. Similarly, the LOW and HIGH currents can be measured by switching the **Charge Pump Gain's** state between **1X** and **4X** in Code Loader.

Let  $F_r$  represent the frequency of the signal applied to the OSC<sub>in</sub> pin, which is simply zero in this case (DC), and let  $F_p$  represent the frequency of the signal applied to the  $f_{IN}$  RF pin. The phase detector is sensitive to the rising edges of  $F_r$  and  $F_p$ . Assuming positive VCO characteristics; the charge pump turns ON and sinks current when the first rising edge of  $F_p$  is detected. Since  $F_r$  has no rising edge, the charge pump continues to sink current indefinitely.

Toggling the **Phase Detector Polarity** state to negative VCO characteristics allows the measurement of the RF charge pump source current. Likewise, selecting **TRI-STATE** (TRI-STATE ID $_{\rm o}$  RF Bit = 1) for **Charge Pump State** in Code Loader facilitates the measurement of the TRI-STATE current.

The measurements are repeated at different temperatures, namely  $T_A = -40^{\circ}C$ ,  $+25^{\circ}C$ , and  $+85^{\circ}C$ .

#### Test Setups (Continued)

#### LMX233xU f<sub>IN</sub> Sensitivity Test Setup DC Power Supply 2.7V - 5.5V LMX2330SLBEB 10 MHz REF OUT **EVALUATION ≶**18Ω BOARD SIGNAL GENERATOR 100 pf 100 MHz - 2500 MHz D<sub>o</sub> RF 100 pF IF OUT GND LMX233xU $\mathsf{f}_{\mathsf{IN}}$ 100 pF 3 dB 100 pF f<sub>IN</sub> RF PAD f<sub>IN</sub> RF GND CODE LOADER 100 pF GND Clock Data $\mu$ WIRE PC 0Ω UNIVERSAL COUNTER LEVEL SHIFT BUFFFR 10136640

The block diagram above illustrates the setup required to measure the LMX233xU device's RF input sensitivity level. The same setup is used for a LMX2330TMEB Evaluation Board. The IF input sensitivity test setup is similar to the RF sensitivity test setup. The purpose of this test is to measure the acceptable signal level to the  $f_{\rm IN}$  RF input of the PLL chip. Outside the acceptable signal range, the feedback divider begins to divide incorrectly and miscount the frequency.

The setup uses an open loop configuration. A power supply is connected to  $V_{cc}$  and swept from 2.7V to 5.5V. The IF PLL is powered down (PWDN IF Bit = 1). By means of a signal generator, an RF signal is applied to the  $f_{\rm IN}$  RF pin. The 3 dB pad provides a 50  $\Omega$  match between the PLL and the signal generator. The OSC<sub>in</sub> pin is tied to  $V_{cc}$ . The N value is typically set to 10000 in Code Loader, i.e. RF N\_CNTRB Word = 156 and RF N\_CNTRA Word = 16 for PRE RF Bit = 1 (LMX2330U) or PRE RF = 0 (LMX2331U and LMX2332U). The feedback divider output is routed to the  $F_o$ LD pin by selecting the **RF PLL N Divider Output** word ( $F_o$ LD Word =

6 or 14) in Code Loader. A Universal Counter is connected to the  $F_o LD$  pin and tied to the 10 MHz reference output of the signal generator. The output of the feedback divider is thus monitored and should be equal to  $f_{\mathsf{IN}}$  RF / N.

The  $f_{\rm IN}$  RF input frequency and power level are then swept with the signal generator. The measurements are repeated at different temperatures, namely  $T_{\rm A} = -40\,^{\circ}{\rm C}$ ,  $+25\,^{\circ}{\rm C}$ , and  $+85\,^{\circ}{\rm C}$ . Sensitivity is reached when the frequency error of the divided RF input is greater than or equal to 1 Hz. The power attenuation from the cable and the 3 dB pad must be accounted for. The feedback divider will actually miscount if too much or too little power is applied to the  $f_{\rm IN}$  RF input. Therefore, the allowed input power level will be bounded by the upper and lower sensitivity limits. In a typical application, if the power level to the  $f_{\rm IN}$  RF input approaches the sensitivity limits, this can introduce spurs and degradation in phase noise. When the power level gets even closer to these limits, or exceeds it, then the RF PLL loses lock.

#### Test Setups (Continued)

#### LMX233xU OSC<sub>in</sub> Sensitivity Test Setup DC Power Supply 2.7V - 5.5VLMX2330SLBEB **EVALUATION** BOARD D<sub>o</sub> RF IF OUT GND LMX233xU fin RF OUT f<sub>IN</sub> RF PLL $\overline{f_{IN}}$ CODE f<sub>IN</sub> RF GNE 100 pF LOADER GND Data $\mu$ WIRE SIGNAL GENERATOR PC 2 MHz - 100 MHz 1000 pF 10 MHz REF OUT GND UNIVERSAL COUNTER LEVEL SHIFT

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The block diagram above illustrates the setup required to measure the LMX233xU device's OSC $_{in}$  buffer sensitivity level. The same setup is used for a LMX2330TMEB Evaluation Board. This setup is similar to the  $f_{IN}$  sensitivity setup except that the signal generator is now connected to the OSC $_{in}$  pin and both  $f_{IN}$  pins are tied to  $V_{CC}$ . The 51  $\Omega$  shunt resistor matches the OSC $_{in}$  input to the signal generator. The R counter is typically set to 1000, i.e. RF R\_CNTR Word = 1000 or IF R\_CNTR Word = 1000. The reference divider output is routed to the  $F_{o}$ LD pin by selecting the **RF PLL R Divider Output** word ( $F_{o}$ LD Word = 2 or 10) or the **IF PLL R Divider Output** word ( $F_{o}$ LD Word = 1 or 9) in Code Loader.

Similarly, a Universal Counter is connected to the  $F_oLD$  pin and is tied to the 10 MHz reference output from the signal generator. The output of the reference divider is monitored and should be equal to  $OSC_{in}/$  RF R\_CNTR or  $OSC_{in}/$  IF R\_CNTR.

Again,  $V_{CC}$  is swept from 2.7V to 5.5V. The OSC<sub>in</sub> input frequency and voltage level are then swept with the signal generator. The measurements are repeated at different temperatures, namely  $T_A = -40^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ , and  $+85^{\circ}\text{C}$ . Sensitivity is reached when the frequency error of the divided input signal is greater than or equal to 1 Hz.

#### Test Setups (Continued)

#### LMX233xU f<sub>IN</sub> Impedance Test Setup DC Power Supply 2.7V - 5.5V LMX2330SLBEB **EVALUATION >**18Ω BOARD 100 pF D, RF 100 pF IF OUT GND LMX233xU $f_{\mathsf{IN}}$ IF 100 pF NETWORK ANALYZER f<sub>IN</sub> RF f<sub>IN</sub> RF CODE GNE LOADER Data OSC: $\mu$ WIRE PC 0Ω

The block diagram above illustrates the setup required to measure the LMX233xU device's RF input impedance. The IF input impedance and reference oscillator impedance setups are very much similar. The same setup is used for a LMX2330TMEB Evaluation Board. Measuring the device's input impedance facilitates the design of appropriate matching networks to match the PLL to the VCO, or in more critical situations, to the characteristic impedance of the printed circuit board (PCB) trace, to prevent undesired transmission line effects.

Before the actual measurements are taken, the Network Analyzer needs to be calibrated, i.e. the error coefficients need to be calculated. Therefore, three standards will be used to calculate these coefficients: an **open**, **short** and a **matched load**. A 1-port calibration is implemented here.

To calculate the coefficients, the PLL chip is first removed from the PCB. The Network Analyzer port is then connected to the RF OUT connector of the evaluation board and the desired operating frequency is set. The typical frequency range selected for the LMX233xU device's RF synthesizer is from 100 MHz to 2500 MHz. The standards will be located down the length of the RF OUT transmission line. The transmission line adds electrical length and acts as an offset from the reference plane of the Network Analyzer; therefore, it

must be included in the calibration. Although not shown, 0  $\Omega$  resistors are used to complete the RF OUT transmission line (trace).

LEVEL SHIFT

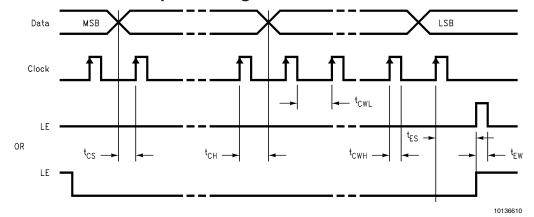
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To implement an **open** standard, the end of the RF OUT trace is simply left open. To implement a **short** standard, a 0  $\Omega$  resistor is placed at the end of the RF OUT transmission line. Last of all, to implement a **matched load** standard, two 100  $\Omega$  resistors in parallel are placed at the end of the RF OUT transmission line. The Network Analyzer calculates the calibration coefficients based on the measured S<sub>11</sub> parameters. With this all done, calibration is now complete.

The PLL chip is then placed on the PCB. A power supply is connected to  $V_{\rm CC}$  and swept from 2.7V to 5.5V. The  $OSC_{\rm in}$  pin is tied to the ground plane. Alternatively, the  $OSC_{\rm in}$  pin can be tied to  $V_{\rm CC}$ . In this setup, the complementary input  $(\overline{f}_{\rm IN}$  RF) is AC coupled to ground. With the Network Analyzer still connected to RF OUT, the measured  $f_{\rm IN}$  RF impedance is displayed.

**Note:** The impedance of the reference oscillator is measured when the oscillator buffer is powered up (PWDN RF Bit = 0 **or** PWDN IF Bit = 0), and when the oscillator buffer is powered down (PWDN RF Bit = 1 **and** PWDN IF Bit = 1).

#### LMX233xU Serial Data Input Timing



#### Notes:

- 1. Data is clocked into the 22-bit shift register on the rising edge of Clock
- 2. The MSB of Data is shifted in first.

#### 1.0 Functional Description

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX233xU, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, programmable reference R and feedback N frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the reference divider to obtain a comparison reference frequency. This reference signal, F<sub>r</sub>, is then presented to the input of a phase/frequency detector and compared with the feedback signal,  $F_p$ , which was obtained by dividing the VCO frequency down by way of the feedback divider. The phase/frequency detector measures the phase error between the F<sub>r</sub> and F<sub>p</sub> signals and outputs control signals that are directly proportional to the phase error. The charge pump then pumps charge into or out of the loop filter based on the magnitude and direction of the phase error. The loop filter converts the charge into a stable control voltage for the VCO. The phase/frequency detector's function is to adjust the voltage presented to the VCO until the feedback signal's frequency and phase match that of the reference signal. When this "Phase-Locked" condition exists, the VCO frequency will be N times that of the comparison frequency, where N is the feedback divider ratio.

#### 1.1 REFERENCE OSCILLATOR INPUT

The reference oscillator frequency for both the RF and IF PLLs is provided from an external reference via the OSC $_{\rm in}$  pin. The reference buffer circuit supports input frequencies from 5 to 40 MHz with a minimum input sensitivity of 0.5 V $_{\rm PP}$ . The reference buffer circuit has an approximate V $_{\rm CC}/2$  input threshold and can be driven from an external CMOS or TTL logic gate. Typically, the OSC $_{\rm in}$  pin is connected to the output of a crystal oscillator.

#### 1.2 REFERENCE DIVIDERS (R COUNTERS)

The reference dividers divide the reference input signal, OSC<sub>in</sub>, by a factor of R. The output of the reference divider circuits feeds the reference input of the phase detector. This reference input to the phase detector is often referred to as the comparison frequency. The divide ratio should be chosen such that the maximum phase comparison frequency ( $F_{\phi RF}$  or  $F_{\phi IF}$ ) of 10 MHz is not exceeded.

The RF and IF reference dividers are each comprised of 15-bit CMOS binary counters that support a continuous integer divide ratio from 3 to 32767. The RF and IF reference divider circuits are clocked by the output of the reference buffer circuit which is common to both.

#### 1.3 PRESCALERS

The  $f_{\rm IN}$  RF ( $f_{\rm IN}$  IF) and  $\overline{f_{\rm IN}}$  RF ( $\overline{f_{\rm IN}}$  IF) input pins drive the input of a bipolar, differential-pair amplifier. The output of the bipolar, differential-pair amplifier drives a chain of ECL D-type flip-flops in a dual modulus configuration. The output of the prescaler is used to clock the subsequent feedback dividers. The RF and IF PLL complementary inputs can be driven differentially, or the negative input can be AC coupled to ground through an external capacitor for single ended configuration. A 32/33 or a 64/65 prescale ratio can be selected for the 2.5 GHz LMX2330U RF synthesizer. A 64/65 or a 128/129 prescale ratio can be selected for both the LMX2331U and LMX2332U RF synthesizers. The IF circuitry contains an 8/9 or a 16/17 prescaler.

#### 1.4 PROGRAMMABLE FEEDBACK DIVIDERS (N COUNTERS)

The programmable feedback dividers operate in concert with the prescalers to divide the input signal,  $f_{\text{IN}}$ , by a factor of N. The output of the programmable reference divider is provided to the feedback input of the phase detector circuit. The divide ratio should be chosen such that the maximum phase comparison frequency  $(F_{\varphi \text{RF}} \text{ or } F_{\varphi \text{IF}})$  of 10 MHz is not exceeded.

The programmable feedback divider circuit is comprised of an A counter (swallow counter) and a B counter (programmble binary counter). The RF N\_CNTRA counter is a 7-bit CMOS swallow counter, programmable from 0 to 127. The IF N\_CNTRA counter is also a 7-bit CMOS swallow counter, but programmable from 0 to 15. The three most significant bits are 'don't cares' in this case. The RF N\_CNTRB and IF N\_CNTRB counters are both 11-bit CMOS binary counters, programmable from 3 to 2047. A continuous integer divide ratio is achieved if  $N \ge P^*$  (P-1), where P is the value of the prescaler selected. Divide ratios less than the minimum continuous divide ratio are achievable as long as the binary programmable counter value is greater than the swallow counter value (N\_CNTRB ≥ N\_CNTRA). Refer to **Sections** 2.6.1, 2.6.2, 2.7.1 and 2.7.2 for details on how to program the N CNTRA and N CNTRB counters. The following equations are useful in determining and programming a particular value of N:

 $N = (P \times N\_CNTRB) + N\_CNTRA$  $f_{IN} = N \times F_{\phi}$ 

#### Definitions:

 $F_{\phi}$ : RF or IF phase detector comparison

frequency

f<sub>IN</sub>: RF or IF input frequencyN\_CNTRA: RF or IF A counter valueN\_CNTRB: RF or IF B counter value

P: Preset modulus of the dual modulus

prescaler

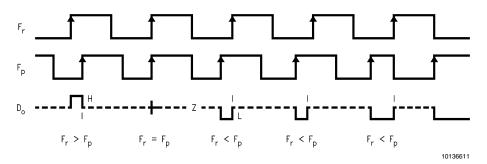
LMX2330U RF synthesizer: P = 32 or 64 LMX2331U RF synthesizer: P = 64 or 128 LMX2332U RF synthesizer: P = 64 or 128 LMX233xU IF synthesizer: P = 8 or 16

#### 1.5 PHASE/FREQUENCY DETECTORS

The RF and IF phase/frequency detectors are driven from their respective N and R counter outputs. The maximum frequency for both the RF and IF phase detector inputs is 10 MHz. The phase/frequency detector outputs control the respective charge pumps. The polarity of the pump-up or pump-down control signals are programmed using the **PD\_POL RF** or **PD\_POL IF** control bits, depending on whether the RF or IF VCO characteristics are positive or negative. Refer to **Sections 2.4.2** and **2.5.2** for more details. The phase/frequency detectors have a detection range of  $-2\pi$  to  $+2\pi$ . The phase/frequency detectors also receive a feedback signal from the charge pump in order to eliminate dead zone.

#### 1.0 Functional Description (Continued)

PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



#### Notes:

- 1. The minimum width of the pump-up and pump-down current pulses occur at the Do RF or Do IF pins when the loop is phase locked.
- 2. The diagram assumes positive VCO characteristics, i.e. PD\_POL RF or PD\_POL IF = 1.
- 3.  $F_r$  is the phase detector input from the reference divider (R counter).
- 4. Fp is the phase detector input from the programmable feedback divder (N counter).
- 5. Do refers to either the RF or IF charge pump output.

#### 1.6 CHARGE PUMPS

The charge pump directs charge into or out of an external loop filter. The loop filter converts the charge into a stable control voltage which is applied to the tuning input of the VCO. The charge pump steers the VCO control voltage towards  $V_{\rm P}$  RF or  $V_{\rm P}$  IF during pump-up events and towards GND during pump-down events. When locked,  $D_{\rm o}$  RF or  $D_{\rm o}$  IF are primarily in a TRI-STATE mode with small corrections occuring at the phase comparator rate. The charge pump output current magnitude can be selected by toggling the  $ID_{\rm o}$  RF or  $ID_{\rm o}$  IF control bits.

#### 1.7 MICROWIRE SERIAL INTERFACE

The programmable register set is accessed via the MI-CROWIRE serial interface. The interface is comprised of three signal pins: Clock, Data and LE (Latch Enable). Serial data is clocked into the 22-bit shift register on the rising edge of Clock. The last two bits decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of four control registers depending on the state of the address bits. The MSB of Data is loaded in first. The synthesizers can be programmed even in power down mode. A complete programming description is provided in **Section 2.0 Programming Description**.

#### 1.8 MULTI-FUNCTION OUTPUTS

The LMX233xU device's  $F_oLD$  output pin is a multi-function output that can be configured as the RF FastLock output, a push-pull analog lock detect output, counter reset, or used to monitor the output of the various reference divider (R counter) or feedback divider (N counter) circuits. The  $F_oLD$  control word is used to select the desired output function. When the PLL is in powerdown mode, the  $F_oLD$  output is pulled to a LOW state. A complete programming description of the multi-function output is provided in **Section 2.8**  $F_oLD$ .

#### 1.8.1 Push-Pull Analog Lock Detect Output

An analog lock detect status generated from the phase detector is available on the  $F_oLD$  output pin if selected. The lock detect output goes HIGH when the charge pump is inactive. It goes LOW when the charge pump is active during a comparison cycle. When viewed with an oscilloscope, narrow negative pulses are observed when the charge pump turns on. The lock detect output signal is a push-pull configuration.

Three separate lock detect signals are routed to the multiplexer. Two of these monitor the 'lock' status of the individual synthesizers. The third detects the condition when both the RF and IF synthesizers are in a 'locked state'. External circuitry however, is required to provide a steady DC signal to indicate when the PLL is in a locked state. Refer to **Section 2.8 F<sub>o</sub>LD** for details on how to program the different lock detect options.

#### 1.0 Functional Description (Continued)

#### 1.8.2 Open Drain FastLock Output

The LMX233xU Fastlock feature allows faster loop response time during lock aquisition. The loop response time (lock time) can be approximately halved if the loop bandwidth is doubled. In order to achieve this, the same gain/ phase relationship at twice the loop bandwidth must be maintained. This can be achieved by increasing the charge pump current from 0.95 mA (ID, RF Bit = 0) in the steady state mode, to 3.8 mA (ID, RF Bit = 1) in Fastlock. When the  $F_0LD$  output is configured as a FastLock output, an open drain device is enabled. The open drain device switches in a parallel resistor R2' to ground, of equal value to resistor R2 of the external loop filter. The loop bandwidth is effectively doubled and stability is maintained. Once locked to the correct frequency, the PLL will return to a steady state condition. Refer to Section 2.8 FoLD for details on how to configure the FoLD output to an open drain Fastlock output.

#### 1.8.3 Counter Reset

Three separate counter reset functions are provided. When the F<sub>o</sub>LD is programmed to **Reset IF Counters**, both the IF feedback divider and the IF reference divider are held at their load point. When the **Reset RF Counters** is programmed, both the RF feedback divider and the RF reference divider are held at their load point. When the **Reset All Counters** mode is enabled, all feedback dividers and reference dividers are held at their load point. When the device is programmed to normal operation, both the feedback divider and reference divider are enabled and resume counting in 'close' alignment to each other. Refer to **Section 2.8 F<sub>o</sub>LD** for more details.

#### 1.8.4 Reference Divider and Feedback Divider Output

The outputs of the various N and R dividers can be monitored by selecting the appropriate  $F_oLD$  word. This is essential when performing  $OSC_{in}$  or  $f_{IN}$  sensitivity measurements. Refer to the **Test Setups** section for more details. Refer to **Section 2.8**  $F_oLD$  for more details on how to route the appropriate divider output to the  $F_oLD$  pin.

#### 1.9 POWER CONTROL

Each synthesizer in the LMX233xU device is individually power controlled by device powerdown bits. The powerdown word is comprised of the PWDN RF (PWDN IF) bit, in conjuction with the TRI-STATE ID<sub>o</sub> RF (TRI-STATE ID<sub>o</sub> IF) bit. The powerdown control word is used to set the operating mode of the device. Refer to Sections 2.4.4, 2.5.4, 2.6.4, and 2.7.4 for details on how to program the RF or IF powerdown bits.

When either the RF synthesizer or the IF synthesizer enters the powerdown mode, the respective prescaler, phase detector, and charge pump circuit are disabled. The Do RF (Do IF),  $f_{IN}$  RF ( $f_{IN}$  IF), and  $\overline{f_{IN}}$  RF ( $\overline{f_{IN}}$  IF) pins are all forced to a high impedance state. The reference divider and feedback divider circuits are held at the load point during powerdown. The oscillator buffer is disabled when both the RF and IF synthesizers are powered down. The OSC<sub>in</sub> pin is forced to a HIGH state through an approximate 100  $k\Omega$  resistance when this condition exists. When either synthesizer is activated, the respective prescaler, phase detector, charge pump circuit, and the oscillator buffer are all powered up. The feedback divider, and the reference divider are held at load point. This allows the reference oscillator, feedback divider, reference divider and prescaler circuitry to reach proper bias levels. After a finite delay, the feedback and reference dividers are enabled and they resume counting in 'close' alignment (the maximum error is one prescaler cycle). The MICROWIRE control register remains active and capable of loading and latching data while in the powerdown mode.

#### **Synchronous Powerdown Mode**

In this mode, the powerdown function is gated by the charge pump. When the device is configured for synchronous powerdown, the device will enter the powerdown mode upon completion of the next charge pump pulse event.

#### **Asynchronous Powerdown Mode**

In this mode, the powerdown function is NOT gated by the completion of a charge pump pulse event. When the device is configured for asynchronous powerdown, the part will go into powerdown mode immediately.

TRI-STATE ID <sub>o</sub>	PWDN	Operating Mode
0	0	PLL Active, Normal Operation
1	0	PLL Active, Charge Pump Output in High Impedance State
0	1	Synchronous Powerdown
1	1	Asynchronous Powerdown

#### Notes:

- 1. TRI-STATE  ${\rm ID_o}$  refers to either the TRI-STATE  ${\rm ID_o}$  RF or TRI-STATE  ${\rm ID_o}$  IF bit .
- 2. PWDN refers to either the PWDN RF or PWDN IF bit.

#### 2.0 Programming Description

#### 2.1 MICROWIRE INTERFACE

The 22-bit shift register is loaded via the MICROWIRE interface. The shift register consists of a 20-bit *Data[19:0] Field* and a 2-bit *Address[1:0] Field* as shown below. The Address Field is used to decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of 4 control registers depending on the state of the address bits. The MSB of Data is loaded in first. The Data Field assignments are shown in **Section 2.3 CONTROL REGISTER CONTENT MAP**.

MSB			LSB
	Data[19:0]		Address[1:0]
21		2	1 0

#### 2.2 CONTROL REGISTER LOCATION

The address bits Address[1:0] decode the internal register address. The table below shows how the address bits are mapped into the target control register.

Addre	ss[1:0]	Target
Fie	eld	Register
0	0	IF R
0	1	RF R
1	0	IF N
1	1	RF N

#### 2.3 CONTROL REGISTER CONTENT MAP

The control register content map describes how the bits within each control register are allocated to specific control functions.

## LMX2330U/LMX2331U/LMX2332U

2.0	Progr	ramm	2.0 Programming Description (Continued)	escr	iptio	) L	ontinuec	<del>=</del>														
Reg.	Most (	Reg. Most Significant Bit	ant Bit							SHE	FT REC	SHIFT REGISTER BIT LOCATION	BIT LO	CATION						Least (	Least Significant Bit	ant Bit
	21	20	19	18	17	16	15	14	13	12	=	10	6	80	7	9	5	4	က	2	-	0
										Data	Data Field										Address	ress
																					Field	pla
IF R		F <sub>o</sub> LD0   F <sub>o</sub> LD2   TRI-	TRI-	ID。	PD_																	
			STATE	Щ	POL							<u> </u>		[4.0]							c	c
			۵		Щ							<u> </u>	_ _ _	ני.4: ארו איס ה דו							>	>
			Щ																			
RF R	F <sub>o</sub> LD1	RF R Fold Folds TRI-	TRI-	ID。	PD_																	
			STATE	RF	POL							ם מ		ONTER 14.01							c	,
			Ω		Æ							ב כ	2	ر اب							>	_
			RF																			
Z L	PWDN	N PRE																				
	些	Щ				_	N O	IF N_CNTRB[10:0]	[0:0]							<u>ш</u>	IF N_CNTRA[6:0]	A[6:0]			-	0
RF N	PWDN	N PRE																				
	Ä	Ä				Ш	R N_CI	RF N_CNTRB[10:0]	0:0]							H.	RF N_CNTRA[6:0]	[A[6:0]			-	-

#### 2.4 IF R REGISTER

The IF R register contains the IF R\_CNTR, PD\_POL IF, ID $_{\rm o}$  IF, and TRI-STATE ID $_{\rm o}$  IF control words, in addition to two bits that compose the F $_{\rm o}$ LD control word. The detailed descriptions and programming information for each control word is discussed in the following sections. IF R\_CNTR[14:0]

Reg.	Most	Sign	ifican	t Bit					SH	IFT R	EGIS	ΓER B	IT LC	CATI	ON				Leas	t Sigr	nificar	nt Bit
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					•			•	•	Doto	Field				•		•	•	•	•	Add	ress
										Data	rieia										Fie	eld
			TRI-																			
IF	E 1 D0		STATE	IDo	PD_ POL							IF R_	CNTR	8[14:0]	I						0	0
R	F <sub>o</sub> LD0	F <sub>0</sub> LD2	ID <sub>0</sub>	IF	IF									.[								
			IF		"																	

#### 2.4.1 IF R\_CNTR[14:0] IF SYNTHESIZER PROGRAMMABLE REFERENCE DIVIDER (R COUNTER)

IF R[2:16]

The IF reference divider (IF R\_CNTR) can be programmed to support divide ratios from 3 to 32767. Divide ratios less than 3 are prohibited.

Divide Ratio							IF R	CNTR	[14:0]						
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

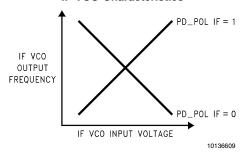
#### 2.4.2 PD\_POL IF IF SYNTHESIZER PHASE DETECTOR POLARITY

IF R[17]

The PD\_POL IF bit is used to control the IF synthesizer's phase detector polarity based on the VCO tuning characteristics.

Control Bit	Register Location	Description	Fun	ction
			0	1
PD_POL IF	IF R[17]	IF Phase Detector	IF VCO Negative	IF VCO Positive
		Polarity	Tuning	Tuning
			Characteristics	Characteristics

#### **IF VCO Characteristics**



#### 2.4.3 ID<sub>o</sub> IF IF SYNTHESIZER CHARGE PUMP CURRENT GAIN

IF R[18]

The ID<sub>o</sub> IF bit controls the IF synthesizer's charge pump gain. Two current levels are available.

Control Bit	Register Location	Description	Fund	ction
			0	1
ID <sub>o</sub> IF	IF R[18]	IF Charge Pump	LOW	HIGH
		Current Gain	0.95 mA	3.80 mA

#### 2.4.4 TRI-STATE ID IF IF SYNTHESIZER CHARGE PUMP TRI-STATE CURRENT

IF R[19]

The TRI-STATE  $ID_o$  IF bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the TRI-STATE  $ID_o$  IF bit.

Furthermore, the TRI-STATE  ${\rm ID_o}$  IF bit operates in conjuction with the PWDN IF bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Fund	ction
			0	1
TRI-STATE ID <sub>o</sub> IF	IF R[19]	IF Charge Pump	IF Charge Pump	IF Charge Pump
		TRI-STATE Current	Normal Operation	Output in High
				Impedance State

#### 2.5 RF R REGISTER

The RF R register contains the RF R\_CNTR, PD\_POL RF,  $ID_o$  RF, and TRI-STATE  $ID_o$  RF control words, in addition to two bits that compose the  $F_oLD$  control word. The detailed descriptions and programming information for each control word is discussed in the following sections.

Reg.	Most	Sign	ifican	t Bit					SH	IFT R	EGIS	ΓER B	IT LC	CATI	ON				Leas	t Sigi	nificai	nt Bit
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										Doto	Field										Add	ress
										Dala	rieiu										Fi	eld
RF			TRI-																			
R			STATE	IDo	PD_							RF R	CNITE	0.11	1						_	4
	F <sub>0</sub> LD1	F <sub>o</sub> LD3	IDo	RF	POL							11 11_	CIVII	ւլ 14.0	1						"	'
			RF		RF																	

#### 2.5.1 RF R\_CNTR[14:0] RF SYNTHESIZER PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) RF R[2:16]

The RF reference divider (RF R\_CNTR) can be programmed to support divide ratios from 3 to 32767. Divide ratios less than 3 are prohibited.

Divide Ratio							RF R	_CNTR	[14:0]						
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

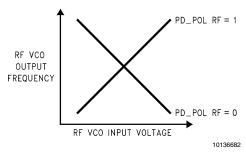
#### 2.5.2 PD\_POL RF RF SYNTHESIZER PHASE DETECTOR POLARITY

RF R[17]

The PD\_POL RF bit is used to control the RF synthesizer's phase detector polarity based on the VCO tuning characteristics.

Control Bit	Register Location	Description	Fund	ction
			0	1
PD_POL RF	RF R[17]	RF Phase Detector	RF VCO Negative	RF VCO Positive
		Polarity	Tuning	Tuning
			Characteristics	Characteristics

#### **RF VCO Characteristics**



#### 2.5.3 ID<sub>o</sub> RF RF SYNTHESIZER CHARGE PUMP CURRENT GAIN

RF R[18]

The ID<sub>o</sub> RF bit controls the RF synthesizer's charge pump gain. Two current levels are available.

Control Bit	Register Location	Description	Fund	ction
			0	1
ID <sub>o</sub> RF	RF R[18]	RF Charge Pump	LOW	HIGH
		Current Gain	0.95 mA	3.80 mA

#### 2.5.4 TRI-STATE ID RF RF SYNTHESIZER CHARGE PUMP TRI-STATE CURRENT

RF R[19]

The TRI-STATE ID<sub>o</sub> RF bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the TRI-STATE ID<sub>o</sub> RF bit.

Furthermore, the TRI-STATE  ${\rm ID_o}$  RF bit operates in conjuction with the PWDN RF bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function		
			0 1		
TRI-STATE ID <sub>o</sub> RF	RF R[19]	RF Charge Pump	RF Charge Pump RF Charge Pump		
		TRI-STATE Current	Normal Operation	Output in High	
			Impedance State		

#### 2.6 IF N REGISTER

The IF N register contains the IF N\_CNTRA, IF N\_CNTRB, PRE IF, and PWDN IF control words. The IF N\_CNTRA and IF N\_CNTRB control words are used to setup the programmable feedback divider. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	p. Most Significant Bit SHIFT REGISTER BIT LOCATION Least Significant Bit SHIFT REGISTER BIT LOCATION												nificai	nt Bit
	21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2												1	0
	Data Field													ress eld
IF N	PWDN PRE IF N_CNTRB[10:0] IF N_CNTRA[6:0]											1	0	

#### 2.6.1 IF N CNTRA[6:0] IF SYNTHESIZER SWALLOW COUNTER (A COUNTER)

IF N[2:8]

The IF N\_CNTRA control word is used to setup the IF synthesizer's A counter. The A counter is a 7-bit swallow counter used in the programmable feedback divider. The IF N\_CNTRA control word can be programmed to values ranging from 0 to 15. The three most significant bits are 'don't care bits' in this case.

Divide Ratio	IF N_CNTRA[6:0]										
	6	5	4	3	2	1	0				
0	X	Х	Х	0	0	0	0				
1	Х	Х	Х	0	0	0	1				
•	•	•	•	•	•	•	•				
15	X	Х	X	1	1	1	1				

#### 2.6.2 IF N\_CNTRB[10:0] IF SYNTHESIZER PROGRAMMABLE BINARY COUNTER (B COUNTER) IF N[9:19]

The IF N\_CNTRB control word is used to setup the IF synthesizer's B counter. The B counter is an 11-bit programmable binary counter used in the programmable feedback divider. The IF N\_CNTRB control word can be programmed to values ranging from 3 to 2047.

Divide	IF N_CNTRB[10:0]										
Ratio	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

#### 2.6.3 PRE IF

#### IF SYNTHESIZER PRESCALER SELECT

IF N[20]

The IF synthesizer utilizes a selectable dual modulus prescaler.

Control Bit	Register Location	Description	Fund	ction
			0	1
PRE IF	IF N[20]	IF Prescaler Select	8/9 Prescaler	16/17 Prescaler
			Selected	Selected

#### 2.6.4 PWDN IF IF SYNTHESIZER POWERDOWN

IF N[21]

The PWDN IF bit is used to switch the IF PLL between a powered up and powered down mode.

Furthermore, the PWDN IF bit operates in conjuction with the TRI-STATE  ${\rm ID_o}$  IF bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function		
			0	1	
PWDN IF	IF N[21]	IF Powerdown	IF PLL Active	IF PLL Powerdown	

#### 2.7 RF N REGISTER

The RF N register contains the RF N\_CNTRA, RF N\_CNTRB, PRE RF, and PWDN RF control words. The RF N\_CNTRA and RF N\_CNTRB control words are used to setup the programmable feedback divider. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	. Most Significant Bit SHIFT REGISTER BIT LOCATION Least Significant Bit												nificar	nt Bit	
	21	21   20   19   18   17   16   15   14   13   12   11   10   9   8   7   6   5   4   3   2											1	0	
	Data Field														ress eld
RF N	PWDN PRE RF N_CNTRB[10:0] RF N_CNTRA[6:0]											1	1		

#### 2.7.1 RF N\_CNTRA[6:0] RF SYNTHESIZER SWALLOW COUNTER (A COUNTER)

RF N[2:8]

The RF N\_CNTRA control word is used to setup the RF synthesizer's A counter. The A counter is a 7-bit swallow counter used in the programmable feedback divider. The RF N\_CNTRA control word can be programmed to values ranging from 0 to 127.

Divide Ratio	RF N_CNTRA[6:0]											
	6	6 5 4 3 2 1 0										
0	0	0	0	0	0	0	0					
1	0	0	0	0	0	0	1					
•	•	•	•	•	•	•	•					
127	1	1	1	1	1	1	1					

#### 2.7.2 RF N\_CNTRB[10:0] RF SYNTHESIZER PROGRAMMABLE BINARY COUNTER (B COUNTER) RF N[9:19]

The RF N\_CNTRB control word is used to setup the RF synthesizer's B counter. The B counter is an 11-bit programmable binary counter used in the programmable feedback divider. The RF N\_CNTRB control word can be programmed to values ranging from 3 to 2047.

Divide		RF N_CNTRB[10:0]										
Ratio	10	9	8	7	6	5	4	3	2	1	0	
3	0	0	0	0	0	0	0	0	0	1	1	
4	0	0	0	0	0	0	0	0	1	0	0	
•	•	•	•	•	•	•	•	•	•	•	•	
2047	1	1	1	1	1	1	1	1	1	1	1	

#### 2.7.3 PRE RF

#### RF SYNTHESIZER PRESCALER SELECT

RF N[20]

The RF synthesizer utilizes a selectable dual modulus prescaler.

#### LMX2330U RF Synthesizer Prescaler Select

Control Bit	Register Location	Description	Fund	ction
			0	1
PRE RF	RF N[20]	RF Prescaler Select	32/33 Prescaler Selected	64/65 Prescaler Selected

#### LMX2331U and LMX2332U RF Synthesizer Prescaler Select

Control Bit	Register Location	Description	Fund	ction
			0	1
PRE RF	RF N[20]	RF Prescaler Select	64/65 Prescaler Selected	128/129 Prescaler Selected

#### 2.7.4 PWDN RF RF SYNTHESIZER POWERDOWN

RF N[21]

The PWDN RF bit is used to switch the RF PLL between a powered up and powered down mode.

Furthermore, the PWDN RF bit operates in conjuction with the TRI-STATE  ${\rm ID_o}$  RF bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function		
			0	1	
PWDN RF	RF N[21]	RF Powerdown	RF PLL Active	RF PLL Powerdown	

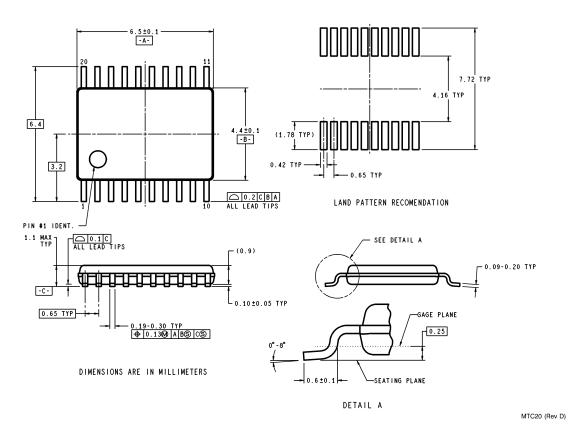
#### 2.8 F<sub>o</sub>LD[3:0] MULTI-FUNCTION OUTPUT SELECT

[RF R[20], IF R[20], RF R [21], IF R[21]]

The F<sub>o</sub>LD control word is used to select which signal is routed to the F<sub>o</sub>LD pin.

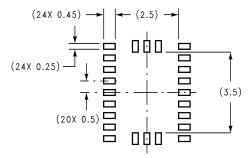
F <sub>o</sub> LD3	F <sub>o</sub> LD2	F <sub>o</sub> LD1	F <sub>o</sub> LD0	F <sub>o</sub> LD Output State
0	0	0	0	LOW Logic State Output
0	0	0	1	IF PLL R Divider Output, Push-Pull Output
0	0	1	0	RF PLL R Divider Output, Push-Pull Output
0	0	1	1	Open Drain Fastlock Output
0	1	0	0	IF PLL Analog Lock Detect, Push-Pull Output
0	1	0	1	IF PLL N Divider Output, Push-Pull Output
0	1	1	0	RF PLL N Divider Output, Push-Pull Output
0	1	1	1	Reset IF Counters, LOW Logic State Output
1	0	0	0	RF Analog Lock Detect, Push-Pull Output
1	0	0	1	IF PLL R Divider Output, Push-Pull Output
1	0	1	0	RF PLL R Divider Output, Push-Pull Output
1	0	1	1	Reset RF Counters, LOW Logic State Output
1	1	0	0	RF and IF Analog Lock Detect, Push-Pull Output
1	1	0	1	IF PLL N Divider Output, Push-Pull Output
1	1	1	0	RF PLL N Divider Output, Push-Pull Output
1	1	1	1	Reset All Counters, LOW Logic State Output

#### Physical Dimensions inches (millimeters) unless otherwise noted



20-Pin Thin Shrink Small Outline Package (TM) NS Package Number MTC20

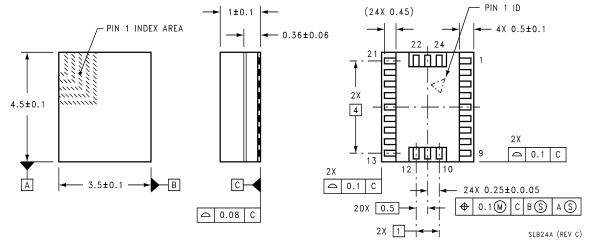
#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

#### RECOMMENDED LAND PATTERN

1:1 RATIO WITH PACKAGE SOLDER PADS



24-Pin Chip Scale Package (SLB) **NS Package Number SLB24A** 

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