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ELECTRONICS

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Jameco Part Number 1726794



# LT1001

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage .....	±22V
Differential Input Voltage .....	±30V
Input Voltage .....	±22V
Output Short Circuit Duration .....	Indefinite

Operating Temperature Range

LT1001AM/LT1001M (OBSOLETE) ..	-55°C to 150°C
LT1001AC/LT1001C .....	0°C to 125°C
Storage: All Devices .....	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .....	300°C

## PACKAGE/ORDER INFORMATION

<p>TOP VIEW OFFSET ADJUST</p> <p>1 8 2 7 3 6 4 5 5 NC 6 OUT 7 V+ 8 VOS TRIM</p> <p>-IN 2 +IN 3 V- (CASE) 4 H PACKAGE METAL CAN</p> <p><math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 150^{\circ}C/W, \theta_{JC} = 45^{\circ}C/W</math></p> <p><b>OBSOLETE PACKAGE</b> Consider the N8 and S8 Packages for Alternate Source</p>	<p>ORDER PART NUMBER</p> <p>LT1001AMH/883 LT1001MH LT1001ACH LT1001CH</p>	<p>TOP VIEW</p> <p>1 VOS TRIM 8 VOS TRIM 2 -IN 7 V+ 3 +IN 6 OUT 4 V- 5 NC</p> <p>N8 PACKAGE 8 PIN PLASTIC DIP S8 PACKAGE 8 PIN PLASTIC SO</p> <p><math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 130^{\circ}C/W</math> (N) <math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 150^{\circ}C/W</math> (S)</p>	<p>ORDER PART NUMBER</p> <p>LT1001ACN8 LT1001CN8 LT1001CS8</p>
	<p>ORDER PART NUMBER</p> <p>LT1001AMJ8/883 LT1001MJ8 LT1001ACJ8 LT1001CJ8</p>		
		<p>S8 PART MARKING</p> <p>1001</p>	
		<p>J8 PACKAGE 8 PIN HERMETIC DIP <math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 100^{\circ}C/W</math> (J)</p>	<p>ORDER PART NUMBER</p>
		<p><b>OBSOLETE PACKAGE</b> Consider the N8 and S8 Packages for Alternate Source</p>	

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ .  $V_S = \pm 15V$ , unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001AM/883 LT1001AC			LT1001M/LT1001C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
$V_{OS}$	Input Offset Voltage	Note 2	LT1001AM/883		7	15	18		60	μV
			LT1001AC		10	25				
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	Notes 3 and 4			0.2	1.0	0.3	1.5		μV/month
$I_{OS}$	Input Offset Current				0.3	2.0	0.4	3.8		nA
$I_b$	Input Bias Current				±0.5	±2.0	±0.7	±4.0		nA
$e_n$	Input Noise Voltage	0.1Hz to 10Hz (Note 3)			0.3	0.6	0.3	0.6		μV <sub>p-p</sub>
$e_n$	Input Noise Voltage Density	$f_0 = 10Hz$ (Note 6) $f_0 = 1000Hz$ (Note 3)			10.3	18.0	10.5	18.0		nV $\sqrt{Hz}$ nV $\sqrt{Hz}$
$A_{VOL}$	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_0 = \pm 12V$ $R_L \geq 1k\Omega, V_0 = \pm 10V$	450	800	400	800				V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	114	126	110	126				dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	110	123	106	123				dB
$R_{in}$	Input Resistance Differential Mode		30	100	15	80				MΩ

1001fb

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_S = \pm 15\text{V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001AM/883			LT1001M/LT1001C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
	Input Voltage Range		±13	±14		±13	±14		V	
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2\text{k}\Omega$	±13	±14		±13	±14		V	
		$R_L \geq 1\text{k}\Omega$	±12	±13.5		±12	±13.5		V	
$S_R$	Slew Rate	$R_L \geq 2\text{k}\Omega$ (Note 5)	0.1	0.25		0.1	0.25		V/ $\mu\text{s}$	
GBW	Gain-Bandwidth Product	(Note 5)	0.4	0.8		0.4	0.8		MHz	
$P_d$	Power Dissipation	No load		46	75		48	80		mW
		No load, $V_S = \pm 3\text{V}$		4	6		4	8		mW

$V_S = \pm 15\text{V}$ ,  $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ , unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001AM/883			LT1001M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage		●	30	60		45	160	$\mu\text{V}$
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Offset Voltage Drift		●	0.2	0.6		0.3	1.0	$\mu\text{V}/^\circ\text{C}$
$I_{OS}$	Input Offset Current		●	0.8	4.0		1.2	7.6	nA
$I_B$	Input Bias Current		●	±1.0	±4.0		±1.5	±8.0	nA
$A_{VOL}$	Large Signal Voltage Gain	$R_L \geq 2\text{k}\Omega$ , $V_O = \pm 10\text{V}$	●	300	700		200	700	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13\text{V}$	●	110	122		106	120	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3$ to $\pm 18\text{V}$	●	104	117		100	117	dB
	Input Voltage Range		●	±13	±14		±13	±14	V
$V_{OUT}$	Output Voltage Swing	$R_L \geq 2\text{k}\Omega$	●	±12.5	±13.5		±12.0	±13.5	V
$P_d$	Power Dissipation	No load	●	55	90		60	100	mW

$V_S = \pm 15\text{V}$ ,  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ , unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001AC			LT1001C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage		●	20	60		30	110	$\mu\text{V}$
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Offset Voltage Drift		●	0.2	0.6		0.3	1.0	$\mu\text{V}/^\circ\text{C}$
$I_{OS}$	Input Offset Current		●	0.5	3.5		0.6	5.3	nA
$I_B$	Input Bias Current		●	±0.7	±3.5		±1.0	±5.5	nA
$A_{VOL}$	Large Signal Voltage Gain	$R_L \geq 2\text{k}\Omega$ , $V_O = \pm 10\text{V}$	●	350	750		250	750	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13\text{V}$	●	110	124		106	123	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3\text{V}$ to $\pm 18\text{V}$	●	106	120		103	120	dB
	Input Voltage Range		●	±13	±14		±13	±14	V
$V_{OUT}$	Output Voltage Swing	$R_L \geq 2\text{k}\Omega$	●	±12.5	±13.8		±12.5	±13.8	V
$P_d$	Power Dissipation	No load	●	50	85		55	90	mW

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Offset voltage for the LT1001AM/883 and LT1001AC are measured after power is applied and the device is fully warmed up. All other grades are measured with high speed test equipment, approximately 1 second after power is applied. The LT1001AM/883 receives 168 hr. burn-in at  $125^\circ\text{C}$ . or equivalent.

**Note 3:** This parameter is tested on a sample basis only.

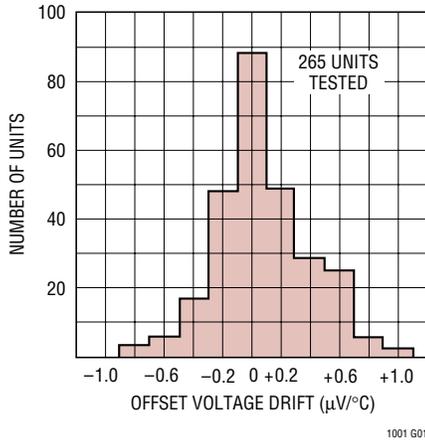
**Note 4:** Long Term Input Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 days are typically  $2.5\mu\text{V}$ .

**Note 5:** Parameter is guaranteed by design.

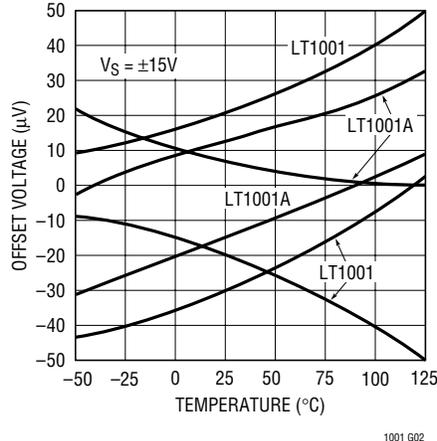
**Note 6:** 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

# TYPICAL PERFORMANCE CHARACTERISTICS

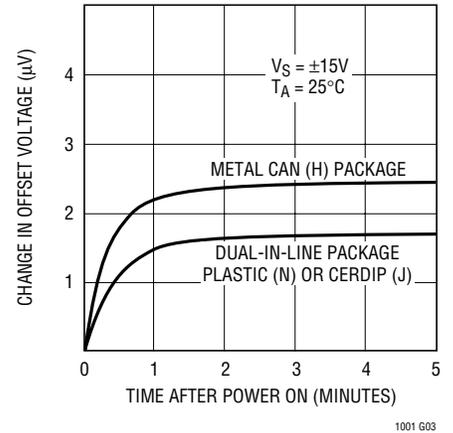
**Typical Distribution of Offset Voltage Drift with Temperature**



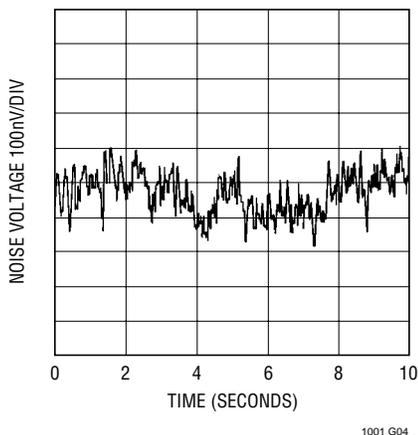
**Offset Voltage Drift with Temperature of Representative Units**



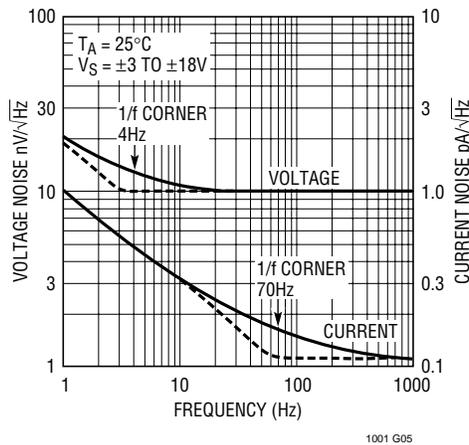
**Warm-Up Drift**



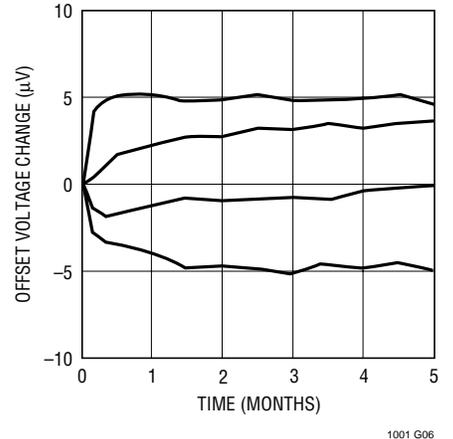
**0.1Hz to 10Hz Noise**



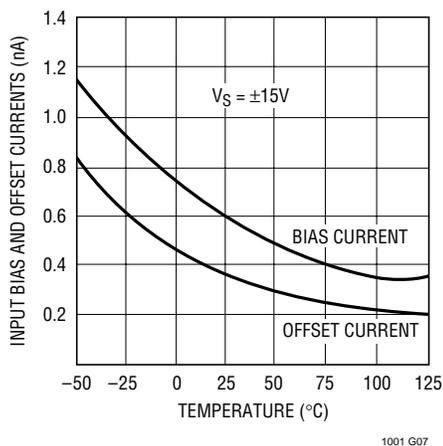
**Noise Spectrum**



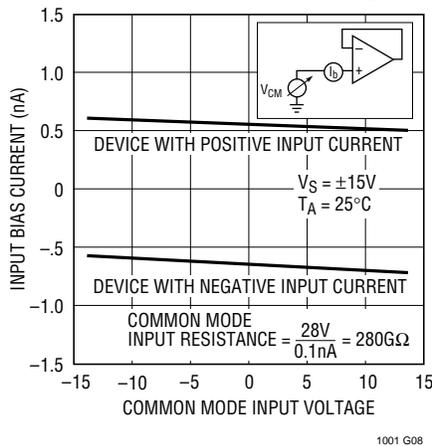
**Long Term Stability of Four Representative Units**



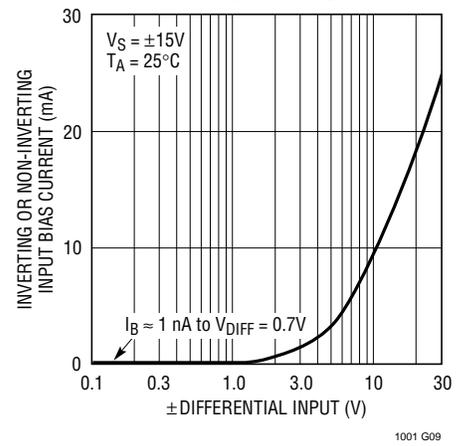
**Input Bias and Offset Current vs Temperature**



**Input Bias Current Over the Common Mode Range**

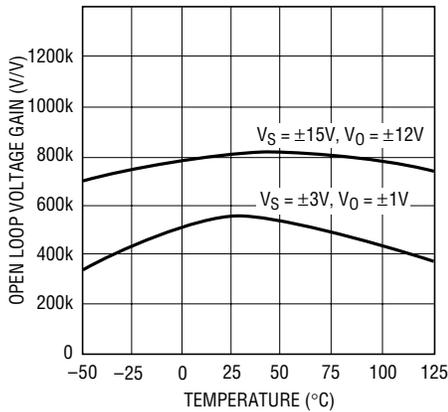


**Input Bias Current vs Differential Input Voltage**

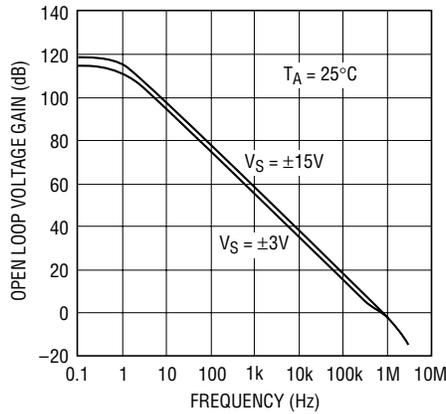


# TYPICAL PERFORMANCE CHARACTERISTICS

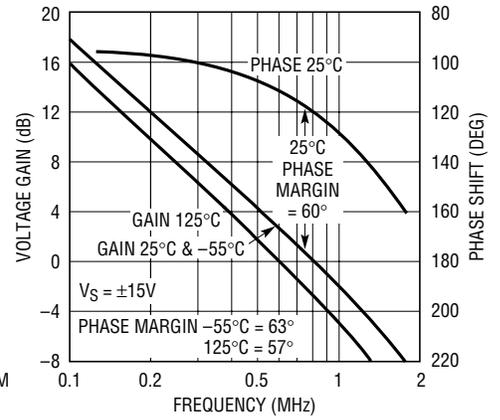
**Open Loop Voltage Gain vs Temperature**



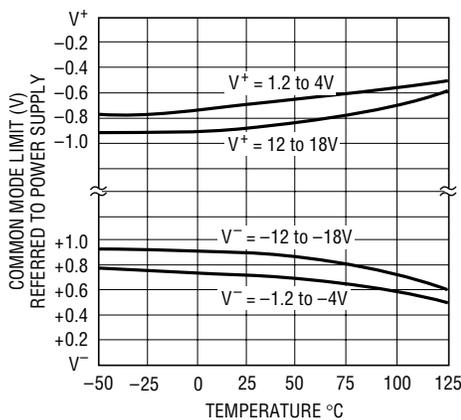
**Open Loop Voltage Gain Frequency Response**



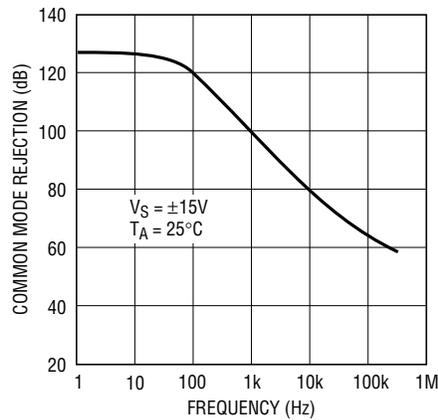
**Gain, Phase Shift vs Frequency**



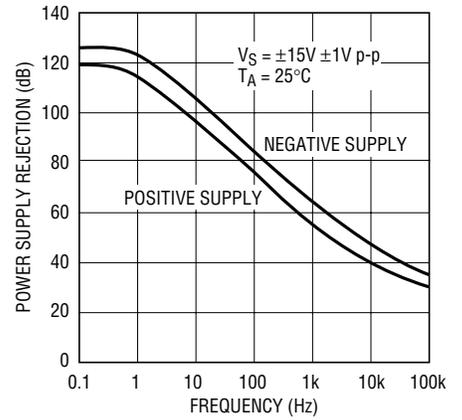
**Common Mode Limit vs Temperature**



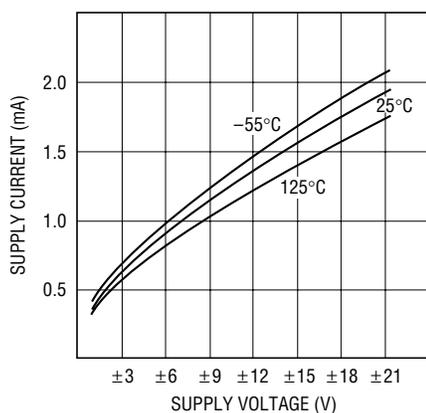
**Common Mode Rejection Ratio vs Frequency**



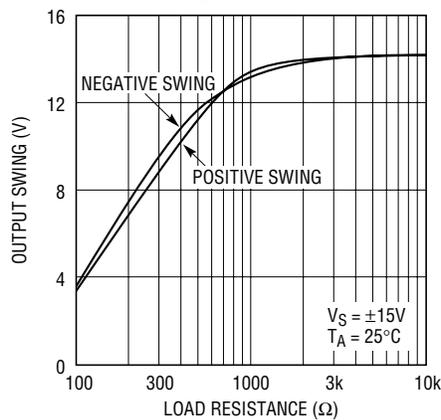
**Power Supply Rejection Ratio vs Frequency**



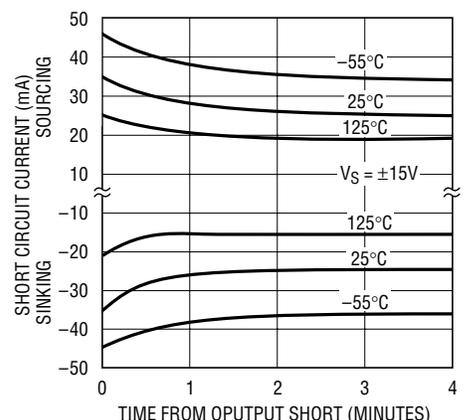
**Supply Current vs Supply Voltage**



**Output Swing vs Load Resistance**

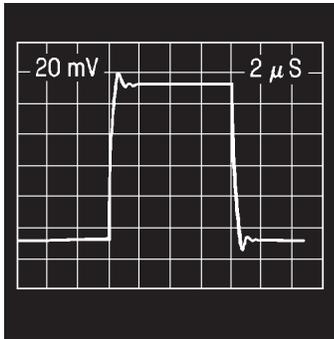


**Output Short-Circuit Current vs Time**



# TYPICAL PERFORMANCE CHARACTERISTICS

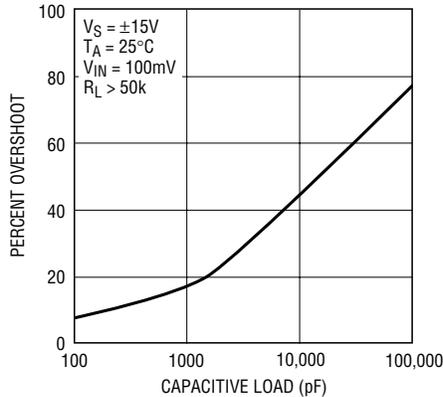
Small Signal Transient Response



$A_V = +1, C_L = 50\text{pF}$

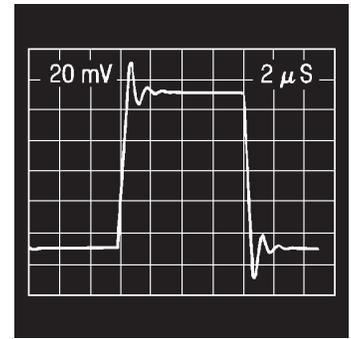
1001 G19

Voltage Follower Overshoot vs Capacitive Load



1001 G20

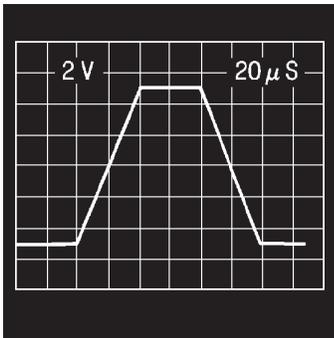
Small Signal Transient Response



$A_V = +1, C_L = 1000\text{pF}$

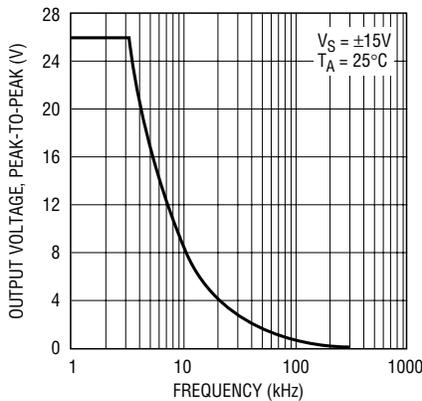
1001 G21

Large Signal Transient Response



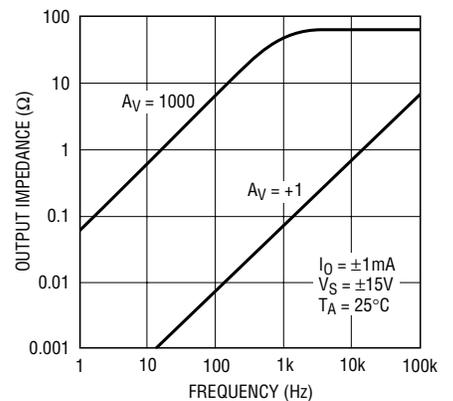
1001 G22

Maximum Undistorted Output vs. Frequency



1001 G23

Closed Loop Output Impedance



1001 G24

## APPLICATIONS INFORMATION

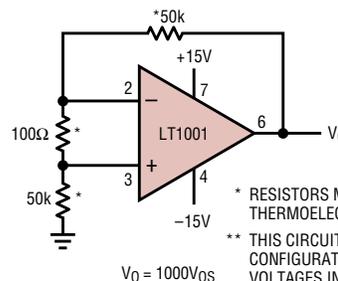
### Application Notes and Test Circuits

The LT1001 series units may be inserted directly into OP-07, OP-05, 725, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT1001 can also be used in 741, LF156 or OP-15 applications provided that the nulling circuitry is removed.

The LT1001 is specified over a wide range of power supply voltages from  $\pm 3\text{V}$  to  $\pm 18\text{V}$ . Operation with lower supplies is possible down to  $\pm 1.2\text{V}$  (two Ni-Cad batteries). However, with  $\pm 1.2\text{V}$  supplies, the device is stable only in closed loop gains of +2 or higher (or inverting gain of one or higher).

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Test Circuit for Offset Voltage and its Drift with Temperature



\* RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.

\*\* THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION FOR THE LT1001, WITH SUPPLY VOLTAGES INCREASED TO  $\pm 20\text{V}$ .

$V_O = 1000V_{OS}$

1001 F01 1001fb

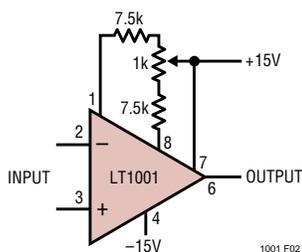
# APPLICATIONS INFORMATION

## Offset Voltage Adjustment

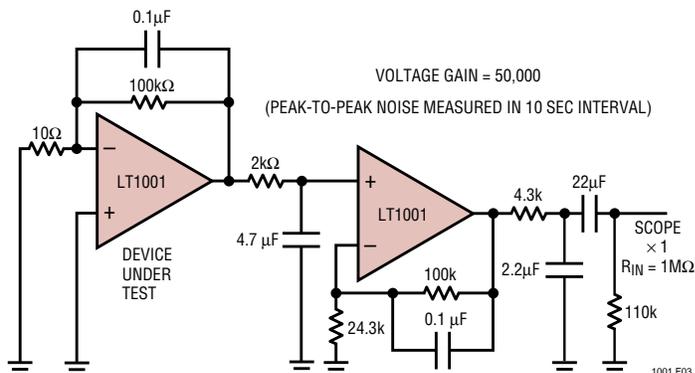
The input offset voltage of the LT1001, and its drift with temperature, are permanently trimmed at wafer test to a low level. However, if further adjustment of  $V_{os}$  is necessary, nulling with a 10k or 20k potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of  $(V_{os}/300)\mu V/^\circ C$ , e.g., if  $V_{os}$  is

adjusted to  $300\mu V$ , the change in drift will be  $1\mu V/^\circ C$ . The adjustment range with a 10k or 20k pot is approximately  $\pm 2.5mV$ . If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example below has an approximate null range of  $\pm 100\mu V$ .

### Improved Sensitivity Adjustment

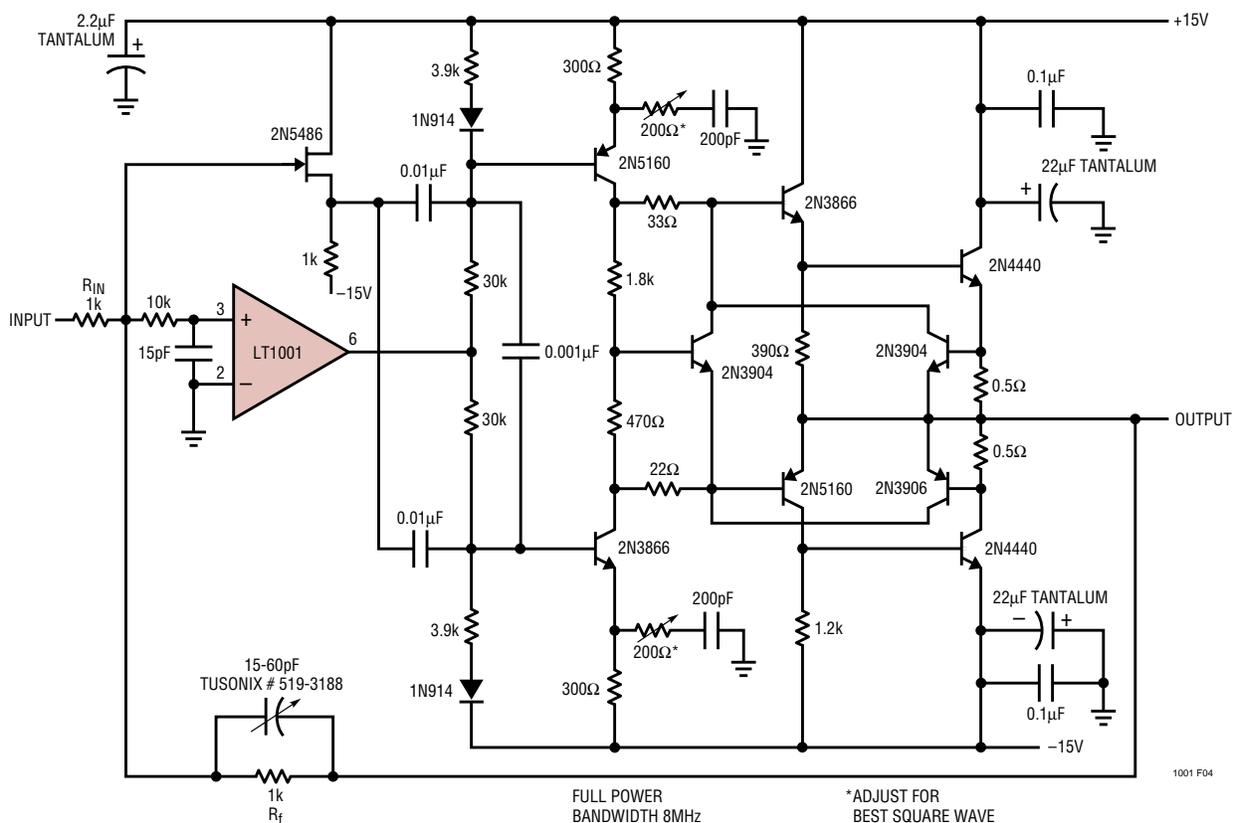


### 0.1Hz to 10Hz Noise Test Circuit



The device under test should be warmed up for three minutes and shielded from air currents.

### DC Stabilized 1000v/µsec Op Amp



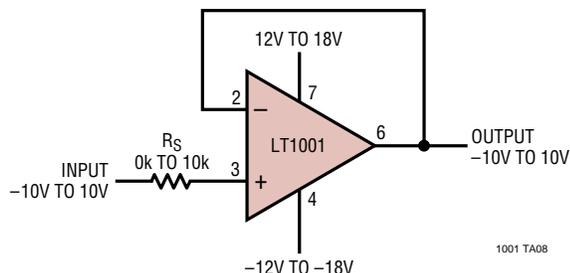
FULL POWER BANDWIDTH 8MHz

\*ADJUST FOR BEST SQUARE WAVE AT OUTPUT



## TYPICAL APPLICATIONS

**Large Signal Voltage Follower  
With 0.001% Worst Case Accuracy**

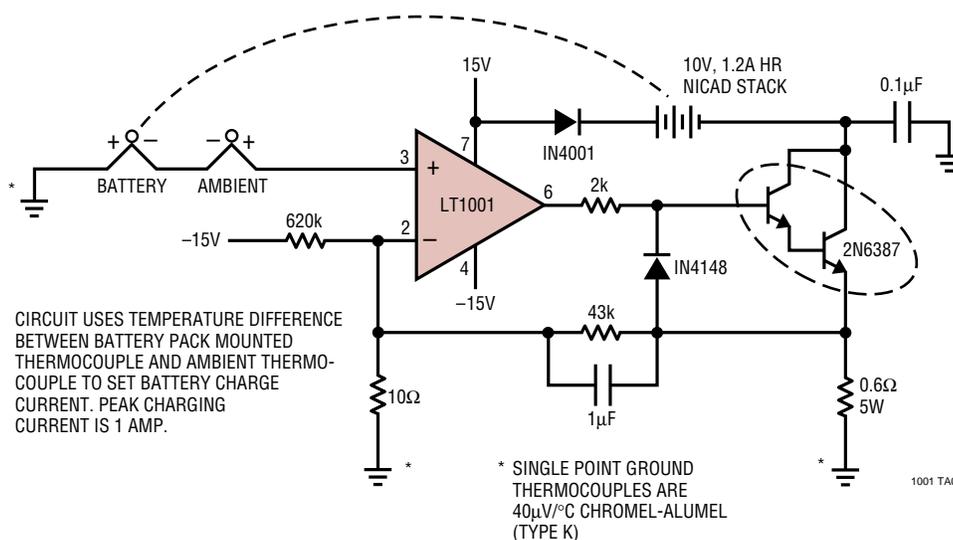


The voltage follower is an ideal example illustrating the overall excellence of the LT1001. The contributing error terms are due to offset voltage, input bias current, voltage gain, common mode and power-supply

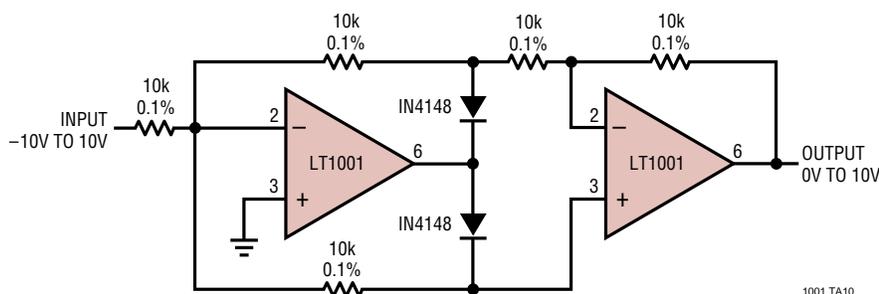
rejections. Worst-case summation of guaranteed specifications is tabulated below.

Error	OUTPUT ACCURACY			
	LT1001AM /883	LT1001C	LT1001AM /883	LT1001C
	25°C Max.	25°C Max.	-55 to 125°C Max.	0 to 70°C Max.
Offset Voltage	15μV	60μV	60μV	110μV
Bias Current	20μV	40μV	40μV	55μV
Common Mode Rejection	20μV	30μV	30μV	50μV
Power Supply Rejection	18μV	30μV	36μV	42μV
Voltage Gain	22μV	25μV	33μV	40μV
Worst-case Sum	95μV	185μV	199μV	297μV
Percent of Full Scale (=20V)	0.0005%	0.0009%	0.0010%	0.0015%

**Thermally Controlled NiCad Charger**

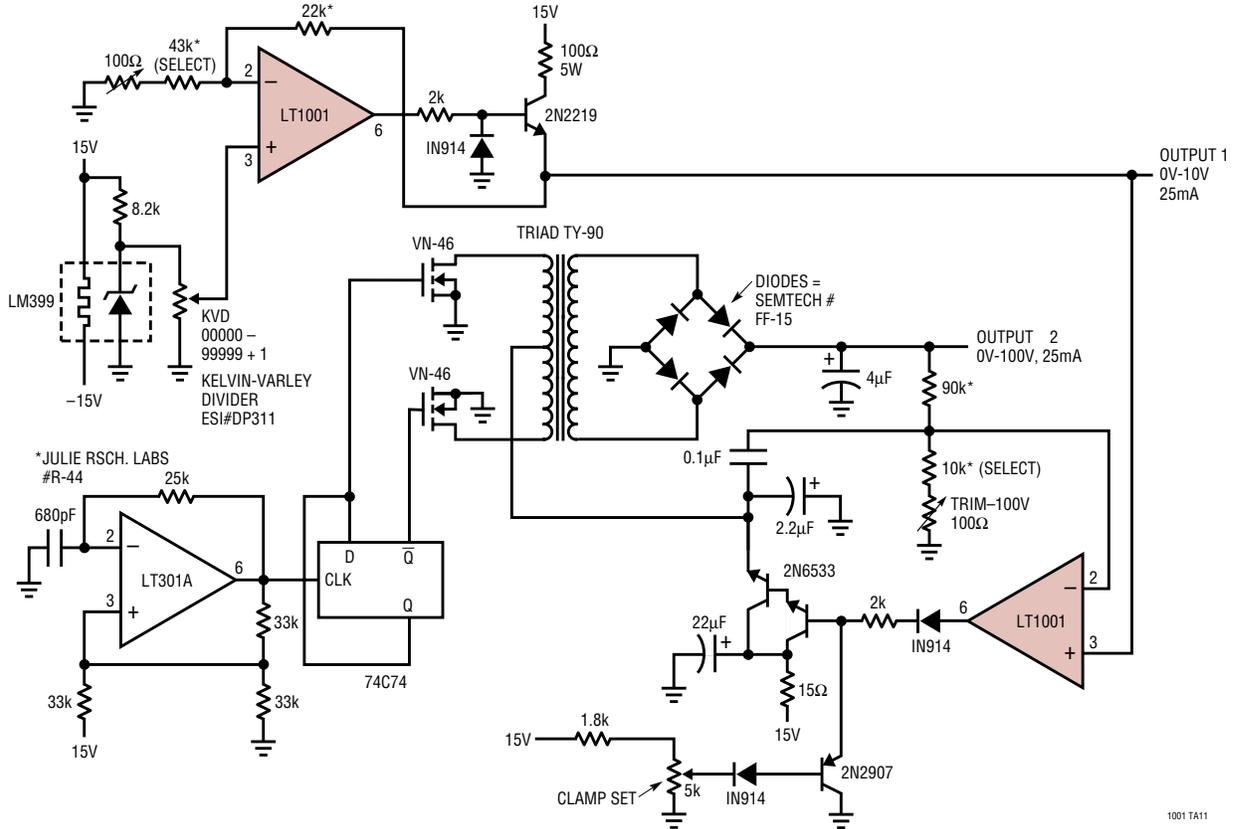


**Precision Absolute Value Circuit**



TYPICAL APPLICATIONS

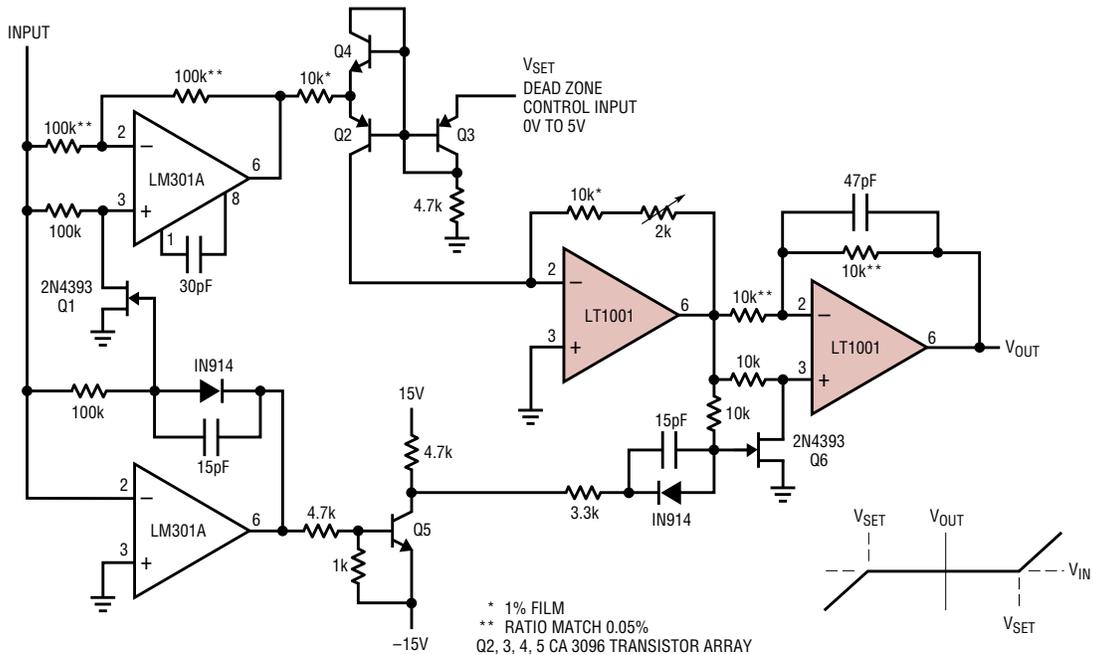
Precision Power Supply with Two Outputs  
 (1) 0V to 10V in 100µV STEPS (2) 0V to 100V in 1mV STEPS



1001 TA11

Dead Zone Generator

BIPOLAR SYMMETRY IS EXCELLENT BECAUSE ONE DEVICE, Q2, SETS BOTH LIMITS



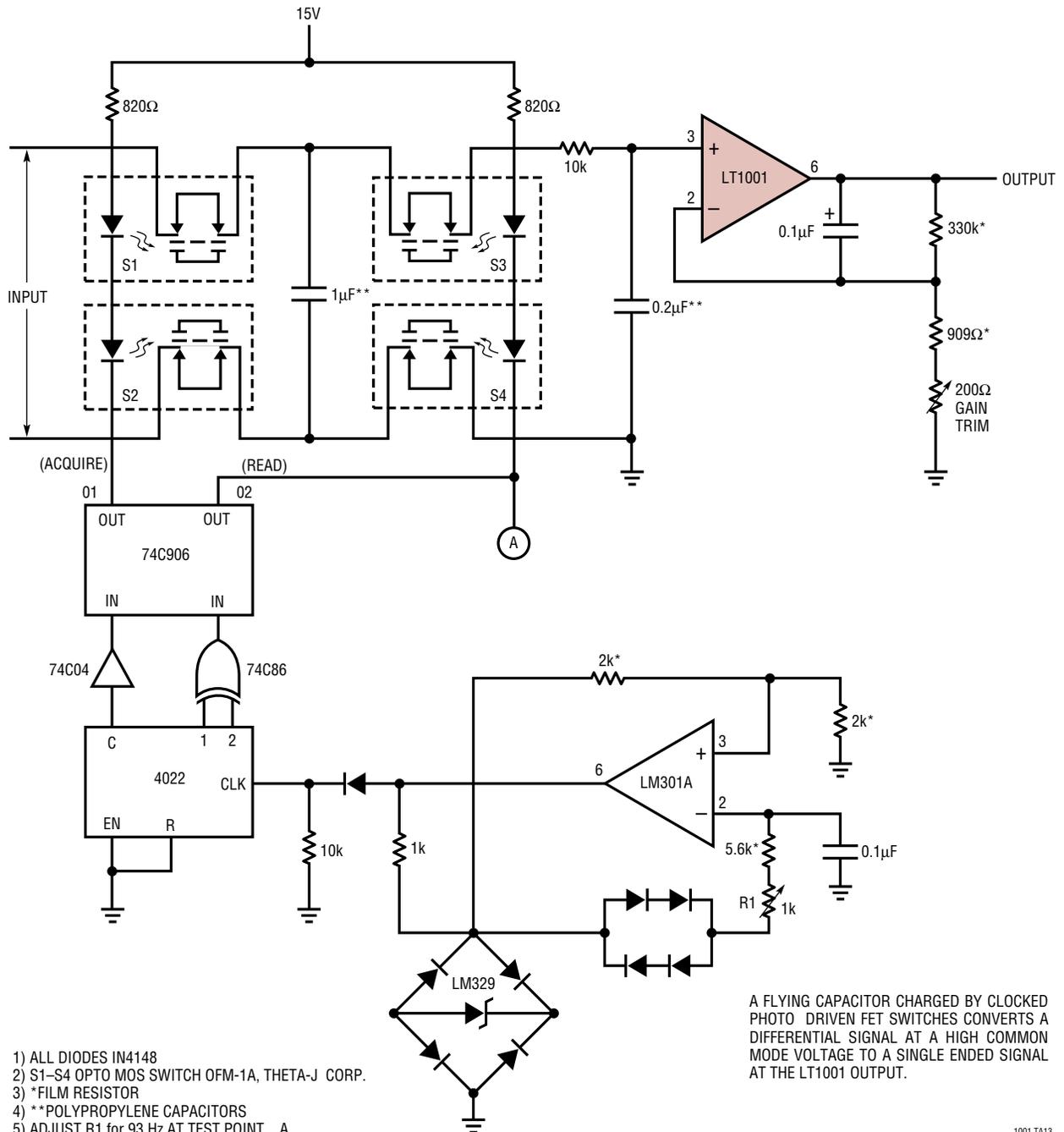
\* 1% FILM  
 \*\* RATIO MATCH 0.05%  
 Q2, 3, 4, 5 CA 3096 TRANSISTOR ARRAY

1001 TA12

1001fb

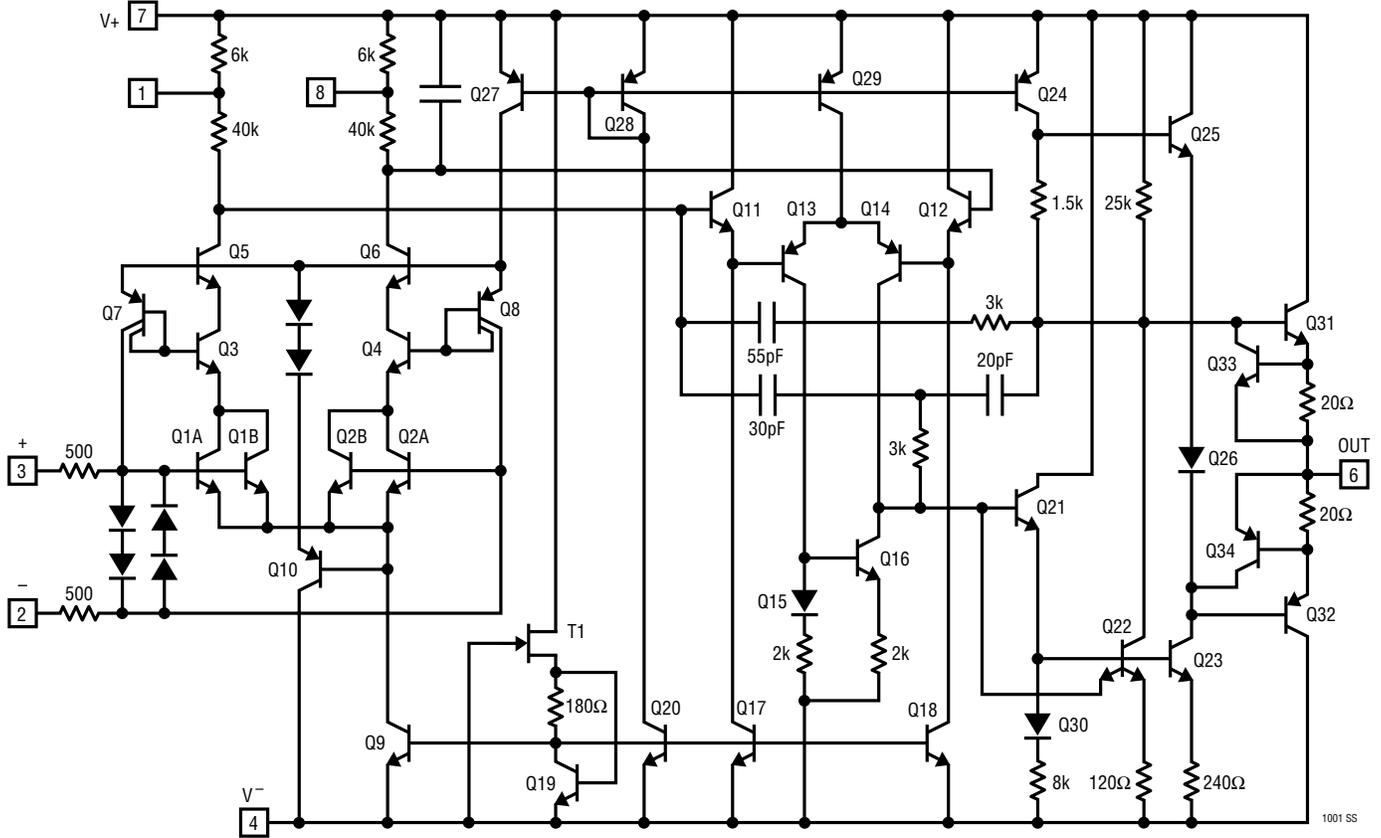
# TYPICAL APPLICATIONS

## Instrumentation Amplifier with $\pm 300V$ Common Mode Range and CMRR > 150dB



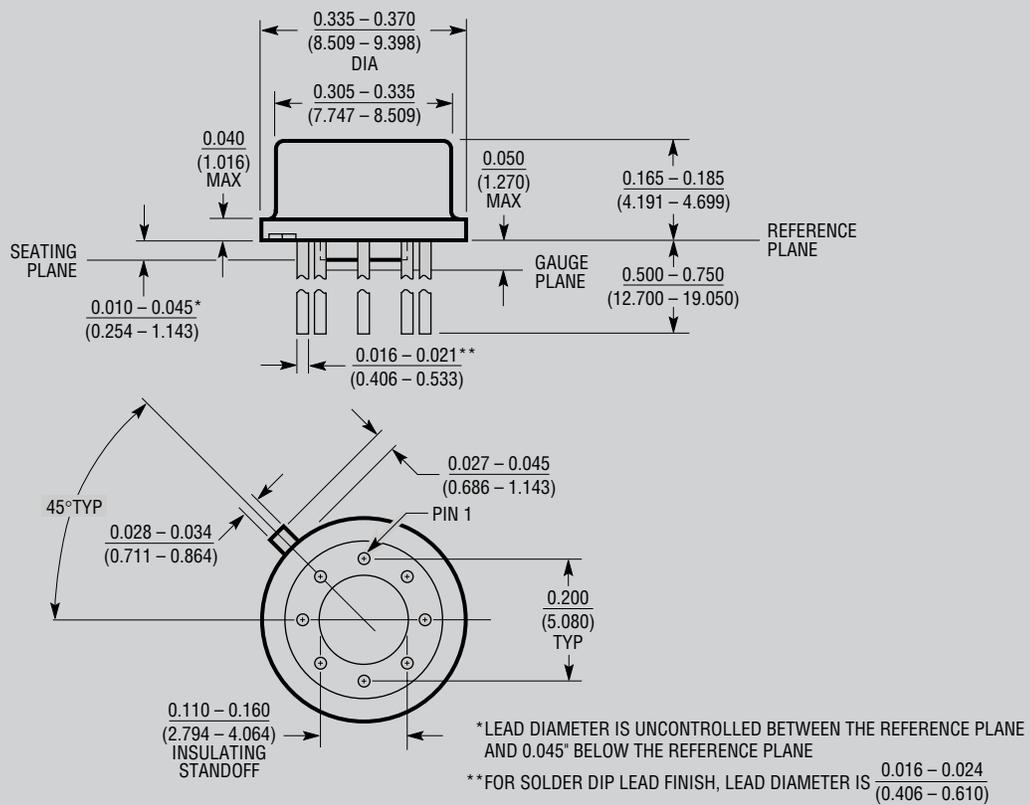
1001 TA13

# SCHEMATIC DIAGRAM



**PACKAGE DESCRIPTION**

**H Package**  
**8-Lead TO-5 Metal Can (.200 Inch PCD)**  
 (Reference LTC DWG # 05-08-1320)

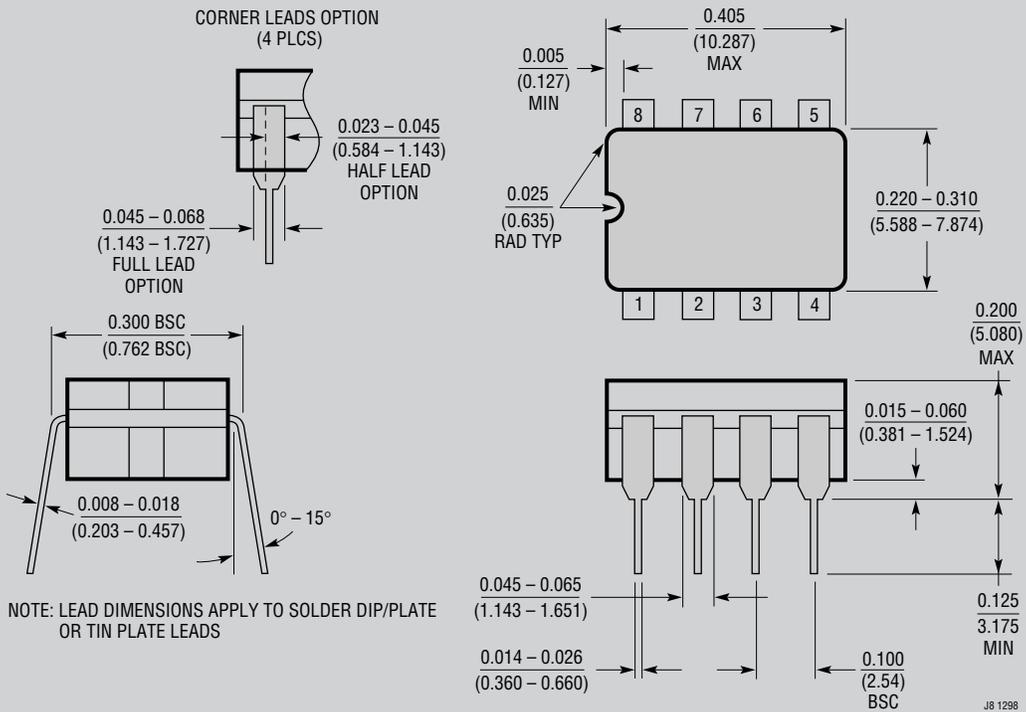


H8(TO-5) 0.200 PCD 1197

**OBSOLETE PACKAGE**

**PACKAGE DESCRIPTION**

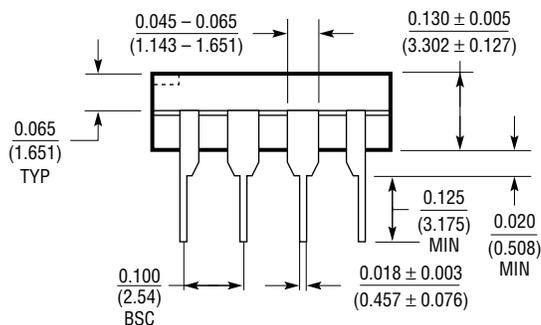
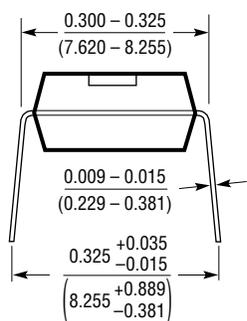
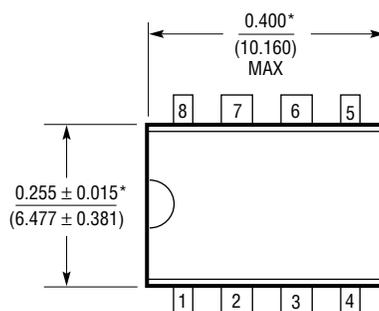
**J8 Package**  
**8-Lead CERDIP (Narrow .300 Inch, Hermetic)**  
 (Reference LTC DWG # 05-08-1110)



**OBSOLETE PACKAGE**

# PACKAGE DESCRIPTION

**N8 Package**  
**8-Lead PDIP (Narrow .300 Inch)**  
 (Reference LTC DWG # 05-08-1510)

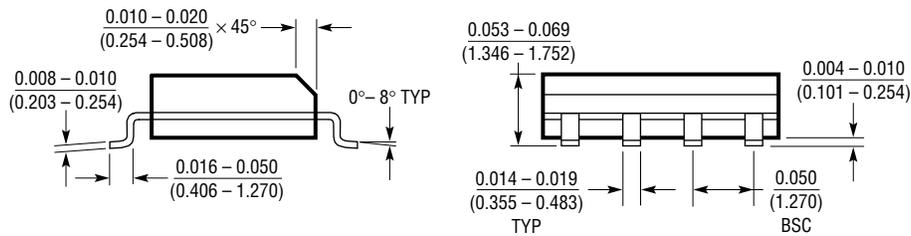
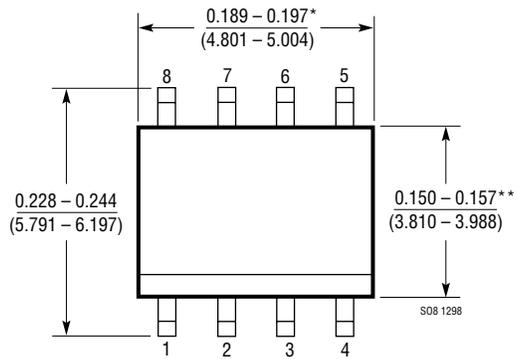


\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N8 1098

**PACKAGE DESCRIPTION**

**S8 Package**  
**8-Lead Plastic Small Outline (Narrow .150 Inch)**  
 (Reference LTC DWG # 05-08-1610)



\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE