LTC3412

2.5A, 4MHz, Monolithic Synchronous Step-Down Regulator

FEATURES

- **High Efficiency: Up to 95%**
- **2.5A Output Current**
- **Low Quiescent Current: 62μA**
- **Low $R_{DS(ON)}$ Internal Switches: 85mΩ**
- **Programmable Frequency: 300kHz to 4MHz**
- No Schottky Diode Required
- ±2% Output Voltage Accuracy
- 0.8V Reference Allows Low Output Voltage
- Selectable Forced Continuous/Burst Mode Operation with Adjustable Burst Clamp
- Synchronizable Switching Frequency
- Low Dropout Operation: 100% Duty Cycle
- Power Good Output Voltage Monitor
- Overtemperature Protection
- Available in 16-Lead Thermally Enhanced TSSOP and QFN Packages

APPLICATIONS

- Portable Instruments
- Battery-Powered Equipment
- Notebook Computers
- Distributed Power Systems
- Cellular Telephones
- Digital Cameras

DESCRIPTION

The LTC®3412 is a high efficiency monolithic synchronous, step-down DC/DC converter utilizing a constant frequency, current mode architecture. It operates from an input voltage range of 2.625V to 5.5V and provides an adjustable regulated output voltage from 0.8V to 5V while delivering up to 2.5A of output current. The internal synchronous power switch with 85mΩ on-resistance increases efficiency and eliminates the need for an external Schottky diode. Switching frequency is set by an external resistor or can be sychronized to an external clock. 100% duty cycle provides low dropout operation extending battery life in portable systems. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

The LTC3412 can be configured for either Burst Mode® operation or forced continuous operation. Forced continuous operation reduces noise and RF interference while Burst Mode operation provides high efficiency by reducing gate charge losses at light loads. In Burst Mode operation, external control of the burst clamp level allows the output voltage ripple to be adjusted according to the requirements of the application. To further maximize battery life, the P-channel MOSFET is turned on continuously in dropout (100% duty cycle).

$\boldsymbol{\mathcal{LT}}$, LT, LTC, LTM, Burst Mode and OPTI-LOOP are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.
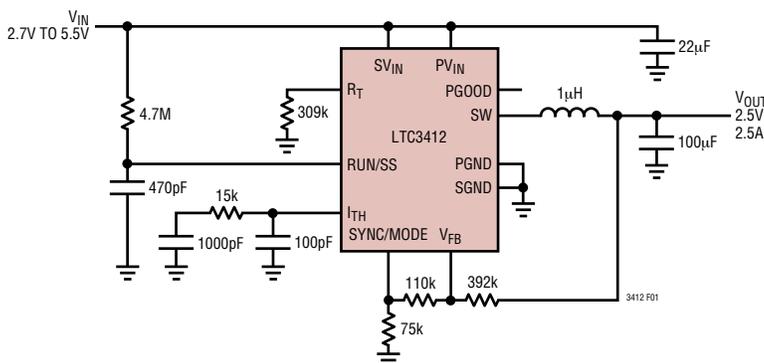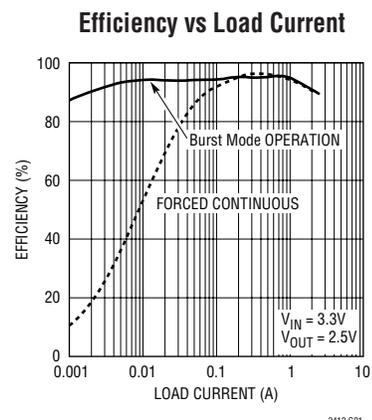
TYPICAL APPLICATION

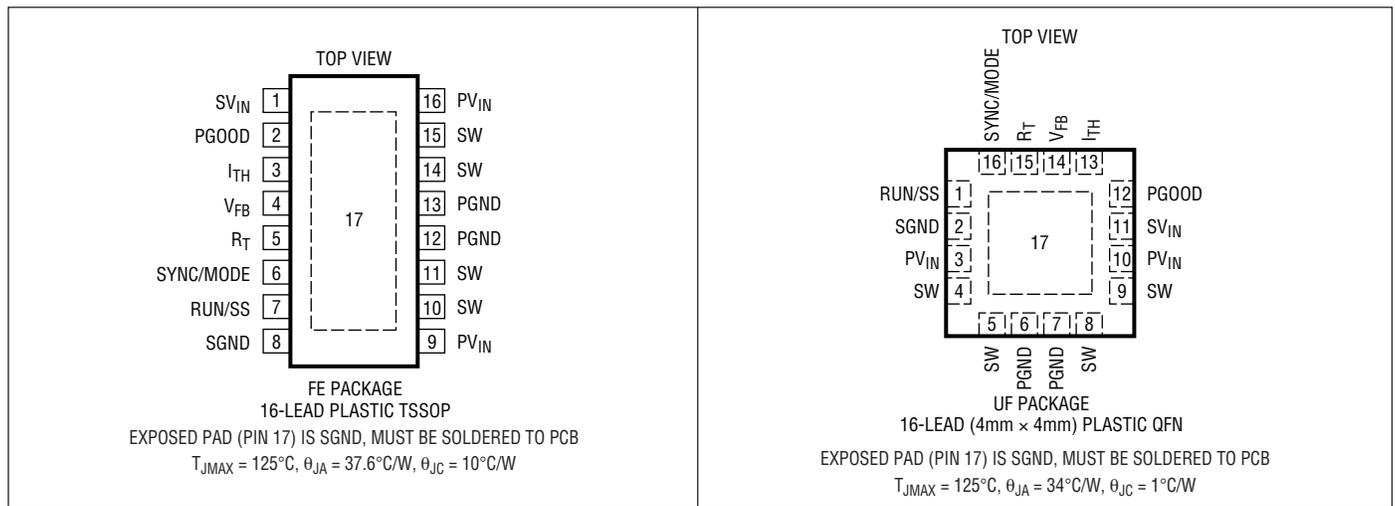Figure 1. 2.5V, 2.5A Step-Down Regulator

Efficiency vs Load Current

LTC3412

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage .... −0.3V to 6V
I_{TH}, RUN, V_{FB} Voltages .... −0.3V to V_{IN}
SYNC/MODE Voltages .... −0.3V to V_{IN}
SW Voltage .... −0.3V to (V_{IN} + 0.3V)
Peak SW Sink and Source Current 6.5A

Operating Temperature
Range (Note 2) .... −40°C to 85°C
Junction Temperature (Note 5) .... 125°C
Lead Temperature (Soldering, 10 sec)
    TSSOP .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

SV$_{IN}$ [1]   [16] PV$_{IN}$
PGOOD [2]   [15] SW
I$_{TH}$ [3]   [14] SW
V$_{FB}$ [4]   [13] PGND
R$_T$ [5]   17   [12] PGND
SYNC/MODE [6]   [11] SW
RUN/SS [7]   [10] SW
SGND [8]   [9] PV$_{IN}$

FE PACKAGE
16-LEAD PLASTIC TSSOP
EXPOSED PAD (PIN 17) IS SGND, MUST BE SOLDERED TO PCB
T_{JMAX} = 125°C, θ_{JA} = 37.6°C/W, θ_{JC} = 10°C/W

TOP VIEW

SYNC/MODE   R$_T$ V$_{FB}$ I$_{TH}$
[16] [15] [14] [13]
RUN/SS [1]   [12] PGOOD
SGND [2]   17   [11] SV$_{IN}$
PV$_{IN}$ [3]   [10] PV$_{IN}$
SW [4]   [9] SW
[5] [6] [7] [8]
SW   PGND   PGND   SW

UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
EXPOSED PAD (PIN 17) IS SGND, MUST BE SOLDERED TO PCB
T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 1°C/W

ORDER PART NUMBER	FE PART MARKING	ORDER PART NUMBER	UF PART MARKING
LTC3412EFE LTC3412IFE	3412EFE 3412IFE	LTC3412EUF	3412

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF   Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SV$_{IN}$	Signal Input Voltage Range			2.625		5.5	V
V$_{FB}$	Regulated Feedback Voltage	(Note 3)	●	0.784	0.800	0.816	V
I$_{FB}$	Voltage Feedback Leakage Current				0.1	0.4	μA
ΔV$_{FB}$	Reference Voltage Line Regulation	V$_{IN}$ = 2.7V to 5.5V (Note 3)	●		0.04	0.2	%/V
V$_{LOADREG}$	Output Voltage Load Regulation	Measured in Servo Loop, V$_{ITH}$ = 0.36V	●		0.02	0.2	%
		Measured in Servo Loop, V$_{ITH}$ = 0.84V	●		−0.02	−0.2	%
ΔV$_{PGOOD}$	Power Good Range				±7.5	±9	%
R$_{PGOOD}$	Power Good Pull-Down Resistance				120	200	Ω

I$_Q$	Input DC Bias Current
	    Active Current
	    Sleep
	    Shutdown
		(Note 4)
		V$_{FB}$ = 0.78V, V$_{ITH}$ = 1V
		V$_{FB}$ = 1V, V$_{ITH}$ = 0V
		V$_{RUN}$ = 0V, V$_{MODE}$ = 0V
					250
					62
					0.02
						330
						80
						1
							μA
							μA
							μA

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_{IN} = 3.3V$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{OSC}	Switching Frequency Switching Frequency Range	$R_{OSC} = 309k\Omega$ (Note 6)		0.88 0.3	0.95	1.1 4	MHz MHz
f_{SYNC}	SYNC Capture Range	(Note 6)		0.3		4	MHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	$I_{SW} = 1A$ (Note 7)			85	110	mΩ
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	$I_{SW} = -1A$ (Note 7)			65	90	mΩ
I_{LIMIT}	Peak Current Limit			4	5.4		A
V_{UVLO}	Undervoltage Lockout Threshold			2.375	2.500	2.625	V
I_{LSW}	SW Leakage Current	$V_{RUN} = 0V$, $V_{IN} = 5.5V$			0.1	1	μA
V_{RUN}	RUN Threshold			0.5	0.65	0.8	V
I_{RUN}	RUN/SS Leakage Current					1	μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3412E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3412I is guaranteed to meet specified performance over the –40°C to 85°C temperature range.

Note 3: The LTC3412 is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (I_{TH}).

Note 4: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 5: T_J is calculated from the ambient temperature T_A and power dissipation as follows: LTC3412: $T_J = T_A + P_D$ (37.6°C/W).
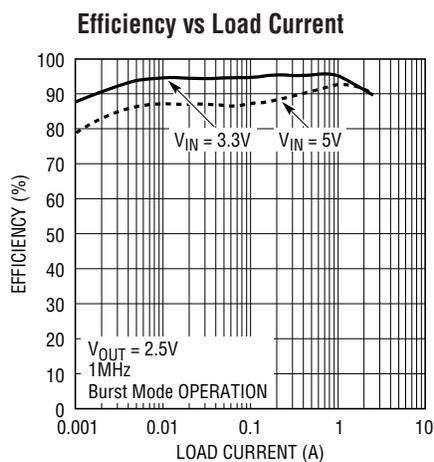
Note 6: 4MHz operation is guaranteed by design and not production tested.

Note 7: Switch on resistance is guaranteed by design and test correlation in the UF package and by production test in the FE package.
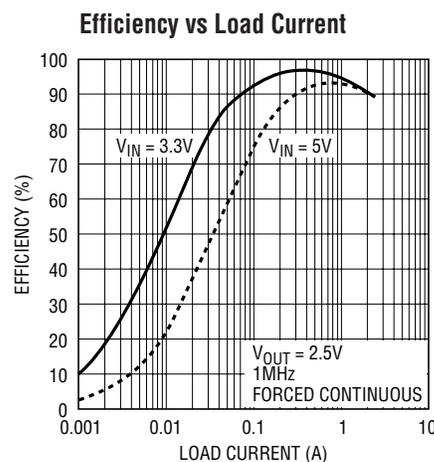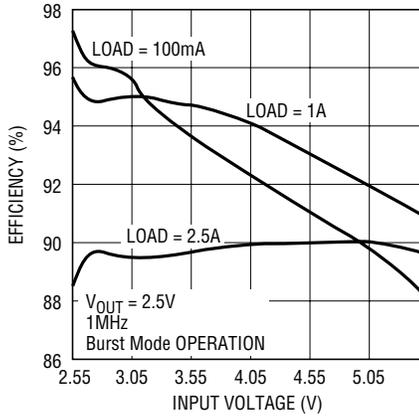
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Load Current
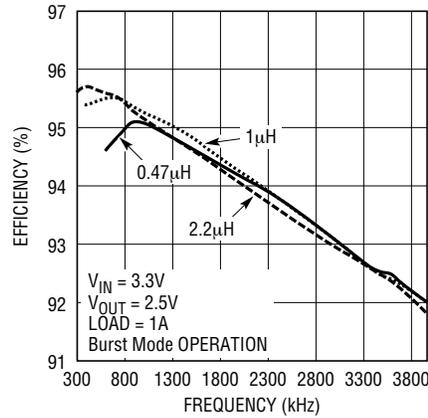

Efficiency vs Load Current

Efficiency vs Load Current
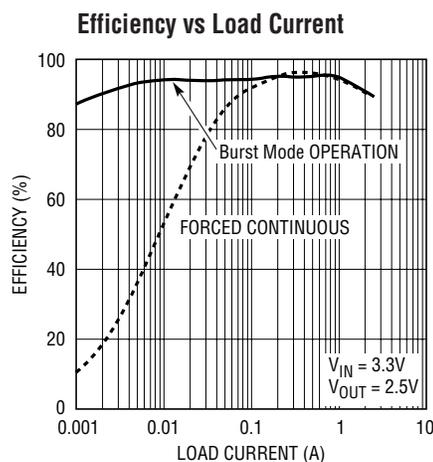
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Input Voltage

LOAD = 100mA
LOAD = 1A
LOAD = 2.5A
V_{OUT} = 2.5V
1MHz
Burst Mode OPERATION

EFFICIENCY (%)
INPUT VOLTAGE (V)
3412 G04

Efficiency vs Frequency

1µH
0.47µH
2.2µH
V_{IN} = 3.3V
V_{OUT} = 2.5V
LOAD = 1A
Burst Mode OPERATION

EFFICIENCY (%)
FREQUENCY (kHz)
3412 G05

Load Regulation

V_{IN} = 3.3V
V_{OUT} = 2.5V
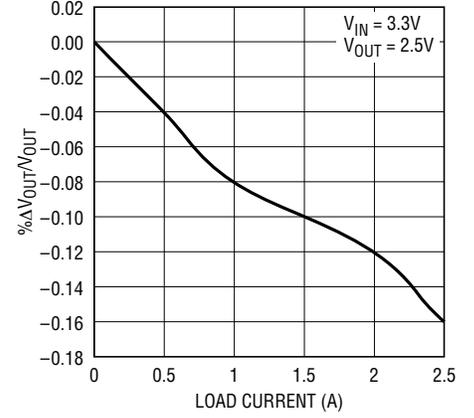
%$\Delta V_{OUT}/V_{OUT}$
LOAD CURRENT (A)
3412 G06

Burst Mode Operation
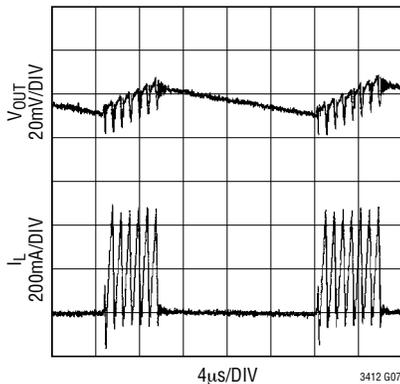
V_{OUT} 20mV/DIV
I_L 200mA/DIV
4µs/DIV
3412 G07
V_{IN} = 3.3V, V_{OUT} = 2.5V
LOAD = 50mA

Load Step Transient Forced Continuous
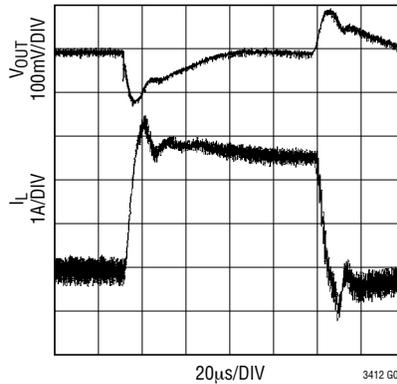
V_{OUT} 100mV/DIV
I_L 1A/DIV
20µs/DIV
3412 G08
V_{IN} = 3.3V, V_{OUT} = 2.5V
LOAD STEP = NO LOAD TO 2.5A

Load Step Transient Burst Mode Operation
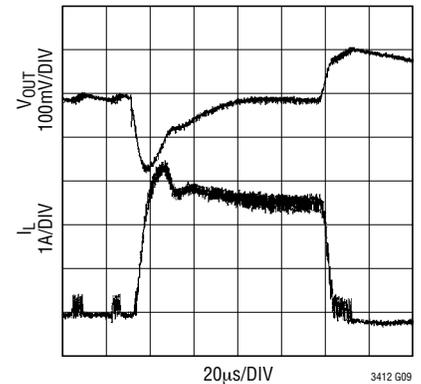
V_{OUT} 100mV/DIV
I_L 1A/DIV
20µs/DIV
3412 G09
V_{IN} = 3.3V, V_{OUT} = 2.5V
LOAD STEP = 50mA TO 2.5A

Start-Up, Burst Mode Operation
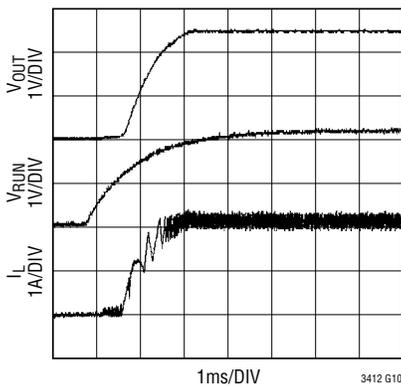
V_{OUT} 1V/DIV
V_{RUN} 1V/DIV
I_L 1A/DIV
1ms/DIV
3412 G10
V_{IN} = 3.3V, V_{OUT} = 2.5V
LOAD = 1Ω

Reference Voltage vs Temperature

V_{IN} = 3.3V
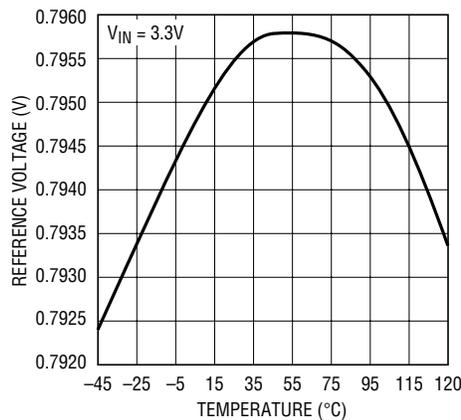
REFERENCE VOLTAGE (V)
TEMPERATURE (°C)
3412 G11

Switch On-Resistance vs Input Voltage

PFET ON-RESISTANCE
NFET ON-RESISTANCE

ON-RESISTANCE (mΩ)
INPUT VOLTAGE (V)
3412 G12

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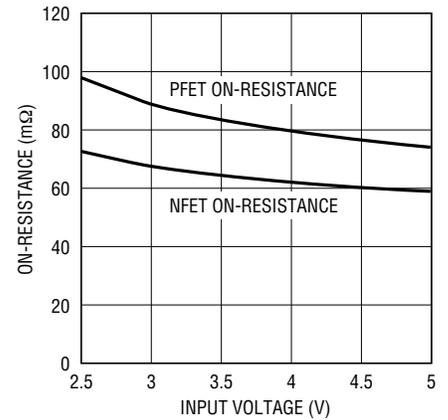
TYPICAL PERFORMANCE CHARACTERISTICS

Switch On-Resistance vs Temperature
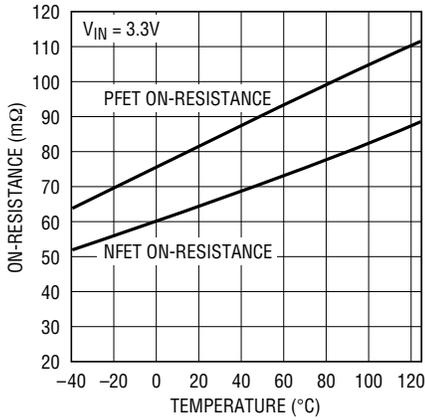
3412 G13

Switch Leakage vs Input Voltage
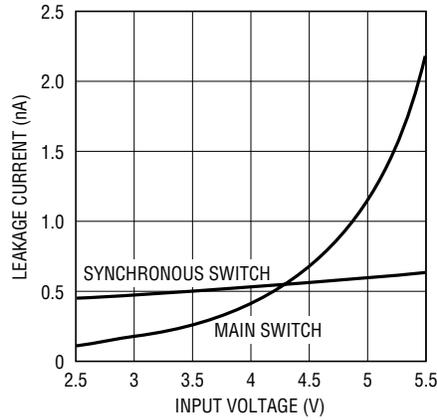
3412 G14

Frequency vs R_{OSC}
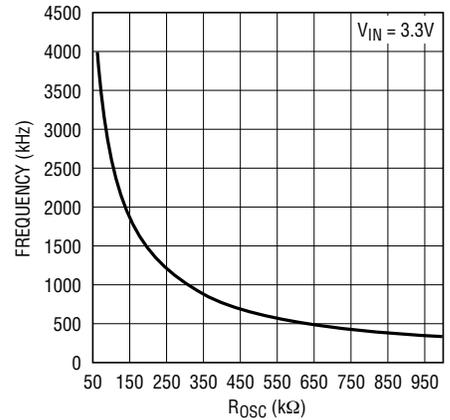
3412 G15

Frequency vs Input Voltage
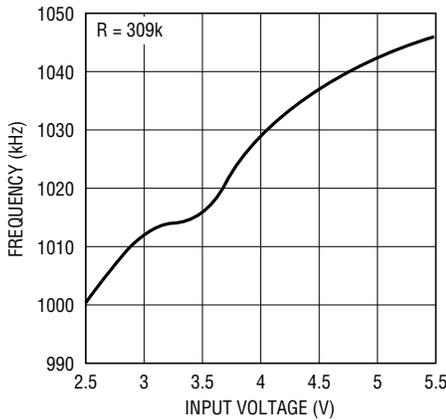
3412 G16

Switching Frequency vs Temperature

3412 G17

DC Supply Current vs Input Voltage

3412 G18

DC Supply Current vs Temperature

3412 G19

Minimum Peak Inductor Current vs Burst Clamp Voltage

3412 G20

Current Limit vs Input Voltage

3412 G21

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LTC3412

PIN FUNCTIONS (FE/UH Package)

SV$_{IN}$ (Pin 1/Pin 11): Signal Input Supply. Decouple this pin to SGND with a capacitor. Normally SV$_{IN}$ is equal to PV$_{IN}$. SV$_{IN}$ can be greater than PV$_{IN}$ but keep the voltage difference between SV$_{IN}$ and PV$_{IN}$ less than 0.5V.
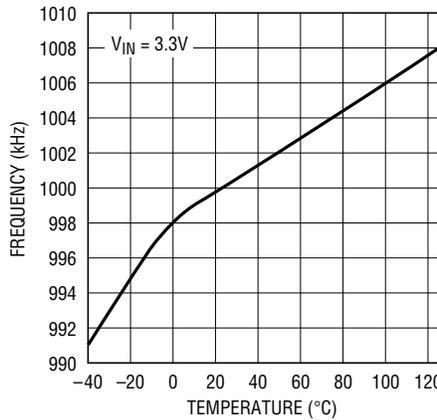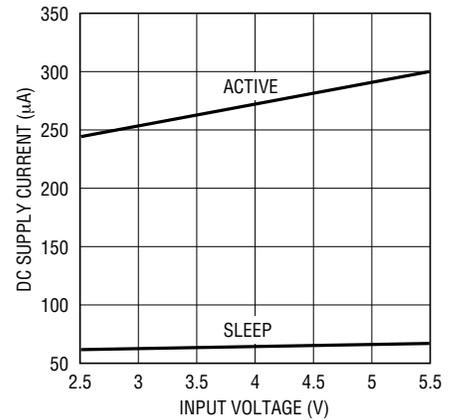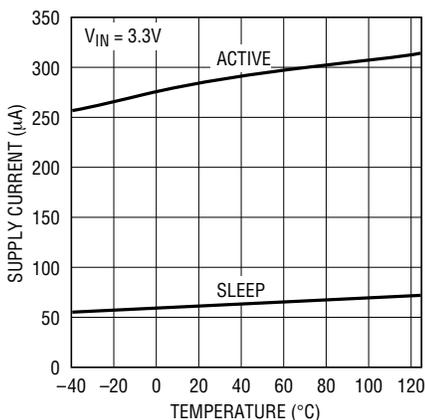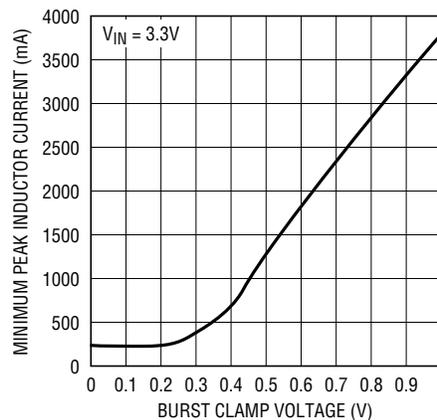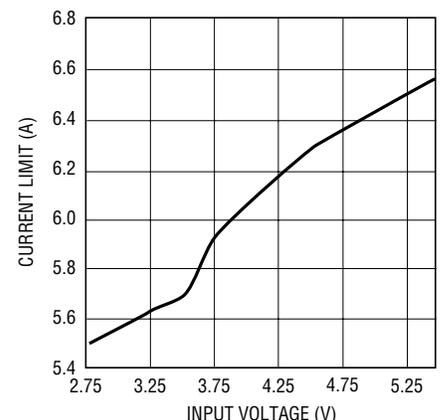
PGOOD (Pin 2/Pin 12): Power Good Output. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of regulation point.

I$_{TH}$ (Pin 3/Pin 13): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is from 0.2V to 1.4V with 0.2V corresponding to the zero-sense voltage (zero current).

V$_{FB}$ (Pin 4/Pin 14): Feedback Pin. Receives the feedback voltage from a resistive divider connected across the output.

R$_T$ (Pin 5/Pin 15): Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the switching frequency.

SYNC/MODE (Pin 6/Pin 16): Mode Select and External Clock Synchronization Input. To select forced continuous, tie to SV$_{IN}$. Connecting this pin to a voltage between 0V and 1V selects Burst Mode operation with the burst clamp set to the pin voltage.

RUN/SS (Pin 7/Pin 1): Run Control and Soft-Start Input. Forcing this pin below 0.5V shuts down the LTC3412. In shutdown all functions are disabled drawing < 1μA of supply current. A capacitor to ground from this pin sets the ramp time to full output current.

SGND (Pin 8/Pin 2): Signal Ground. All small-signal components, compensation components and the exposed pad on the bottom side of the IC should connect to this ground, which in turn connects to PGND at one point.

PV$_{IN}$ (Pins 9, 16/Pins 3, 10): Power Input Supply. Decouple this pin to PGND with a capacitor.

SW (Pins 10, 11, 14, 15/Pins 4, 5, 8, 9): Switch Node Connection to the Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

PGND (Pins 12, 13/Pins 6, 7): Power Ground. Connect this pin close to the (–) terminal of C$_{IN}$ and C$_{OUT}$.

Exposed Pad (Pin 17/Pin 17): Signal Ground. Must be soldered to PCB for electrical connection and thermal performance.

FUNCTIONAL BLOCK DIAGRAM
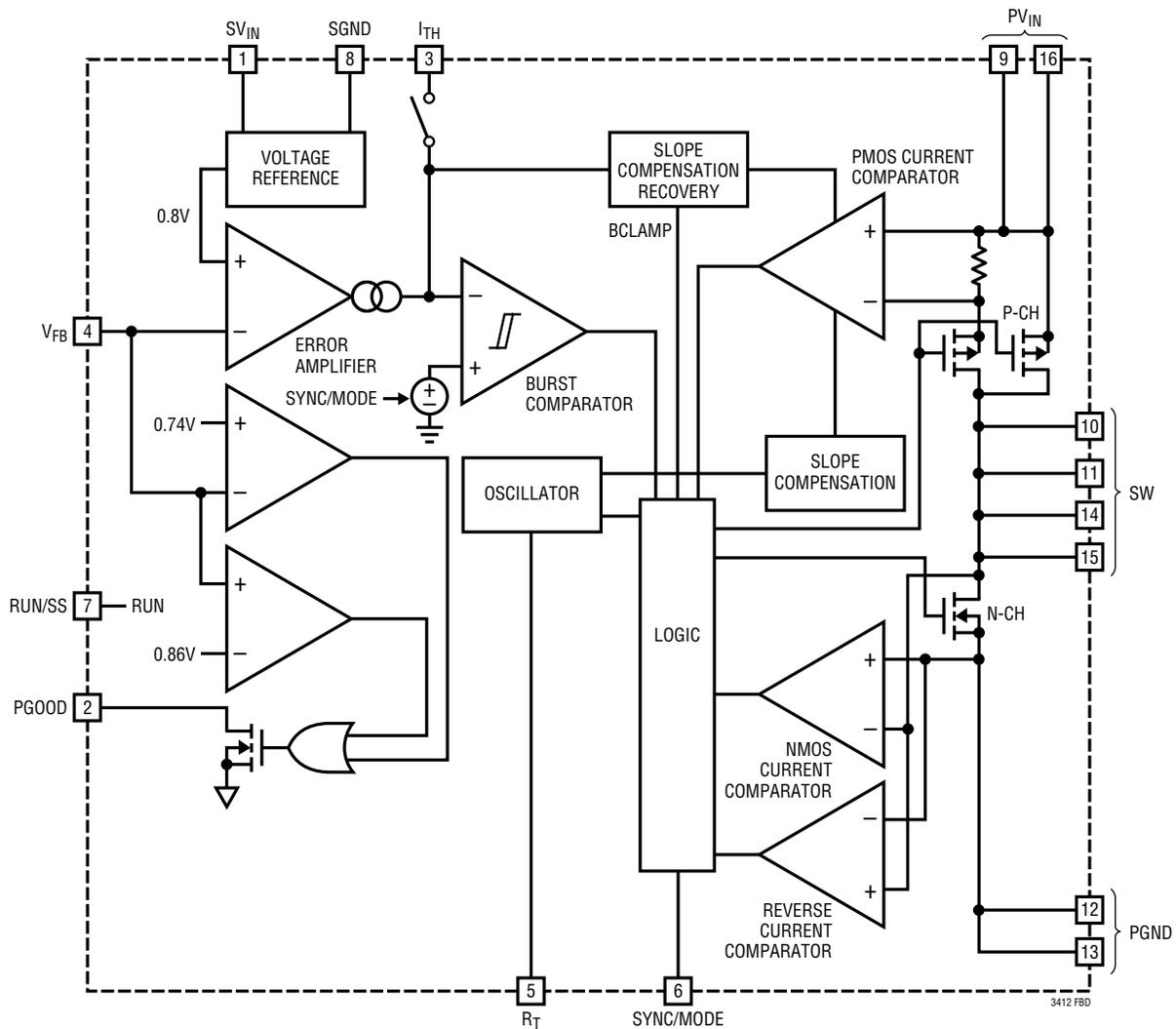
OPERATION

Main Control Loop

The LTC3412 is a monolithic, constant-frequency, current mode step-down DC/DC converter. During normal operation, the internal top power switch (P-channel MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the current comparator trips and turns off the top power MOSFET. The peak inductor current at which the current comparator shuts off the top power switch is controlled by the voltage on the I_{TH} pin. The error amplifier adjusts the voltage on the I_{TH} pin by comparing the feedback signal from a resistor divider on the V_{FB} pin with an internal 0.8V reference. When the load

current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises the I_{TH} voltage until the average inductor current matches the new load current. When the top power MOSFET shuts off, the synchronous power switch (N-channel MOSFET) turns on until either the bottom current limit is reached or the beginning of the next clock cycle. The bottom current limit is set at –2A for forced continuous mode and 0A for Burst Mode operation.

The operating frequency is set by an external resistor connected between the R_T pin and ground. The practical switching frequency can range from 300kHz to 4MHz.

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OPERATION

Overvoltage and undervoltage comparators will pull the PGOOD output low if the output voltage comes out of regulation by ±7.5%. In an overvoltage condition, the top power MOSFET is turned off and the bottom power MOSFET is switched on until either the overvoltage condition clears or the bottom MOSFET's current limit is reached.

Forced Continuous Mode

Connecting the SYNC/MODE pin to SV_{IN} will disable Burst Mode operation and force continuous current operation. At light loads, forced continuous mode operation is less efficient than Burst Mode operation but may be desirable in some applications where it is necessary to keep switching harmonics out of a signal band. The output voltage ripple is minimized in this mode.

Burst Mode Operation

Connecting the SYNC/MODE pin to a voltage between 0V to 1V enables Burst Mode operation. In Burst Mode operation, the internal power MOSFETs operate intermittently at light loads. This increases efficiency by minimizing switching losses. During Burst Mode operation, the minimum peak inductor current is externally set by the voltage on the SYNC/MODE pin and the voltage on the I_{TH} pin is monitored by the burst comparator to determine when sleep mode is enabled and disabled. When the average inductor current is greater than the load current, the voltage on the I_{TH} pin drops. As the I_{TH} voltage falls below 150mV, the burst comparator trips and enables sleep mode. During sleep mode, the top MOSFET is held off and the I_{TH} pin is disconnected from the output of the error amplifier. The majority of the internal circuitry is also turned off to reduce the quiescent current to 62µA while the load current is solely supplied by the output capacitor. When the output voltage drops, the I_{TH} pin is reconnected to the output of the error amplifier and the top power MOSFET along with all the internal circuitry is switched back on. This process repeats at a rate that is dependent on the load demand.

Pulse skipping operation can be implemented by connecting the SYNC/MODE pin to ground. This forces the burst clamp level to be at 0V. As the load current decreases, the peak inductor current will be determined by the voltage on the I_{TH} pin until the I_{TH} voltage drops below 200mV. At this point, the peak inductor current is determined by the minimum on-time of the current comparator. If the load demand is less than the average of the minimum on-time inductor current, switching cycles will be skipped to keep the output voltage in regulation.

Frequency Synchronization

The internal oscillator of the LTC3412 can be synchronized to an external clock connected to the SYNC/MODE pin. The frequency of the external clock can be in the range of 300kHz to 4MHz. For this application, the oscillator timing resistor should be chosen to correspond to a frequency that is 25% lower than the synchronization frequency. During synchronization, the burst clamp is set to 0V and each switching cycle begins at the falling edge of the external clock signal.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-channel MOSFET and the inductor.

Low Supply Operation

The LTC3412 is designed to operate down to an input supply voltage of 2.625V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-channel and N-channel power switches increases. The user should calculate the power dissipation when the LTC3412 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at duty cycles greater than 50%. It is accomplished

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OPERATION

internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, the maximum inductor peak current is reduced when slope compensation is added. In the LTC3412, however, slope compensation recovery is implemented to keep the maximum inductor peak current constant throughout the range of duty cycles. This keeps the maximum output current relatively constant regardless of duty cycle.

Short-Circuit Protection

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. To prevent current runaway from occurring, a secondary current limit is imposed on the inductor current. If the inductor valley current increases larger than 4.8A, the top power MOSFET will be held off and switching cycles will be skipped until the inductor current falls to a safe level.

APPLICATIONS INFORMATION

The basic LTC3412 application circuit is shown in Figure 1. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Operating Frequency

Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and switching losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency of the LTC3412 is determined by an external resistor that is connected between the R_T pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_{OSC} = \frac{3.23 \cdot 10^{11}}{f(Hz)}(\Omega) - 10k\Omega$$

Although frequencies as high as 4MHz are possible, the minimum on-time of the LTC3412 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 110ns. Therefore, the minimum duty cycle is equal to 100 • 110ns • f(Hz).

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{fL}\right]\left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f\Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor value will also have an effect on Burst Mode operation. The transition from low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

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APPLICATIONS INFORMATION

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, mollypermalloy, or Kool Mµ® cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coiltronics, Coilcraft, Toko and Sumida.

C$_{IN}$ and C$_{OUT}$ Selection

The input capacitance, C$_{IN}$, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V$_{IN}$ = 2V$_{OUT}$, where I$_{RMS}$ = I$_{OUT}$/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C$_{OUT}$ is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV$_{OUT}$, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since ΔI$_L$ increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and

APPLICATIONS INFORMATION

the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.8V\left(1 + \frac{R2}{R1}\right)$$

The resistive divider allows the V_{FB} pin to sense a fraction of the output voltage as shown in Figure 2.
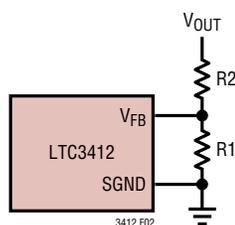

Figure 2. Setting the Output Voltage

Burst Clamp Programming

If the voltage on the SYNC/MODE pin is less than V_{IN} by 1V, Burst Mode operation is enabled. During Burst Mode operation, the voltage on the SYNC/MODE pin determines the burst clamp level which sets the minimum peak inductor current, I_{BURST}, for each switching cycle according to the following equation:

$$I_{BURST} = \left(V_{BURST} - 0.2V\right)\left(\frac{3.75A}{0.8V}\right)$$

V_{BURST} is the voltage on the SYNC/MODE pin. I_{BURST} can be programmed in the range of 0A to 3.75A. For values of V_{BURST} greater than 1V, I_{BURST} is set at 3.75A. For values of V_{BURST} less than 0.2V, I_{BURST} is set at 0A. As the output load current drops, the peak inductor current decreases to keep the output voltage in regulation. When the output load current demands a peak inductor current that is less than I_{BURST}, the burst clamp will force the peak inductor

current to remain equal to I_{BURST} regardless of further reductions in the load current. Since the average inductor current is greater than the output load current, the voltage on the I_{TH} pin will decrease. When the I_{TH} voltage drops to 150mV, sleep mode is enabled in which both power MOSFETs are shut off along with most of the circuitry to minimize power consumption. All circuitry is turned back on and the power MOSFETs begin switching again when the output voltage drops out of regulation. The value for I_{BURST} is determined by the desired amount of output voltage ripple. As the value of I_{BURST} increases, the sleep period between pulses and the output voltage ripple increase. The burst clamp voltage, V_{BURST}, can be set by a resistor divider from the V_{FB} pin to the SGND pin as shown in Figure 1.

Pulse skipping, which is a compromise between low output voltage ripple and efficiency, can be implemented by connecting the SYNC/MODE pin to ground. This sets I_{BURST} to 0A. In this condition, the peak inductor current is limited by the minimum on-time of the current comparator, and the lowest output voltage ripple is achieved while still operating discontinuously. During very light output loads, pulse skipping allows only a few switching cycles to be skipped while maintaining the output voltage in regulation.

Frequency Synchronization

The LTC3412's internal oscillator can be synchronized to an external clock signal. During synchronization, the top MOSFET turn-on is locked to the falling edge of the external frequency source. The synchronization frequency range is 300kHz to 4MHz. Synchronization only occurs if the external frequency is greater than the frequency set by the external resistor. Because slope compensation is generated by the oscillator's RC circuit, the external frequency should be set 25% higher than the frequency set by the external resistor to ensure that adequate slope compensation is present.

Soft-Start

The RUN/SS pin provides a means to shut down the LTC3412 as well as a timer for soft-start. Pulling the RUN/SS pin below 0.5V places the LTC3412 in a low quiescent current shutdown state ($I_Q < 1\mu A$).

APPLICATIONS INFORMATION

The LTC3412 contains an internal soft-start clamp that gradually raises the clamp on I_{TH} after the RUN/SS pin is pulled above 2V. The full current range becomes available on I_{TH} after 1024 switching cycles. If a longer soft-start period is desired, the clamp on I_{TH} can be set externally with a resistor and capacitor on the RUN/SS pin as shown in Figure 1. The soft-start duration can be calculated by using the following formula:

$$t_{SS} = R_{SS}C_{SS} \ln\left(\frac{V_{IN}}{V_{IN} - 1.8V}\right) \text{(Seconds)}$$

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% − (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I^2R losses.

The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG}=f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. In continuous mode the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Thermal Considerations

In most applications, the LTC3412 does not dissipate much heat due to its high efficiency. But, in applications where the LTC3412 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3412 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

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APPLICATIONS INFORMATION

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider the LTC3412 in dropout at an input voltage of 3.3V, a load current of 2.5A and an ambient temperature of 70°C. From the typical performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 70°C is approximately 97mΩ. Therefore, power dissipated by the part is:

$$P_D = (I_{LOAD}^2)(R_{DS(ON)}) = (2.5A)^2(97m\Omega) = 0.61W$$

For the TSSOP package, the θ_{JA} is 37.6°C/W. Thus the junction temperature of the regulator is:

$$T_J = 70°C + (0.61W)(37.6°C/W) = 93°C$$

which is below the maximum junction temperature of 125°C.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD}(ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The I_{TH} pin external components and output capacitor shown in Figure 1 will provide adequate compensation for most applications.

Design Example

As a design example, consider using the LTC3412 in an application with the following specifications: V_{IN} = 2.7V to 4.2V, V_{OUT} = 2.5V, $I_{OUT(MAX)}$ = 2.5A, $I_{OUT(MIN)}$ = 10mA, f = 1MHz. Because efficiency is important at both high and low load current, Burst Mode operation will be utilized.

First, calculate the timing resistor:

$$R_{OSC} = \frac{3.23 \cdot 10^{11}}{1 \cdot 10^6} - 10k = 313k$$

Use a standard value of 309k. Next, calculate the inductor value for about 40% ripple current at maximum V_{IN}:

$$L = \left(\frac{2.5V}{(1MHz)(1A)}\right)\left(1 - \frac{2.5V}{4.2V}\right) = 1.01\mu H$$

Using a 1μH inductor, results in a maximum ripple current of:

$$\Delta I_L = \left(\frac{2.5V}{(1MHz)(1\mu H)}\right)\left(1 - \frac{2.5V}{4.2V}\right) = 1.01A$$

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. In this application, two tantalum capacitors will be used to provide the bulk capacitance and a ceramic capacitor in parallel to lower the total effective ESR. For this design, two 100μF tantalum capacitors in parallel with a 10μF ceramic capacitor will be used. C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = (2.5A)\left(\frac{2.5V}{4.2V}\right)\sqrt{\frac{4.2V}{2.5V} - 1} = 1.23A_{RMS}$$

Decoupling the PV_{IN} and SV_{IN} pins with a 22μF ceramic capacitor and a 220μF tantalum capacitor is adequate for most applications.

The burst clamp and output voltage can now be programmed by choosing the values of R1, R2 and R3. The voltage on the MODE pin will be set to 0.32V by the resistor divider consisting of R2 and R3. A burst clamp voltage of 0.32V will set the minimum inductor current, I_{BURST}, as follows:

$$I_{BURST} = (0.32V - 0.2V)\left(\frac{3.75V}{0.8V}\right) = 563mA$$

APPLICATIONS INFORMATION

If we set the sum of R2 and R3 to 185k, then the following equations can be solved:

$$R2 + R3 = 185k$$

$$1 + \frac{R2}{R3} = \frac{0.8V}{0.32V}$$

The last two equations shown result in the following values for R2 and R3: R2 = 110k , R3 = 75k. The value of R1 can now be determined by solving the equation shown below:

$$1 + \frac{R1}{185k} = \frac{2.5V}{0.8V}$$

$$R1 = 393k$$

A value of 392k will be selected for R1. Figure 4 shows the complete schematic for this design example.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3412. Check the following in your layout.

1. A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small-signal components returning to the SGND pin at one point which is then connected to the PGND pin close to the LTC3412. The exposed pad should be connected to SGND.

2. Connect the (+) terminal of the input capacitor(s), C_{IN}, as close as possible to the PV_{IN} pin. This capacitor provides the AC current into the internal power MOSFETs.

3. Keep the switching node, SW, away from all sensitive small-signal nodes.

4. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. You can connect the copper areas to any DC net (PV_{IN}, SV_{IN}, V_{OUT}, PGND, SGND, or any other DC rail in your system).

5. Connect the V_{FB} pin directly to the feedback resistors. The resistor divider must be connected between V_{OUT} and SGND.
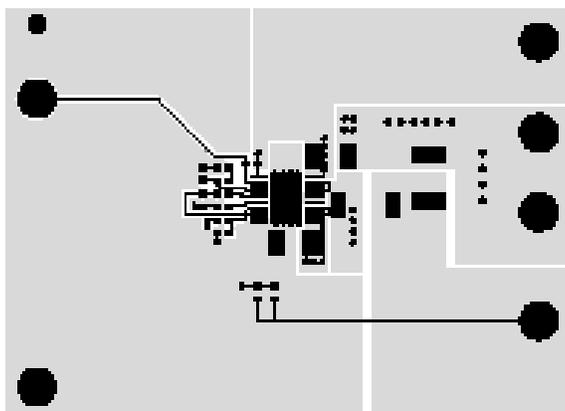
Top Side
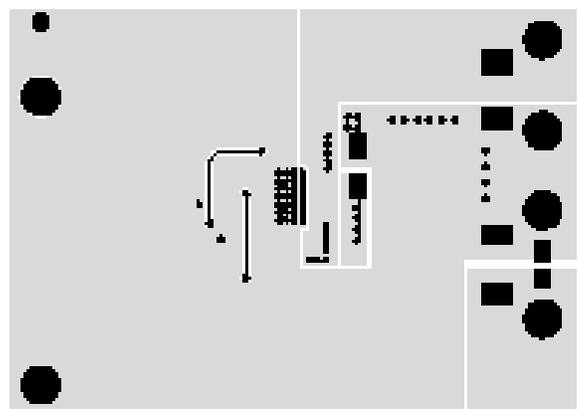
Bottom Side

Figure 3. LTC3412 Layout Diagram
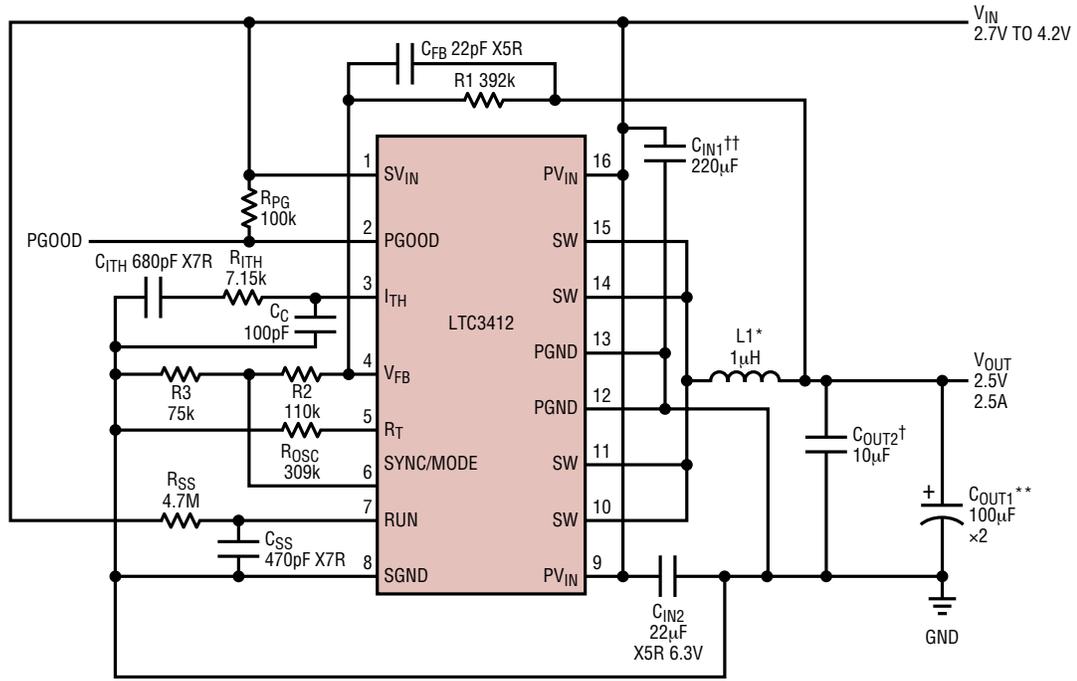
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LINEAR TECHNOLOGY

APPLICATIONS INFORMATION

Figure 4. Single Lithium-Ion to 2.5V, 2.5A Regulator at 1MHz, Burst Mode Operation Using POSCAPs

TYPICAL APPLICATIONS

2.5V, 2.5A Regulator Using All Ceramic Capacitors
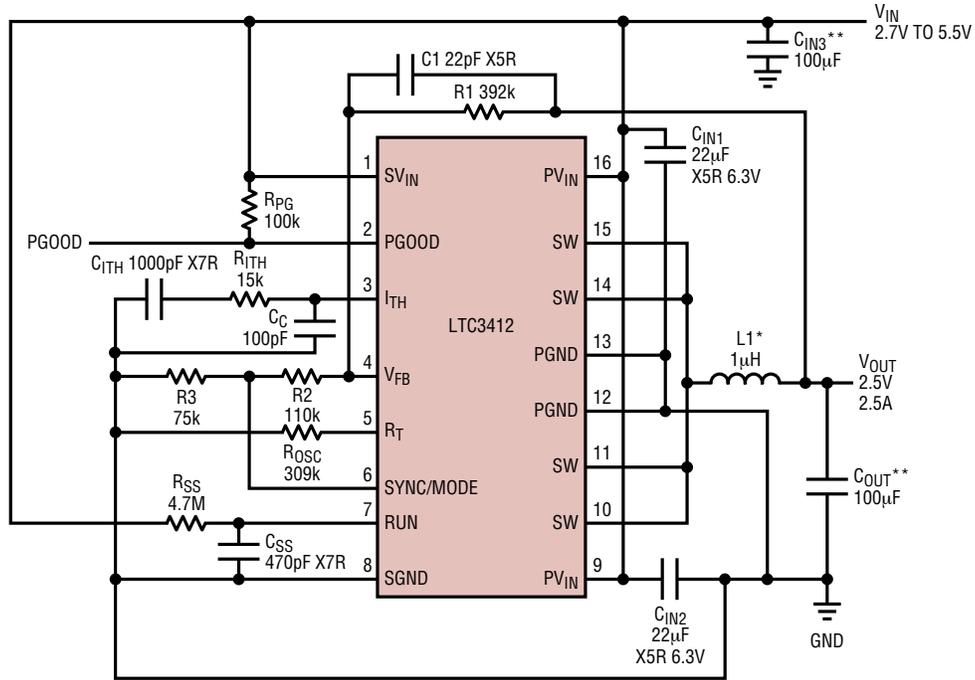
*TOKO D62CB A920CY-1ROM
**TDK C4532X5R0J107M

3412 F05

1.8V, 2.5A Step-Down Regulator at 1MHz, Burst Mode Operation

*SUMIDA CR431R0
**AVX 12066D226MAT

3412 TA05

3412fb

TYPICAL APPLICATIONS

2.5V, 2.5A Low Output Noise Regulator at 2MHz

Circuit components:

- C_{IN3} 0.1µF X5R
- R_{IN} 5Ω
- C_{FF} 22pF X7R
- R1 392k
- V_{IN} 3.3V
- C_{IN1}** 100µF
- R_{PG} 100k
- PGOOD
- C_{ITH} 1000pF X7R
- R_{ITH} 22.1k
- C1 56pF
- R2 182k
- R_{OSC} 137k
- R_{SS} 4.7M
- C_{SS} 470pF X7R
- L1 0.47µH*
- V_{OUT} 2.5V 2.5A
- C_{OUT}** 100µF ×2
- C_{IN2} 100µF**

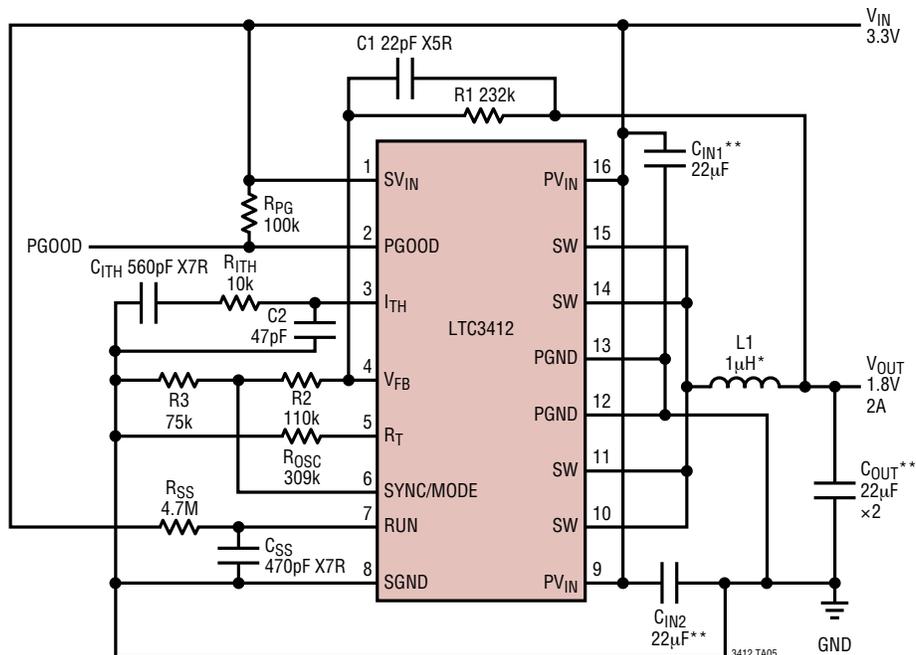LTC3412 pin connections:

Pin	Name	Pin	Name
1	SV_{IN}	16	PV_{IN}
2	PGOOD	15	SW
3	I_{TH}	14	SW
4	V_{FB}	13	PGND
5	R_T	12	PGND
6	SYNC/MODE	11	SW
7	RUN	10	SW
8	SGND	9	PV_{IN}

GND

3412 TA06

*VISHAY DALE IHLP-2525CZ-01 0.47
**TDK C4532X5R0J107M

Efficiency vs Load Current
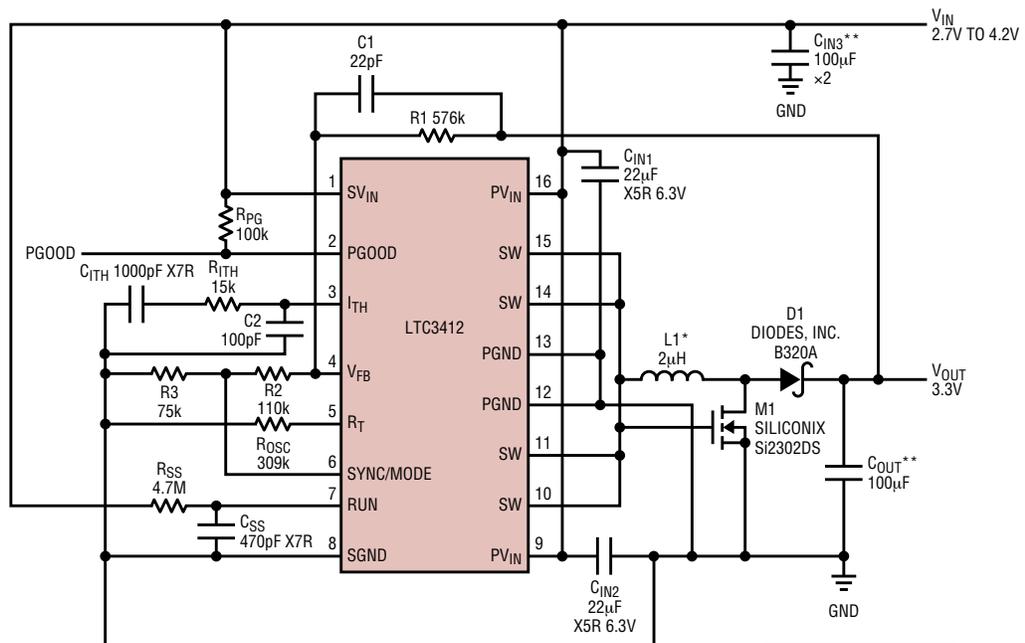**2MHz, Low Noise**

3412 TA07

TYPICAL APPLICATIONS

3.3V, 2.5A Step-Down Regulator at 1MHz, Forced Continuous Mode Operation
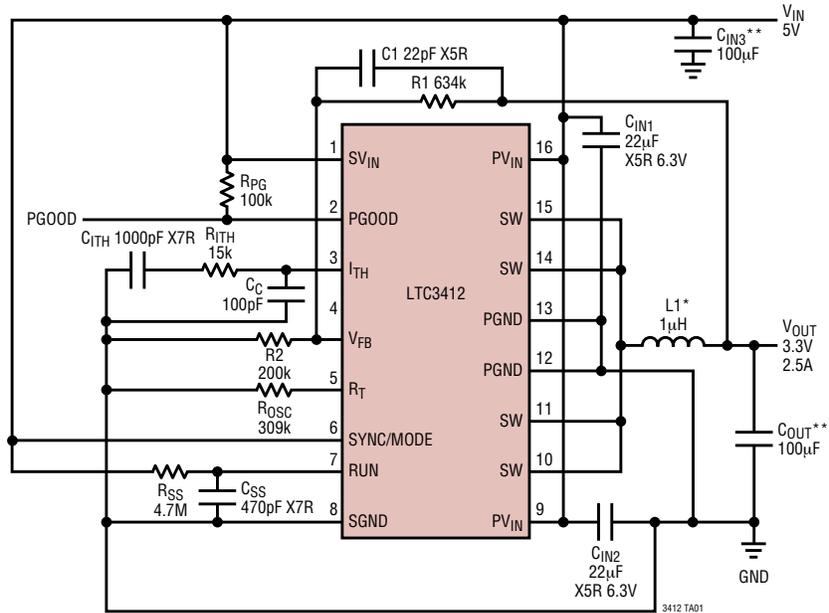
*PULSE P1166.162T
**TDK C4532X5R0J107M

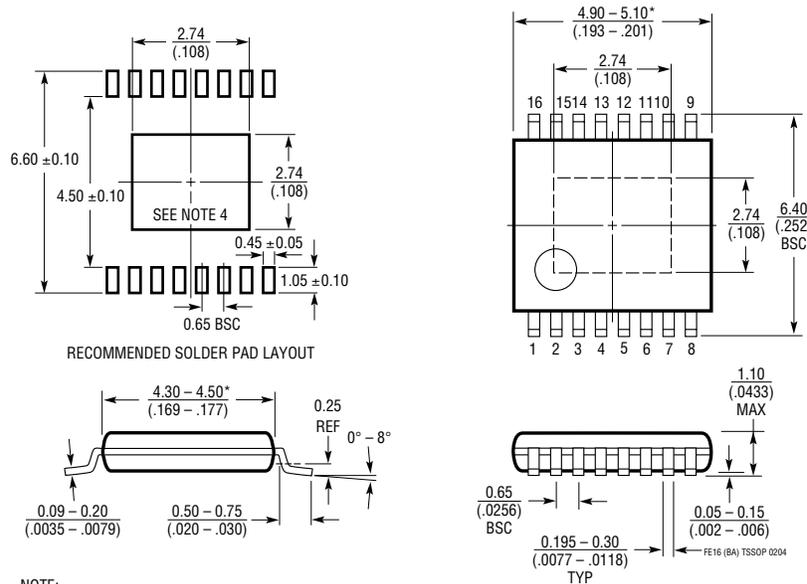**Lithium-Ion to 3.3V, Single Inductor Buck-Boost Converter**

*TOKO D63CB
**TDK C4532X5R0J107M

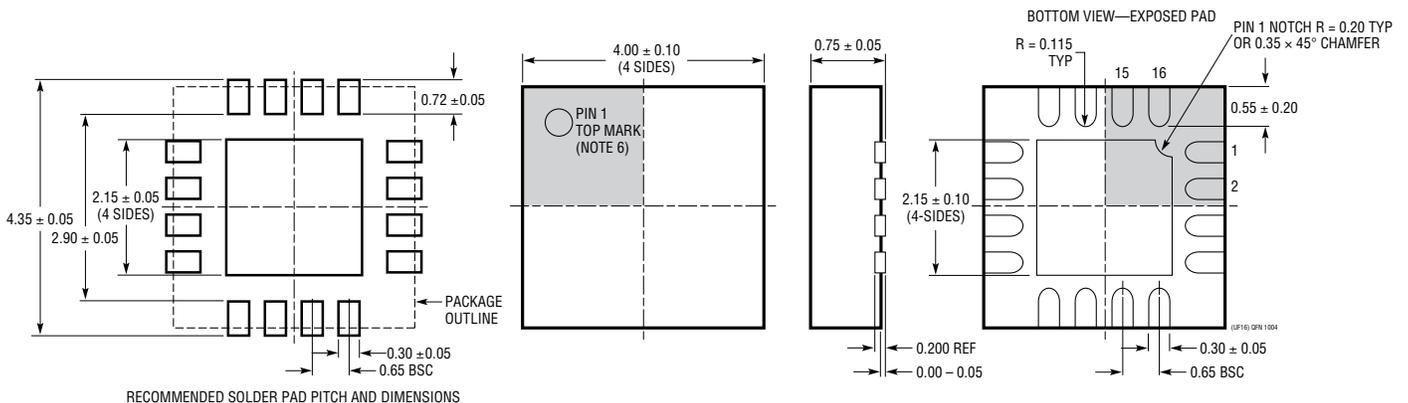| V_IN	MAXIMUM I_OUT
2.7V	800mA
3V	900mA
3.5V	1.05A
4.2V	1.2A

3412fb

PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BA

2.74
(.108)

6.60 ±0.10
4.50 ±0.10
SEE NOTE 4
2.74
(.108)

0.45 ±0.05
1.05 ±0.10
0.65 BSC

RECOMMENDED SOLDER PAD LAYOUT

4.90 – 5.10*
(.193 – .201)

2.74
(.108)

16 15 14 13 12 11 10 9

2.74
(.108)

6.40
(.252)
BSC

1 2 3 4 5 6 7 8

4.30 – 4.50*
(.169 – .177)

0.25
REF
0° – 8°

0.09 – 0.20
(.0035 – .0079)

0.50 – 0.75
(.020 – .030)

1.10
(.0433)
MAX

0.65
(.0256)
BSC

0.05 – 0.15
(.002 – .006)

0.195 – 0.30
(.0077 – .0118)
TYP

FE16 (BA) TSSOP 0204

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

4. RECOMMENDED MINIMUM PCB METAL SIZE
FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.150mm (.006") PER SIDE

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)

0.72 ±0.05

4.35 ± 0.05

2.15 ± 0.05
(4 SIDES)
2.90 ± 0.05

PACKAGE
OUTLINE

0.30 ±0.05
0.65 BSC

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

4.00 ± 0.10
(4 SIDES)

PIN 1
TOP MARK
(NOTE 6)

0.75 ± 0.05

2.15 ± 0.10
(4-SIDES)

0.200 REF
0.00 – 0.05

BOTTOM VIEW—EXPOSED PAD

R = 0.115
TYP

PIN 1 NOTCH R = 0.20 TYP
OR 0.35 × 45° CHAMFER

15 16

0.55 ± 0.20

1

2

0.30 ± 0.05
0.65 BSC

(UF16) QFN 1004

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
ON THE TOP AND BOTTOM OF PACKAGE

3412fb

LTC3412

TYPICAL APPLICATION

2.5V, 2.5A Step-Down Regulator Synchronized to 1.25MHz

*TOKO D62CB A920CY-1ROM
**TDK C4532X5R0J107M

3412 TA02
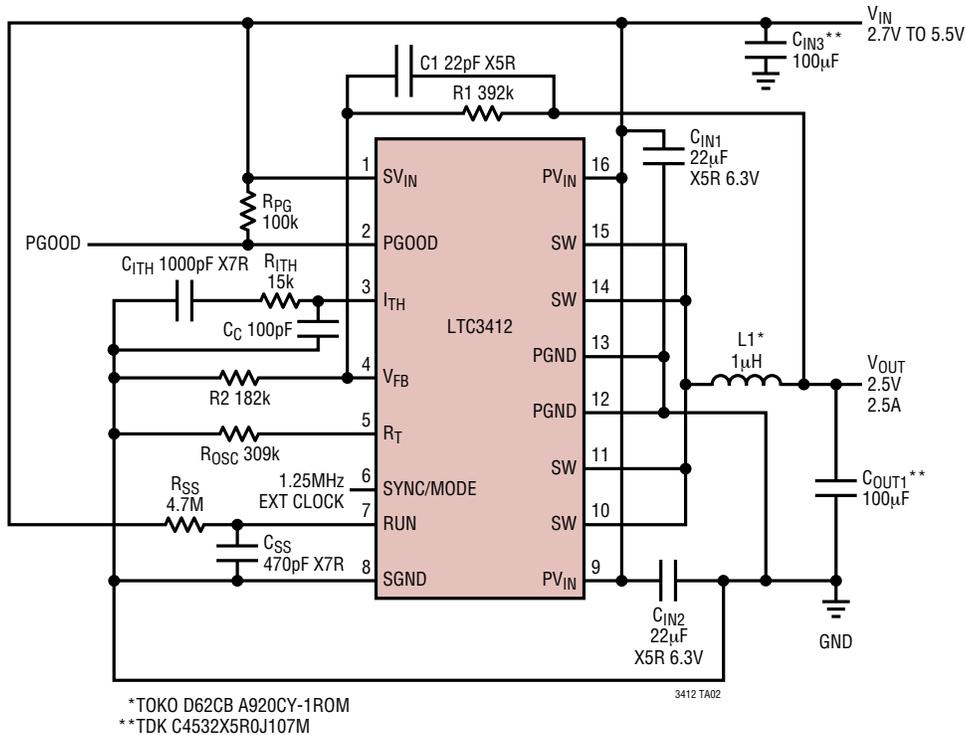
RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1701/LTC1701B	700mA (I_{OUT}), 1MHz Step-Down Converter	V_{IN} = 2.5V to 5V, B Version: Burst Mode Defeat, ThinSOT™
LTC1772/LTC1772B	Constant 550kHz Current Mode Step-Down DC/DC Controller	V_{IN} = 2.5V to 9.8V, 94% Efficiency, 100% Duty Cycle, ThinSOT
LTC1773	Constant Frequency 550kHz Step-Down DC/DC Controller	V_{IN} = 2.65V to 8.5V, 95% Efficiency, V_{OUT} from 0.8V to V_{IN}, MSOP-10
LTC1875	1.5A (I_{OUT}), 500kHz Synchronous Step-Down Converter	V_{IN} = 2.65V to 6V, 95% Efficiency, PLL, SSOP-16
LTC1877	600mA (I_{OUT}), 500kHz Synchronous Step-Down Converter	V_{IN} = 2.65V to 10V, 95% Efficiency, MSOP-8
LTC1878	600mA (I_{OUT}), 550kHz Synchronous Step-Down Converter	V_{IN} = 2.65V to 6V, 95% Efficiency, MSOP-8
LTC1879	1.2A (I_{OUT}), 550kHz Synchronous Step-Down Converter	V_{IN} = 2.65V to 10V, 95% Efficiency, SSOP-16
LTC3404	600mA (I_{OUT}), 1.4MHz Synchronous Step-Down Converter	V_{IN} = 2.65V to 6V, 95% Efficiency, MSOP-8
LTC3405A	300mA (I_{OUT}), 1.5MHz Synchronous Step-Down Converter	V_{IN} = 2.65V to 6V, 96% Efficiency, ThinSOT Package
LTC3406/LTC3406B	600mA (I_{OUT}), 1.5MHz Synchronous Step-Down Converter	V_{IN} = 2.5V to 5.5V, 95% Efficiency, ThinSOT, B Version: Burst Mode Defeat
LTC3411	1.25A (I_{OUT}), 4MHz Synchronous Step-Down Converter	V_{IN} = 2.5V to 5.5V, 95% Efficiency, MSOP-10

ThinSOT is a trademark of Linear Technology Corporation.

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