

# 3A, 3MHz Micropower Synchronous Boost Converter with Output Disconnect

## FEATURES

- **Synchronous Rectification: Up to 96% Efficiency**
- **True Output Disconnect**
- **Inrush Current Limiting**
- **Very Low Quiescent Current: 12 $\mu$ A**
- **Up to 1.5A Continuous Output Current**
- Fixed Frequency Operation Up to 3MHz
- 0.5V to 4.5V Input Range
- 2.4V to 5.25V Adjustable Output Voltage
- Guaranteed 1V Start-Up
- Programmable Current Limit
- Programmable Soft-Start
- Synchronizable Oscillator
- Manual or Automatic Burst Mode<sup>®</sup> Operation
- Low-Battery Comparator
- <1 $\mu$ A Shutdown Current
- 1.22V Reference Output Voltage
- Small (4mm  $\times$  4mm) Thermally Enhanced QFN Package

## APPLICATIONS

- Handheld Computers
- Cordless Phones
- GPS Receivers
- Battery Backup Supplies

## DESCRIPTION

The LTC<sup>®</sup>3421 is a high efficiency, current mode, fixed frequency, step-up DC/DC converter with true output disconnect and inrush current limiting. The device includes a 0.10 $\Omega$  N-channel MOSFET switch and a 0.14 $\Omega$  P-channel synchronous rectifier. This product has the ability to simply program the output voltage, switching frequency, current limit, soft-start, Burst Mode threshold and loop compensation with external passive components.

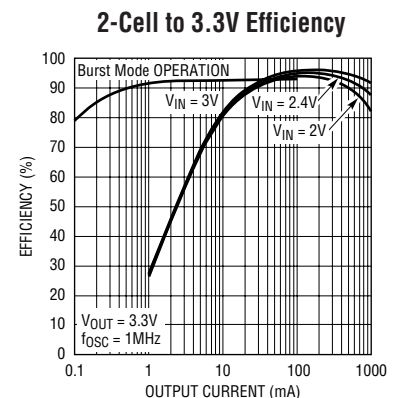
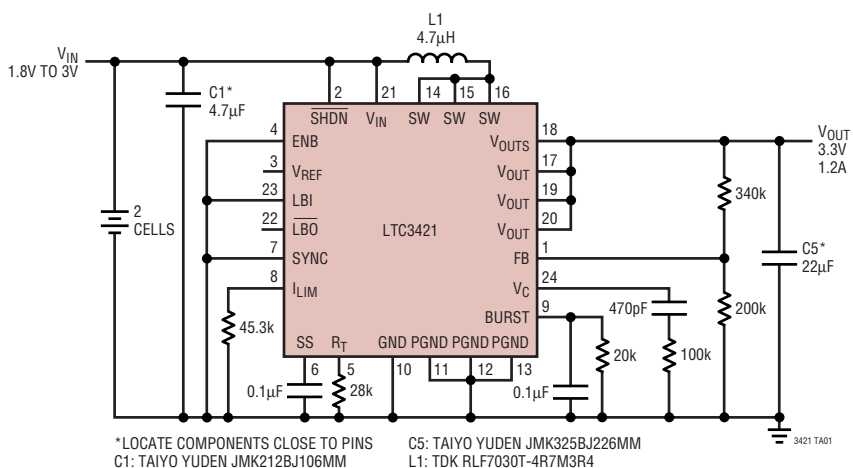
Quiescent current is only 12 $\mu$ A during Burst Mode operation, maximizing battery life in portable applications. The oscillator frequency can be programmed up to 3MHz and can be synchronized to an external clock applied to the SYNC pin. An open-drain uncommitted low-battery comparator is included. The part maintains operation in applications with a secondary cell powering the output voltage during shutdown.

Other features include: 1 $\mu$ A shutdown, antiringing control, thermal limit and reference output.

The LTC3421 is available in a small 4mm  $\times$  4mm QFN package.

**LT**, LTC and LT are registered trademarks of Linear Technology Corporation. Burst Mode is a registered trademark of Linear Technology Corporation.

## TYPICAL APPLICATION



3421 GD2

3421f

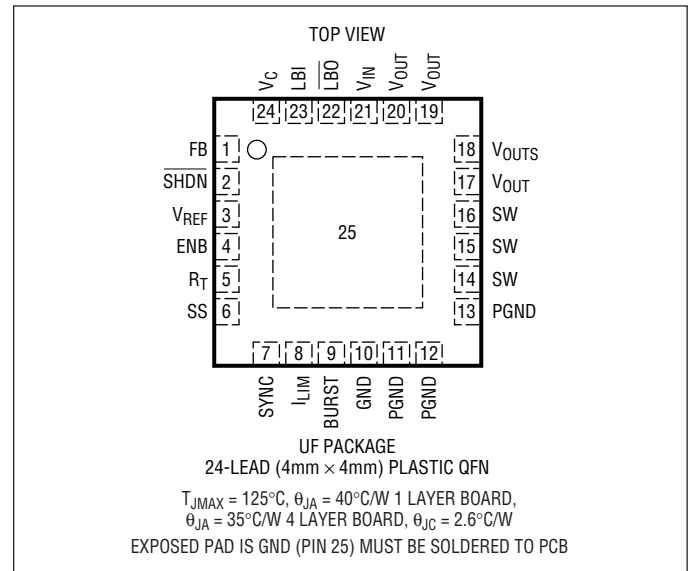


## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$ ,  $V_{OUT}$ ,  $V_{OUTS}$  Voltage ..... -0.3V to 6V  
 BURST, SHDN, SS, ENB, SW,  
 LBO, LBI, SYNC Voltages ..... -0.3V to 6V  
 Operating Temperature Range  
 (Notes 2, 5) ..... -40°C to 85°C  
 Storage Temperature Range ..... -65°C to 125°C  
 Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC3421EUF

UF PART MARKING

3421

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ .  $V_{IN} = 1.2\text{V}$ ,  $V_{OUT} = 3.3\text{V}$ ,  $R_T = 28\text{k}$ , unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum $V_{IN}$ Start-Up Voltage	$I_{LOAD} < 1\text{mA}$		0.88	1	V
Minimum $V_{IN}$ Operating Voltage	(Note 4)	●		0.5	V
Output Voltage Adjust Range		2.25		5.25	V
		● 2.40		5.25	V
Feedback Voltage		● 1.196	1.220	1.244	V
Feedback Input Current	$V_{FB} = 1.22\text{V}$		1	50	nA
Quiescent Current—Burst Mode Operation	$V_C = 0\text{V}$ , $\text{ENB} = 0\text{V}$ (Note 3)		12	20	$\mu\text{A}$
	$V_C = 0\text{V}$ , $\text{ENB} = 2\text{V}$ (Note 3)		23	50	$\mu\text{A}$
Quiescent Current—Shutdown	$\text{SHDN} = 0\text{V}$ , $\text{ENB} = 0\text{V}$		0.1	1	$\mu\text{A}$
	$\text{SHDN} = 0\text{V}$ , $\text{ENB} > 1.4\text{V}$		0.2	2	$\mu\text{A}$
Quiescent Current—Active	(Note 3)		0.6	1.1	mA
NMOS Switch Leakage			0.1	5	$\mu\text{A}$
PMOS Switch Leakage			0.1	10	$\mu\text{A}$
NMOS Switch On Resistance			0.1		$\Omega$
PMOS Switch On Resistance			0.14		$\Omega$
NMOS Current Limit	$I_{LIM}$ Resistor = 105k	●	1	1.5	A
	$I_{LIM}$ Resistor = 36.5k	●	3	4.2	A
Max Duty Cycle		●	84	91	%
Min Duty Cycle		●		0	%



## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 1.2\text{V}$ ,  $V_{OUT} = 3.3\text{V}$ ,  $R_T = 28\text{k}$ , unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Accuracy		●	0.85	1	1.15	MHz
SYNC Input High		●	2.2			V
SYNC Input Low		●			0.8	V
SYNC Input Current		●		0.01	1	$\mu\text{A}$
ENB Input High		●	1.2			V
ENB Input Low		●			0.4	V
ENB Input Current		●			1	$\mu\text{A}$
SHDN Input High	$V_{OUT} = 0\text{V}$ (Initial Start-Up) $V_{OUT} > 2.4\text{V}$		1.00 0.65			V V
SHDN Input Low					0.25	V
SHDN Input Current		●		0.01	1	$\mu\text{A}$
REF Output Voltage		●	1.183	1.22	1.257	V
REF Output Current Range			-100		8	$\mu\text{A}$
Error Amp Transconductance				45		$\mu\text{S}$
LBI Threshold	Falling Edge	●	0.58	0.6	0.62	V
LBI Input Current		●		0.01	1	$\mu\text{A}$
LBO Low Voltage	$V_{IN} = 0\text{V}$ , $I_{SINK} = 1\text{mA}$ $V_{IN} = 0\text{V}$ , $I_{SINK} = 20\text{mA}$			12.0 0.25	50 0.5	mV V
LBO Leakage	$V_{PGOOD} = 5.5\text{V}$			0.01	1	$\mu\text{A}$
SS Current Source	$V_{SS} = 1\text{V}$		1.2	2.4	5	$\mu\text{A}$
BURST Threshold Voltage	Falling Edge		0.87	0.97	1.07	V

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The LTC3421E is guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . Specifications over the  $40^\circ\text{C}$  to  $85^\circ\text{C}$  operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** Current is measured into the  $V_{OUTS}$  pin since the supply current is bootstrapped to the output. The current will reflect to the input supply by  $(V_{OUT}/V_{IN}) \cdot \text{Efficiency}$ . The outputs are not switching.

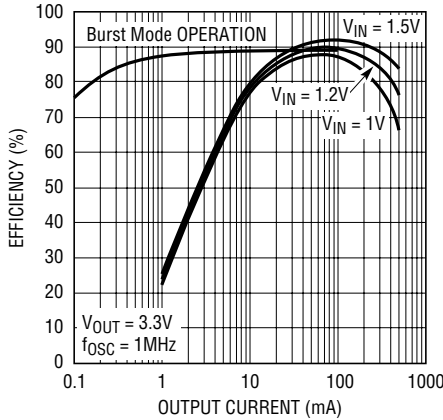
**Note 4:** Once  $V_{OUT}$  is greater than  $2.4\text{V}$ , the IC is not dependent on the  $V_{IN}$  supply.

**Note 5:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $125^\circ\text{C}$  when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

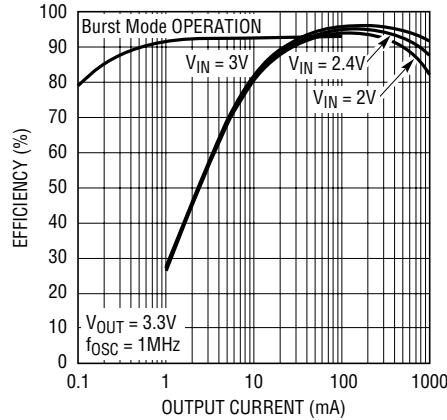


## TYPICAL PERFORMANCE CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , unless otherwise specified)

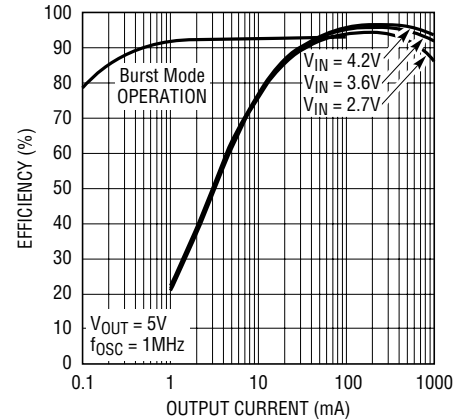
### Single Cell to 3.3V Efficiency



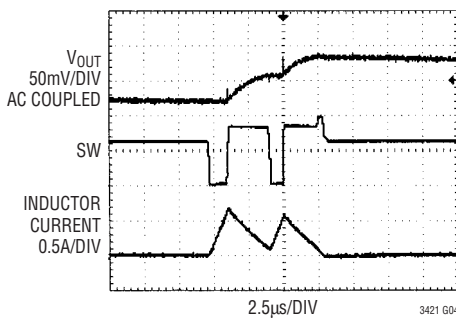
### 2-Cell to 3.3V Efficiency



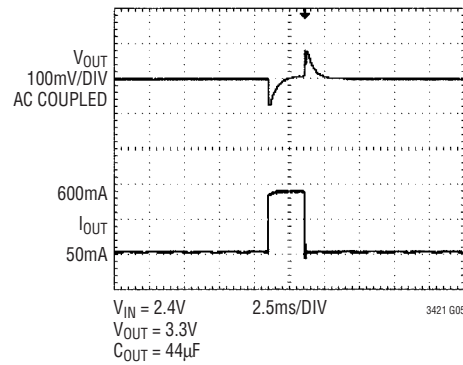
### Li-Ion to 5V Efficiency



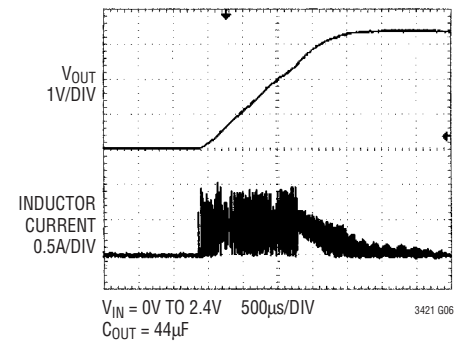
### Burst Mode Operation



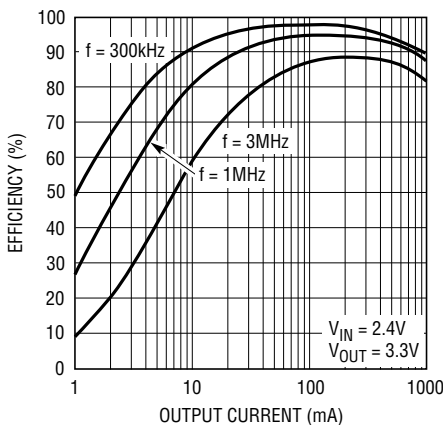
### Load Transient Response



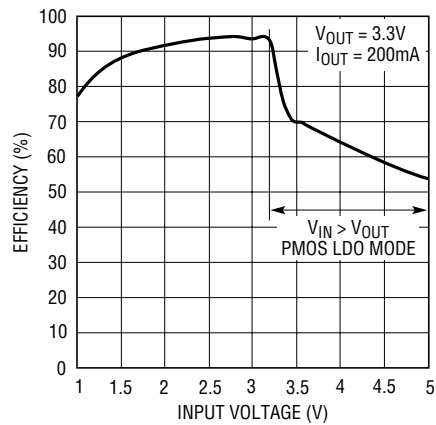
### Inrush Current Control



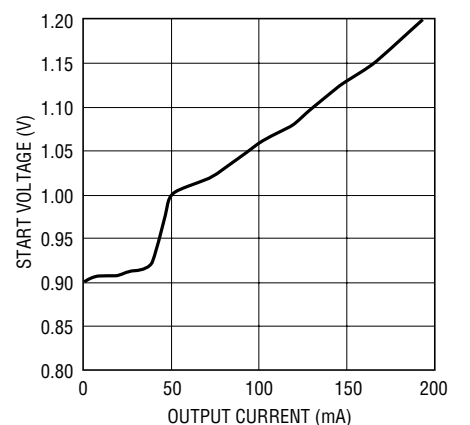
### Efficiency vs Frequency



### Efficiency vs VIN

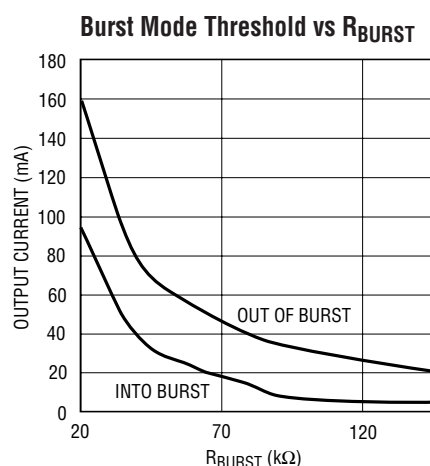


### Start-Up Voltage vs Output Current

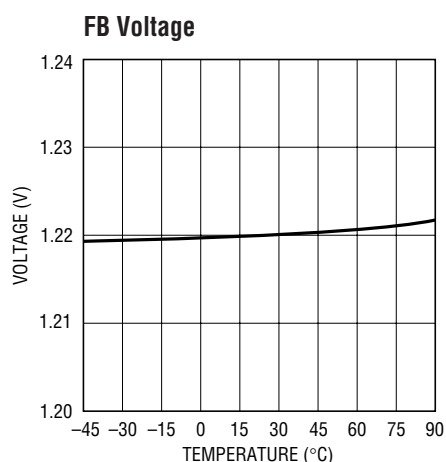




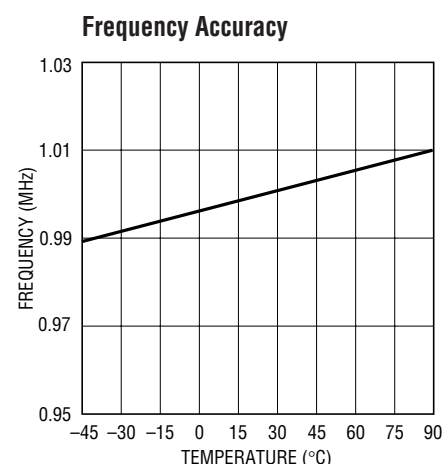
## TYPICAL PERFORMANCE CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , unless otherwise specified)



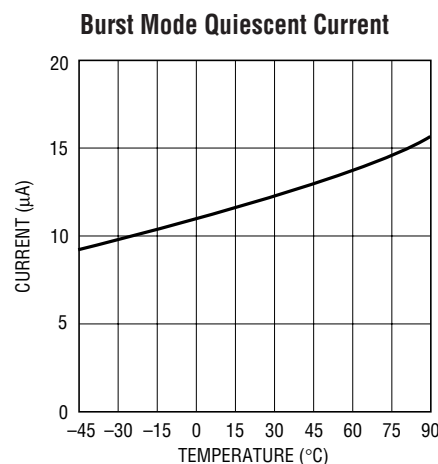
3421 G10



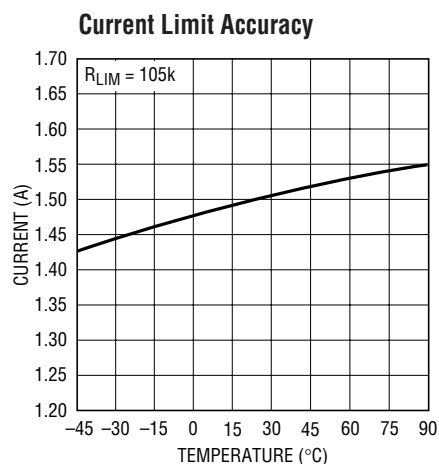
3421 G11



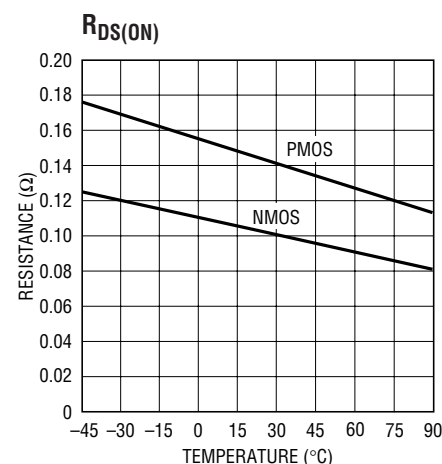
3421 G12



3421 G13



3421 G14



3421 G15

## PIN FUNCTIONS

**FB (Pin 1):** Feedback Pin. Connect resistor divider tap here. The output voltage can be adjusted from 2.4V to 5.25V. The feedback reference voltage is typically 1.220V.

**SHDN (Pin 2):** Shutdown Pin. Less than 0.25V on this pin shuts down the IC. The IC is enabled when the SHDN voltage is greater than 1V. Once  $V_{OUT}$  is above 2.2V, hysteresis is applied to the pin (–500nA out of the pin) allowing it to operate at a logic high while the battery can drop to 0.5V.

**$V_{REF}$  (Pin 3):** Buffered 1.22V Reference Output. This pin can source up to 100μA and sink up to 8μA. This pin must be decoupled with a 0.1μF capacitor for stability.

**ENB (Pin 4):** Reference Output ( $V_{REF}$ ) and Low-Battery Comparator Enable. When ENB = Low, the  $V_{REF}$  output and low-battery comparator are disabled, which lowers the quiescent current by 5μA. When ENB = High, the  $V_{REF}$  output and the low-battery comparator are enabled. During shutdown, if the ENB = High and the output voltage is pulled up to greater than 2.5V from a secondary source such as a coin cell through a Schottky diode, the  $V_{REF}$  output and low-battery comparator becomes powered from the output voltage and enabled.

3421f



## PIN FUNCTIONS

**R<sub>T</sub> (Pin 5):** Connect a resistor to ground to program the oscillator frequency according to the formula:

$$f_{\text{OSC}} = \frac{28,100}{R_T}$$

where  $f_{\text{OSC}}$  is in kHz and  $R_T$  is in k $\Omega$ .

**SS (Pin 6):** Soft-Start Pin. Connect a capacitor from this pin to ground to set the soft-start time according to the formula:

$$t(\text{ms}) = C_{\text{SS}}(\mu\text{F}) \cdot 320$$

The nominal soft-start charging current is 2.5 $\mu\text{A}$ . The active range of SS is from 0.8V to 1.6V.

**SYNC (Pin 7):** Oscillator Synchronization Pin. A clock pulse width of 100ns to 2 $\mu\text{s}$  is required to synchronize the internal oscillator. If not used SYNC should be grounded.

**I<sub>LIM</sub> (Pin 8):** Current Limit Adjust Pin. Connect a resistor from this pin to ground to set the peak current limit threshold for the N-channel MOSFET according to the formula (note that this is the peak current in the inductor):

$$I_{\text{LIM}} = \frac{150}{R}$$

where  $I$  is in amps and  $R$  is in k $\Omega$ .

**BURST (Pin 9):** Burst Mode Threshold Adjust Pin. A resistor/capacitor combination from this pin to ground programs the average load current at which automatic Burst Mode operation is entered, according to the formula:

$$R_{\text{BURST}} = \frac{2}{I_{\text{BURST}}}$$

where  $R_{\text{BURST}}$  is in k $\Omega$  and  $I_{\text{BURST}}$  is in amps.

$$C_{\text{BURST}} \geq \frac{C_{\text{OUT}} \cdot V_{\text{OUT}}}{10,000}$$

where  $C_{\text{BURST(MIN)}}$  and  $C_{\text{OUT}}$  are in  $\mu\text{F}$ .

For manual control of Burst Mode operation, ground the BURST pin to force Burst Mode operation or connect it to  $V_{\text{OUT}}$  to force fixed frequency PWM mode. Note that the BURST pin must not be pulled higher than  $V_{\text{OUT}}$ .

**GND (Pin 10):** Signal Ground Pin. Connect to ground plane near the  $R_T$  resistor, error amp compensation components and feedback divider.

**PGND (Pins 11 to 13):** Source Terminal of Power Internal N-Channel MOSFET.

**SW (Pins 14 to 16):** Switch Pin for Inductor Connection. For applications where  $V_{\text{OUT}} > 4.3\text{V}$ , a Schottky diode from SW to  $V_{\text{OUT}}$  or to a snubber circuit is required to maintain absolute maximum rating for SW. (see Application Circuits for 5V).

**V<sub>OUT</sub> (Pins 17, 19 and 20):** The output of the synchronous rectifier and bootstrapped power source for the IC. A ceramic bypass capacitor is required to be very close to the  $V_{\text{OUT}}$  and PGND pins of the IC.

**V<sub>OUTS</sub> (Pin 18):**  $V_{\text{OUT}}$  Sense Pin. Connect  $V_{\text{OUTS}}$  directly to an output filter capacitor. The top of the feedback divider network should also be tied to this point.

**V<sub>IN</sub> (Pin 21):** Input Supply Pin. Connect this pin to the input supply and decouple with at least a 4.7 $\mu\text{F}$  ceramic capacitor.

**LBO (Pin 22):** Open-Drain Output. This pin pulls low when the LBI input is below 0.6V. The open-drain output can sink up to 20mA. During Burst Mode operation LBO is only active during the time the IC wakes up to service the output.

**LBI (Pin 23):** Low-Battery Comparator Input. Typical threshold voltage is 0.6V with 30mV hysteresis. This function is enabled when the ENB pin is high. The low-battery comparator will operate off  $V_{\text{IN}}$  or  $V_{\text{OUT}}$ , whichever is greater.

**V<sub>C</sub> (Pin 24):** Error Amp Output. A frequency compensation network is connected from this pin to ground to compensate the loop. See the section Compensating the Feedback Loop for guidelines.

**Exposed Pad (Pin 25):** Ground. This pin must be soldered to the PCB and is typically connected through the power GND plane.



The schematic diagram illustrates the internal architecture of the LT8602S Buck-Boost Converter. Key components and their connections include:

- Input Stage:** The input voltage  $V_{IN}$  (pin 21) is connected to the antiringing network and the antixcross conduction block. The output of the antixcross conduction block is connected to the PMOS switch (pin 14) and the NMOS switch (pin 15).
- Power Stage:** The PMOS switch (pin 14) and NMOS switch (pin 15) are connected to the output node  $V_{OUT}$  (pin 18). The output node is connected to the output filter capacitor  $C_P$  (pin 24) and the output resistor  $R_Z$  (pin 9).
- Feedback Loop:** The output voltage  $V_{OUT}$  is connected to the feedback pin (pin 1) through a resistor  $R_2$ . The feedback pin is also connected to the error amplifier (pin 1) and the current limit block (pin 8).
- Control Logic:** The current limit block (pin 8) is connected to the current limit pin (pin 8) and the current comparator (pin 1). The current comparator is connected to the current limit pin (pin 8) and the current limit block (pin 8).
- Thermal Regulation:** The thermal regulation/shutdown block (pin 2) is connected to the shutdown pin (pin 2) and the shutdown pin (pin 2).
- Output Stage:** The output stage includes a burst comparator (pin 9) and a slope compensator (pin 9).
- Power and Grounding:** The circuit is powered by a 1V to 4.5V input and has a 2.40V to 5.25V output range. It includes multiple ground connections (GND, PGND, EXPOSED PAD) and a 3421 BD identifier.



## OPERATION

### LOW VOLTAGE START-UP

The LTC3421 includes an independent start-up oscillator designed to start-up at input voltages of 0.85V typical. The frequency and peak current limit during start-up are internally controlled. The device can start-up under some load (see graph of Start-Up Current vs Input Voltage). Soft-start and inrush current limiting are provided during start-up as well as normal mode. The same soft-start capacitor is used for each operating mode.

When either  $V_{IN}$  or  $V_{OUT}$  exceeds 2.25V, the IC enters normal operating mode. Once the output voltage exceeds the input by 0.3V, the IC powers itself from  $V_{OUT}$  instead of  $V_{IN}$ . At this point the internal circuitry has no dependency on the  $V_{IN}$  input voltage, eliminating the requirement for a large input capacitor. The input voltage can drop as low as 0.5V without affecting circuit operation. The limiting factor for the application becomes the availability of the power source to supply sufficient energy to the output at the low voltages and the maximum duty cycle, which is clamped at 91% typical.

### LOW NOISE FIXED FREQUENCY OPERATION

#### Shutdown

The part is shut down by pulling  $\overline{SHDN}$  below 0.3V, and activated by pulling the pin initially above 1V and maintaining a high state down to 0.5V. Note that the  $\overline{SHDN}$  pin can be driven above  $V_{IN}$  or  $V_{OUT}$  as long as it is limited to less than the absolute maximum rating.

#### Soft-Start

The soft-start time is programmed with an external capacitor to ground on the SS pin. An internal current source charges it with a nominal 2.5 $\mu$ A. The voltage on the SS pin (in conjunction with the external resistor on the  $I_{LIM}$  pin) is used to control the peak current limit until the voltage on the capacitor exceeds 1.6V, at which point the external resistor sets the peak current. In the event of a commanded shutdown or a thermal shutdown, the capacitor is discharged automatically. Note that Burst Mode operation is inhibited during the soft-start time.

$$t(\text{ms}) = C_{SS}(\mu\text{F}) \cdot 320$$

### Oscillator

The frequency of operation is set through a resistor from the  $R_T$  pin to ground. An internally trimmed timing capacitor resides inside the IC. The oscillator can be synchronized with an external clock applied to the SYNC pin. When synchronizing the oscillator, the free running frequency must be set to an approximately 30% lower frequency than the desired synchronized frequency.

### Current Sensing

Lossless current sensing converts the peak current signal to a voltage to sum in with the internal slope compensation. This summed signal is compared to the error amplifier output to provide a peak current control command for the PWM. The slope compensation in the IC is adaptive to the input voltage and output voltage. Therefore, the converter provides the proper amount of slope compensation to ensure stability, but not an excess to cause a loss of phase margin in the converter.

### Error Amplifier

The error amplifier is a transconductance amplifier, with its positive input internally connected to the 1.22V reference and its negative input connected to FB. A simple compensation network is placed from COMP to ground. Internal clamps limit the minimum and maximum error amplifier output voltage for improved large-signal transient response. During sleep (in Burst Mode operation), the compensation pin is high impedance; however, clamps limit the voltage on the external compensation network, preventing the compensation capacitor from discharging to zero during the sleep time.

### Current Limit

The programmable current limit circuit sets the maximum peak current. This clamp level is programmed with a resistor from  $I_{LIM}$  to ground. In Burst Mode operation, the current limit is automatically set to a nominal value of 0.6A peak for optimal efficiency.

$$I_{LIM} = \frac{150}{R}$$

where I is in amps and R is in k $\Omega$ .



## OPERATION

### Zero Current Amplifier

The zero current amplifier monitors the inductor current to the output and shuts off the synchronous rectifier once the current is below 50mA typical, preventing negative inductor current.

### Antiringing Control

The antiringing control places a resistor across the inductor to damp the ringing on the SW pin in discontinuous conduction mode. The  $LC_{SW}$  ringing ( $L$  = inductor,  $C_{SW}$  = capacitance on SW pin) is low energy, but can cause EMI radiation.

### $V_{REF}$

The internal 1.22V reference is buffered and brought out to REFOUT. It is active when the ENB pin is pulled high (above 1.4V). For stability, a minimum of a 0.1 $\mu$ F capacitor must be placed on the pin. The output can source up to 100 $\mu$ A and sink up to 8 $\mu$ A. For the lowest possible quiescent current in Burst Mode operation, the reference output should be disabled by grounding the ENB pin.

### Burst Mode OPERATION

Burst Mode operation can be automatic or user controlled. In automatic operation, the IC will automatically enter Burst Mode operation at light load and return to fixed frequency PWM mode for heavier loads. The user can program the average load current at which the mode transition occurs using a single resistor.

The oscillator is shut down in this mode, since the on time is determined by the time it takes the inductor current to reach a fixed peak current and the off time is determined by the time it takes for the inductor current to return to zero.

In Burst Mode operation, the IC delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the IC is consuming only 12 $\mu$ A of quiescent current. In this mode, the output ripple has a variable frequency component with load current and will be typically 2% peak-peak. This maximizes efficiency at very light loads by minimizing switching and quiescent losses. Burst Mode ripple can be reduced slightly by

increasing the output capacitance. Another method of reducing Burst Mode ripple is to place a small feed-forward capacitor across the upper resistor in the  $V_{OUT}$  feedback divider network.

During Burst Mode operation, the  $V_C$  pin is disconnected from the error amplifier in an effort to hold the voltage on the external compensation network where it was before entering Burst Mode operation. To minimize the effects of leakage current and stray resistance, voltage clamps limit the min and max voltage on  $V_C$  during Burst Mode operation. This minimizes the transient experienced when a heavy load is suddenly applied to the converter after being in Burst Mode operation for an extended period of time.

For automatic operation, an RC network should be connected from BURST to ground. The value of the resistor will control the average load current ( $I_{BURST}$ ) at which Burst Mode operation will be entered and exited (there is hysteresis to prevent oscillation between modes). The equation given for the capacitor on BURST is for the minimum value to prevent ripple on BURST from causing the part to oscillate in and out of Burst Mode operation at the current where the mode transition occurs.

$$R_{BURST} = \frac{2}{I_{BURST}}$$

where  $R_{BURST}$  is in k $\Omega$  and  $I_{BURST}$  is in amps.

$$C_{BURST} \geq \frac{C_{OUT} \cdot V_{OUT}}{10,000}$$

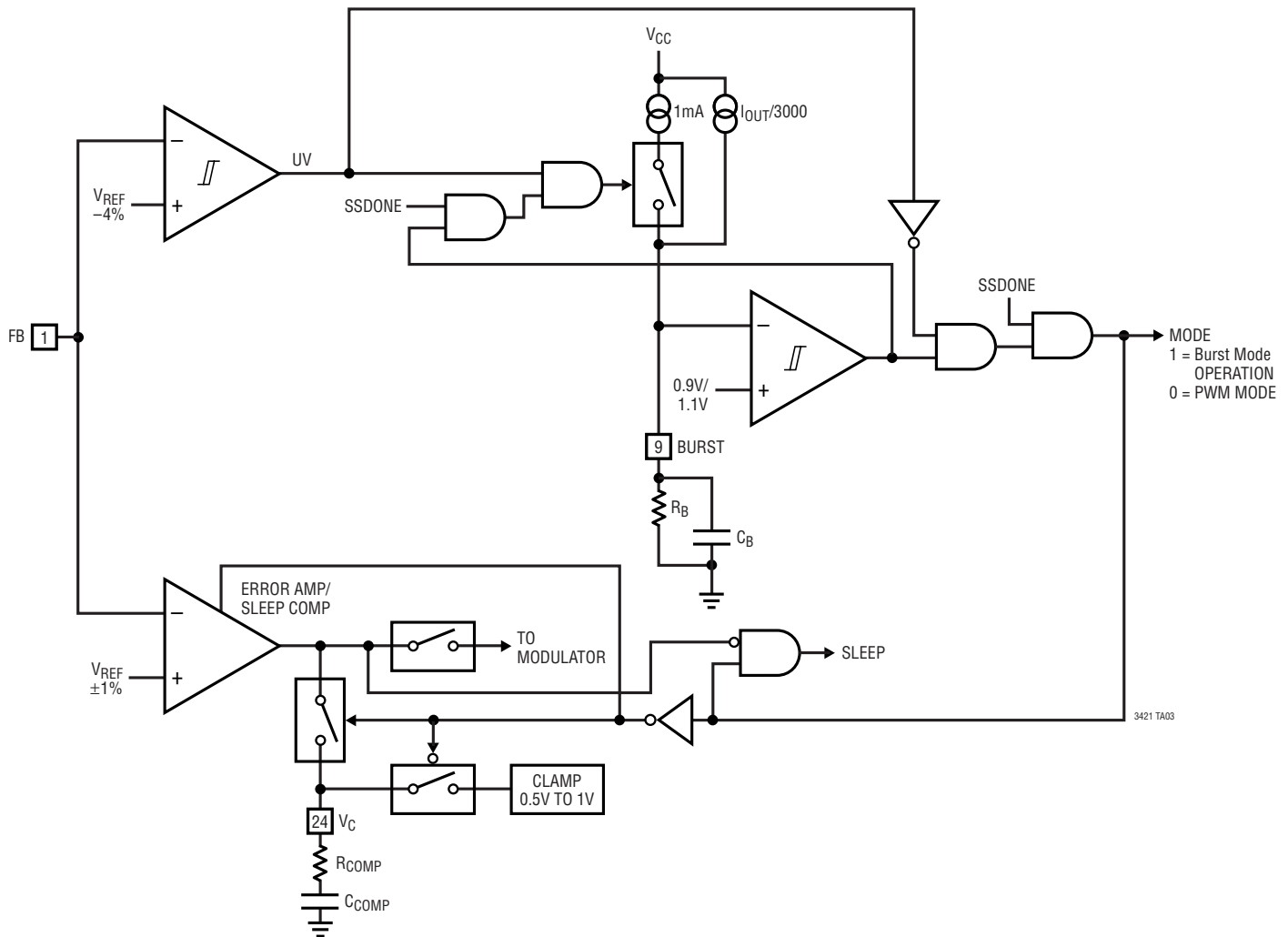
where  $C_{BURST(MIN)}$  and  $C_{OUT}$  are in  $\mu$ F.

In the event that a sudden load transient causes FB to deviate by more than 4% from the regulation value, an internal pull-up is applied to BURST, forcing the part quickly out of Burst Mode operation. For optimum transient response when going between Burst Mode operation and PWM mode, the mode should be controlled manually by the host. This way PWM mode can be commanded before the load step occurs, minimizing output voltage droop. For manual control of Burst Mode operation, the RC network can be eliminated. To force fixed frequency PWM mode, BURST should be connected to  $V_{OUT}$ . To force Burst Mode operation, BURST should be grounded.



## OPERATION

Simplified Diagram of Automatic Burst Mode Control Circuit



The circuit connected to BURST should be able to sink or source up to 2mA. Note that Burst Mode operation is inhibited during start-up and soft-start.

Note that if  $V_{IN}$  is above  $V_{OUT} - 0.3V$ , the part will exit Burst Mode operation and the synchronous rectifier will be disabled.

Note that if the load applied during forced Burst Mode operation exceeds the current that can be supplied, the output voltage will start to droop and the part will automatically come out of Burst Mode operation and enter fixed frequency mode, raising  $V_{OUT}$ . The maximum current that can be supplied in Burst Mode operation is given by:

$$I_{O(MAX)} = \frac{0.55}{2 \cdot \frac{1 + (V_{OUT} - V_{IN})}{V_{IN}}} \text{ in amps}$$

### OUTPUT DISCONNECT AND INRUSH LIMITING

The LTC3421 is designed to allow true output disconnect by eliminating body diode conduction of the internal P-channel MOSFET rectifier. This allows  $V_{OUT}$  to go to zero volts during shutdown without drawing any current from the input source. It also allows for inrush current limiting at turn-on, minimizing surge currents seen by the input supply. Note that to obtain the advantages of output



## OPERATION

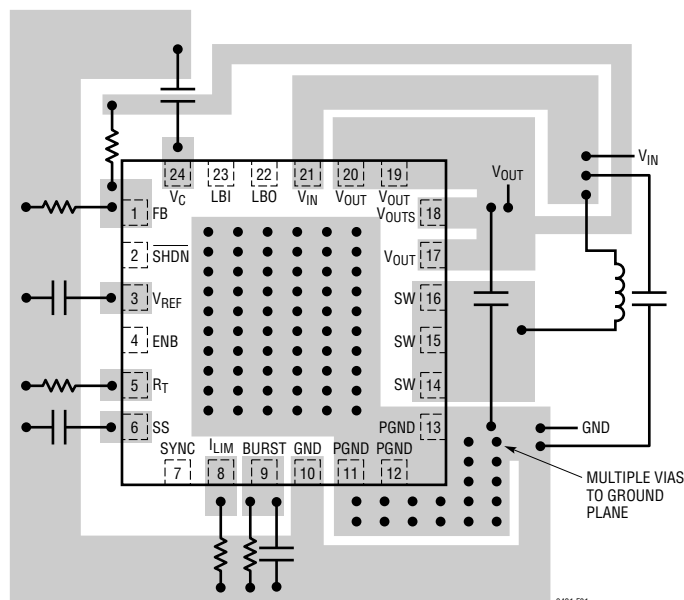
disconnect, there must not be any external Schottky diodes connected between the SW pins and  $V_{OUT}$ .

**Note:** Board layout is extremely critical to minimize voltage overshoot on the SW pins due to stray inductance. Keep the output filter capacitors as close as possible to the

$V_{OUT}$  pins and use very low ESR/ESL ceramic capacitors, tied to a good ground plane. In  $V_{OUT} > 4.3V$  applications, a Schottky diode is required from the switch nodes to  $V_{OUT}$  to limit the peak switch voltage to less than 6V unless some form of external snubbing is employed. (See 5V Applications section.)

## APPLICATIONS INFORMATION

### COMPONENT SELECTION



**Figure 1. Recommended Component Placement.** Traces Carrying High Current are Direct (PGND, SW,  $V_{OUT}$ ). Trace Area at FB and  $V_C$  are Kept Low. Lead Length to Battery Should be Kept Short.  $V_{IN}$  and  $V_{OUT}$  Ceramic Capacitors Should be as Close to the IC Pins as Possible

### Inductor Selection

The high frequency operation of the LTC3421 allows the use of small surface mount inductors. The minimum inductance value is proportional to the operating frequency and is limited by the following constraints:

$$L > \frac{3}{f} \text{ and } L > \frac{V_{IN(MIN)} \cdot (V_{OUT(MAX)} - V_{IN(MIN)})}{f \cdot \text{Ripple} \cdot V_{OUT(MAX)}}$$

where

$f$  = Operating Frequency in MHz

Ripple = Allowable Inductor Current Ripple (Amps Peak-Peak)

$V_{IN(MIN)}$  = Minimum Input Voltage

$V_{OUT(MAX)}$  = Maximum Output Voltage

The inductor current ripple is typically set to 20% to 40% of the maximum inductor current.

For high efficiency, choose an inductor with high frequency core material, such as ferrite, to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the  $I^2R$  losses and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support peak inductor currents in the 1A to 4A region. To minimize radiated noise, use a toroidal or shielded inductor. See Table 1 for suggested inductor suppliers and Table 2 for a list of capacitor suppliers.

**Table 1. Inductor Vendor Information**

SUPPLIER	PHONE	FAX	WEB SITE
Coilcraft	(847) 639-6400	(847) 639-1469	www.coilcraft.com
Coiltronics	(561) 241-7876	(516) 241-9339	
Murata	USA: (814) 237-1431 (800) 831-9172	USA: (814) 238-0490	www.murata.com
Sumida	USA: (847) 956-0666 Japan: 81-3-3607-5111	USA: (847) 956-0702 Japan: 81-3-3607-5144	www.sumida.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com
TOKO	(847) 297-0070	(847) 669-7864	www.toko.com



## APPLICATIONS INFORMATION

### Output Capacitor Selection

The output voltage ripple has two components to it. The bulk value of the capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The maximum ripple due to charge is given by:

$$V_{RBULK} = \frac{I_P \cdot V_{IN}}{C_{OUT} \cdot V_{OUT} \cdot f}$$

where  $I_P$  = peak inductor current.

The ESR (equivalent series resistance) is usually the most dominant factor for ripple in most power converters. The ripple due to capacitor ESR is simply given by:

$$V_{RCESR} = I_P \cdot C_{ESR}$$

where  $C_{ESR}$  = capacitor series resistance.

Low ESR capacitors should be used to minimize output voltage ripple. For surface mount applications, AVX TPS series tantalum capacitors, Sanyo POSCAP or Taiyo Yuden ceramic capacitors are recommended. For through-hole applications, Sanyo OS-CON capacitors offer low ESR in a small package size.

In some layouts it may be necessary to place a 1 $\mu$ F low ESR ceramic capacitor as close to the  $V_{OUT}$  and GND pins as possible.

### Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the input source and reduces input switching noise. Since the IC can operate at voltages below 0.5V once the output is regulated, the demand on the input capacitor is much less. In most applications 1 $\mu$ F per amp of peak input current is recommended. Taiyo Yuden offers very low ESR ceramic capacitors, for example the 1 $\mu$ F in a 0603 case (JMK107BJ105MA).

**Table 2. Capacitor Vendor Information**

SUPPLIER	PHONE	FAX	WEB SITE
AVX	(803) 448-9411	(803) 448-1943	www.avxcorp.com
Sanyo	(619) 661-6322	(619) 661-1055	www.sanyovideo.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com
Murata	USA: (814) 237-1431 (800) 831-9172	USA: (814) 238-0490	www.murata.com
Taiyo Yuden	(408) 573-4150	(408) 573-4159	www.t-yuden.com

### Operating Frequency Selection

There are several considerations in selecting the operating frequency of the converter. The first is, which are the sensitive frequency bands that cannot tolerate any spectral noise? The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter capacitors go down in value and size. The trade off is in efficiency since the switching losses due to gate charge are going up proportional with frequency.

Another operating frequency consideration is whether the application can allow "pulse skipping." In this mode, the minimum on time of the converter cannot support the duty cycle, so the converter ripple will go up and there will be a low frequency component of the output ripple. In many applications where physical size is the main criterion, running the converter in this mode is acceptable. In applications where it is preferred not to enter this mode, the maximum operating frequency is given by:

$$f_{MAX\_NOSKIP} = \frac{V_{OUT} - V_{IN}}{V_{OUT} \cdot t_{ON(MIN)}} \text{ Hz}$$

where  $t_{ON(MIN)}$  = minimum on time = 120ns.

### Thermal Considerations

To deliver the power that the LTC3421 is capable of, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the large thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible. In the event that the junction temperature gets too high, the peak current limit will automatically be decreased. If the junction temperature continues to rise, the part will go into thermal shutdown, and all switching will stop until the temperature drops.

### $V_{IN} > V_{OUT}$ Operation

The LTC3421 will maintain voltage regulation when the input voltage is above the output voltage. This is achieved by terminating the switching on the synchronous PMOS and applying  $V_{IN}$  statically on the gate. This will ensure the



## APPLICATIONS INFORMATION

volts • seconds of the inductor will reverse during the time current is flowing to the output. Since this mode will dissipate more power in the IC, the maximum output current is limited in order to maintain an acceptable junction temperature.

$$I_{OUT(MAX)} = \frac{125 - T_A}{40 \cdot ((V_{IN} + 1.5) - V_{OUT})}$$

where  $T_A$  = ambient temperature.

For example at  $V_{IN} = 4.5V$  and  $V_{OUT} = 3.3V$ , the maximum output current is 370mA.

### Short Circuit

The LTC3421 output disconnect feature allows output short circuit while maintaining a maximum set current limit. The IC has incorporated internal features such as current limit and thermal shutdown for protection from an excessive overload or short circuit. In applications that require a prolonged short circuit, it is recommended to limit the power dissipation in the IC to maintain an acceptable junction temperature. The circuit in Figure 2 will limit the maximum current during a prolonged short by reducing the current limit value in a short circuit by disconnecting R2 with the N-channel MOSFET switch. R3 and C1 provide a soft-start function after a short circuit. Resistor R1 lowers the current limit value as  $V_{IN}$  rises, maintaining a relatively constant power. The current limit equation for the circuit in Figure 2 is given by:

$$I_{LIMIT} = \left( \frac{0.6}{R_{LIM}} - \frac{V_{IN} - 0.6}{R1} \right) \cdot 250$$

where  $I_{LIMIT}$  is in Amps;  $R_{LIM}$  and R1 are in k $\Omega$ .

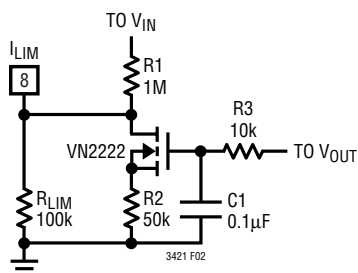


Figure 2. Current Limit Foldback Circuit for Extended Short Conditions

### Closing the Feedback Loop

The LTC3421 uses current mode control with internal adaptive slope compensation. Current mode control eliminates the 2nd order filter due to the inductor and output capacitor exhibited in voltage mode controllers, and simplifies it to a single pole filter response. The product of the modulator control to output DC gain and the error amp open-loop gain gives the DC gain of the system:

$$G_{DC} = G_{CONTROL\_OUTPUT} \cdot G_{EA} \cdot \frac{V_{REF}}{V_{OUT}}$$

$$G_{CONTROL} = \frac{2 \cdot V_{IN}}{I_{OUT}}, G_{EA} \approx 2000$$

The output filter pole is given by:

$$f_{FILTER\_POLE} = \frac{I_{OUT}}{\pi \cdot V_{OUT} \cdot C_{OUT}}$$

where  $C_{OUT}$  is the output filter capacitor.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{OUT}}$$

where  $R_{ESR}$  is the capacitor equivalent series resistance.

A troublesome feature of the boost regulator topology is the right-half plane zero (RHP) and is given by:

$$f_{RHPZ} = \frac{V_{IN}^2}{2 \cdot \pi \cdot I_{OUT} \cdot L}$$

At heavy loads this gain increase with phase lag can occur at a relatively low frequency. The loop gain is typically rolled off before the RHP zero frequency.

The typical error amp compensation is shown in Figure 3. The equations for the loop dynamics are as follows:

$$f_{POLE1} \approx \frac{1}{2 \cdot \pi \cdot 20e6 \cdot C_{C1}} \text{ which is extremely close to DC}$$

$$f_{ZERO1} \approx \frac{1}{2 \cdot \pi \cdot R_Z \cdot C_{C1}}$$

$$f_{POLE2} \approx \frac{1}{2 \cdot \pi \cdot R_Z \cdot C_{C2}}$$



## APPLICATIONS INFORMATION

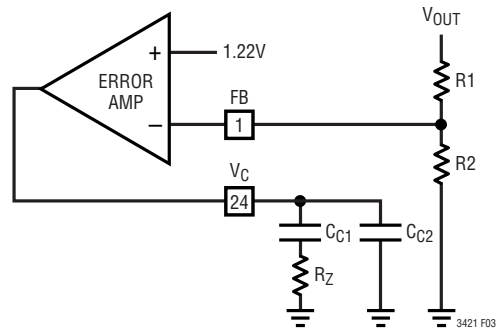


Figure 3

## TYPICAL APPLICATION

## 5V Applications

When the output voltage is programmed above 4.3V it is necessary to add a Schottky diode either from SW to  $V_{OUT}$ , or to a snubber network in order to maintain an acceptable peak voltage on SW. The Schottky to the

output will provide a peak efficiency improvement but will negate the output disconnect feature. If output disconnect is required, the Schottky to an active snubber network is suggested as shown in Figure 4.

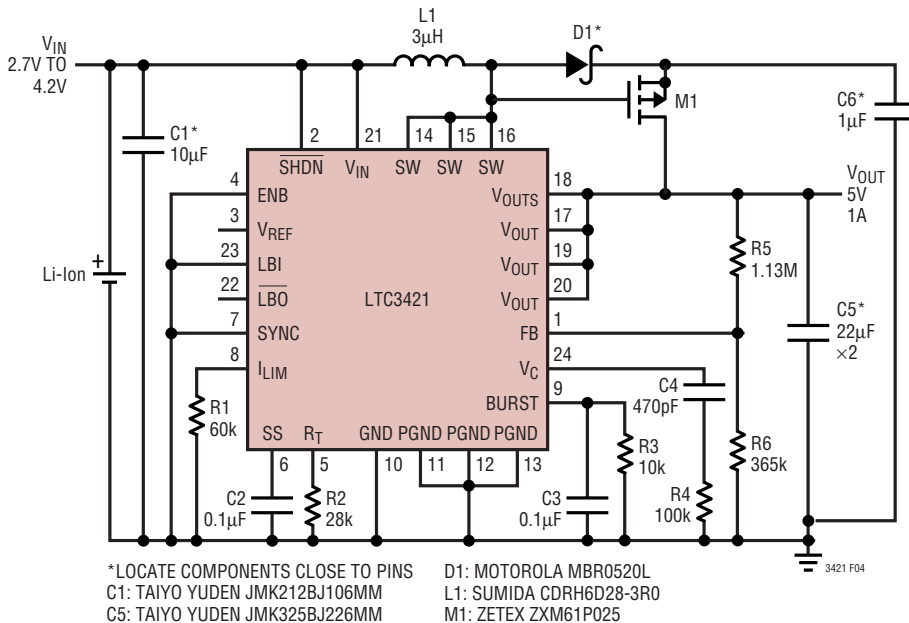
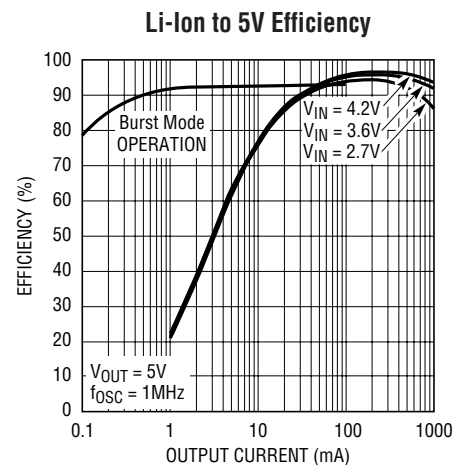


Figure 4. Lithium-Ion to 5V at 1A Application with an Active Snubber Circuit



3421 G03

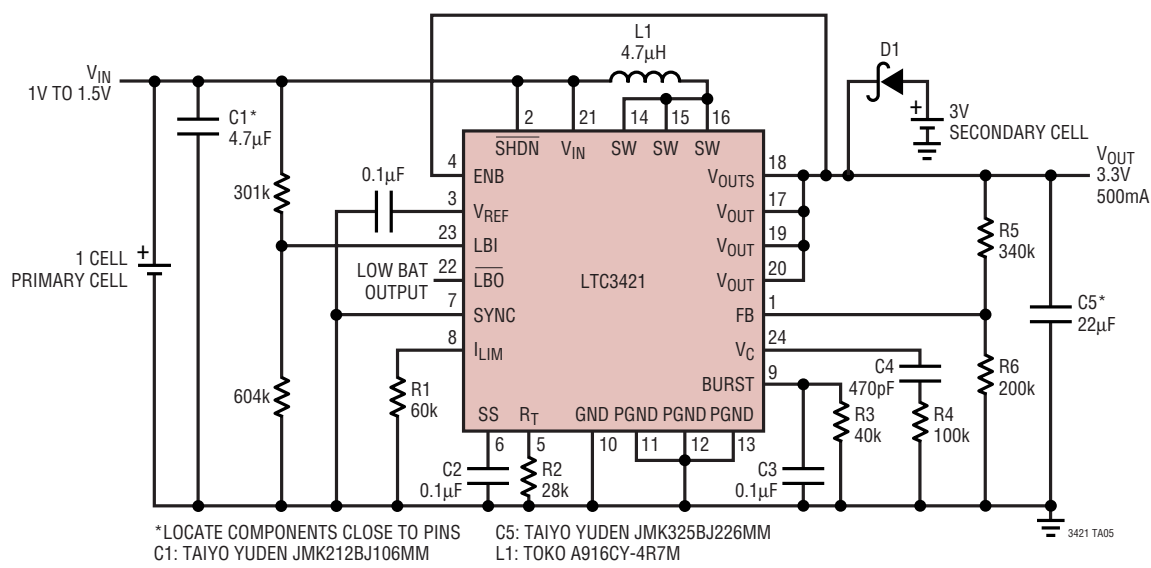




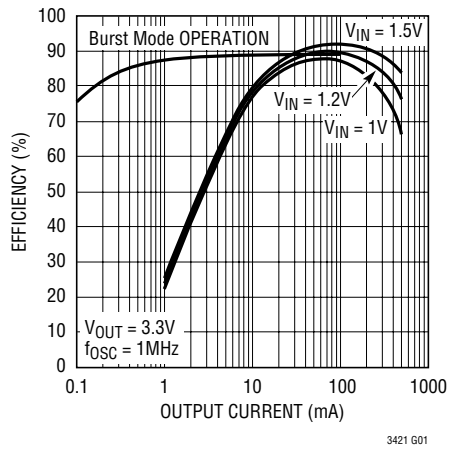


TYPICAL APPLICATION

Single Cell to 3.3V at 500mA with Secondary Cell Backup During Shutdown. LOWBAT and VREF Output are Enabled



Single Cell to 3.3V Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1371/LT1371HV	3A (ISW), 500kHz, High Efficiency Step-Up DC/DC Converters	VIN: 2.7V to 30V, VOUT(MAX): 35V/42V, IQ: 4mA, ISD: <12µA, DD, T0220-7, S20
LTC3400/LTC3400B	600mA (ISW), 1.2MHz, Synchronous Step-Up DC/DC Converters	92% Efficiency, VIN: 0.85V to 5V, VOUT(MAX): 5V, IQ: 19µA/300µA, ISD: <1µA, ThinSOT
LTC3401	1A (ISW), 3MHz, Synchronous Step-Up DC/DC Converter	97% Efficiency, VIN: 0.5V to 5V, VOUT(MAX): 5.5V, IQ: 38µA, ISD: <1µA, MS10
LTC3402	2A (ISW), 3MHz, Synchronous Step-Up DC/DC Converter	97% Efficiency, VIN: 0.5V to 5V, VOUT(MAX): 5.5V, IQ: 38µA, ISD: <1µA, MS10
LTC3425	5A (ISW), 8MHz, 4-Phase Synchronous Step-Up DC/DC Converter	95% Efficiency, VIN: 0.5V to 4.5V, VOUT(MAX): 5.25V, IQ: 12µA, 8MHz, Low Ripple in QFN