

M50940-XXXSP/FP, M50941-XXXSP/FP PRELIMINARY (M50945-XXXSP/FP) M50945-XXXSP/FP

Notice: These are not a final specification. Some parametric limits are subject to change.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50940-XXXSP, the M50941-XXXSP and the M50945-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 64-pin shrink plastic molded DIP.

These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50940-XXXSP, the M50941-XXXSP and the M50945-XXXSP are noted below. The following explanations apply to the M50940-XXXSP. Specification variations for other chips, these are noted accordingly.

Type name	ROM size	RAM size
M50940-XXXSP	4096 bytes	128 bytes
M50941-XXXSP	8192 bytes	192 bytes
M50945-XXXSP	16384 bytes	256 bytes

The differences between the M50940-XXXSP and the M50940-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

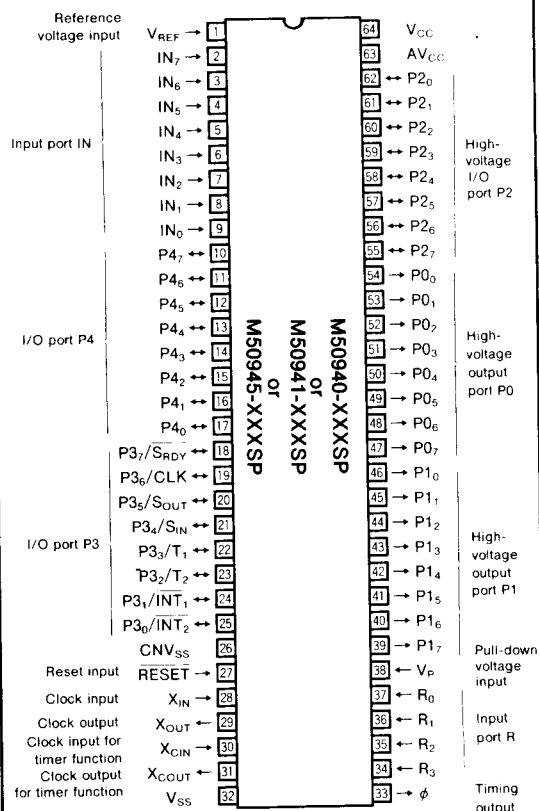
FEATURES

- Number of basic instructions 69
- Instruction execution time
..... $2\mu s$ (minimum instructions at 4MHz frequency)
- Single power supply $f(X_{IN})=4MHz$ $5V \pm 10\%$
 $f(X_{IN})=1MHz$ $3 \sim 5.5V$
- Power dissipation
normal operation mode (at 4MHz frequency) 15mW
low-speed operation mode (at 32kHz frequency for clock function) 0.3mW
- Subroutine nesting 64 levels (M50940)
96 levels (M50941, M50945)
- Interrupt 8 types, 5 vectors
- 8-bit timer 3 (2 when used as serial I/O)
- 16-bit timer 1 (Two 8-bit timers make one set)
- Programmable I/O ports (Ports P3, P4) 16
- Input ports (Ports IN, R) 12
- High-voltage output ports (Ports P0, P1) 16
- High-voltage programmable I/O ports (Port P2) 8
- Serial I/O (8-bit) 1
- A-D conversion 8-bit, 8 channel
- PWM function 1
- Two clock generator circuits
(One is for main clock, the other is for clock function)

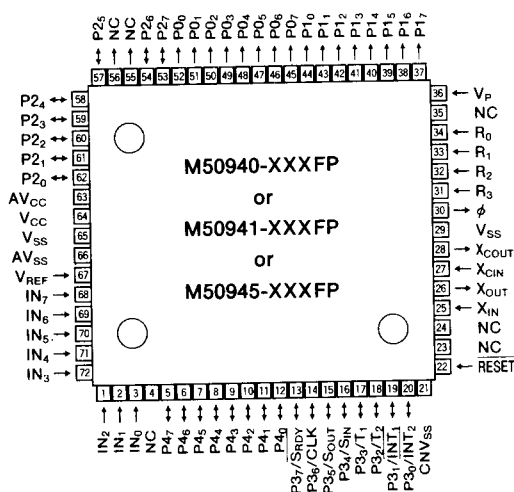
APPLICATION

Microwave oven, Air conditioner, Fan heater
Office automation equipment, Copying machine, Medical instruments
VCR, TV, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B



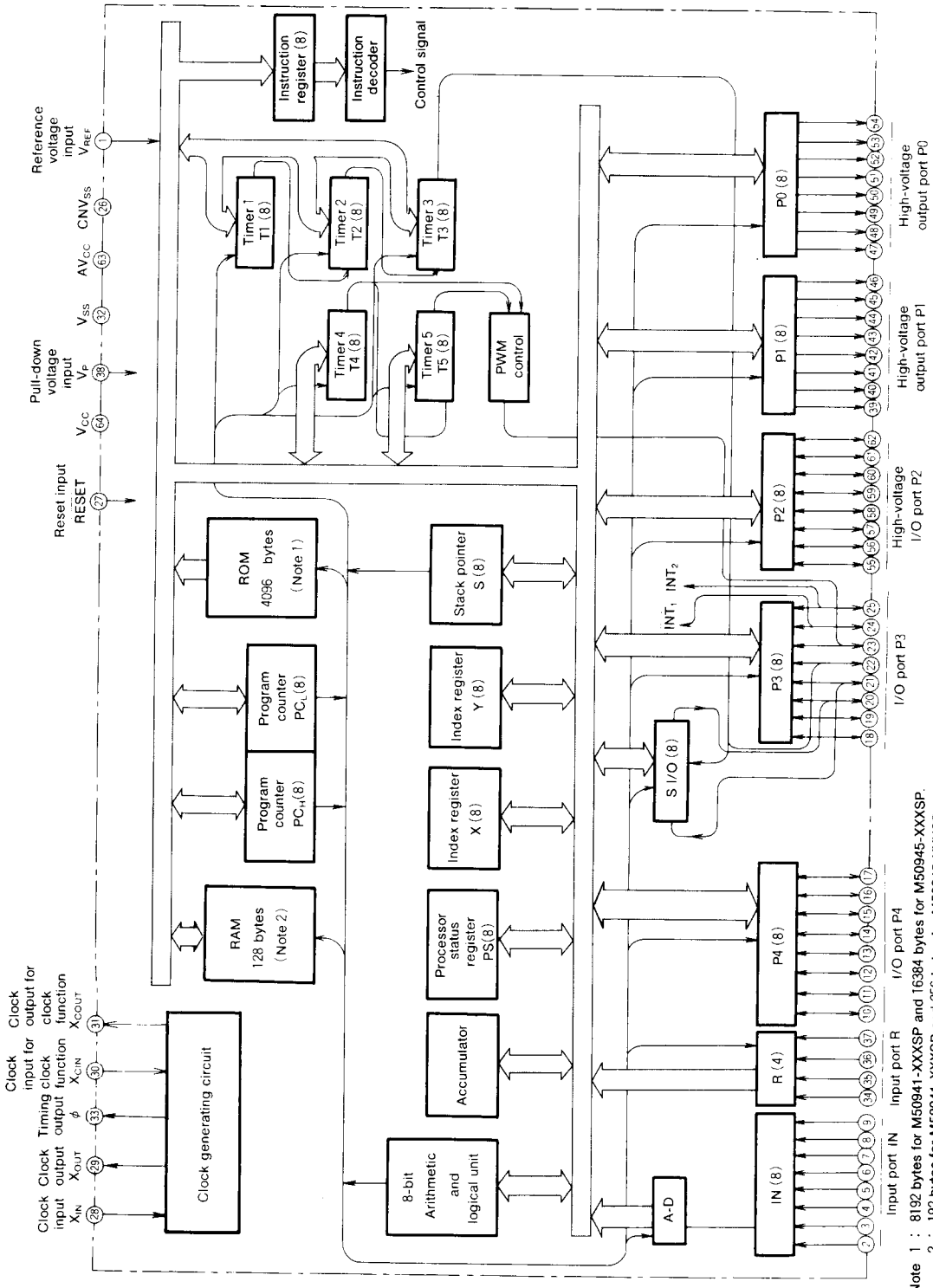
Outline 72P6

NC : No connection

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M50940-XXXSP BLOCK DIAGRAM



Note 1 : 8192 bytes for M50941-XXXSP and 16384 bytes for M50945-XXXSP.
 2 : 192 bytes for M50941-XXXSP and 256 bytes for M50945-XXXSP.

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FUNCTIONS OF M50940-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency)
Clock frequency			4.2MHz (main clock input), 32kHz (for clock function)
Memory size	ROM		4096bytes (8192bytes for M50941-XXXSP 16384 bytes for M50945-XXXSP)
	RAM		128bytes (192bytes for M50941-XXXSP 256 bytes for M50945-XXXSP)
Input/Output ports	P0, P1	Output	8-bit×2
	P2	I/O	8-bit×1
	P3, P4	I/O	8-bit×2
	IN	Input	8-ch analog input (This port is in common with 8-bit parallel digital input)
	R	Input	4-bit×1
Serial I/O			8-bit×1
Timers			8-bit timer×3, (2 when serial I/O is used)
Subroutine nesting			16-bit timer×1, (combination of two 8-bit timers)
Interrupt			64 Levels (max.) (96 Levels (max.) for M50941-XXXSP and M50945-XXXSP)
Clock generating circuit			Two external interrupts, three timer interrupts (or two timers, one serial I/O)
Supply voltage			Two built-in circuits (ceramic or quartz crystal oscillator)
Power dissipation			5V±10% (at f(X _{IN})=4MHz), 3.0~5.5V (at f(X _{IN})≤1.0MHz)
Input/Output characteristics	At high-speed operation		15mW (at f(X _{IN})=4MHz)
	At low-speed operation		0.3mW (at f(X _{CIN})=32kHz)
	At stop mode		1μA (at clock stop)
Memory expansion	Input/Output voltage		5V (port P3, P4)
	Output current		V _{CC} -36V (port P0, P1, P2)
			-12mA (port P0, P1, P2: high-voltage P-channel open drain output)
Operating temperature range			-5~-+10mA (port P3, P4: CMOS tri-state output)
Device structure			Possible
Package			-10~70℃
Device structure			CMOS silicon gate
Package			64-pin shrink plastic molded DIP
Package			72-pin plastic molded QFP

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PIN DESCRIPTION

Pin	Name	Input/ output	Functions
V_{CC} , V_{SS}	Supply voltage		Power supply inputs $5V \pm 10\%$ to V_{CC} , and 0V to V_{SS} .
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS} .
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P0, P1 and P2.
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than $2\mu s$ (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open. This clock can be used as a program controlled the system clock.
X_{COUT}	Clock output for clock function	Output	
$P0_0 \sim P0_7$	Output port P0	Output	Port P0 is an 8-bit output port. Output structure is high-voltage P-channel open drain. A pull-down transistor is built-in between the V_P pin and this port. At reset, this port is set to a "L" level.
$P1_0 \sim P1_7$	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0.
$P2_0 \sim P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is P-channel open drain. A pull-down transistor is built-in between the V_P pin and this port.
$P3_0 \sim P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port with CMOS tri-state output. The other functions are basically the same as port P2. $P3_0$, $P3_1$, $P3_2$ and $P3_3$ pins are in common with $\overline{INT_2}$, $\overline{INT_1}$, T_2 , and T_1 , respectively. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{SRDY}$, CLK, S_{OUT} , and S_{IN} , pins, respectively.
$P4_0 \sim P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port with CMOS tri-state output. The other functions are basically the same as port P2.
$R_0 \sim R_3$	Input port R	Input	Port R is a 4-bit input port.
$IN_0 \sim IN_7$	Analog input port IN	Input	Port IN is the analog input pin to the A-D converter. It also has a dual function and works as a normal input port.
AV_{CC}	Voltage input for A-D		This is the power supply input pin for the A-D converter.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.

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BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50940-XXXSP is shown in Figure 1. Addresses $F000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 4096 bytes (8192 bytes for M50941-XXXSP and 16384 bytes for M50945-XXXSP). Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and inter-

rupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required.

The RAM, I/O port, timer, etc. addresses are already assigned for the zero page. Addresses 0000_{16} to $007F_{16}$ are assigned for the built-in RAM which consists of 128 bytes (192 bytes for M50941-XXXSP and 256 bytes for M50945-XXXSP) of static RAM. This RAM is used as the stack during subroutine calls and interrupts, in addition to data storage.

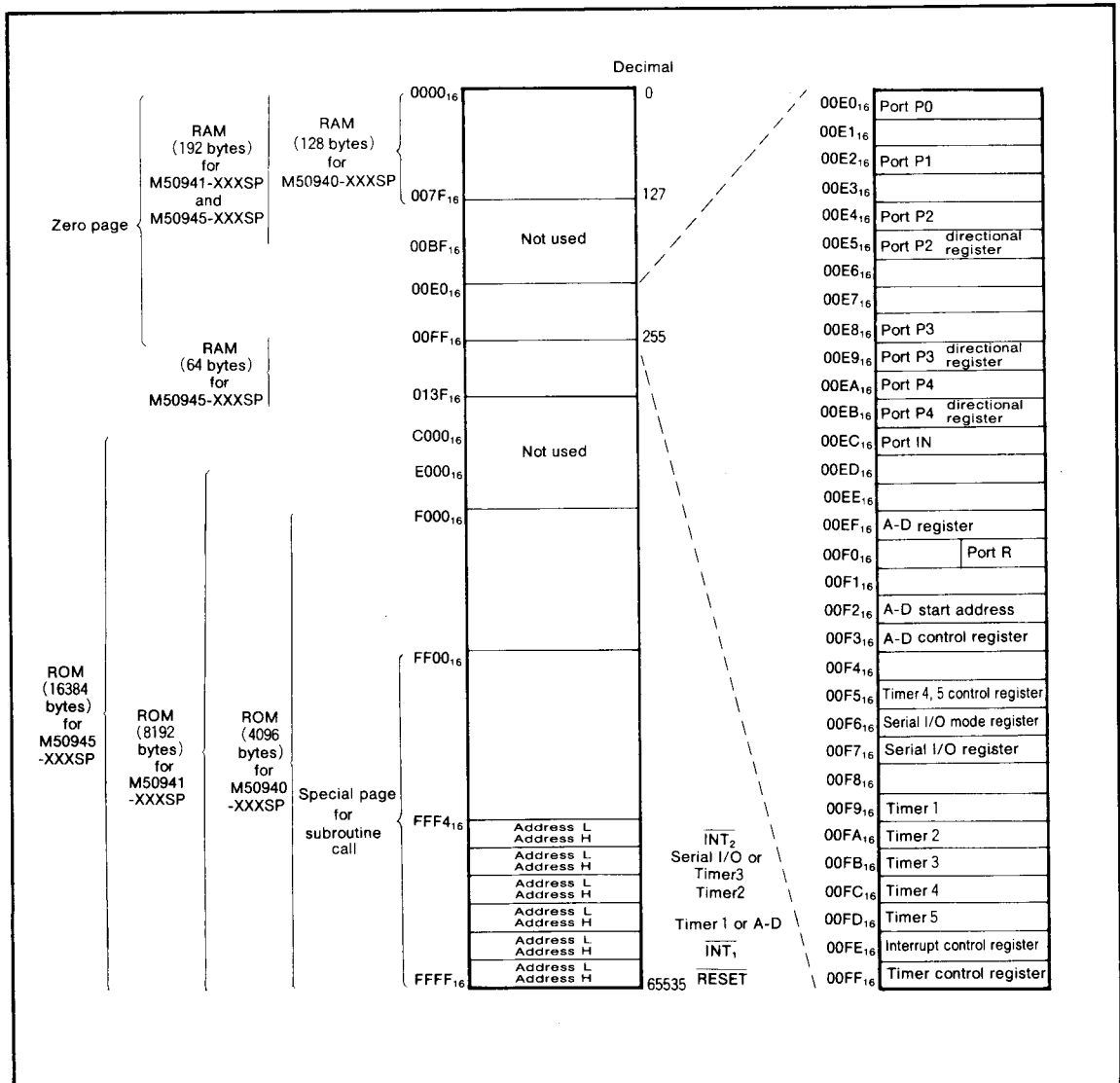


Fig.1 Memory map

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CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, input/output, etc., is executed mainly through the accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register. In the index register X addressing mode, the value of the OPERAND added to the contents of the index register X specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register. In the index register Y addressing mode, the value of the OPERAND added to the contents of the index register Y specifies the real address.

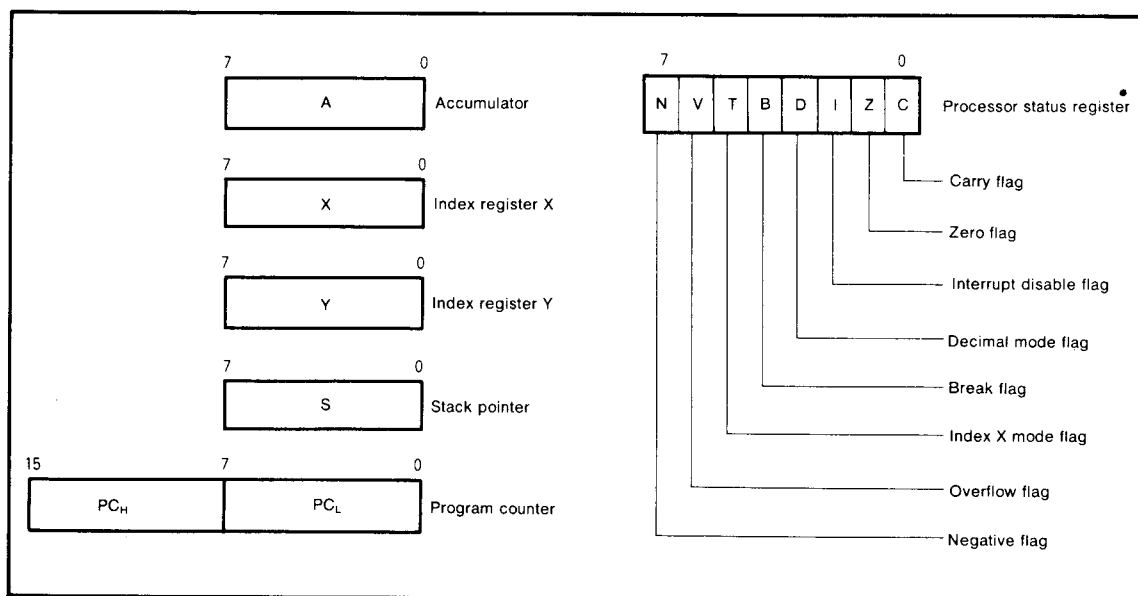


Fig.2 Register structure

STACK POINTER (S)

The stack pointer is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

When an interrupt occurs, the higher 8 bits of the program counter is pushed into the stack first, the stack pointer is decremented, and then the lower 8 bits of the program counter is pushed into the stack. Next the contents of the processor status register is pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter and processor status register data is popped off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically, so a Push Accumulator instruction (PHA) is provided to execute this function. Restoring the accumulator to its previous value is accomplished by the Pop Accumulator instruction (PLA). It is executed in the reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed and popped to and from the stack with the PHP and PLP instructions, respectively.

During a subroutine call, only the Program Counter is pushed into the stack. Therefore, any registers that should not be destroyed should be pushed into the stack manually. To return from a subroutine call, the RTS instruction is used.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The 8-bit PS is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic Logic Unit (ALU) immediately after an operation. It is also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "0". If the result is not zero, the zero flag will be set to "1".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt is accepted, this flag is automatically set to "1" to prevent from other interrupts until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the B flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the T flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or -128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the V flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the N flag. There are no instructions for directly setting or resetting the N flag.

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INTERRUPT

The M50940-XXXSP can be interrupted from eight sources; $\overline{INT}_1$, timer 1 or A-D, timer 2, timer 3 or serial I/O, and the $\overline{INT}_2$ or BRK instruction.

The value of bit 2 of the serial I/O mode register (address 00F6₁₆) determines whether the interrupt is from timer 3 or from serial I/O. When bit 2 is "1" the interrupt is from serial I/O, and when bit 2 is "0" the interrupt is from timer 3. Also, when bit 2 is "1", parts of port 3 are used for serial I/O. Bit 3 of the A-D control register (address 00F3₁₆) determines if an interrupt is from timer 1 or from the A-D. When bit 3 is "0", the interrupt is from timer 1, when bit 3 is "1" the interrupt is from the A-D. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as an interrupt.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag (I) is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The Reset interrupt is the highest priority interrupt and can never be inhibited. Except for the Reset interrupt, all interrupt are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be

controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0". The interrupt request bits are set when the following conditions occur:

- (1) When the $\overline{INT}_1$ or $\overline{INT}_2$ pins go from "H" to "L"
- (2) When the contents of timer 1, timer 2, timer 3 (or the serial I/O counter) go to "0".

These request bits can be reset by the program but can not be set.

Since the BRK instruction and the $\overline{INT}_2$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT}_2$ generated the interrupt.

Table 1. Interrupt vector address and priority.

Interrupt	Priority	Vector address
RESET	1	FFFF ₁₆ , FFFE ₁₆
$\overline{INT}_1$	2	FFFD ₁₆ , FFFC ₁₆
Timer 1 or A-D	3	FFFB ₁₆ , FFFA ₁₆
Timer 2	4	FFF9 ₁₆ , FFF8 ₁₆
Timer 3 or serial I/O	5	FFF7 ₁₆ , FFF6 ₁₆
$\overline{INT}_2$ (BRK)	6	FFF5 ₁₆ , FFF4 ₁₆

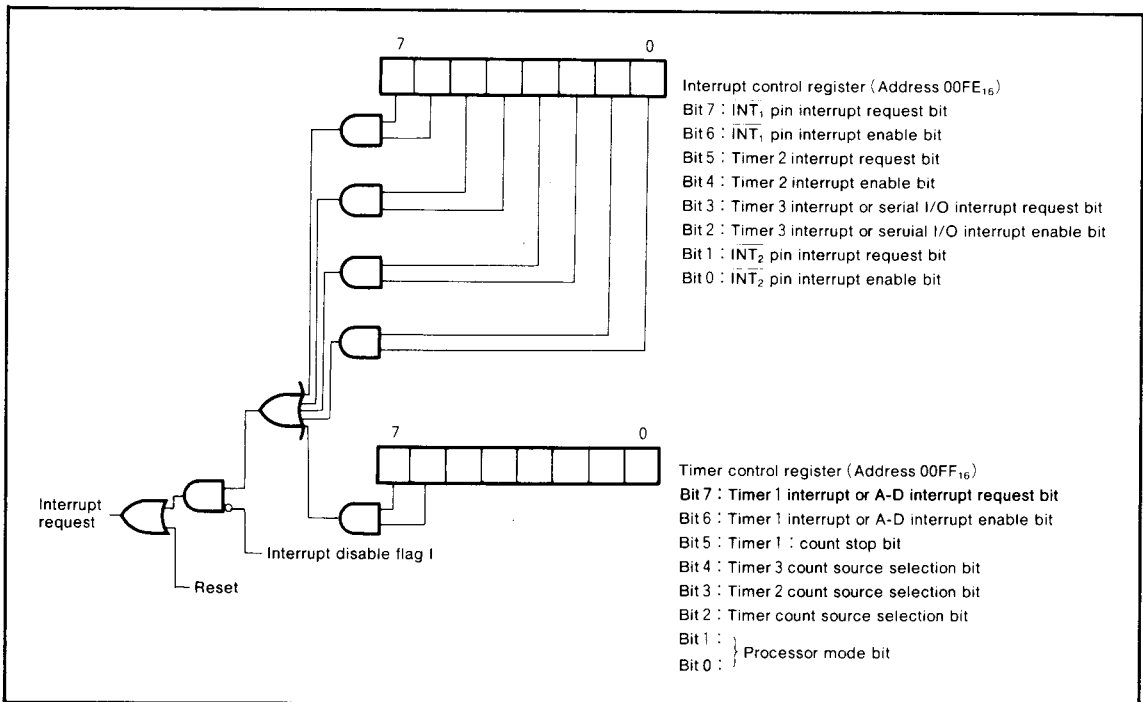


Fig.3 Interrupt control

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TIMER

The M50940-XXXSP has five timers; timer 1, timer 2, timer 3, timer 4 and timer 5. Since P_3 (in serial I/O mode) and timer 3 use some of the same architecture, they cannot be used at the same time (see serial I/O section). The count source for each timer can be selected by using bit 2, 3 and 4 of the timer control register (address $00FF_{16}$), as shown in Figure 5. For more details about timer 4 and timer 5, see the PWM section.

A block diagram of timer 1 through 5 is shown in Figure 5. All of the timers are down count timers and have 8-bit latches. When a timer counter reaches "0", the contents of the reload latch are loaded into the timer and the next count pulse is input to a timer. The division ratio of the timers is $1/(n+1)$, where n is the contents of the timer latch.

The timer interrupt request bit is set to "1" at the next clock pulse after the timer reaches "0". The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see Interrupt section). The starting/stopping of timer 1 can be controlled by bit 5 of the timer control register. If bit 5 (address $00FF_{16}$) is "0", the timer starts counting and when bit 5 is "1", the timer stops.

After a STP instruction is executed, timer 2, timer 1, and the clock (ϕ divided by 4) are connected in series (regardless of the status of the 2 through 3 of the timer control register). This state is canceled if the timer 2 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 1, count stop bit), and bit 4 of interrupt control register (timer 2 interrupt enable bit) bit 6 of the timer control register (timer 1 interrupt enable bit) must be set to "0". For more

details on the STP instruction, refer to the oscillation circuit section.

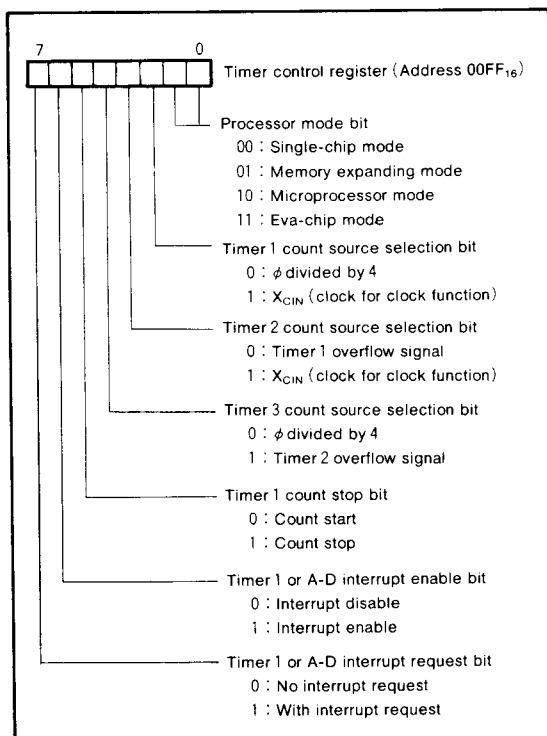


Fig.4 Structure of timer control register

PWM

The M50940-XXXSP has a pulse width modulated (PWM) output control circuit. The circuit outputs a variable duty cycle signal that can be used for a programmable pulse width and frequency. Timers 4 and 5 are used for the PWM. The control of these timers is explained in Figure 6 and the rectangular waveform is shown in Figure 7.

At reset, the PWM output is in a floating state. When timers 4 and 5 are not used for PWM control, they can be cascaded and used as a 16-bit timer. However, when used as a 16-bit timer, the interrupt function (such as timer 1 through timer 3) cannot be used.

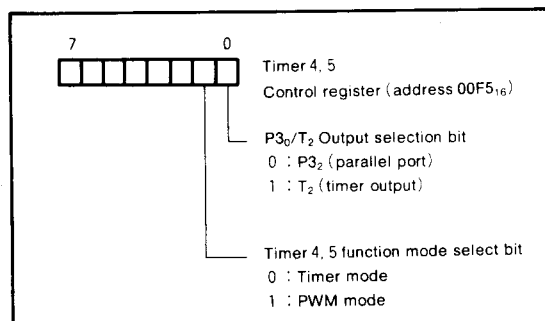


Fig.6 Structure of timer 4, 5 control register

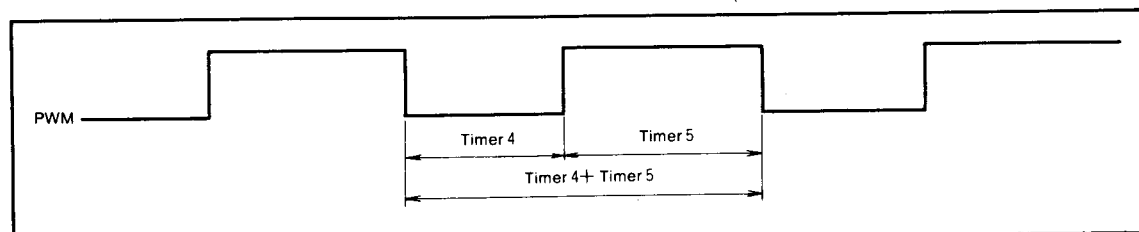


Fig.7 PWM rectangular wave form

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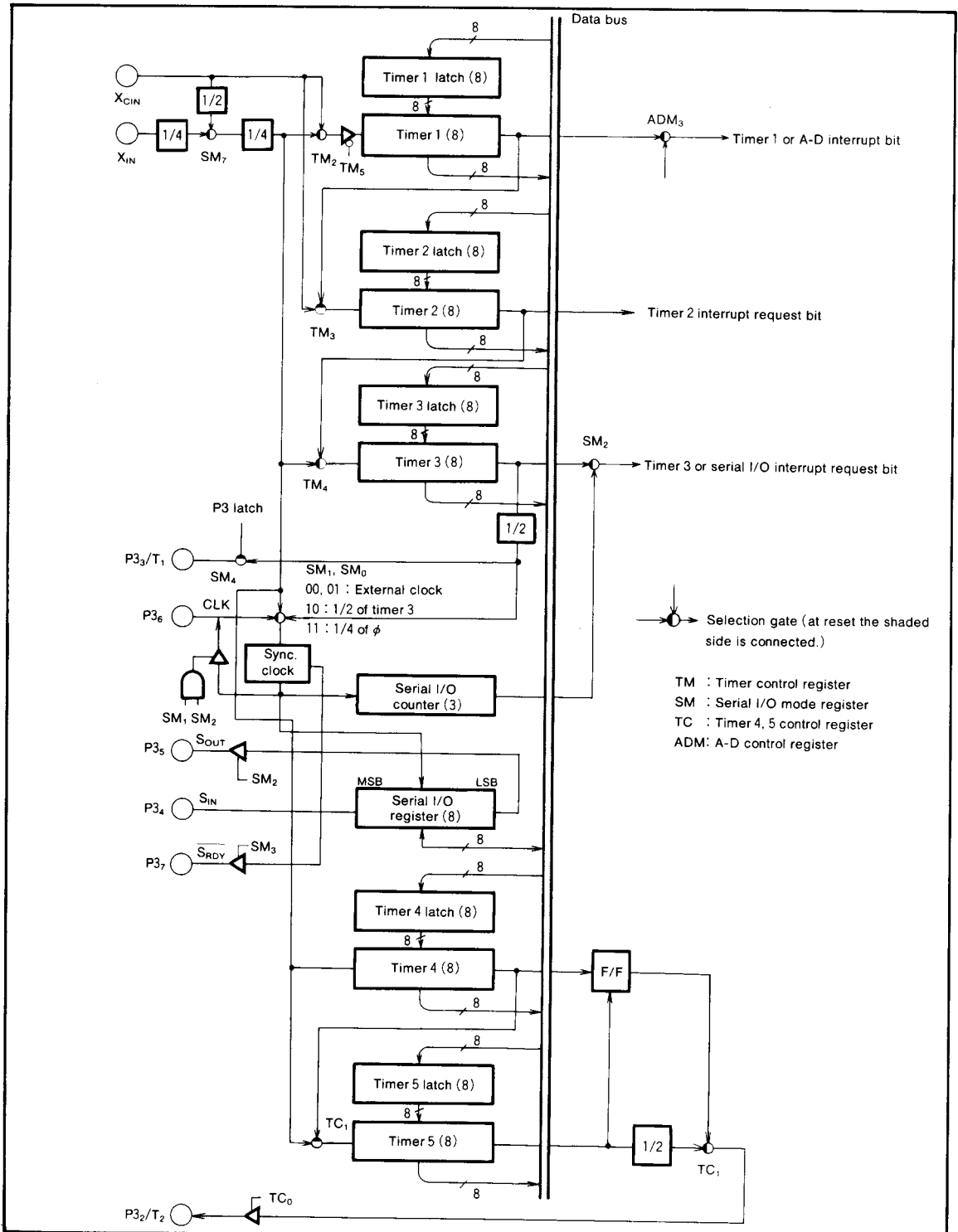


Fig.5 Block diagram of timer 1 through 5

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SERIAL I/O

A block diagram of the serial I/O is shown in Figure 8. In the serial I/O mode, the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O (S_{OUT} , S_{IN}) pins are used as P3₇, P3₆, P3₅, and P3₄, respectively.

The serial I/O mode register (address 00F6₁₆) is an 8-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source. When these bits are [00] or [01], an external clock from P3₆ is selected. When these bits are [10], the overflow signal (from timer 3) divided by two becomes the synchronous clock. Therefore, changing the tim-

er period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 (ie. 4 μ s at 4MHz) becomes the clock.

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", P3₆ becomes an I/O pin of the synchronous clock. When an internal synchronous is selected, the clock is output from P3₆. If an external synchronous clock is selected, the clock is input to P3₆. And P3₅ will be a serial output and P3₄ will be a serial input. To use P3₄ as a serial input, set the directional register bit which corresponds to P3₄ to "0". For more information on the directional register, refer to the I/O pin section.

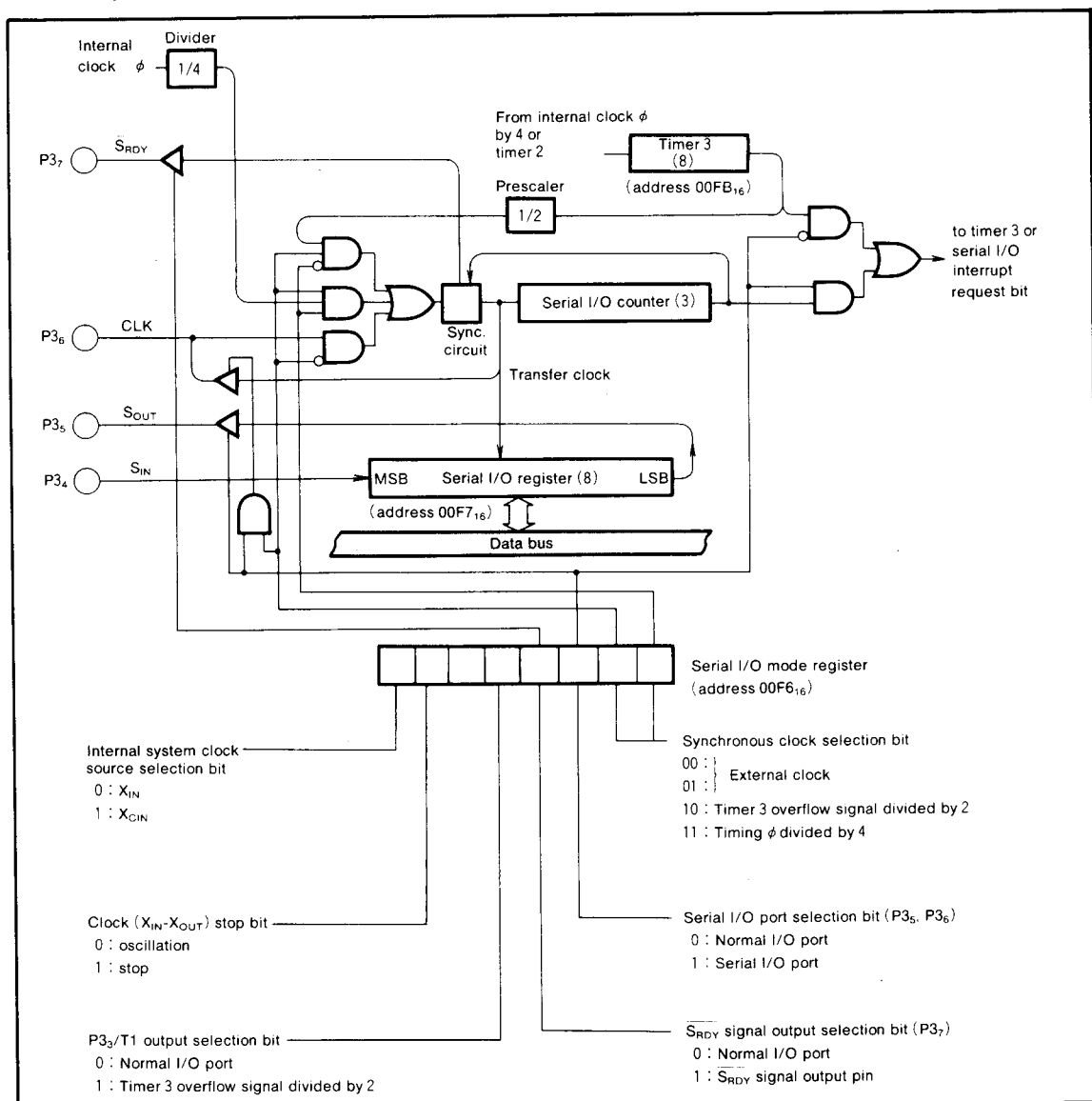


Fig.8 Block diagram of serial I/O

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To use the serial I/O, bit 2 needs to be set to "1", if it is "0" P3₆ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 3. bit 3 determines if P3₇ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 3="0").

The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50940-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial

data is output to P3₅. During the rising edge of this clock, data can be input from P3₄ and the data in the serial I/O register will be shifted 1-bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External clock—If an external clock is used, the interrupt request will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 9, and connections between two M50940-XXXSPs are shown in Figure 10.

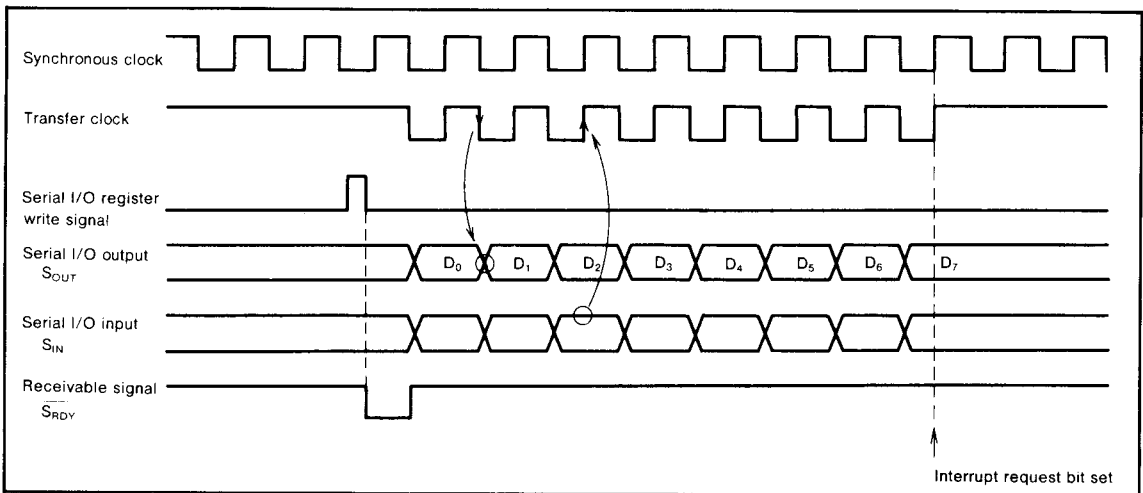


Fig.9 Serial I/O timing

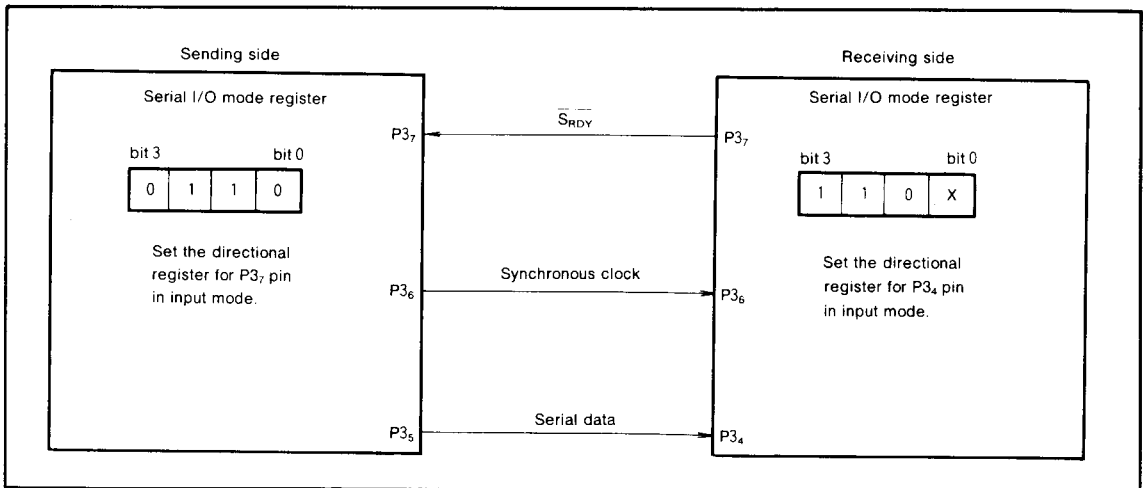


Fig.10 Example of serial I/O connection

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RESET CIRCUIT

The M50940-XXXSP is reset according to the sequence shown in Figure 15. And starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address when the $\overline{\text{RESET}}$ pin is held at "L" level for more than $2\mu\text{s}$ while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level.

	Address	
(1) Port P0 register	($E0_{16}$) ...	0 0 ₁₆
(2) Port P1 register	($E2_{16}$) ...	0 0 ₁₆
(3) Port P2 directional register	($E5_{16}$) ...	0 0 ₁₆
(4) Port P3 directional register	($E9_{16}$) ...	0 0 ₁₆
(5) Port P4 directional register	(EB_{16}) ...	0 0 ₁₆
(6) Serial I/O mode register	($F6_{16}$) ...	0 0 ₁₆
(7) A-D control register	($F3_{16}$) ...	1 0 0 0 0 0
(8) Timer 4, 5 control register	($F5_{16}$) ...	0 0
(9) Interrupt control register	(FE_{16}) ...	0 0 ₁₆
(10) Timer control register	(FF_{16}) ...	0 0 ₁₆
(11) Interrupt disable flag for processor status register	(PS) ...	1
(12) Program counter	(PC_H) ...	Contents of address $FFFF_{16}$
	(PC_L) ...	Contents of address $FFFE_{16}$

Since the contents of both registers other than those listed above (including timer 1, timer 2, timer 3, and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values.

Fig.13 Internal state of microcomputer at reset

The internal initializations following reset are shown in Figure 13.

An example of the reset circuit is shown in Figure 14.

When the power on reset is used, the $\overline{\text{RESET}}$ pin must be held "L" until the oscillation of X_{IN} - X_{OUT} becomes stable.

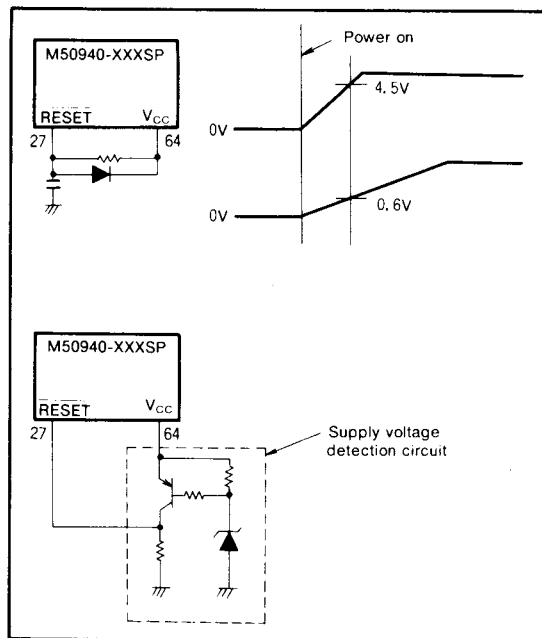


Fig.14 Example of reset circuit

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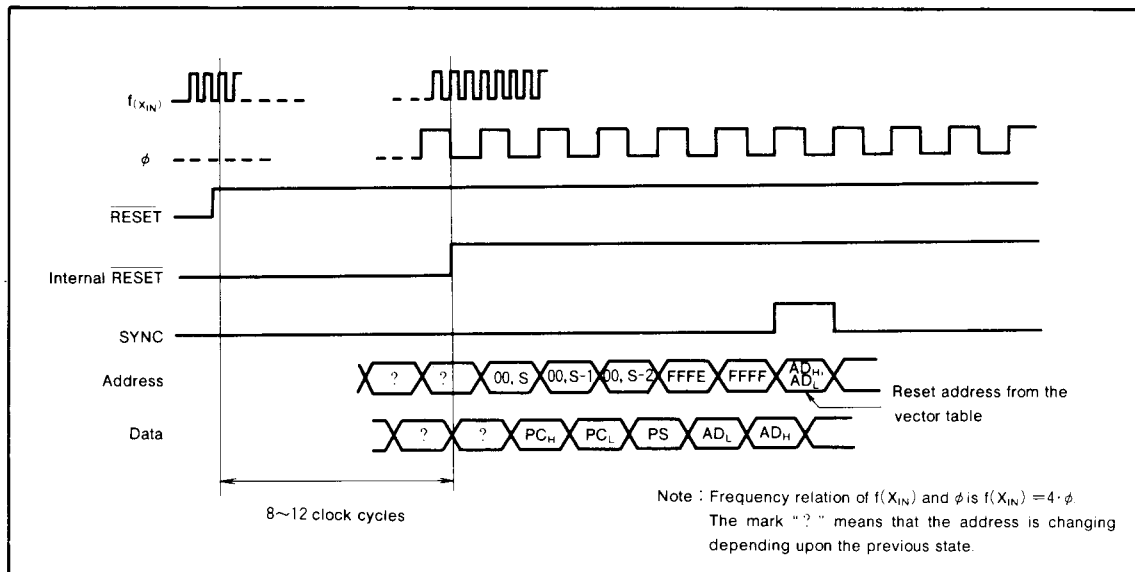


Fig.15 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit output port with P-channel open drain and high voltage outputs (V_{CC} -36V). Each pin has a built-in pull-down transistor connected to V_P . As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$.

Depending on the status of the processor status register (bit 0 and bit 1 of address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode, and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode section.

(2) Port P1

In the single-chip mode, Port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode section.

(3) Port P2

Port P2 is an 8-bit I/O port with P-channel open drain outputs. As shown in the memory map of Figure 1, port P2 can be accessed as memory at address $00E4_{16}$ of zero page. Port P2 has a direction register (address $00E5_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a

previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are V_{PP} level and the signal levels can thus be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

(4) Port P3

Port P3 is an 8-bit I/O port having CMOS outputs. Each pin is shared with serial I/O, timer overflow (T1, T2) and external interrupt input functions. These functions remain the same even if the device is used in other modes.

(5) Port P4

Port P4 is an 8-bit I/O port with CMOS outputs. During all modes except single chip mode, $P4_1$ and $P4_0$ function as both SYNC and R/W outputs as well as I/O ports (see processor mode section).

(6) Port R

Port R is a 4-bit input port.

(7) Port IN

Port IN is an 8-bit input port to the A-D converter. It can also be used as an input port by reading the input data into address $00EC_{16}$. However, this port cannot be read during A-D conversion.

(8) Clock ϕ output pin

This is the timing output pin. When selected the main clock (X_{IN} - X_{OUT}) as the internal system clock, the clock frequency divided by four is outputted. However, when selected the clock for clock function (X_{CIN} - X_{COUT}), the clock frequency divided by two is outputted.

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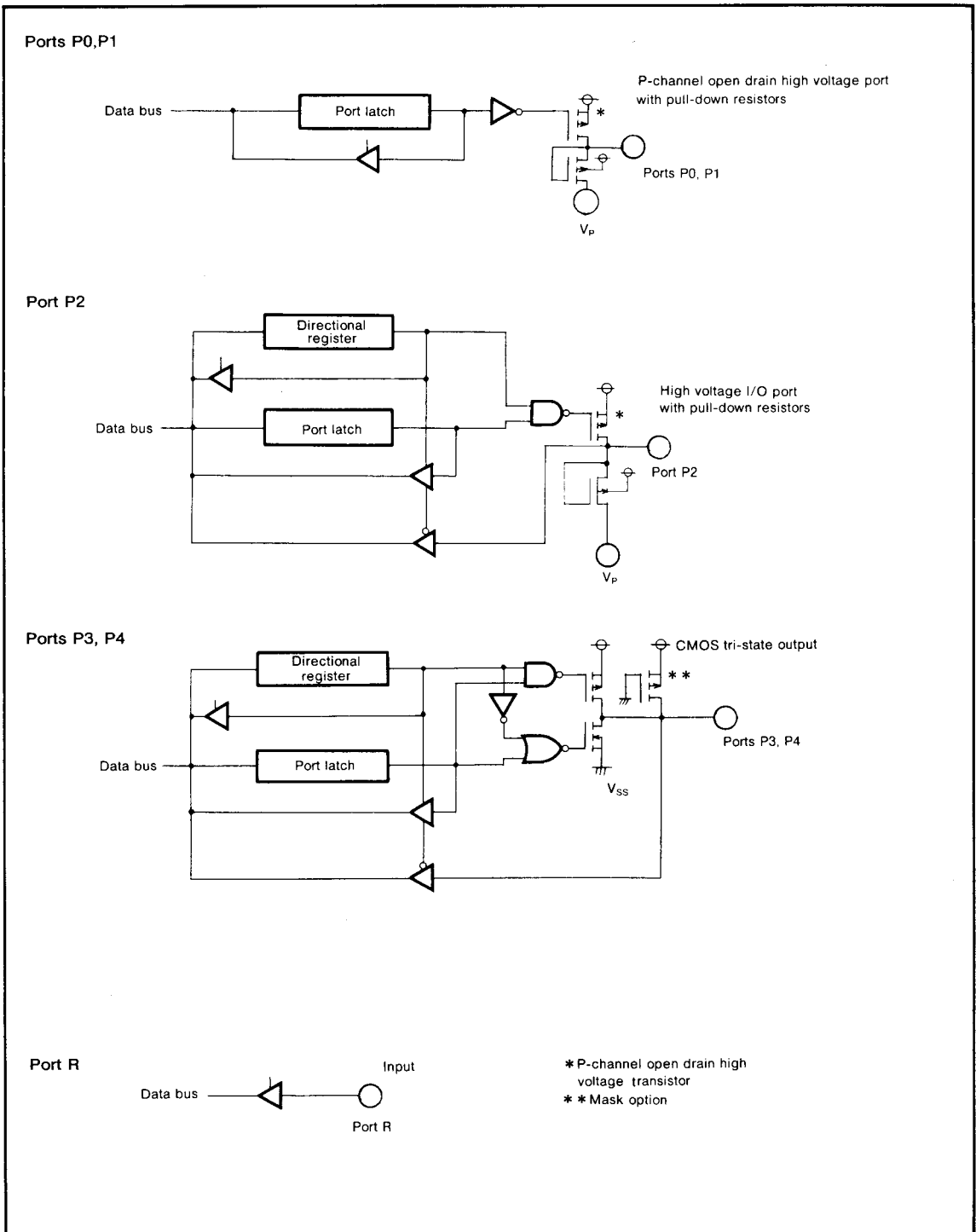


Fig.16 Block diagram of port P0~P4 and port R (single-chip mode)

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PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 of address $00FF_{16}$), four different operation modes can be selected; single chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, $P0 \sim P2$ can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports. Figure 18 shows the functions of ports $P0 \sim P2$, and $P4$ corresponding to each mode.

The memory map of the single-chip mode is illustrated in Figure 1, and the other modes are shown in Figure 17. By connecting the CNV_{SS} to V_{SS} , all four modes can be selected through software by changing the processor mode register. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

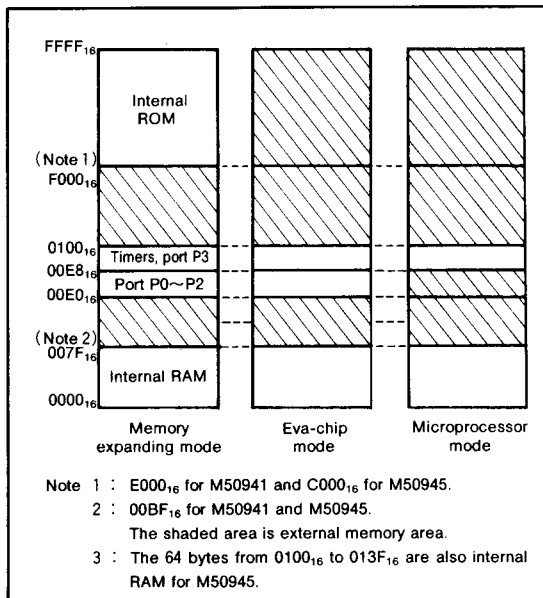


Fig.17 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS} . Ports $P0 \sim P4$ will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

The lower 8 bits of address data for port $P0$ is output when ϕ goes to the "H" state. When ϕ goes to the "L" state, $P0$ retains its original I/O functions.

Port $P1$'s higher 8 bits of address data are output when ϕ goes to the "H" state and as it changes back to the "L" state it retains its original I/O functions.

Port $P2$ retains its original output functions while ϕ is at the "H" state, and works as a data bus of $D_7 \sim D_0$ (including instruction code) while at the "L" state.

Pins $P4_1$ and $P4_0$ output the SYNC and $R/\bar{W}$ control signals, respectively while ϕ is in the "H" state.

When in the "L" state, $P4_1$ and $P4_0$ retain their original I/O functions.

The $R/\bar{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

In this mode, port $P0$ and $P1$ are used as the system address bus and the original function of the I/O pin is lost. Port $P2$ becomes the data bus ($D_7 \sim D_0$) and loses its normal I/O functions. Port $P4_1$ and $P4_0$ become the SYNC and $R/\bar{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]

When 10V is supplied to the CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. This mode has almost the same function as the memory expanding mode except that it needs all its programs to come from the outside (including ROM programs). The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

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TM₁ TM₀ Mode Port	0	0	1	1
	0	1	1	0
	Single-chip mode	Memory expanding mode	Eva-chip mode	Microprocessor mode
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	
Port P4			Same as left	

Fig.18 Processor mode and functions of ports P0~P2, P4

Table 2. Relationship between CNV_{SS} Pin Input Level and Processor Mode

CNV _{SS}	Mode	Explanation
V _{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V _{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

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CLOCK GENERATING CIRCUIT

The M50940-XXXSP has two internal clock generating circuit. Figure 21 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ . Bit 7 of serial I/O mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN} .

Figure 19 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacture's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input form the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 20.

The M50940-XXXSP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 1 and timer 2 are forcibly connected and $\phi/4$ is selected as timer 1 input. Before executing the STP instruction, appropriate values must be set in timer 1 and timer 2 to enable the oscillator to stabilize when restarting oscillation. Before executing the STP instruction, the timer 1 count stop bit must be set to supply ("0"), timer 1 interrupt enable bit and timer 2 interrupt enable bit must be set to disable ("0"), and timer 2 interrupt request bit must be set to no request ("0").

Oscillation is restarted (release the stop mode) when $\overline{INT_1}$, $\overline{INT_2}$, or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 2 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes because no wait time is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock ($120\mu A$ max. at $f(X_{CIN}) = 32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of serial I/O mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 22 shows the transition of states for the system clock.

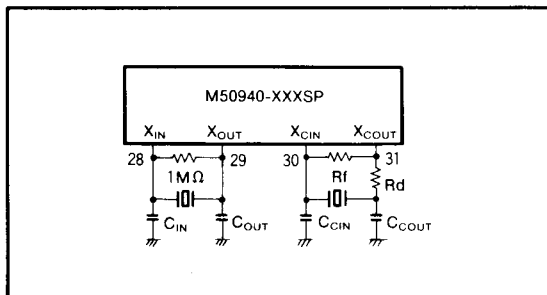


Fig.19 External ceramic resonator circuit

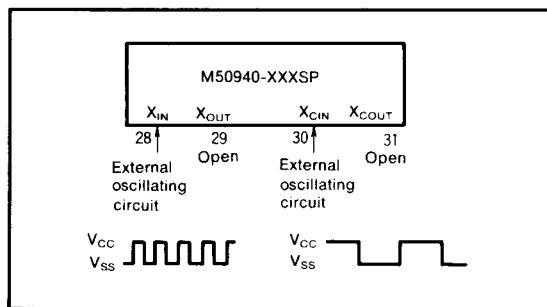


Fig.20 External clock input circuit

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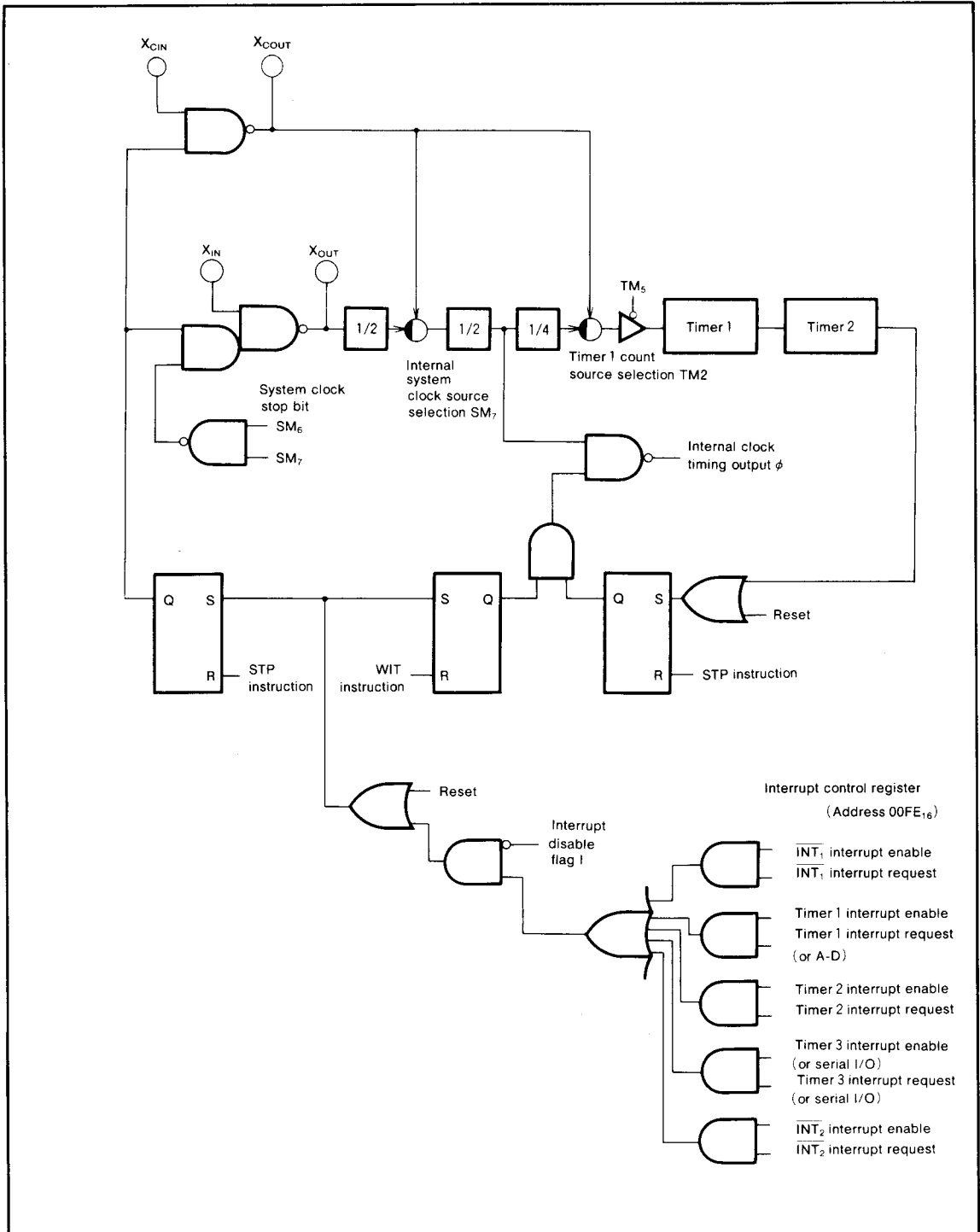


Fig.21 Block diagram of clock generating circuit

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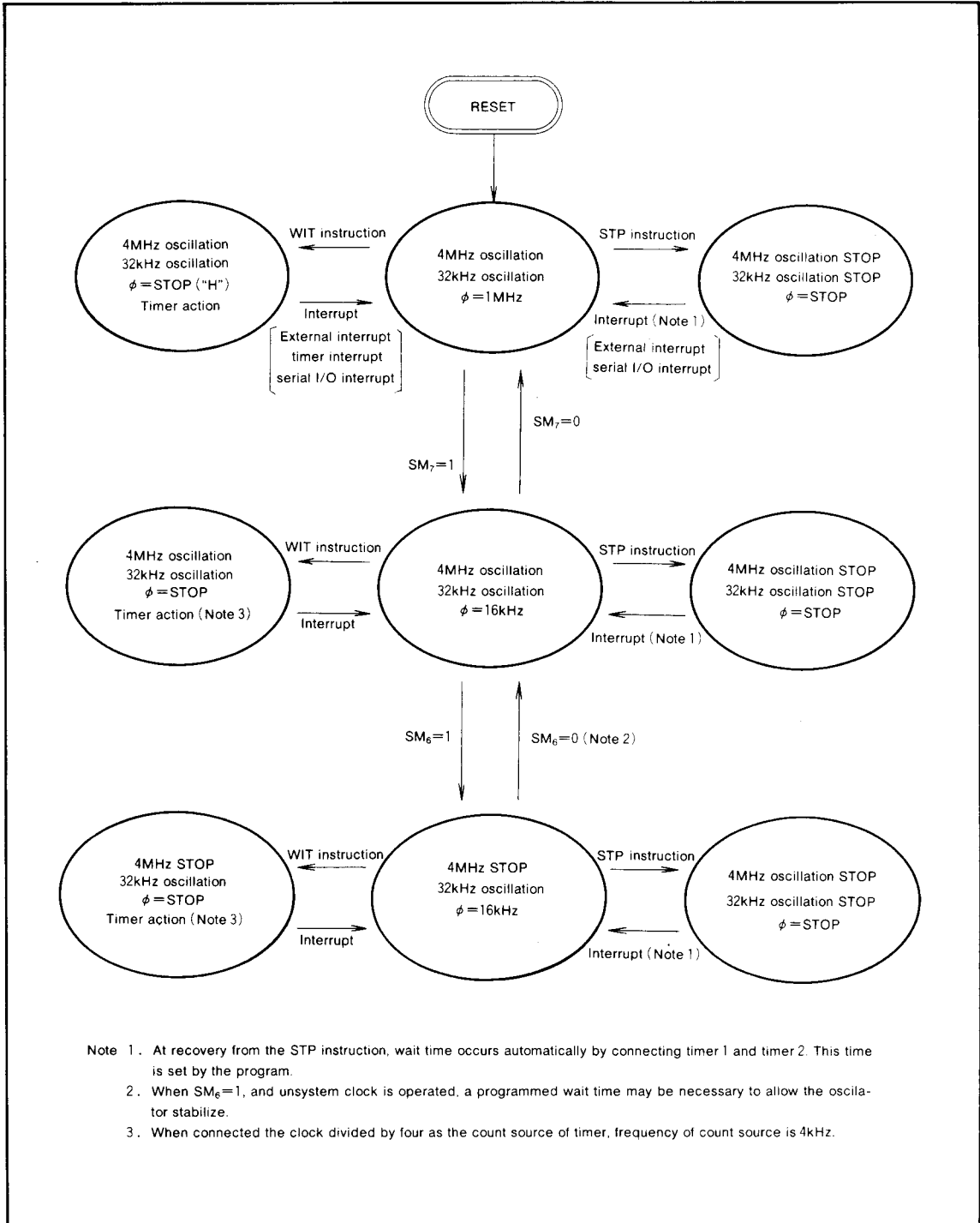


Fig.22 Transition of states for the system clock

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<An example of flow for system>



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PROGRAMMING NOTES

- (1) The frequency ratio of the timer is $1/(n+1)$. ($n=0\sim 255$)
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) When the timer 1, timer 2, or timer 3 is input the clock except $\phi/4$ or it divided by timer, read the contents of these timers either while the input of these timers are not changing or after counting of timers are stopped.
- (4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (5) A NOP instruction must be used after the execution of a PLP instruction.
- (6) Notes on serial I/O
 - ① Set "0" in the serial I/O interrupt enable bit (bit 2 of address $00FE_{16}$) before setting the serial I/O mode.
 - ② Insert at least one instruction and set "0" in the serial I/O interrupt request bit (bit 3 of address $00FE_{16}$) after setting the serial I/O mode.
 - ③ Set "1" in the serial I/O interrupt enable bit after the operation described in ②.
- (7) The timer 1 and the timer 2 must be set the necessary value immediately before the execution of a STP instruction.
- (8) Notes on A-D conversion
 - ① Set "0" in the A-D interrupt enable bit (bit 6 of address $00FF_{16}$) before setting A-D conversion.
 - ② Insert at least one instruction and set "0" in the A-D interrupt request bit (bit 7 of address $00FF_{16}$) after setting the A-D conversion.
 - ③ Set "1" in the A-D interrupt enable bit after the operation described in ②.
 - ④ Set "0" in bit 3 of the A-D control register (address $00F3_{16}$) before using a STP instruction.
- (9) Notes on timer 4 and timer 5 using as watchdog timer
 - ① Do not use these timers when using STP instruction or stopping or switching the clock.
 - ② It does not operate correctly in some writing timing to timer 4 and timer 5.
- (10) The V_{REF} pin must be kept open or connected to V_{SS} at the low power dissipation mode.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM confirmation form
 - (2) mark specification form
 - (3) ROM data EPROM 3 sets
- Write the following option on the mask ROM confirmation form
- Port P3 pull-up transistor bit
 - Port P4 pull-up transistor bit

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} output transistors are at "OFF" state.	$-0.3 \sim 7$	V
V_P	Pull-down input voltage		$V_{CC} - 38 \sim V_{CC} + 0.3$	V
V_I	Input voltage CNV_{SS}		$-0.3 \sim 13$	V
V_I	Input voltage $R_0 \sim R_3, X_{IN}, X_{CIN}, RESET$		$-0.3 \sim 7$	V
V_I	Input voltage $P_3 \sim P_7, P_4 \sim P_7, IN_0 \sim IN_7, V_{REF}$		$-0.3 \sim V_{CC} + 0.3$	V
V_I	Input voltage $P_2 \sim P_7$		$V_{CC} - 38 \sim V_{CC} + 0.3$	V
V_O	Output voltage $P_3 \sim P_7, P_4 \sim P_7, X_{COUT}, X_{OUT}, \phi$		$-0.3 \sim V_{CC} + 0.3$	V
V_O	Output voltage $P_0 \sim P_7, P_1 \sim P_7, P_2 \sim P_7$		$V_{CC} - 38 \sim V_{CC} + 0.3$	V
P_d	Power dissipation	$T_a = 25^\circ C$	1000 (Note 1)	mW
$Topr$	Operating temperature		$-10 \sim 70$	$^\circ C$
$Tstg$	Storage temperature		$-40 \sim 125$	$^\circ C$

Note 1. 600mW for QFP type.

RECOMMEND OPERATING CONDITIONS

($V_{CC} = 5V \pm 10\%$, $T_a = -10 \sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	$f(X_{IN}) = 4MHz$	4.5	5	5.5	V
		$f(X_{IN}) \leq 1MHz$	3	5	5.5	
V_P	Pull-down supply voltage		$V_{CC} - 36$		V_{CC}	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P_3 \sim P_7, P_4 \sim P_7, IN_0 \sim IN_7, CNV_{SS}$		$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage $R_0 \sim R_3$		$0.4V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage $RESET, X_{IN}, X_{CIN}$		$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage $P_2 \sim P_7$		$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $P_3 \sim P_7, P_4 \sim P_7, IN_0 \sim IN_7, CNV_{SS}$		0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage $R_0 \sim R_3$		0		$0.12V_{CC}$	V
V_{IL}	"L" input voltage $RESET$		0		$0.12V_{CC}$	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		$0.16V_{CC}$	V
V_{IL}	"L" input voltage $P_2 \sim P_7$		$V_{CC} - 36$		$0.2V_{CC}$	V
$I_{OH(sum)}$	"H" sum output current $P_0 \sim P_7, P_1 \sim P_7, P_2 \sim P_7$				-120	mA
$I_{OH(sum)}$	"H" sum output current $P_3 \sim P_7, P_4 \sim P_7$				-30	mA
$I_{OL(sum)}$	"L" sum output current $P_3 \sim P_7, P_4 \sim P_7$				60	mA
$I_{OH(peak)}$	"H" peak output current $P_0 \sim P_7, P_1 \sim P_7, P_2 \sim P_7$				-24	mA
$I_{OH(peak)}$	"H" peak output current $P_3 \sim P_7, P_4 \sim P_7$				-10	mA
$I_{OL(peak)}$	"L" peak output current $P_3 \sim P_7, P_4 \sim P_7$				20	mA
$I_{OH(avg)}$	"H" average output current $P_0 \sim P_7, P_1 \sim P_7, P_2 \sim P_7$				-12	mA
$I_{OH(avg)}$	"H" average output current $P_3 \sim P_7, P_4 \sim P_7$				-5	mA
$I_{OL(avg)}$	"L" average output current $P_3 \sim P_7, P_4 \sim P_7$				10	mA
$f(X_{IN})$	Clock oscillating frequency	$V_{CC} = 5V$			4.3	MHz
		$V_{CC} = 3V$			1.1	
$f(X_{CIN})$	Clock oscillating frequency for clock function	$V_{CC} = 5V$			500	kHz
		$V_{CC} = 3V$			300	

- Note 1. The maximum "H" input voltage for CNV_{SS} is +12V.
2. The duty cycle for these oscillation frequency is 50%.
3. When the low speed mode is used, the clock input oscillation frequency for the timer must satisfy the following expression:

$$f(X_{CIN}) < f(X_{IN}) / 3$$

4. The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms cycle.
5. $f(X_{IN})$ must be less than 50kHz when the external clock is to be used.

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 25^\circ C$, $f(X_{IN}) = 4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P3_0 \sim P3_7, P4_0 \sim P4_7$	$V_{CC} = 5V, I_{OH} = -5mA$ $V_{CC} = 3V, I_{OH} = -1.5mA$	3 2			V
V_{OH}	"H" output voltage ϕ	$V_{CC} = 5V, I_{OH} = -2.5mA$ $V_{CC} = 3V, I_{OH} = -0.8mA$	3 2			V
V_{OH}	"H" output voltage $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7$	$V_{CC} = 5V, I_{OH} = -12mA$ $V_{CC} = 3V, I_{OH} = -3mA$	3 2			V
V_{OL}	"L" output voltage $P3_0 \sim P3_7, P4_0 \sim P4_7$	$V_{CC} = 5V, I_{OL} = 10mA$ $V_{CC} = 3V, I_{OL} = 3mA$			2 1	V
V_{OL}	"L" output voltage ϕ	$V_{CC} = 5V, I_{OL} = 2.5mA$ $V_{CC} = 3V, I_{OL} = 0.8mA$			2 1	V
$V_{T+} - V_{T-}$	Hysteresis $P3_0/\overline{INT_2}, P3_1/\overline{INT_1}$	use as interrupt input $V_{CC} = 5V$ $V_{CC} = 3V$	0.3 0.15		1 0.7	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{RESET}$	$V_{CC} = 5V$ $V_{CC} = 3V$		0.5 0.35	0.7	V
$V_{T+} - V_{T-}$	Hysteresis $P3_6/CLK$	use as CLK input $V_{CC} = 5V$ $V_{CC} = 3V$	0.3 0.15		1 0.7	V
$V_{T+} - V_{T-}$	Hysteresis X_{IN}	$V_{CC} = 5V$ $V_{CC} = 3V$	0.1 0.06		0.5 0.3	V
$V_{T+} - V_{T-}$	Hysteresis X_{CIN}	$V_{CC} = 5V$ $V_{CC} = 3V$	0.1 0.06		0.5 0.3	V
I_{IL}	"L" input current $P3_0 \sim P3_7, P4_0 \sim P4_7$	$V_i = 0V$ without pull-up T_r $V_i = 0V$, with pull-up T_r	$V_{CC} = 5V$ $V_{CC} = 3V$ $V_{CC} = 5V$ $V_{CC} = 3V$		-5 -4 -35 -12 -70 -25 -140 -40	μA
I_{IL}	"L" input current $IN_0 \sim IN_7$	$V_i = 0V$	$V_{CC} = 5V$ $V_{CC} = 3V$		-5 -4	μA
I_{IL}	"L" input current $\overline{RESET}, X_{IN}, X_{CIN}, R_0 \sim R_3$	$V_i = 0V$	$V_{CC} = 5V$ $V_{CC} = 3V$		-5 -4	μA
I_{IL}	"L" input current $P2_0 \sim P2_7$	$V_i = 0V$ $V_i = V_{CC} - 36V$			-5 -30	μA
I_{IH}	"H" input current $P3_0 \sim P3_7, P4_0 \sim P4_7$	$V_i = 5V$, without pull-up transistor			5	μA
I_{IH}	"H" input current $IN_0 \sim IN_7$	$V_i = 5V$, not use as analog input			5	μA
I_{IH}	"H" input current $P2_0 \sim P2_7$	reading operation $V_i = 5V$ normal operation $V_i = 5V$			100 5	μA
I_{IH}	"H" input current $\overline{RESET}, X_{IN}, X_{CIN}, R_0 \sim R_3$	$V_i = 5V$			5	μA
I_{IH}	"H" input current V_{REF}	$V_i = 5V$			5	mA
I_{OL}	"L" output current $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7$	$V_P = V_{CC} - 36V, V_{OL} = V_{CC}$	150	500	900	μA
I_{CC}	Supply current	Open output ports, $V_P = V_{CC}$, input port is V_{SS} , at normal operation.	$X_{IN} = 4MHz, V_{CC} = 5V$ $X_{IN} = 1MHz, V_{CC} = 3V$	3 0.4	6	mA
		Open output ports, $V_P = V_{CC}$, input port is V_{SS} , at wait mode.	$X_{IN} = 4MHz, V_{CC} = 5V$ $X_{IN} = 1MHz, V_{CC} = 3V$	1 0.2		
		Open output ports, $V_P = V_{CC}$, input port is V_{SS} , at normal operation, stop X_{IN} and $X_{OUT}, X_{CIN} = 32kHz$.	$V_{CC} = 5V$ $V_{CC} = 3V$	60 25	200	
		Open output ports, $V_P = V_{CC}$, input port is V_{SS} , at wait mode, stop X_{IN} and $X_{OUT}, X_{CIN} = 32kHz$.	$V_{CC} = 5V$ $V_{CC} = 3V$	40 15		
		Stop all oscillation.	$T_a = 25^\circ C$ $V_{CC} = 5V$ $V_{CC} = 3V$	0.1 0.06		μA
			$V_{CC} = 5V$ $V_{CC} = 3V$	1 0.6	10	
			$T_a = 70^\circ C$ $V_{CC} = 5V$ $V_{CC} = 3V$			
I_{ACC}	Supply current for A-D	at A-D converting time		2	4	mA
V_{RAM}	RAM retention voltage	Oscillation stops	2		5.5	V

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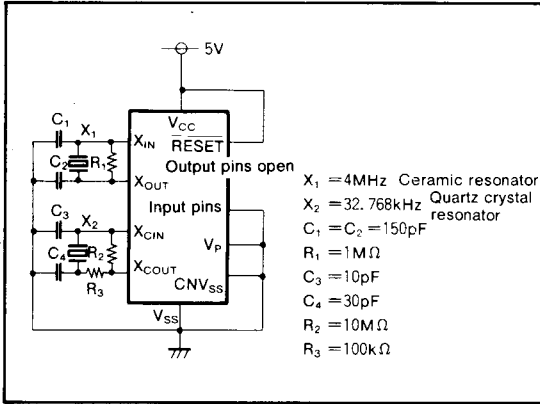


Fig.23 Test circuit for measuring supply current

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5\text{V}$, $V_{SS}=0\text{V}$, $T_a=25^\circ\text{C}$, $f(X_{IN})=4\text{MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Absolute accuracy	$V_{CC}=AV_{CC}=V_{REF}=5.12\text{V}$			± 3	LSB
R_{LADDER}	Ladder resistor value		1			$\text{k}\Omega$
t_{CONV}	Conversion time	High-speed : $\phi=1\text{MHz}$			72	μs
		Low-speed : $\phi=1\text{MHz}$			288	
V_{REF}	Reference input voltage				V_{CC}	V
V_{IA}	Analog input voltage				V_{REF}	V

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TIMING REQUIREMENTS

Single-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$ unless other wise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{SU(P3D-\phi)}$	Port P3 input setup time		270			ns
$t_{SU(P4D-\phi)}$	Port P4 input setup time		270			ns
$t_{SU(RD-\phi)}$	Port R input setup time		270			ns
$t_{SU(IND-\phi)}$	Port IN input setup time		270			ns
$t_{H(\phi-P2D)}$	Port P2 input hold time		20			ns
$t_{H(\phi-P3D)}$	Port P3 input hold time		20			ns
$t_{H(\phi-P4D)}$	Port P4 input hold time		20			ns
$t_{H(\phi-RD)}$	Port R input hold time		20			ns
$t_{H(\phi-IND)}$	Port IN input hold time		20			ns
$t_C(X_{IN})$	External clock input cycle time (X_{IN})		230			ns
$t_W(X_{IN})$	External clock input pulse width (X_{IN})		75			ns
$t_C(X_{CIN})$	External clock input cycle time (X_{CIN})		2			ms
$t_W(X_{CIN})$	External clock input pulse width (X_{CIN})		1			ms
t_r	External clock rising edge time				25	ns
t_f	External clock falling edge time				25	ns

Memory expanding mode and eva-chip mode

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{H(\phi-P2D)}$	Port P2 input hold time		20			ns

Microprocessor mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{H(\phi-P2D)}$	Port P2 input hold time		20			ns

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SWITCHING CHARACTERISTICS

Single-chip mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_d(\phi \rightarrow P0Q)$	Port P0 data output delay time	Fig. 25			230	ns
$t_d(\phi \rightarrow P1Q)$	Port P1 data output delay time				230	ns
$t_d(\phi \rightarrow P2Q)$	Port P2 data output delay time				230	ns
$t_d(\phi \rightarrow P3Q)$	Port P3 data output delay time	Fig. 24			230	ns
$t_d(\phi \rightarrow P4Q)$	Port P4 data output delay time				230	ns

Memory expanding mode and eva-chip mode

($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_d(\phi \rightarrow P0A)$	Port P0 address output delay time	Fig. 25			250	ns
$t_d(\phi \rightarrow P0AF)$	Port P0 address output delay time				250	ns
$t_d(\phi \rightarrow P0Q)$	Port P0 data output delay time				200	ns
$t_d(\phi \rightarrow P0QF)$	Port P0 data output delay time				200	ns
$t_d(\phi \rightarrow P1A)$	Port P1 address output delay time				250	ns
$t_d(\phi \rightarrow P1AF)$	Port P1 address output delay time				250	ns
$t_d(\phi \rightarrow P1Q)$	Port P1 data output delay time				200	ns
$t_d(\phi \rightarrow P1QF)$	Port P1 data output delay time				200	ns
$t_d(\phi \rightarrow P2Q)$	Port P2 data output delay time				300	ns
$t_d(\phi \rightarrow P2QF)$	Port P2 data output delay time				300	ns
$t_d(\phi \rightarrow R/W)$	R/W signal output delay time				250	ns
$t_d(\phi \rightarrow R/WF)$	R/W signal output delay time				250	ns
$t_d(\phi \rightarrow P4_0Q)$	Port P4 ₀ data output delay time	Fig. 24			200	ns
$t_d(\phi \rightarrow P4_0QF)$	Port P4 ₀ data output delay time				200	ns
$t_d(\phi \rightarrow SYNC)$	SYNC signal output delay time				250	ns
$t_d(\phi \rightarrow SYNCF)$	SYNC signal output delay time				250	ns
$t_d(\phi \rightarrow P4_1Q)$	Port P4 ₁ data output delay time				200	ns
$t_d(\phi \rightarrow P4_1QF)$	Port P4 ₁ data output delay time				200	ns

Microprocessor mode ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=4MHz$ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_d(\phi \rightarrow P0A)$	Port P0 address output delay time	Fig. 25			250	ns
$t_d(\phi \rightarrow P1A)$	Port P1 address output delay time				250	ns
$t_d(\phi \rightarrow P2Q)$	Port P2 data output delay time				300	ns
$t_d(\phi \rightarrow P2QF)$	Port P2 data output delay time				300	ns
$t_d(\phi \rightarrow R/W)$	R/W signal output delay time	Fig. 24			250	ns
$t_d(\phi \rightarrow SYNC)$	SYNC signal output delay time				250	ns

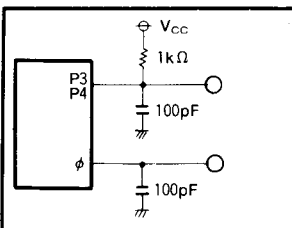


Fig.24 Test circuit of ports P3 and P4

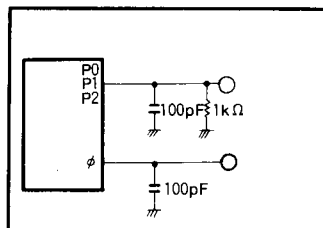


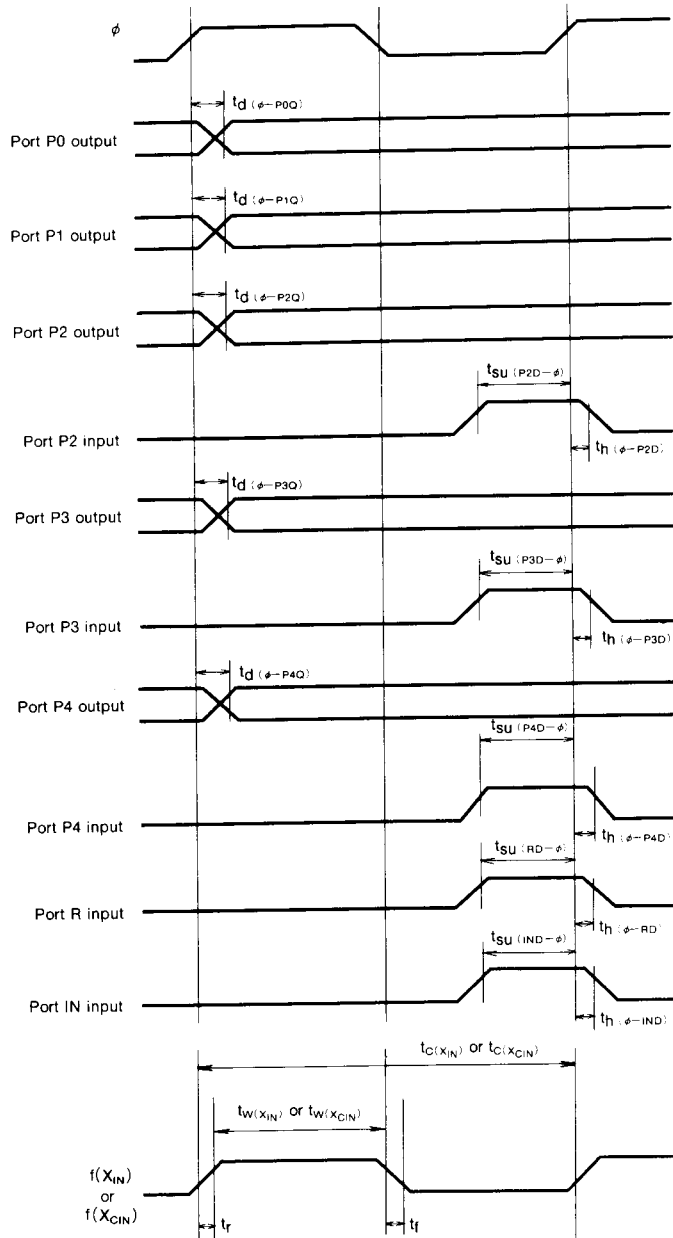
Fig.25 Test circuit of ports P0, P1, and P2

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TIMING DIAGRAMS

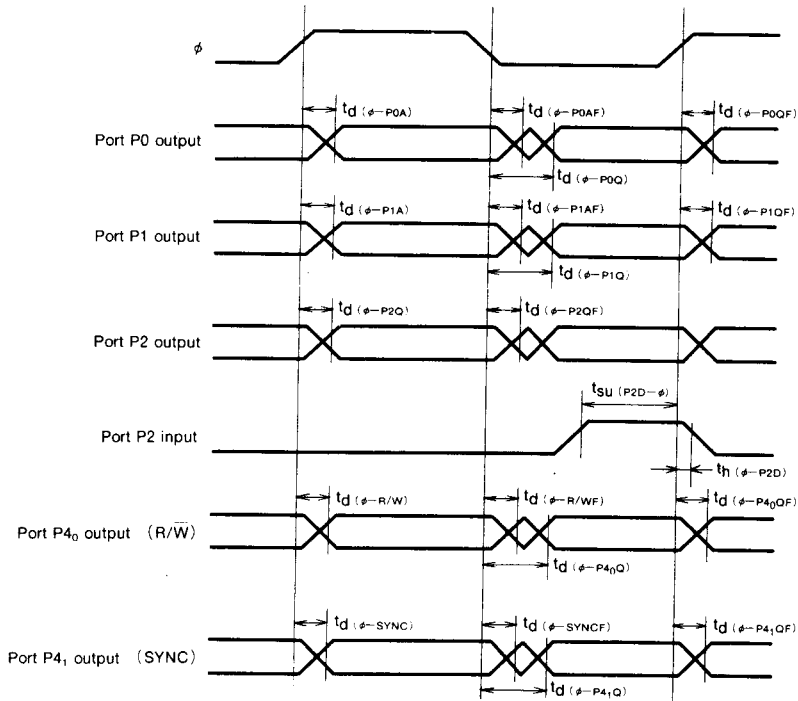
In single-chip mode



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