

## 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH $\pm 15$ -kV ESD PROTECTION

Check for Samples: [MAX3222E](#)

### FEATURES

- **ESD Protection for RS-232 Bus Pins**
  - $\pm 15$ -kV Human-Body Model (HBM)
  - $\pm 8$ -kV IEC61000-4-2, Contact Discharge
  - $\pm 15$ -kV IEC61000-4-2, Air-Gap Discharge
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates With 3-V to 5.5-V  $V_{CC}$  Supply**
- **Operates up to 500 kbit/s**
- **Two Drivers and Two Receivers**
- **Low Standby Current . . . 1  $\mu$ A Typ**
- **External Capacitors . . . 4  $\times$  0.1  $\mu$ F**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **Alternative High-Speed Pin-Compatible Device (1 Mbit/s) for SNx5C3222E**

### APPLICATIONS

- **Battery-Powered Systems**
- **PDA's**
- **Notebooks**
- **Laptops**
- **Palmtop PCs**
- **Hand-Held Equipment**

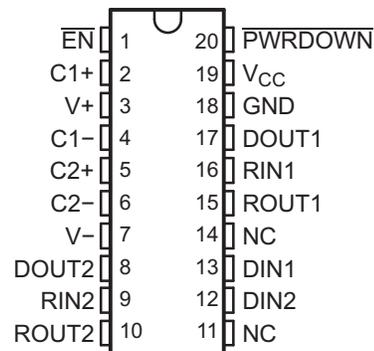
### DESCRIPTION/ORDERING INFORMATION

The MAX3222E consists of two line drivers, two line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin to pin (serial-port connection pins, including GND).

The MAX3222E can be placed in the power-down mode by setting the power-down ( $\overline{\text{PWRDOWN}}$ ) input low, which draws only 1  $\mu$ A from the power supply. When the device is powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled;  $V+$  is lowered to  $V_{CC}$ , and  $V-$  is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting enable ( $\overline{\text{EN}}$ ) high.

The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at typical data signaling rates up to 500 kbit/s and a maximum of 30-V/ $\mu$ s driver output slew rate.

DB, DW, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**ORDERING INFORMATION**

| $T_A$         | PACKAGE <sup>(1)</sup> <sup>(2)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|---------------------------------------|--------------|-----------------------|------------------|
| 0°C to 70°C   | SOIC – DW                             | Tube of 25   | MAX3222ECDW           | MAX3222EC        |
|               |                                       | Reel of 2000 | MAX3222ECDWR          |                  |
|               | SSOP – DB                             | Tube of 70   | MAX3222ECDB           | MP222EC          |
|               |                                       | Reel of 2000 | MAX3222ECDBR          |                  |
|               | TSSOP – PW                            | Tube of 70   | MAX3222ECPW           | MP222EC          |
|               |                                       | Reel of 2000 | MAX3222ECPWR          |                  |
| –40°C to 85°C | SOIC – DW                             | Tube of 25   | MAX3222EIDW           | MAX3222EI        |
|               |                                       | Reel of 2000 | MAX3222EIDWR          |                  |
|               | SSOP – DB                             | Tube of 70   | MAX3222EIDB           | MP222EI          |
|               |                                       | Reel of 2000 | MAX3222EIDBR          |                  |
|               | TSSOP – PW                            | Tube of 70   | MAX3222EIPW           | MP222EI          |
|               |                                       | Reel of 2000 | MAX3222EIPWR          |                  |

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**Table 1. FUNCTION TABLES****EACH DRIVER <sup>(1)</sup>**

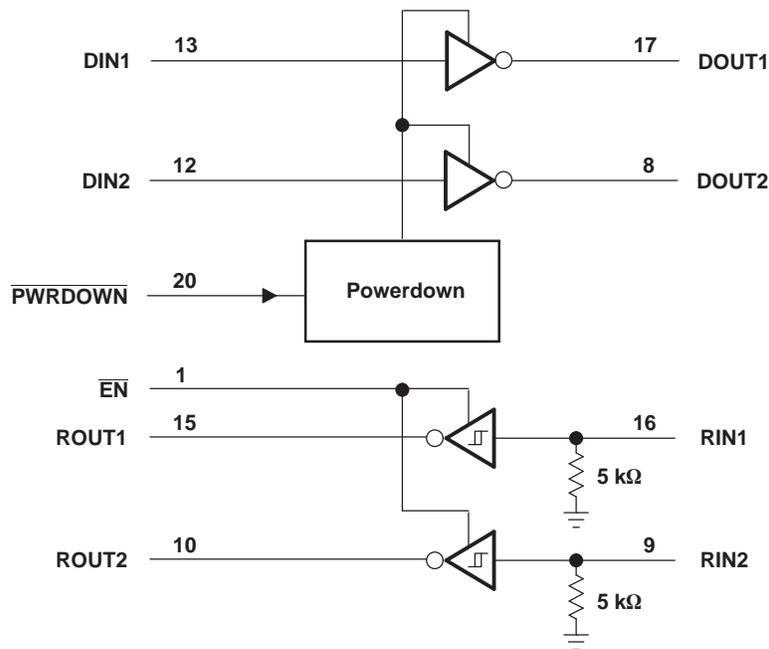
| INPUTS |                             | OUTPUT<br>DOUT |
|--------|-----------------------------|----------------|
| DIN    | $\overline{\text{PWRDOWN}}$ |                |
| X      | L                           | Z              |
| L      | H                           | H              |
| H      | H                           | L              |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

**Table 2. EACH RECEIVER <sup>(1)</sup>**

| INPUTS |                        | OUTPUT<br>ROUT |
|--------|------------------------|----------------|
| RIN    | $\overline{\text{EN}}$ |                |
| L      | L                      | H              |
| H      | L                      | L              |
| X      | H                      | Z              |
| Open   | L                      | H              |

(1) H = high level, L = low level, X = irrelevant,  
Z = high impedance (off),  
Open = input disconnected or connected driver off

**LOGIC DIAGRAM (POSITIVE LOGIC)**


Pin numbers are for the DB, DW, and PW packages.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

|               |   | MIN   | MAX   | UNIT           |      |
|---------------|---|---|-------|----------------|------|
| $V_{CC}$      | Supply voltage range <sup>(2)</sup>                 | -0.3  | 6     | V              |      |
| $V+$          | Positive-output supply voltage range <sup>(2)</sup> | -0.3  | 7     | V              |      |
| $V-$          | Negative-output supply voltage range <sup>(2)</sup> | 0.3   | -7    | V              |      |
| $V+ - V-$     | Supply voltage difference <sup>(2)</sup>            |   | 13    | V              |      |
| $V_I$         | Input voltage range                                 | Driver ( $\overline{EN}$ , $\overline{PWRDOWN}$ ) | -0.3  | 6              | V    |
|               |   | Receiver  | -25   | 25             |      |
| $V_O$         | Output voltage range                                | Driver  | -13.2 | 13.2           | V    |
|               |   | Receiver  | -0.3  | $V_{CC} + 0.3$ |      |
| $\theta_{JA}$ | Package thermal impedance <sup>(3) (4)</sup>        | DB package  |       | 70             | °C/W |
|               |   | DW package  |       | 58             |      |
|               |   | PW package  |       | 83             |      |
| $T_J$         | Operating virtual junction temperature              |   | 150   | °C             |      |
| $T_{stg}$     | Storage temperature range                           | -65   | 150   | °C             |      |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**See [Figure 5](#)

|                |   |   | MIN                     | NOM | MAX | UNIT |
|----------------|---|---|-------------------------|-----|-----|------|
| Supply voltage |   | $V_{CC} = 3.3\text{ V}$                     | 3                       | 3.3 | 3.6 | V    |
|                |   | $V_{CC} = 5\text{ V}$                       | 4.5                     | 5   | 5.5 |      |
| $V_{IH}$       | Driver and control high-level input voltage | DIN, $\overline{EN}$ , $\overline{PWRDOWN}$ | $V_{CC} = 3.3\text{ V}$ | 2   |     | V    |
|                |   |   | $V_{CC} = 5\text{ V}$   | 2.4 |     |      |
| $V_{IL}$       | Driver and control low-level input voltage  | DIN, $\overline{EN}$ , $\overline{PWRDOWN}$ |                         |     | 0.8 | V    |
| $V_I$          | Driver and control input voltage            | DIN, $\overline{EN}$ , $\overline{PWRDOWN}$ | 0                       | 5.5 |     | V    |
| $V_I$          | Receiver input voltage                      |   | -25                     | 25  |     | V    |
| $T_A$          | Operating free-air temperature              | MAX3222EC                                   | 0                       | 70  |     | °C   |
|                |   | MAX3222EI                                   | -40                     | 85  |     |      |

(1) Test conditions are C1–C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047  $\mu\text{F}$ , C2–C4 = 0.33  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

**ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

| PARAMETER |  | TEST CONDITIONS                           | MIN | TYP <sup>(2)</sup> | MAX     | UNIT          |
|-----------|--|---|-----|--------------------|---------|---------------|
| $I_I$     | Input leakage current ( $\overline{EN}$ , $\overline{PWRDOWN}$ ) |   |     | $\pm 0.01$         | $\pm 1$ | $\mu\text{A}$ |
| $I_{CC}$  | Supply current   | No load, $\overline{PWRDOWN}$ at $V_{CC}$ |     | 0.3                | 1       | mA            |
|           | Supply current (powered off)                                     | No load, $\overline{PWRDOWN}$ at GND      |     | 1                  | 10      | $\mu\text{A}$ |

(1) Test conditions are C1–C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047  $\mu\text{F}$ , C2–C4 = 0.33  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

## DRIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

| PARAMETER       |   | TEST CONDITIONS   |                      | MIN  | TYP <sup>(2)</sup> | MAX | UNIT |
|-----------------|---|---|----------------------|--|--------------------|-----|------|
| V <sub>OH</sub> | High-level output voltage                   | DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = GND             |                      | 5  | 5.4                |     | V    |
| V <sub>OL</sub> | Low-level output voltage                    | DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = V <sub>CC</sub> |                      | -5   | -5.4               |     | V    |
| I <sub>IH</sub> | High-level input current                    | V <sub>I</sub> = V <sub>CC</sub>                            |                      |  | ±0.01              | ±1  | μA   |
| I <sub>IL</sub> | Low-level input current                     | V <sub>I</sub> at GND                                       |                      |  | ±0.01              | ±1  | μA   |
| I <sub>OS</sub> | Short-circuit output current <sup>(3)</sup> | V <sub>CC</sub> = 3.6 V                                     | V <sub>O</sub> = 0 V |  | ±35                | ±60 | mA   |
|                 |   | V <sub>CC</sub> = 5.5 V                                     |                      |  |                    |     |      |
| r <sub>o</sub>  | Output resistance                           | V <sub>CC</sub> , V+, and V- = 0 V, V <sub>O</sub> = ±2 V   |                      | 300  | 10M                |     | Ω    |
| I <sub>OZ</sub> | Output leakage current                      | PWRDOWN = GND   |                      | V <sub>CC</sub> = 3 V to 3.6 V, V <sub>O</sub> = ±12 V   |                    | ±25 | μA   |
|                 |   |   |                      | V <sub>CC</sub> = 4.5 V to 5.5 V, V <sub>O</sub> = ±10 V |                    | ±25 |      |

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

| PARAMETER          |  | TEST CONDITIONS  |   | MIN | TYP <sup>(2)</sup> | MAX | UNIT   |
|--------------------|--|--|---|-----|--------------------|-----|--------|
|                    | Maximum data rate  | C <sub>L</sub> = 1000 pF, One DOUT switching,                    | R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 1</a> | 250 | 500                |     | kbit/s |
| t <sub>sk(p)</sub> | Pulse skew <sup>(3)</sup>                                    | C <sub>L</sub> = 150 pF to 2500 pF, See <a href="#">Figure 2</a> | R <sub>L</sub> = 3 kΩ to 7 kΩ,                      |     | 300                |     | ns     |
| SR(tr)             | Slew rate, transition region (see <a href="#">Figure 1</a> ) | R <sub>L</sub> = 3 kΩ to 7 kΩ, V <sub>CC</sub> = 3.3 V           | C <sub>L</sub> = 150 pF to 1000 pF                  | 6   |                    | 30  | V/μs   |
|                    |  |  | C <sub>L</sub> = 150 pF to 2500 pF                  | 4   |                    | 30  |        |

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

### ESD Protection

|                        |                                 | TYP | UNIT |
|------------------------|---------------------------------|-----|------|
| Driver outputs (DOUTx) | Human-Body Model (HBM)          | ±15 | kV   |
|                        | IEC61000-4-2, Air-Gap Discharge | ±15 |      |
|                        | IEC61000-4-2, Contact Discharge | ±8  |      |

## RECEIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

| PARAMETER        |   | TEST CONDITIONS                | MIN                   | TYP <sup>(2)</sup>    | MAX | UNIT |
|------------------|---|--------------------------------|-----------------------|-----------------------|-----|------|
| V <sub>OH</sub>  | High-level output voltage                               | I <sub>OH</sub> = -1 mA        | V <sub>CC</sub> - 0.6 | V <sub>CC</sub> - 0.1 |     | V    |
| V <sub>OL</sub>  | Low-level output voltage                                | I <sub>OL</sub> = 1.6 mA       |                       |                       | 0.4 | V    |
| V <sub>IT+</sub> | Positive-going input threshold voltage                  | V <sub>CC</sub> = 3.3 V        |                       | 1.5                   | 2.4 | V    |
|                  |   | V <sub>CC</sub> = 5 V          |                       | 1.8                   | 2.4 |      |
| V <sub>IT-</sub> | Negative-going input threshold voltage                  | V <sub>CC</sub> = 3.3 V        | 0.6                   | 1.2                   |     | V    |
|                  |   | V <sub>CC</sub> = 5 V          | 0.8                   | 1.5                   |     |      |
| V <sub>hys</sub> | Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> ) |                                |                       | 0.3                   |     | V    |
| I <sub>OZ</sub>  | Output leakage current                                  | $\overline{EN} = 1$            |                       | ±0.05                 | ±10 | µA   |
| r <sub>i</sub>   | Input resistance  | V <sub>I</sub> = ±3 V to ±25 V | 3                     | 5                     | 7   | kΩ   |

- (1) Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V<sub>CC</sub> = 5 V ± 0.5 V.  
 (2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

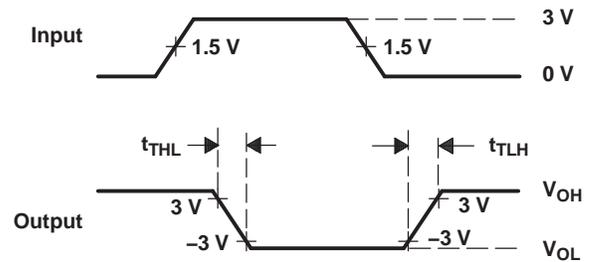
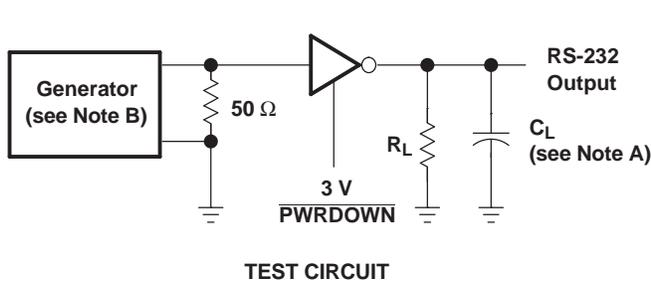
| PARAMETER          |   | TEST CONDITIONS  | TYP <sup>(2)</sup> | UNIT |
|--------------------|---|--|--------------------|------|
| t <sub>PLH</sub>   | Propagation delay time, low- to high-level output | C <sub>L</sub> = 150 pF, See <a href="#">Figure 3</a>                        | 300                | ns   |
| t <sub>PHL</sub>   | Propagation delay time, high- to low-level output | C <sub>L</sub> = 150 pF, See <a href="#">Figure 3</a>                        | 300                | ns   |
| t <sub>en</sub>    | Output enable time                                | C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 4</a> | 200                | ns   |
| t <sub>dis</sub>   | Output disable time                               | C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 4</a> | 200                | ns   |
| t <sub>sk(p)</sub> | Pulse skew <sup>(3)</sup>                         | See <a href="#">Figure 3</a>   | 300                | ns   |

- (1) Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V<sub>CC</sub> = 5 V ± 0.5 V.  
 (2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.  
 (3) Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

### ESD Protection

|                        |                                 | TYP | UNIT |
|------------------------|---------------------------------|-----|------|
| Receiver inputs (RINx) | Human-Body Model (HBM)          | ±15 | kV   |
|                        | IEC61000-4-2, Air-Gap Discharge | ±15 |      |
|                        | IEC61000-4-2, Contact Discharge | ±8  |      |

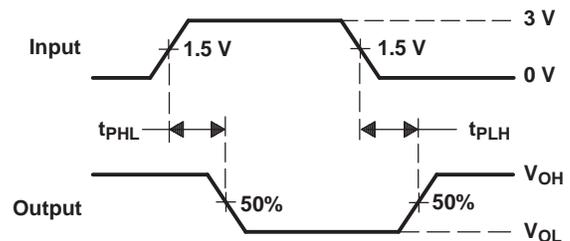
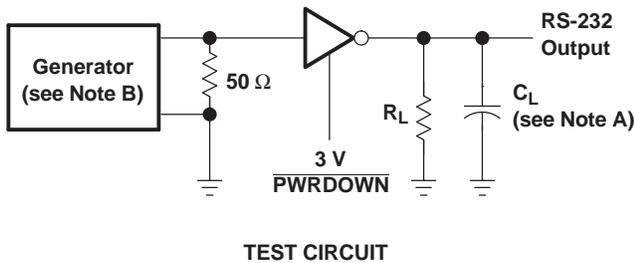
PARAMETER MEASUREMENT INFORMATION



$$SR(tr) = \frac{6V}{t_{THL} \text{ or } t_{TLH}}$$

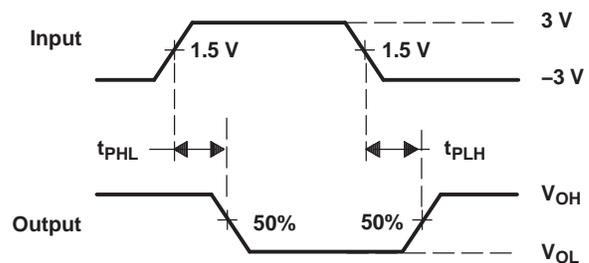
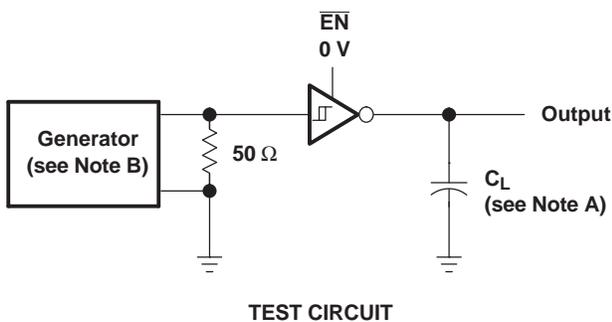
- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

Figure 1. Driver Slew Rate



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

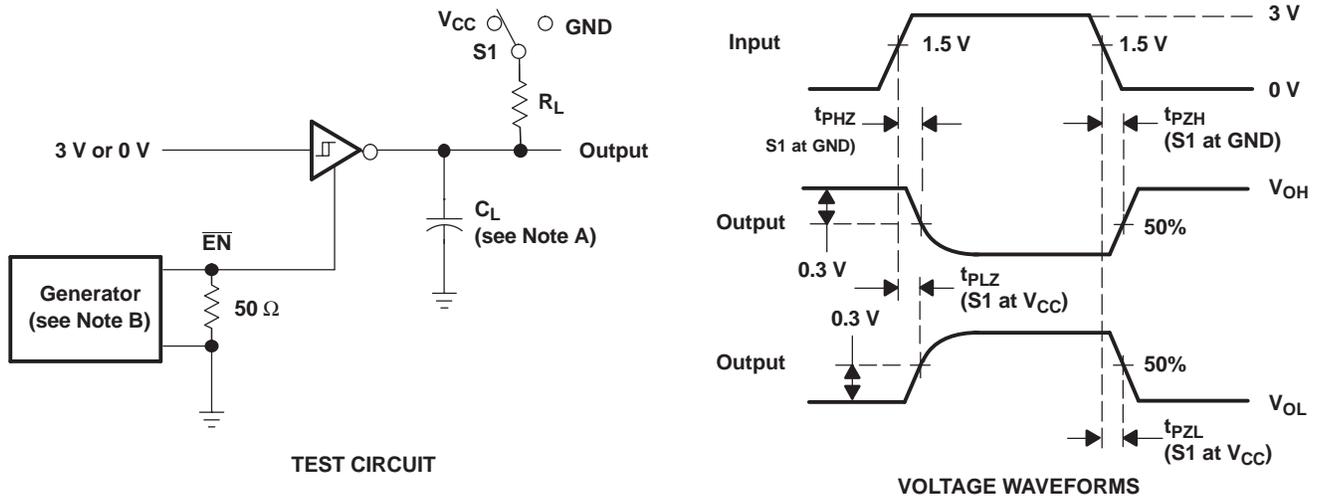
Figure 2. Driver Pulse Skew



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

Figure 3. Receiver Propagation Delay Times

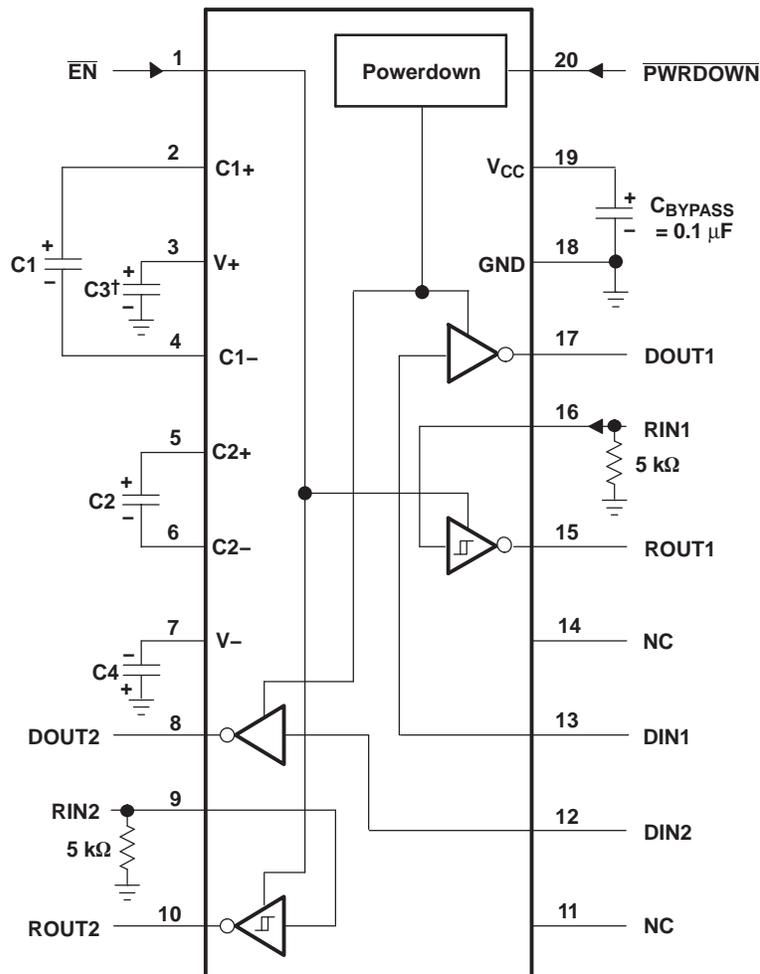
PARAMETER MEASUREMENT INFORMATION (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

Figure 4. Receiver Enable and Disable Times

APPLICATION INFORMATION



† C3 can be connected to V<sub>CC</sub> or GND.

NOTES: A. Resistor values shown are nominal.

B. NC – No internal connection

C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V<sub>CC</sub> vs CAPACITOR VALUES

| V <sub>CC</sub> | C1       | C2, C3, and C4 |
|-----------------|----------|----------------|
| 3.3 V ± 0.3 V   | 0.1 μF   | 0.1 μF         |
| 5 V ± 0.5 V     | 0.047 μF | 0.33 μF        |
| 3 V to 5.5 V    | 0.1 μF   | 0.47 μF        |

Figure 5. Typical Operating Circuit and Capacitor Values

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MAX3222ECDB      | ACTIVE        | SSOP         | DB                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MP222EC                 | <a href="#">Samples</a> |
| MAX3222ECDBR     | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MP222EC                 | <a href="#">Samples</a> |
| MAX3222ECDW      | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX3222EC               | <a href="#">Samples</a> |
| MAX3222ECDWR     | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MAX3222EC               | <a href="#">Samples</a> |
| MAX3222ECPW      | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MP222EC                 | <a href="#">Samples</a> |
| MAX3222ECPWG4    | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MP222EC                 | <a href="#">Samples</a> |
| MAX3222ECPWR     | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MP222EC                 | <a href="#">Samples</a> |
| MAX3222ECPWRG4   | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | MP222EC                 | <a href="#">Samples</a> |
| MAX3222EIDB      | ACTIVE        | SSOP         | DB                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MP222EI                 | <a href="#">Samples</a> |
| MAX3222EIDBG4    | ACTIVE        | SSOP         | DB                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MP222EI                 | <a href="#">Samples</a> |
| MAX3222EIDBR     | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MP222EI                 | <a href="#">Samples</a> |
| MAX3222EIDBRG4   | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MP222EI                 | <a href="#">Samples</a> |
| MAX3222EIDW      | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MAX3222EI               | <a href="#">Samples</a> |
| MAX3222EIDWR     | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MAX3222EI               | <a href="#">Samples</a> |
| MAX3222EIPW      | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MP222EI                 | <a href="#">Samples</a> |
| MAX3222EIPWG4    | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MP222EI                 | <a href="#">Samples</a> |
| MAX3222EIPWR     | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MP222EI                 | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples        |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|----------------|
| MAX3222EIPWRG4   | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | MP222EI                 | <b>Samples</b> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

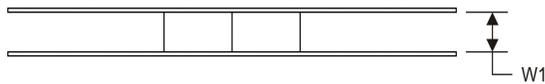
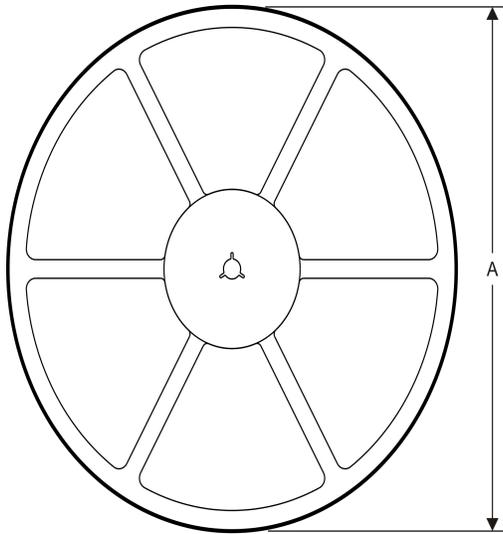
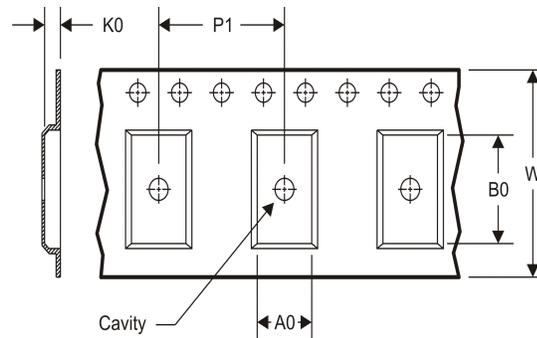
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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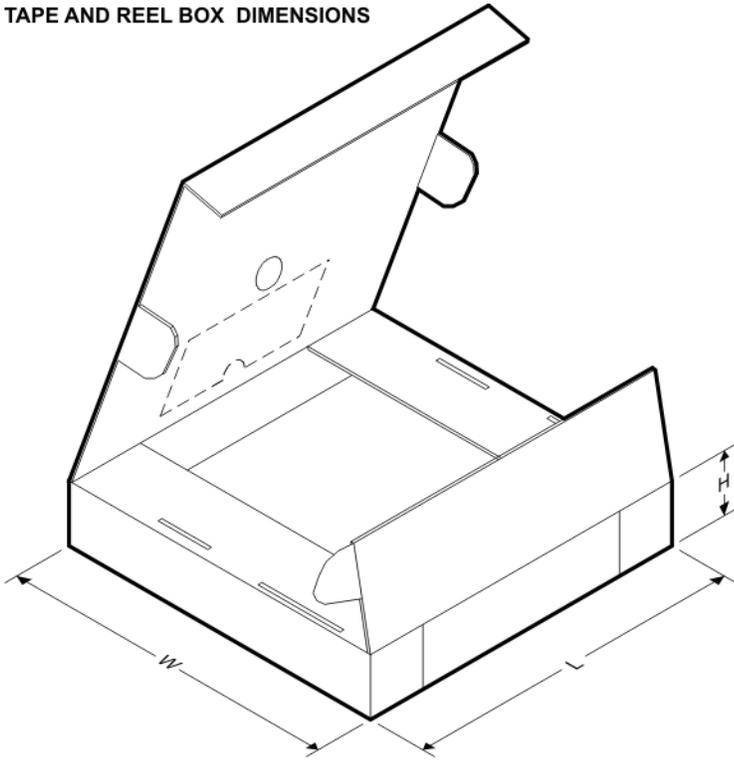
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MAX3222ECDBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| MAX3222ECDWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.0    | 2.7     | 12.0    | 24.0   | Q1            |
| MAX3222ECPWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| MAX3222EIDBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| MAX3222EIDWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.0    | 2.7     | 12.0    | 24.0   | Q1            |
| MAX3222EIPWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |

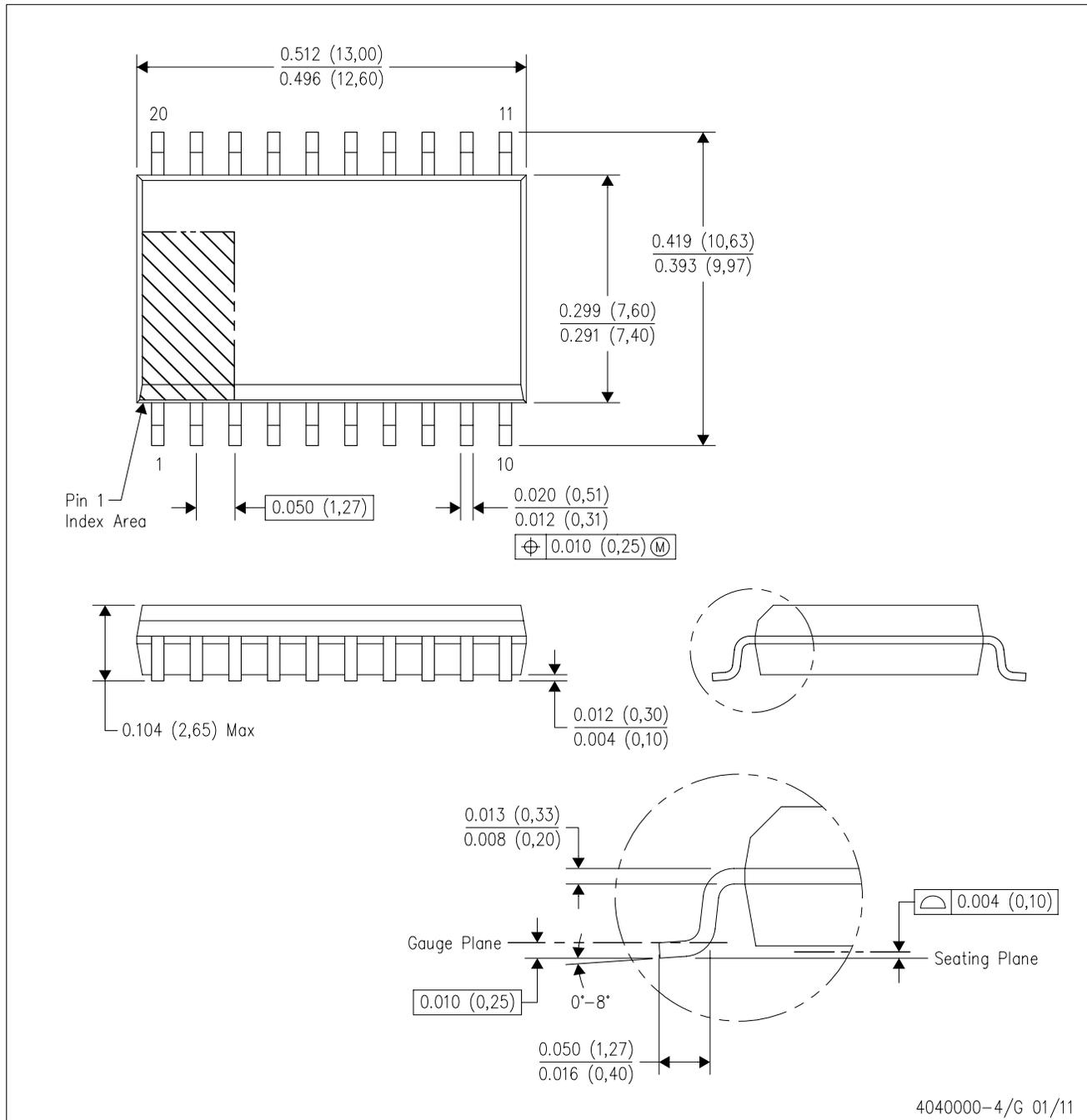
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MAX3222ECDBR | SSOP         | DB              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| MAX3222ECDWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| MAX3222ECPWR | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| MAX3222EIDBR | SSOP         | DB              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| MAX3222EIDWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| MAX3222EIPWR | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |

DW (R-PDSO-G20)

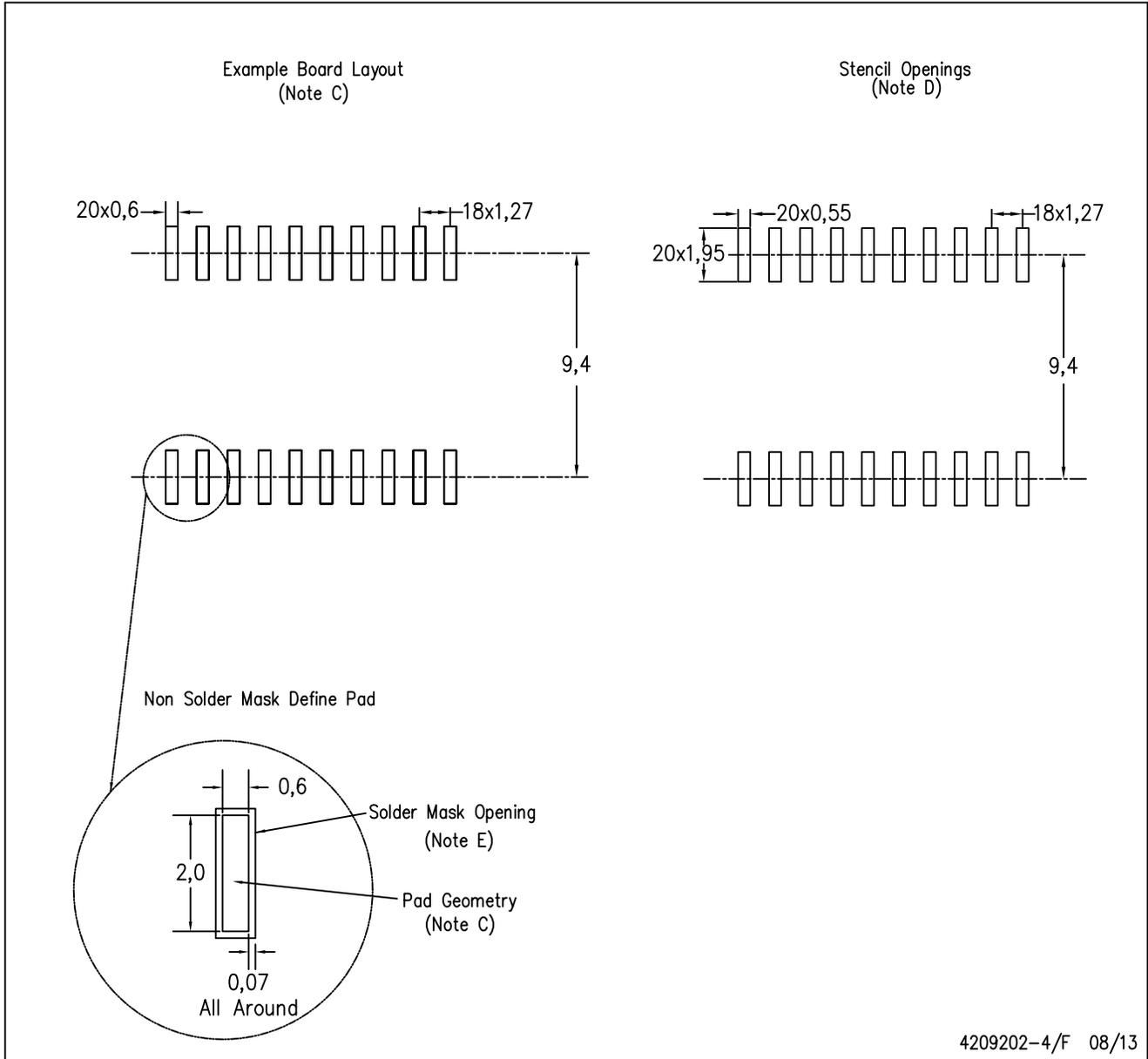
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

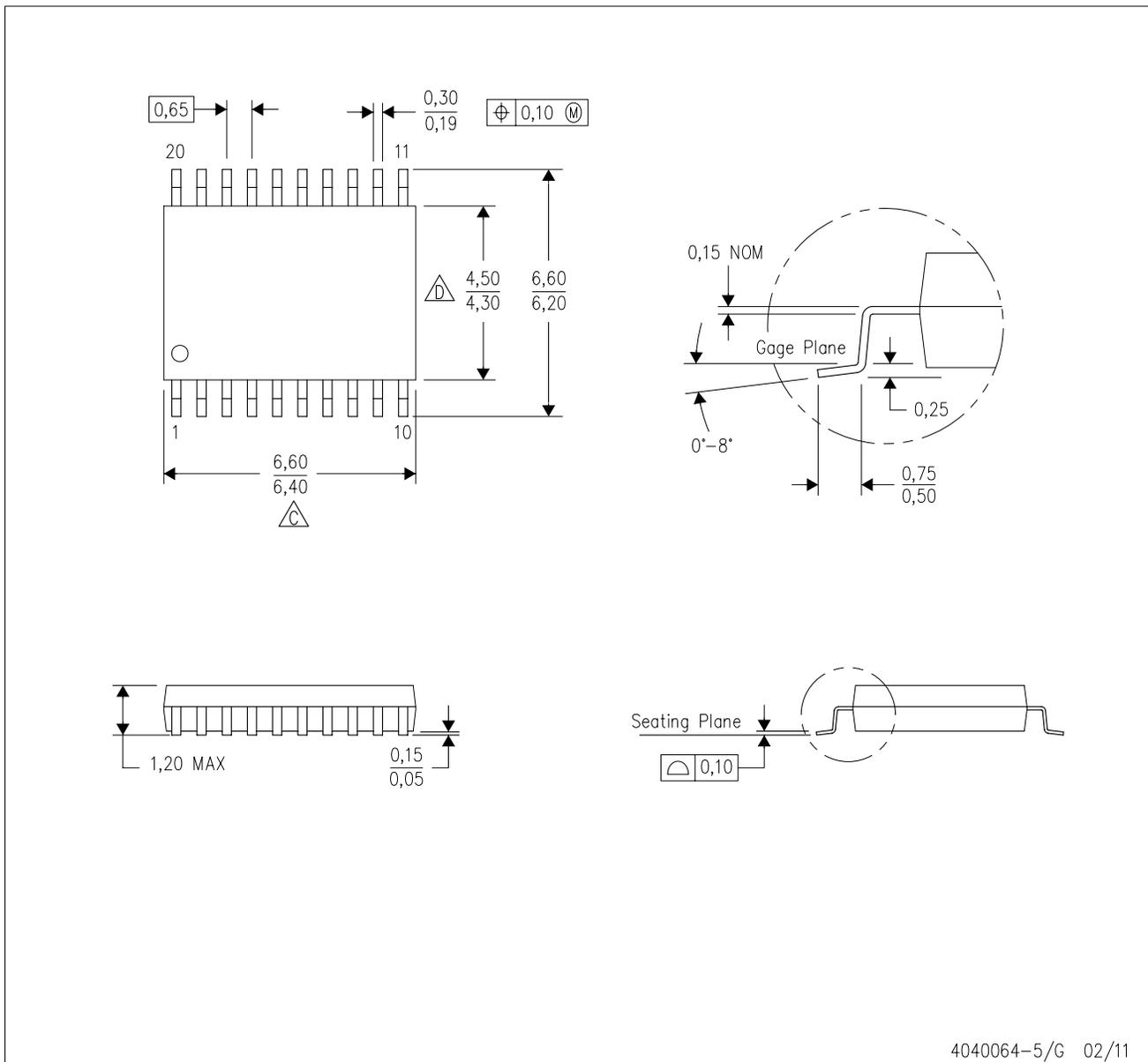


4209202-4/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

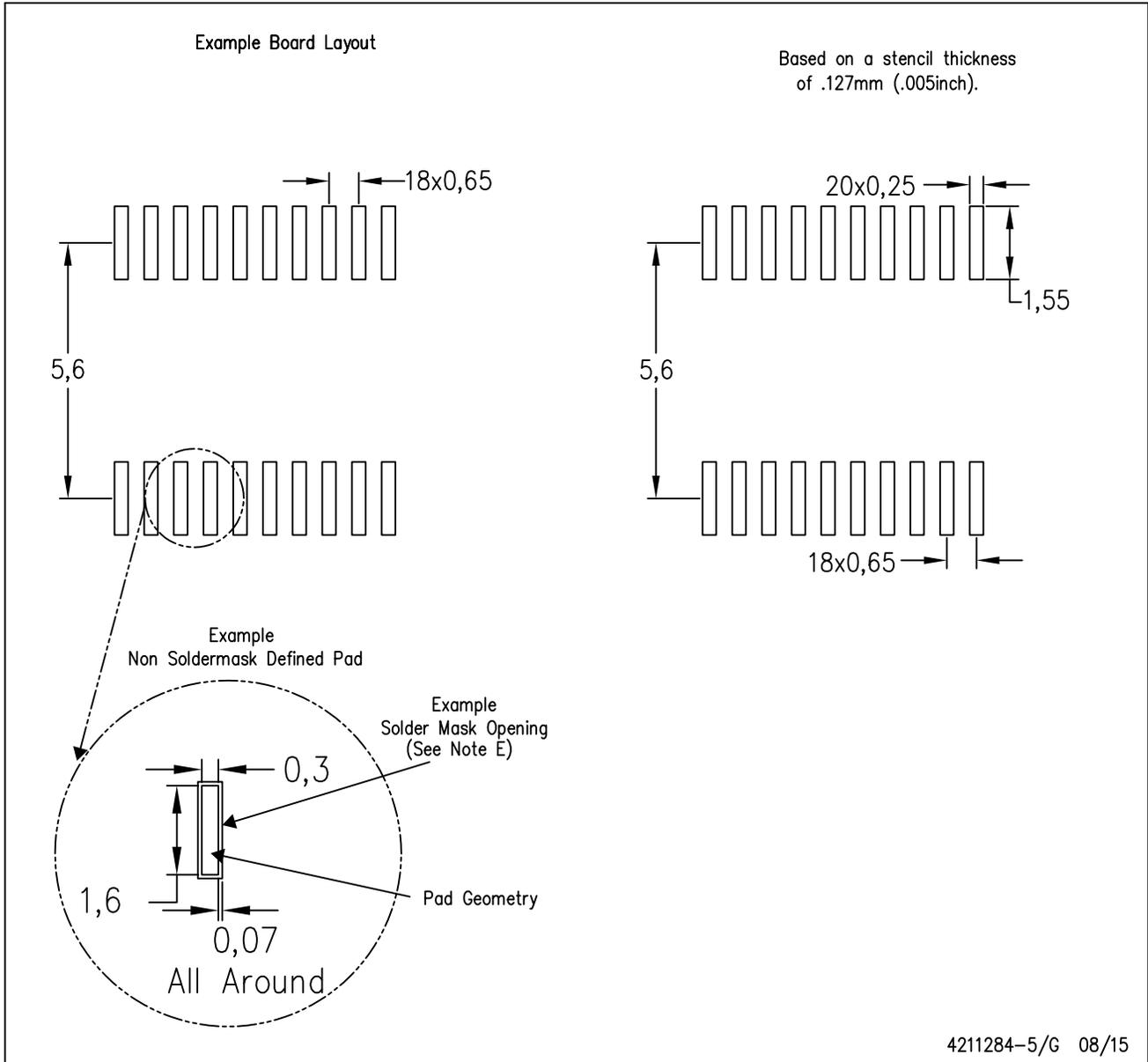
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

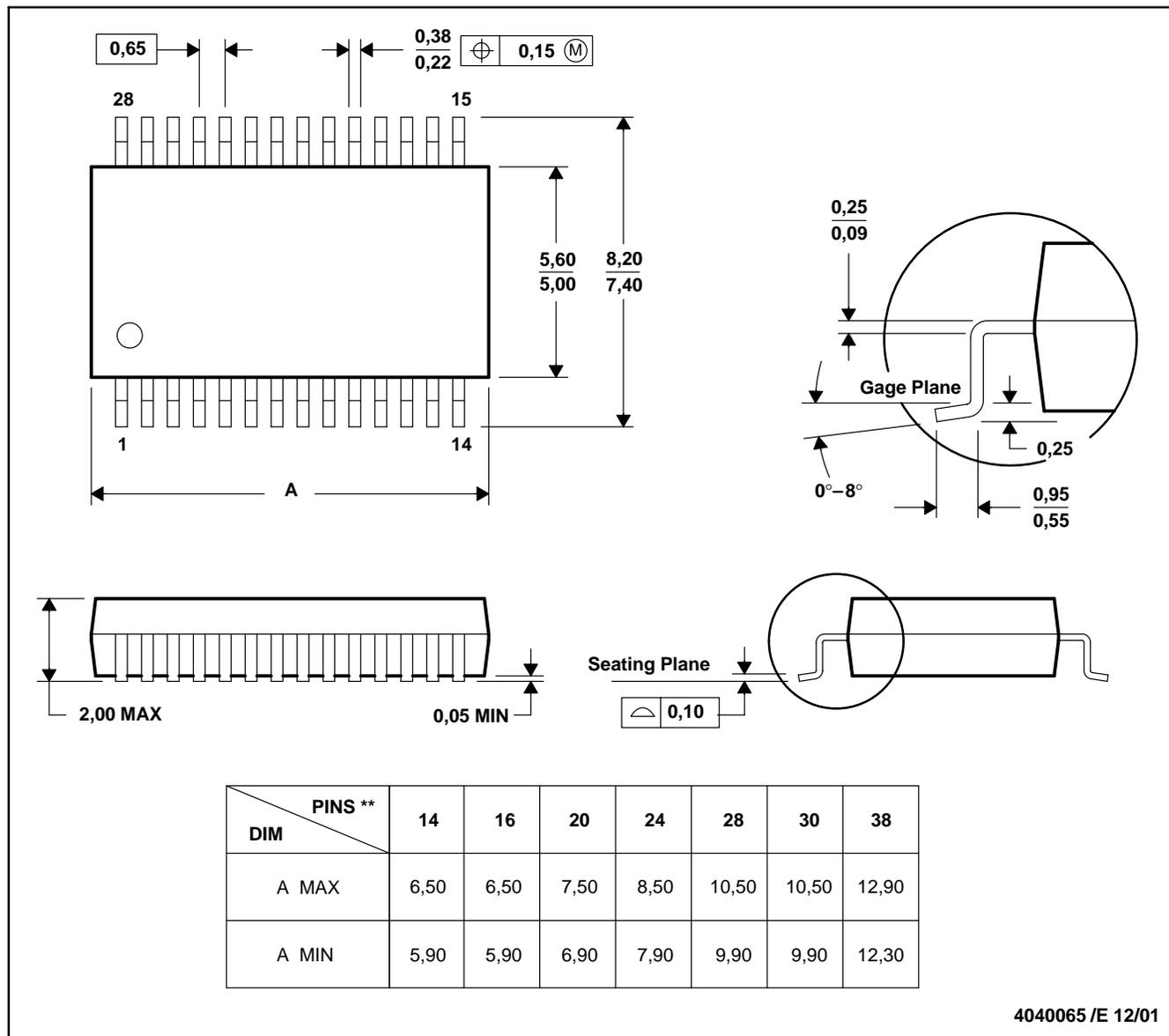


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

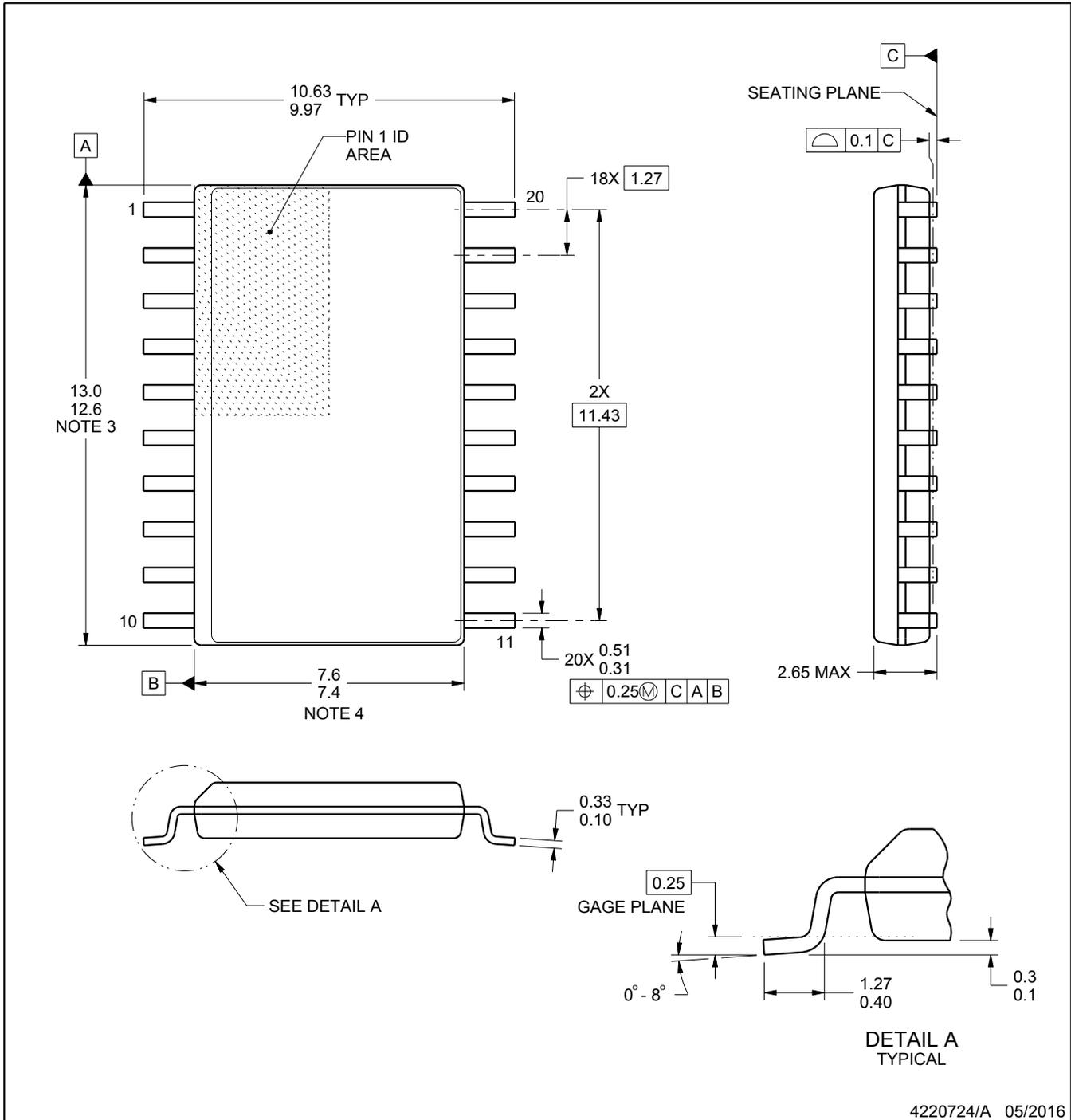
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

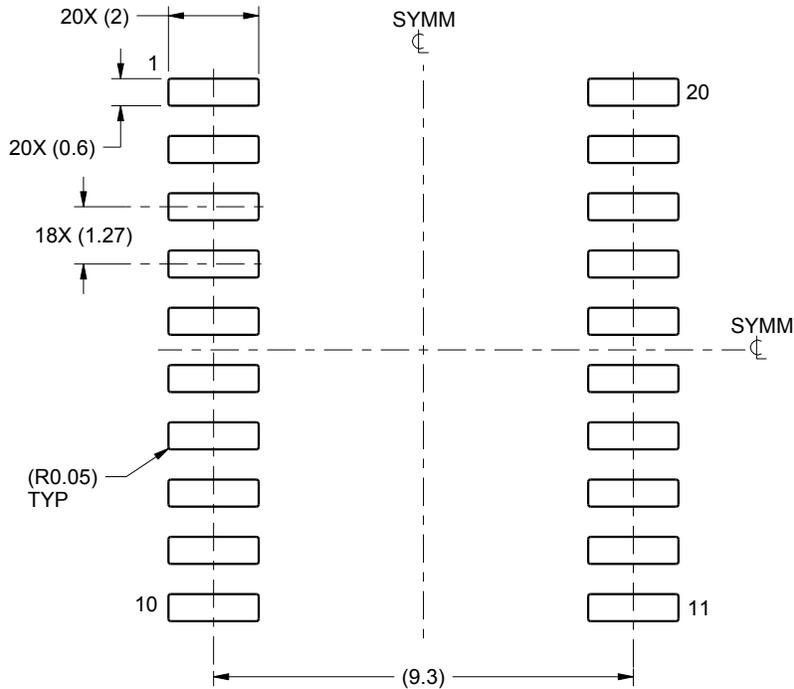
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

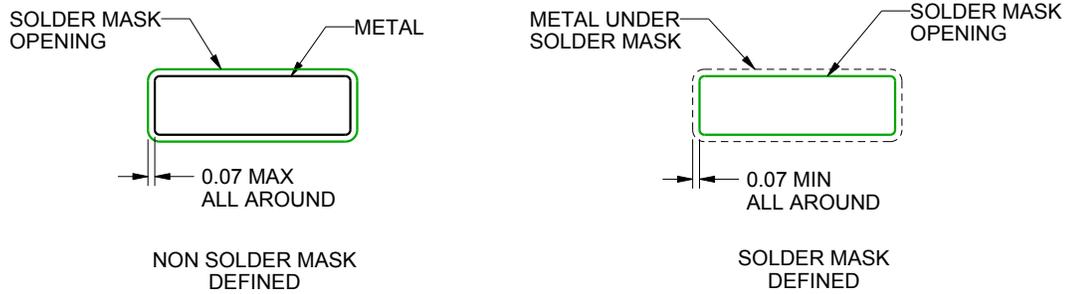
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

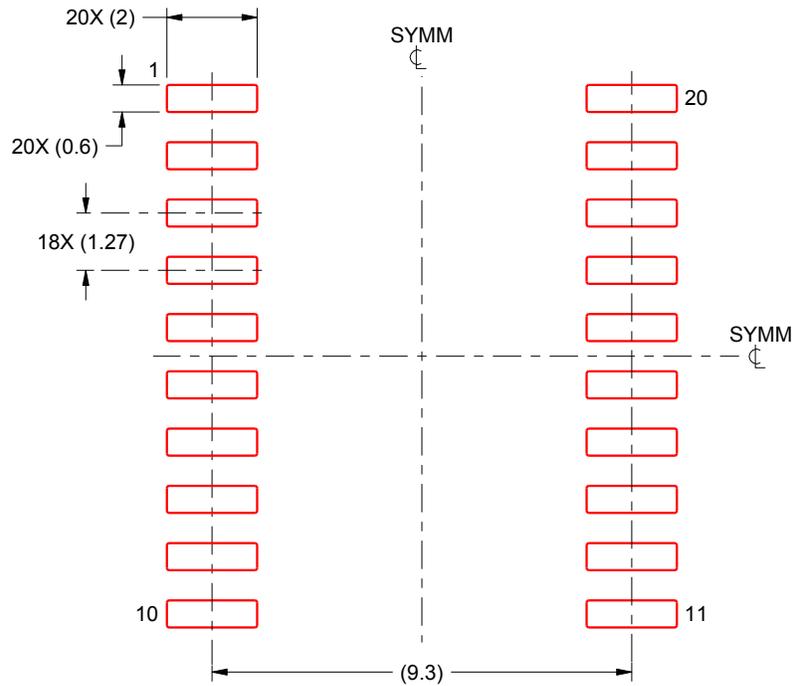
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

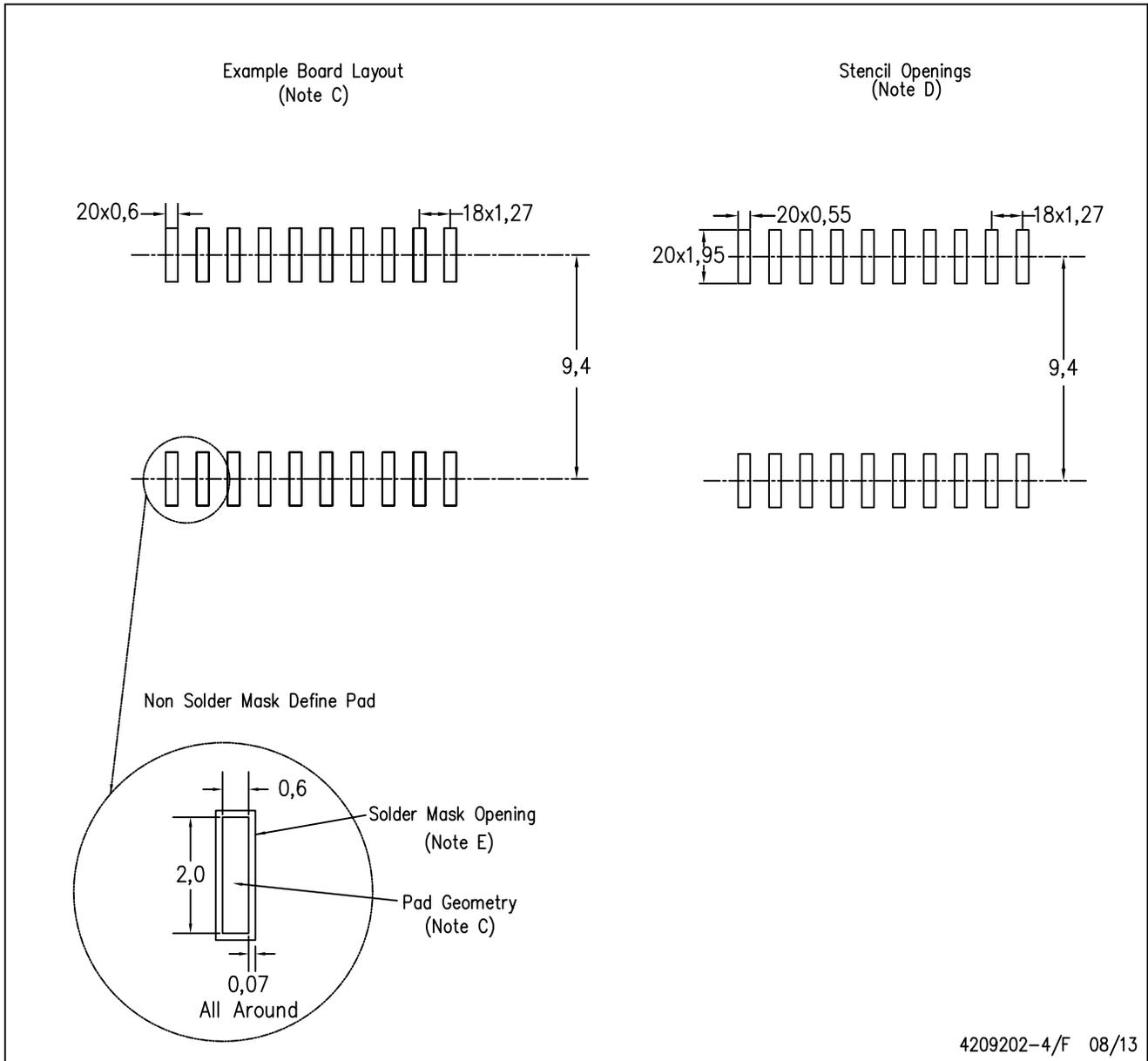
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
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| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
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