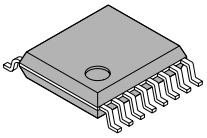
MB15FxxSL Series

Dual PLL Frequency Synthesizers with On-Chip Prescalers

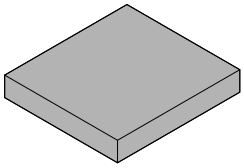
Description

The Fujitsu FxxSL series dual PLLs are serial input frequency synthesizers operating up to 2.5 GHz. They have built-in dual-modulus prescalers enabling pulse swallow operation. The latest advanced BiCMOS technology is used resulting in a super low supply current. A refined charge pump design (Fujitsu's Super Charger) provides fast tuning along with low spurious noise and phase noise characteristics. The F-series is ideally suited for digital mobile communications, including GSM, DCS1800, PCS1900, IS-136, IS-95: and ISM applications.

Packages



16-pin plastic SSOP,
FPT-16P-M05



16-pin plastic BCC,
LCC-16P-M06

Features

- MB15F02SL and MB15F03SL: RF and IF PLLs
- MB15F07SL and MB15F08SL: Dual RF PLLs
- Very low spurious and phase noise characteristics
- Low operating voltage: 2.4 to 3.6 volts
- Low operating current: 3.0 to 7.5 mA (typical)
- Power-saving current: 0.1µA (typical)
- Wide operating temperature: –40 to +85°C
- Plastic 16-pin SSOP and 16-pin BCC packages
- Reference counter:
  - 14-bit programmable divider: 3 to 16383
- 18-bit programmable divider:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 3 to 2047
- Software selectable charge pump current (±1.5 or ±6.0 mA)
- Evaluation Kits available

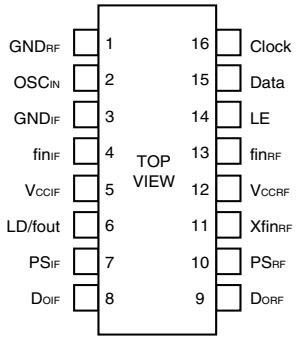
Parameter	MB15F02SL	MB15F03SL	MB15F07SL	MB15F08SL
RF Frequency of Operation, max.	1.2 GHz	1.75 GHz	1.1 GHz	2.5 GHz
IF/RF Frequency of Operation, max	500 MHz	600 MHz	1.1 GHz	1.1 GHz
Low Power Supply Voltage	2.7V	2.7V	2.7V	2.7V
Low Power Supply Current	3.0 mA	5.0 mA	5.0 mA	7.0 mA
Prescaler Divide Ratios	RF = 64/65 or 128/129, IF = 8/9 or 16/17		RF = 64/65 or 128/129 RF = 64/65 or 128/129	Rx = 32/33 or 64/65 Tx = 16/17 or 32/33
Power-Saving Function	0.1µA typ.			

Dual PLL Frequency Synthesizers with On-Chip Prescalers

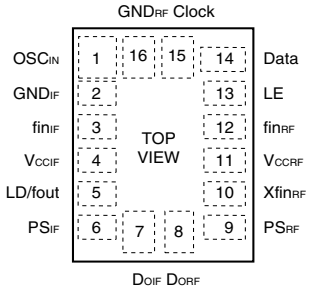
Table of Contents

Pin Descriptions: MB15F02SL, MB15F03SL

Pin No.		Pin Name	I/O	Descriptions
SSOP	BCC			
1	16	GND_{RF}	–	Ground for RF-PLL section
2	1	OSC_{IN}	I	Programmable reference divider input. TCXO should be connected via an AC coupling capacitor.
3	2	GND_{IF}	–	Ground for IF-PLL section
4	3	fin_{IF}	I	Prescaler input pin for IF-PLL Connection to an external VCO should be via AC coupling.
5	4	Vcc_{IF}	–	Power supply voltage input pin for IF-PLL section
6	5	LD/f_{OUT}	O	Lock detect signal output (LD)/phase comparator monitoring output (f_{OUT}) Output signal is selected by LDS bit in the serial data. LDS bit = "H" outputs fout signal. LDS bit = "L" ;outputs LD signal.
7	6	PS_{IF}	I	Power-saving mode control for IF-PLL section. This pin must be set at "L" during Power-ON. (Open is prohibited.) PS_{IF} = "H" sets normal mode. PS_{IF} = "L" sets power-saving mode.
8	7	Do_{IF}	O	Charge pump output for IF-PLL section Phase characteristics of phase detector can be selected via programming of the FC-bit.
9	8	Do_{RF}	O	Charge pump output for RF-PLL section Phase characteristics of phase detector can be selected via programming of the FC-bit.
10	9	PS_{RF}	I	Power-saving mode control for RF-PLL section. This pin must be set at "L" during Power-ON. (Open is prohibited.) PS_{RF} = "H" sets normal mode. PS_{RF} = "L" sets power-saving mode.
11	10	$Xfin_{RF}$	I	Prescaler complementary input for RF-PLL section Pin should be grounded via a capacitor.
12	11	Vcc_{RF}	–	Power supply voltage input pin for RF-PLL section, shift register and oscillator input buffer When power is OFF, latched data of RF-PLL is lost.
13	12	fin_{RF}	I	Prescaler input pin for RF-PLL Connection to an external VCO should be via AC coupling.
14	13	LE	I	Load enable signal input (with a Schmitt trigger input buffer) When the LE bit is set "H", data in shift register is transferred to corresponding latch according to control bit in the serial data.
15	14	Data	I	Serial data input (with a Schmitt trigger input buffer) Data is transferred to corresponding latch (IF-reference counter, IF-program counter, RF-reference counter, RF-program counter) according to control bit in the serial data.
16	15	Clock	I	Clock input for the 23-bit shift register (with a Schmitt trigger input buffer) One bit of data is shifted into shift register on a rising edge of the clock.

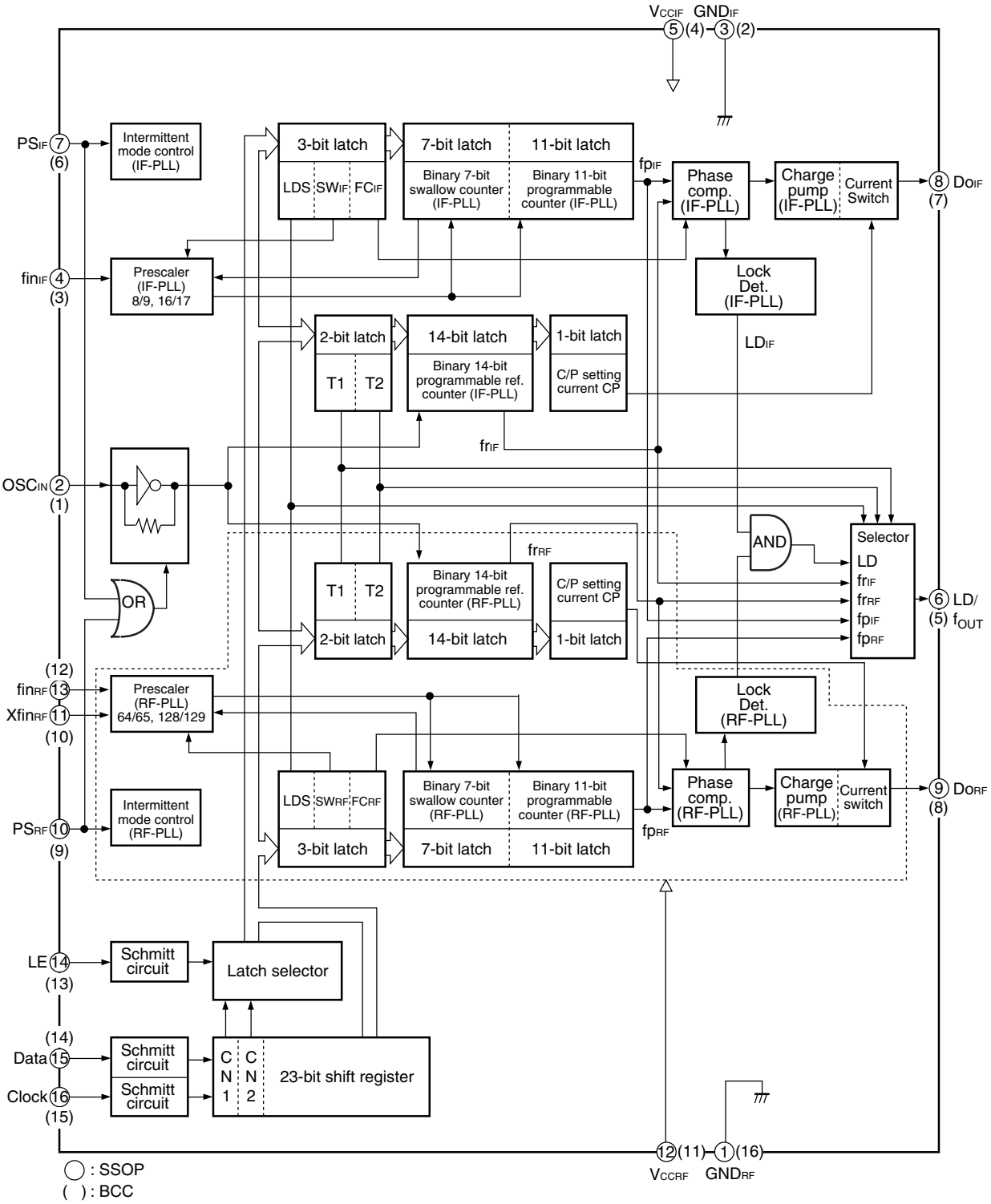


FPT-16P-M05



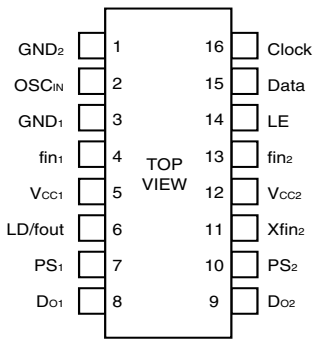
LCC-16P-M04

Block Diagram: MB15F02SL, MB15F03SL

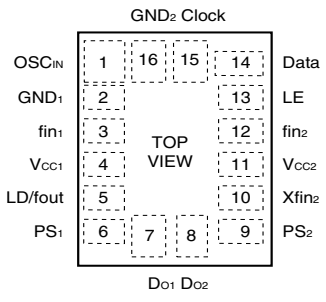


Pin Descriptions: MB15F07SL, MB15F08SL

Pin No.		Pin name	I/O	Descriptions
SSOP	BCC			
1	16	GND_2	–	Ground for PLL2 section
2	1	OSC_{IN}	I	Programmable reference divider input. TCXO should be connected via an AC coupling capacitor.
3	2	GND_1	–	Ground for PLL1 section
4	3	fin_1	I	Prescaler input pin for PLL1 Connection to an external VCO should be via AC coupling.
5	4	V_{CC1}	–	Power supply voltage input pin for PLL1 section
6	5	LD/fout	O	Lock detect signal output (LD)/phase comparator monitoring output (f_{OUT}) Output signal is selected by LDS bit in the serial data. LDS bit = "H" outputs f_{OUT} signal. LDS bit = "L" outputs LD signal.
7	6	PS_1	I	Power-saving mode control for PLL1 section. This pin must be set at "L" during Power-ON. (Open is prohibited.) PS_1 = "H" sets normal mode. PS_1 = "L" sets power-saving mode.
8	7	Do_1	O	Charge pump output for PLL1 section Phase characteristics of phase detector can be selected via programming of the FC-bit.
9	8	Do_2	O	Charge pump output for PLL2 section Phase characteristics of phase detector can be selected via programming of the FC-bit.
10	9	PS_2	I	Power-saving mode control for PLL2 section. This pin must be set at "L" during Power-ON. (Open is prohibited.) PS_2 = "H" sets normal mode. PS_2 = "L" sets power-saving mode.
11	10	$Xfin_2$	I	Prescaler complementary input for PLL2 section Pin should be grounded via a capacitor.
12	11	V_{CC2}	–	Power supply voltage input pin for PLL 2 section, shift register and oscillator input buffer When power is OFF, latched data of PLL2 is lost.
13	12	fin_2	I	Prescaler input pin for PLL2 Connection to an external VCO should be via AC coupling.
14	13	LE	I	Load enable signal input (with a Schmitt trigger input buffer) When LE bit is set "H", data in shift register is transferred to corresponding latch according to control bit in serial data.
15	14	Data	I	Serial data input (with a Schmitt trigger input buffer) Data is transferred to corresponding latch (PLL1-reference counter, PLL1-program counter, PLL2-reference counter, PLL2-program counter) according to control bit in the serial data.
16	15	Clock	I	Clock input for 23-bit shift register (with a Schmitt trigger input buffer) One bit of data is shifted into shift register on a rising edge of the clock.

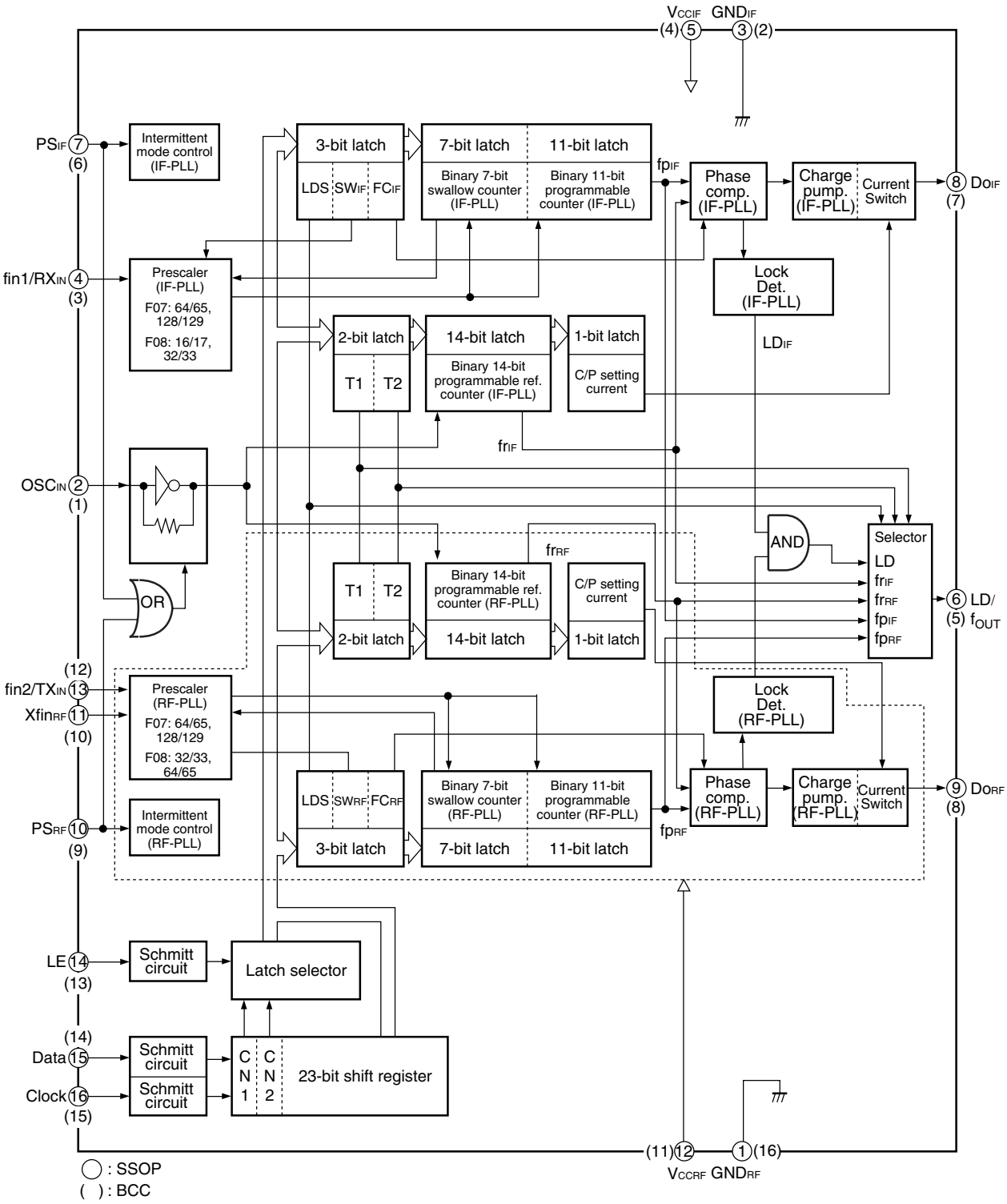


FPT-16P-M05



LCC-16P-M04

Block Diagram: MB15F07SL, MB15F08SL



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	–0.5 to +4.0	V	
Input voltage	V_I	–0.5 to V_{CC} +0.5	V	
Output voltage	V_O	–0.5 to V_{CC}	V	
Output Current	I_O	–10 to +10	mA	Except D_O
	I_{DO}	–25 to +25	mA	D_O output
Storage temperature	T_{STG}	–55 to +125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{CC}	2.7	3.0	3.6	V
Input voltage	V_I	GND	–	V_{CC}	V
Operating temperature	Ta	–40	–	+85	°C

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges. Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Fujitsu representative beforehand.

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

Electrical Characteristics

Device Specifications

V_{CC} = 2.4 to 3.6 V, Ta = –40 to +85°C

Parameter	Symbol	MB15F02SL	MB15F03SL	Symbol	MB15F07SL	MB15F08SL
Power supply current	I_{CCIF}*1	1.2 mA	1.2 mA	I_{CCPLL1}*1	2.5 mA	2.6 mA
	I_{CCRF}*1	1.8 mA	2.3 mA	I_{CCPLL2}*1	2.5 mA	4.4 mA
Power-saving current	I_{PSIF}*2	0.1µA	0.1µA	I_{PSPLL1}*2	0.1µA	0.1µA
	I_{PSRF}*2	0.1µA	0.1µA	I_{PSPLL2}*2	0.1µA	0.1µA
Operating frequency	fin_{IF}*3	50 - 500 MHz	50 - 600 MHz	fin_{PLL1},*3 Tx	0.1 - 1.1 GHz	0.1 - 1.1 GHz
	fin_{RF}	0.1 - 1.2 GHz	0.1 - 1.75 GHz	fin_{PLL2}, Rx	0.1 - 1.1 GHz	0.4 - 2.5 GHz
	OSCin*3	3 - 40 MHz	3 - 40 MHz	OSCin*3	3 - 40 MHz	3 - 40 MHz

General Specifications

Parameter		Symbol	Condition		Value Min.	Value Typ.	Value Max.	Unit
Input sensitivity	$fin_{IF, PLL1, Tx}$	$Pfin_{IF, PLL1, Tx}$	50Ω load system (Refer to measurement circuit)		–15*5,*6,*7,*8 (F08-10)	–	+2	dBm
	$fin_{RF, PLL2, Rx}$	$Pfin_{RF, PLL2, Rx}$	50Ω load system (Refer to measurement circuit)		–15*5,*6,*7,*8	–	+2	dBm
	OSC_{IN}	V_{OSC}			0.5	–	V_{CC}	Vp-p
Input voltage	Data, Clock, LE, PS, ZC	V_{IH}	–		$V_{CC} \times 0.7$	–		V
		V_{IL}	–		–	–	$V_{CC} \times 0.3$	
Input current	Data, Clock, LE, PS	I_{IH}*4	–		–1.0	–	+1.0	µA
		I_{IL}*4	–		–1.0	–	+1.0	
	OSC_{IN}	I_{IH}	–		0	–	+100	µA
		I_{IL}*4	–		–100	–	0	
Output voltage	LD/f_{OUT}	V_{OH}	V_{CC} = 3.0V, I_{OH} = –1 mA		V_{CC} –0.4	–		V
		V_{OL}	V_{CC} = 3.0V, I_{OL} = 1 mA		–	–	0.4	
	Do	V_{DOH}	V_{CC} = 3.0V, I_{OH} = –1 mA		V_{CC} –0.4	–		V
		V_{DOL}	V_{CC} = 3.0V, I_{OL} = 1 mA		–	–	0.4	
High impedance cutoff current	Do	I_{OFF}	V_{CC} = 3.0V V_{OFF} = .5V to Vcc-0.5V		–	–	2.5	nA
Output current	LD/fout	I_{OH}*4	V_{CC} = 3.0V		–1.0	–	–	mA
		I_{OL}	V_{CC} = 3.0V		–	–	1.0	mA
	Do	I_{DOH}*4	V_{CC} = 3.0 , V_{DOH} = V_{CC}/2, Ta = +25°C	CS bit = "H"	–	–6.0	–	mA
				CS bit = "L"	–	–1.5	–	mA
		I_{DOL}	V_{CC} = 3.0V, V_{DOL}= V_{CC}/2, Ta = +25°C	CS bit = "H"	–	6.0	–	mA
				CS bit = "L"	–	1.5	–	mA
Charge pump current characteristics	I_{DOL}/I_{DOH}	I_{DOMT}*9	V_{DO} = V_{CC}/2		–	3	–	%
	vs V_{DO}	I_{DOVD}*10	0.5V ≤ V_{DO} ≤ V_{CC} – 0.5V		–	10	–	%
	vs Ta	I_{DOTA}*11	–40°C ≤ Ta ≤ +85°C, V_{DO} = V_{CC}/2		–	10	–	%

Note: See footnotes on the following page.

Electrical Characteristics

*1 Conditions; fosc = 12 MHz, Ta = +25°C, in locking state. $V_{CCIF} = V_{CCRF} = 2.7$ V
*2 $V_{CCIF} = V_{CCRF} = 3.0$ V, fosc = 12.8 MHz, Ta = +25°C, in power saving mode.
*3 AC coupling. 1000pF capacitor is connected under the condition of minimum operating frequency.
*4 The symbol "–" (minus) means direction of current flow.

***5 MB15F02SL IF Input Sensitivity:**

Prescaler Divided Ratio	Charge Pump Current fin_{IF}	Operating Frequency	$Pfin_{IF}$(min)
16/17	1.5mA mode	50MHz ≦ fin ≦ 500MHz	–15dBm
	6.0mA mode	50MHz ≦ fin ≦ 300MHz	–15dBm
		300MHz < fin ≦ 500MHz	–10dBm
8/9	1.5mA mode	50MHz ≦ fin ≦ 300MHz*	–15dBm
		300MHz < fin ≦ 500MHz	–15dBm
	6.0mA mode	50MHz ≦ fin ≦ 300MHz*	–15dBm
		300MHz < fin ≦ 500MHz	–10dBm

* V_{CC} = 2.7V to 3.6V at 500MHz
V_{CC} = 2.4V to 3.6V, Ta = –40°C to +85°C at fin < 500MHz

***6 MB15F03SL IF Input Sensitivity:**

Prescaler Divided Ratio	Charge Pump Current fin_{IF}	Operating Frequency	$Pfin_{IF}$(min)
16/17	1.5mA mode	50MHz ≦ fin ≦ 600MHz	–15dBm
	6.0mA mode	50MHz ≦ fin ≦ 300MHz	–15dBm
		300MHz < fin ≦ 600MHz	–10dBm
8/9	1.5mA mode	50MHz ≦ fin ≦ 300MHz	–15dBm
		300MHz < fin ≦ 600MHz*	–15dBm
	6.0mA mode	50MHz ≦ fin ≦ 300MHz	–15dBm
		300MHz < fin ≦ 600MHz*	–10dBm

* V_{CC} = 3.0V to 3.6V at 600MHz

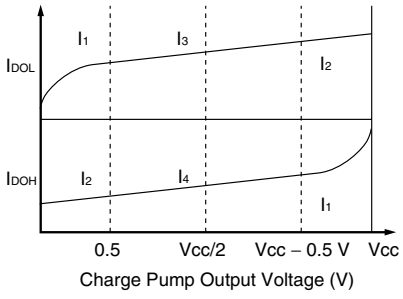
***7 MB15F07SL RF Input Sensitivity:**

	Prescaler Divided Ratio	Charge Pump Current	Pfin(min)
fin_1	64/65	1.5mA mode	–10dBm
		6.0mA mode	–10dBm
	128/129	1.5mA mode	–15dBm
		6.0mA mode	–15dBm
fin_2	64/65	1.5mA mode	–15dBm
		6.0mA mode	–10dBm
	128/129	1.5mA mode	–15dBm
		6.0mA mode	–15dBm

***8 MB15F08SL RF Input Sensitivity:**

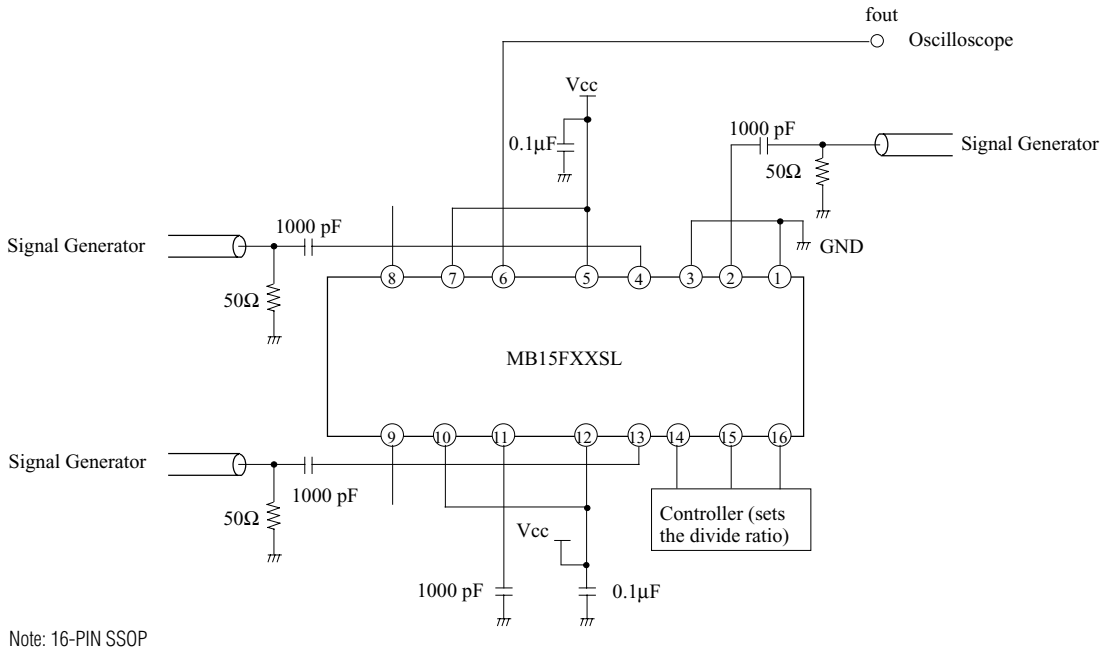
	fin operating frequency	Pfin(min)
fin Tx	100MHz ≦ fin ≦ 1100MHz	–10dBm
fin Rx	400MHz ≦ fin ≦ 2200MHz	–15dBm
	2200MHz ≦ fin ≦ 2500MHz	–10dBm

Charge Pump Characteristics (see diagram at right.)



*9 V_{CC} = 3.0 V, Ta = +25°C $(|I_3| - |I_4|)/[(|I_3| + |I_4|)/2] \times 100(\%)$
*10 V_{CC} = 3.0 V, Ta = +25°C $[(|I_2| - |I_1|)/2]/[(|I_1| + |I_2|)/2] \times 100(\%)$ (Applied to each I_{DOL}, I_{DOH})
*11 V_{CC} = 3.0 V, $[|I_{DO(85°C)} - I_{DO(-40°C)}|/2]/[|I_{DO(85°C)} + I_{DO(-40°C)}|/2] \times 100(\%)$ (Applied to each I_{DOL}, I_{DOH})

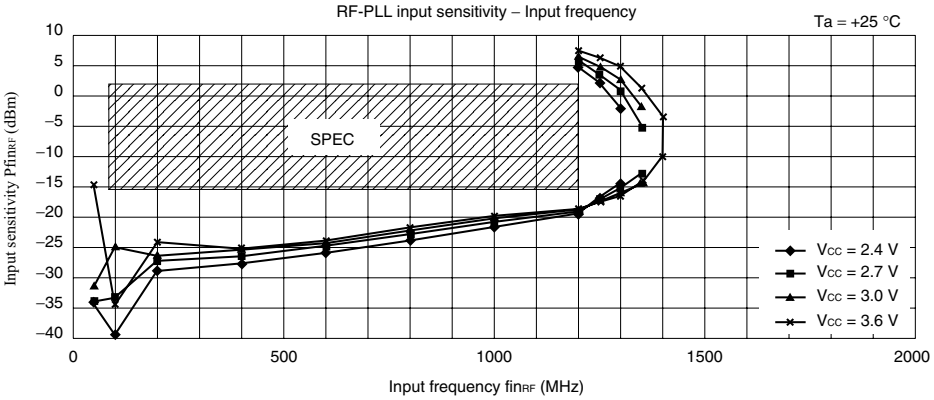
Measurement Circuit (For Measuring Input Sensitivity of f_{IN} and OSC_{IN})



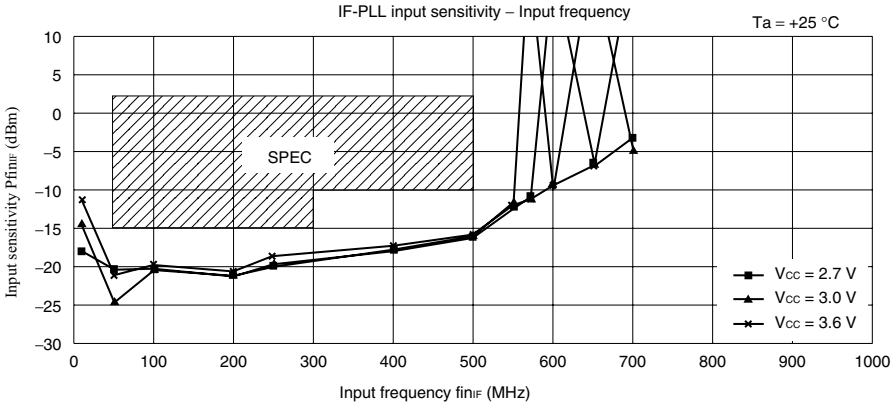
Note: 16-PIN SSOP

Typical Electrical Characteristics: MB15F02SL

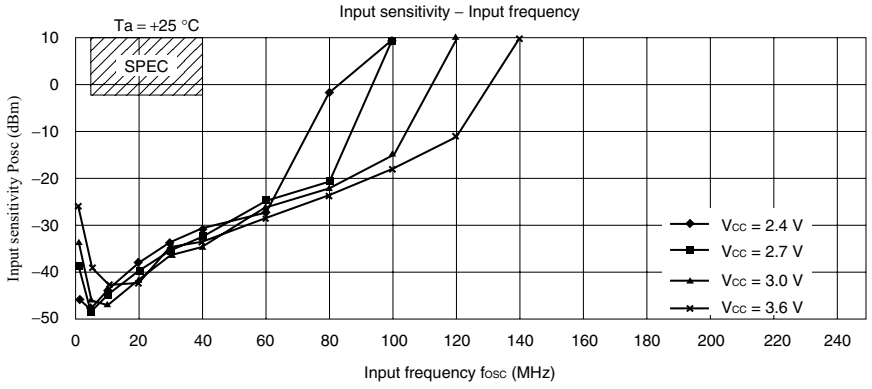
Input Sensivity of f_{IN} (RF) Versus Input Frequency



Input Sensivity of f_{IN} (IF) Versus Input Frequency



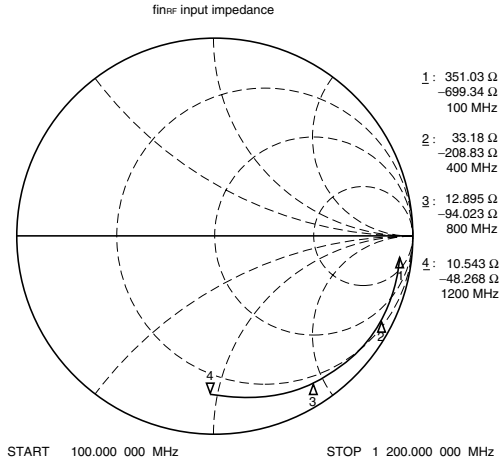
Input Sensivity of OSC_{IN} (IF) versus Input Frequency



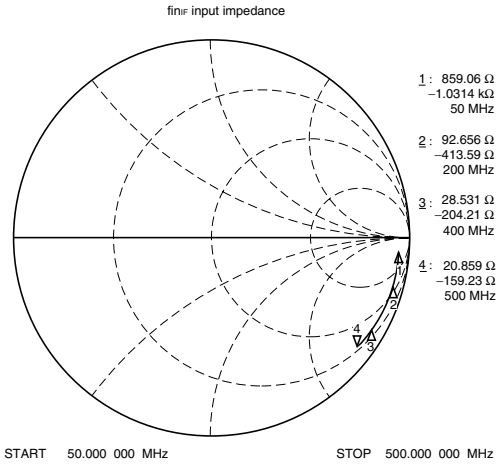
Typical Electrical Characteristics: MB15F02SL

Input Impedance

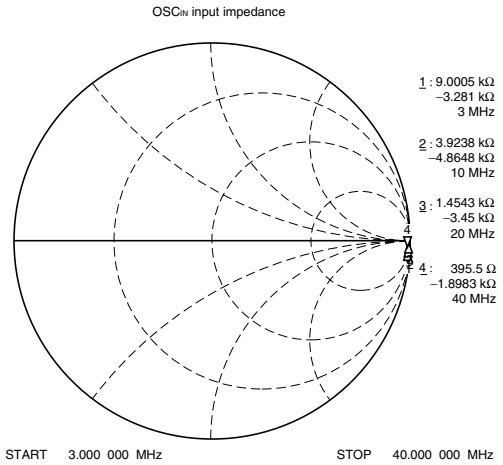
fin_{IF} Pin



fin_{RF} Pin



OSC_{IN} Pin

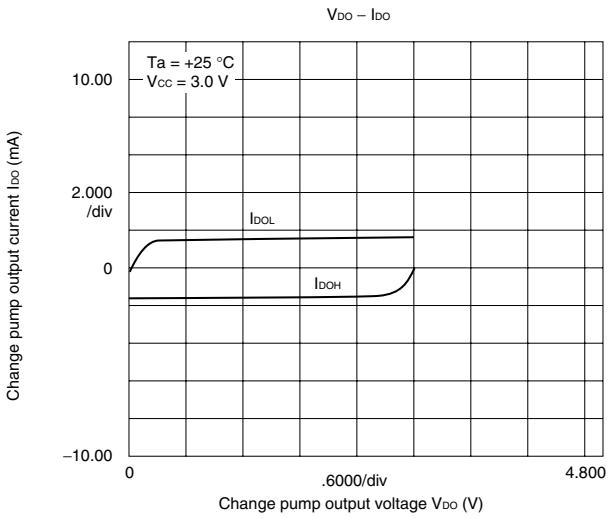


Typical Electrical Characteristics: MB15F02SL

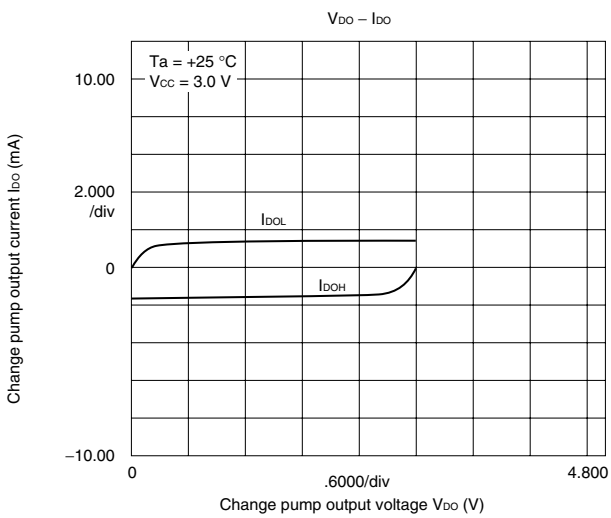
Conditions: Ta = +25°C
V_{CC}= 3.0V

Do ouput current: 1.5 mA mode

RF

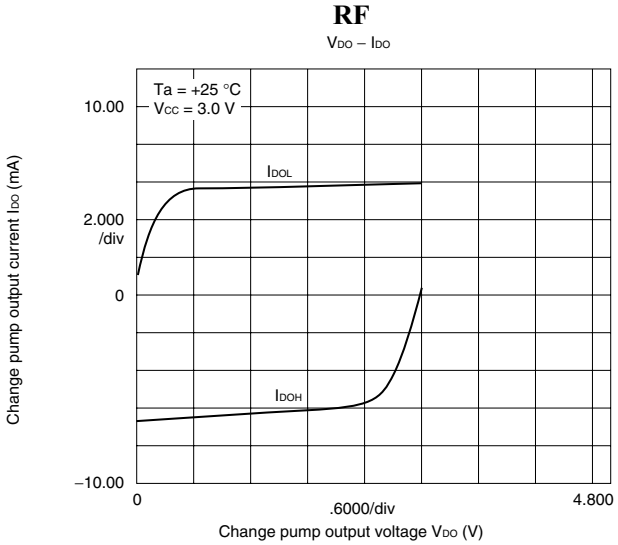


IF

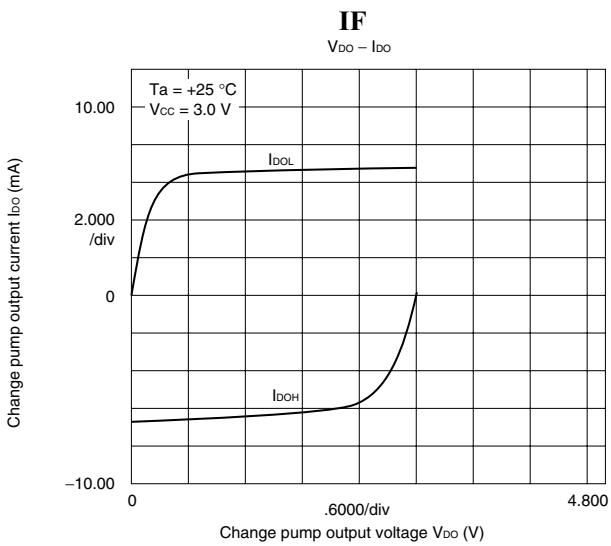


Do output current: 6.0 mA mode

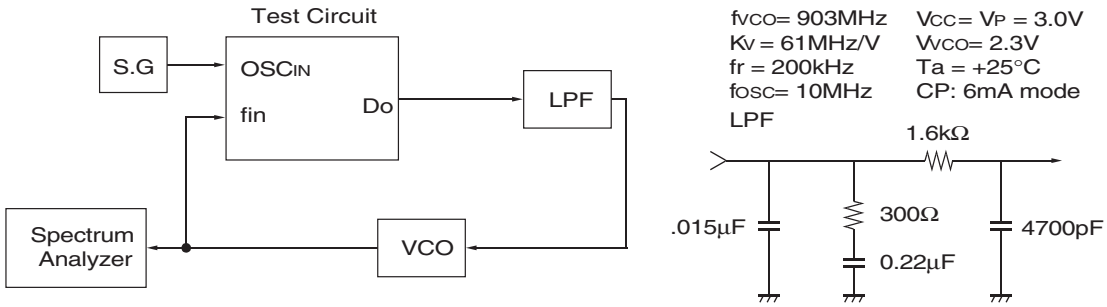
RF



IF

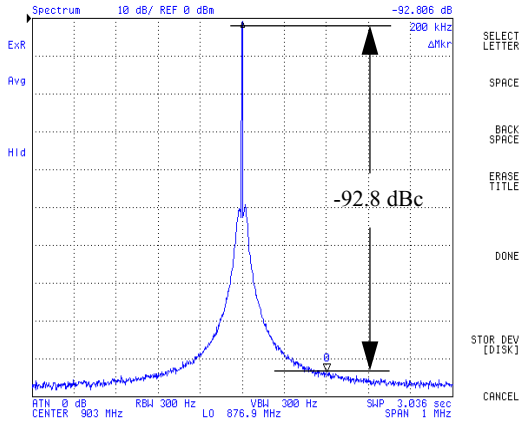


Reference Information: MB15F02SL

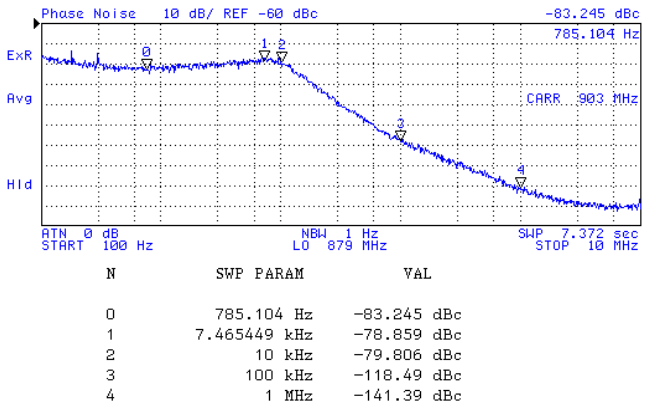


Typical plots measured with the test circuit are shown below. The plots show lock up time, phase noise and reference leakage.

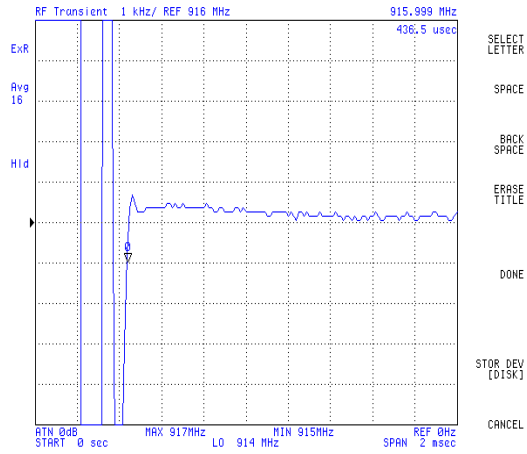
RF PLL Reference Leakage
@ 200 kHz offset = -92.8 dBc



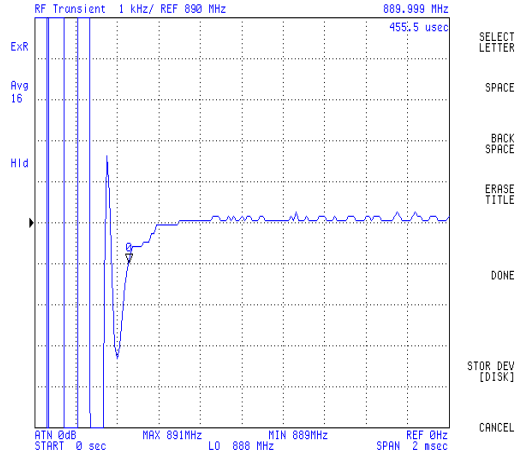
RF PLL Phase Noise
@ max within loop band = -78.8 dBc/Hz



RF PLL Lock Up Time = 437µs
890.000 MHz → 916.000 MHz, within ± 1kHz)

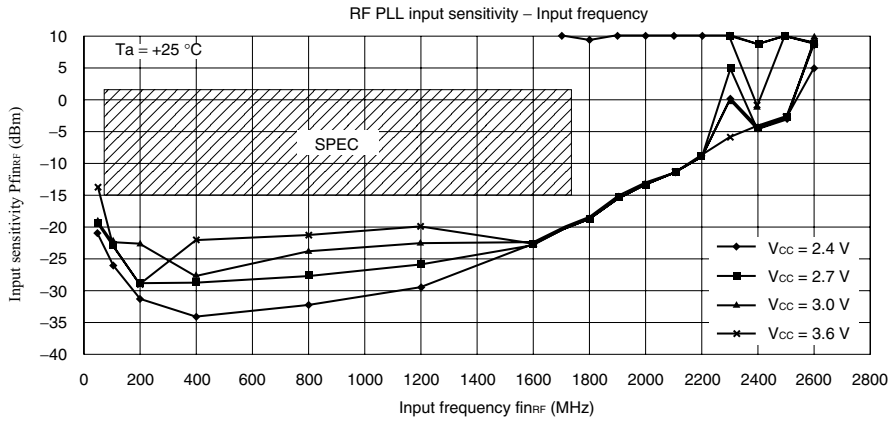


RF PLL Lock Up Time = 456µs
(916.000 MHz → 890.000 MHz, within ± 1kHz)

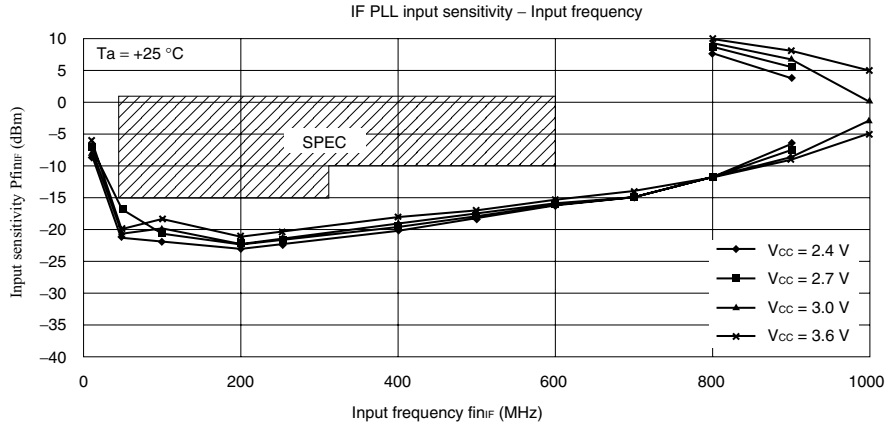


Typical Electrical Characteristics: MB15F03SL

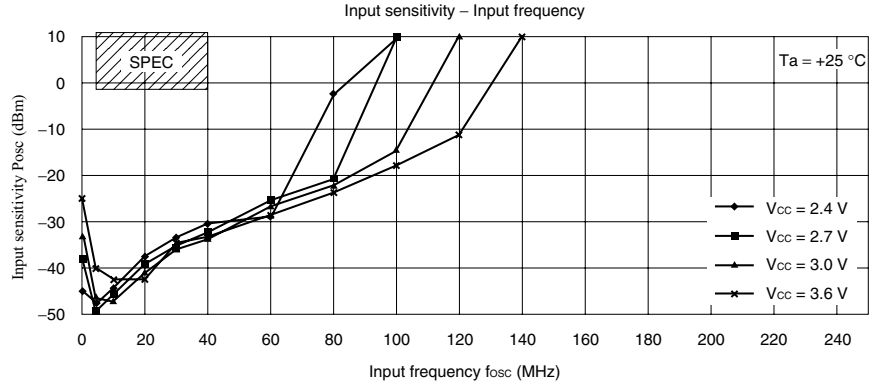
Input Sensivity of f_{IN} (RF) Versus Input Frequency



Input Sensivity of f_{IN} (IF) Versus Input Frequency



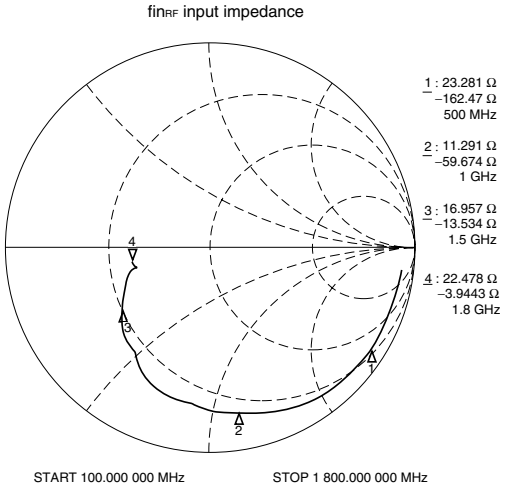
Input Sensivity of OSC_{IN} Versus Input Frequency



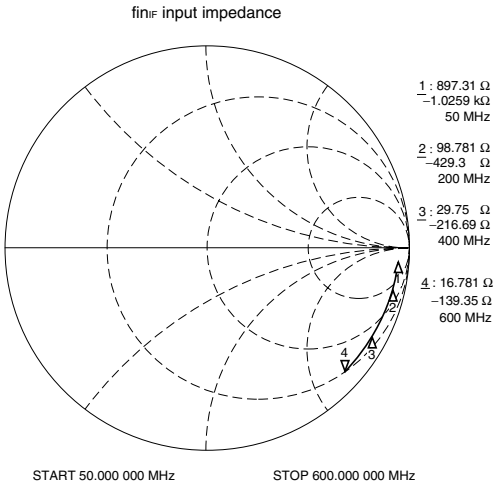
Typical Electrical Characteristics: MB15F03SL

Input Impedance

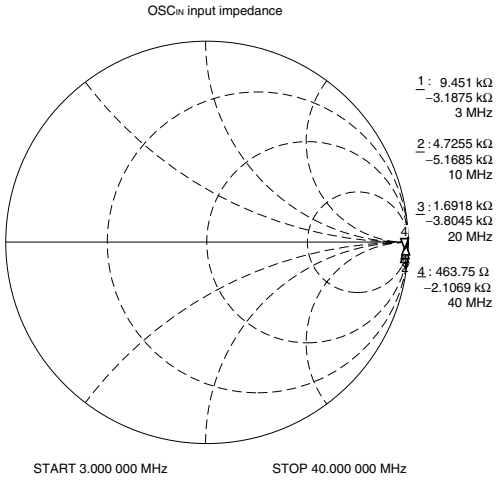
fin_{IF} Pin



fin_{RF} Pin



OSC_{IN} Pin

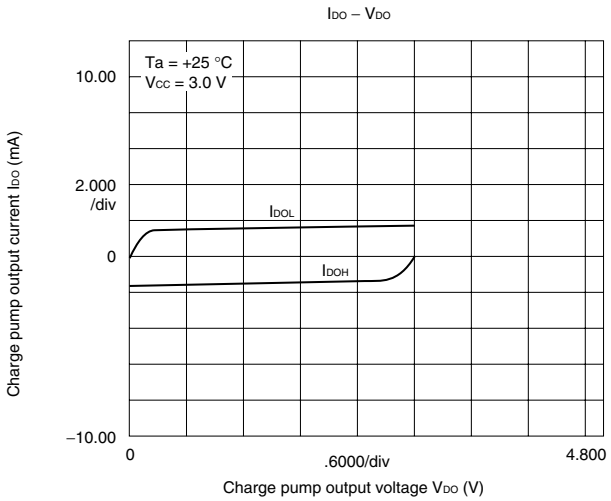


Typical Electrical Characteristics: MB15F03SL

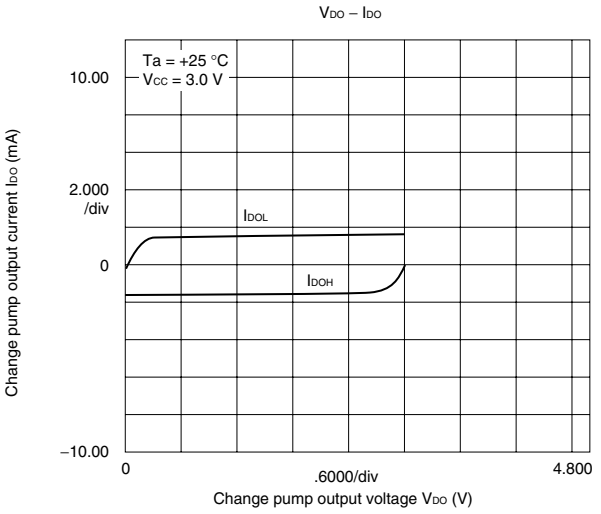
Conditions: Ta = +25°C
V_{CC}= 3.0V

Do output current: 1.5 mA mode

RF

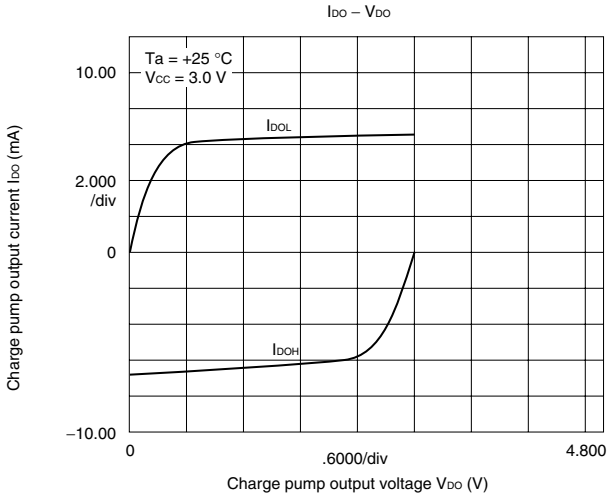


IF

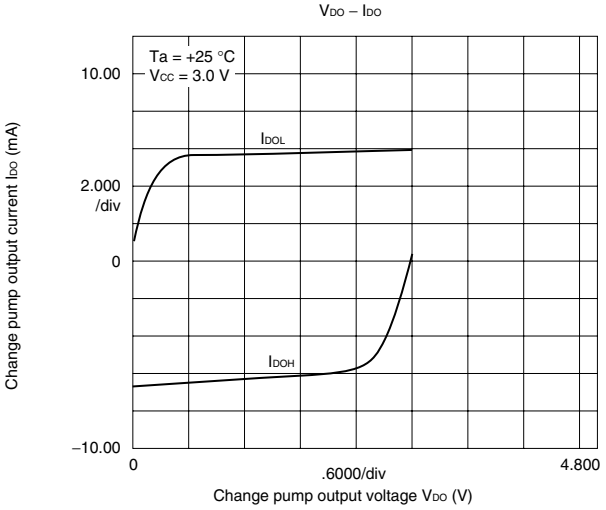


Do output current: 6.0 mA mode

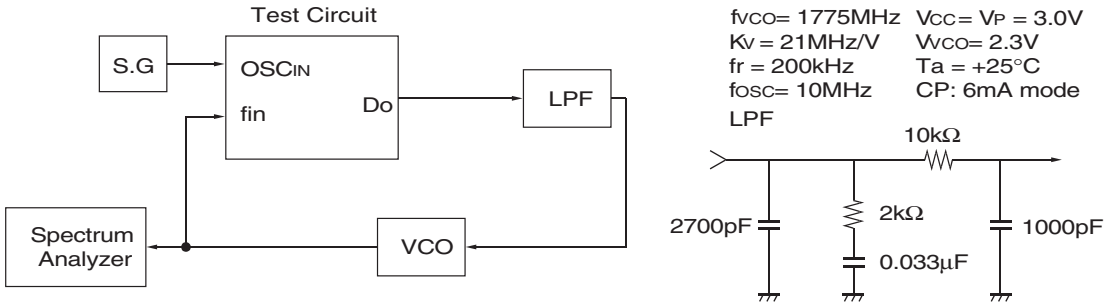
RF



IF

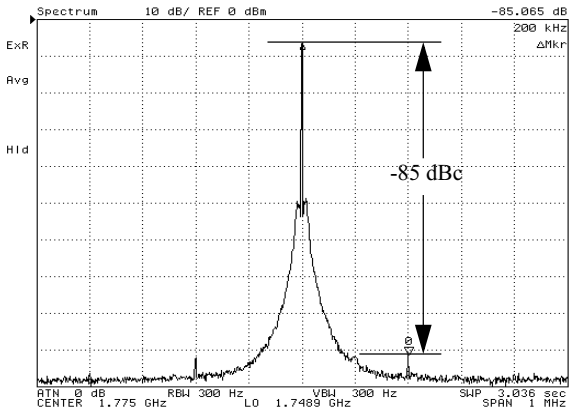


Reference Information: MB15F03SL

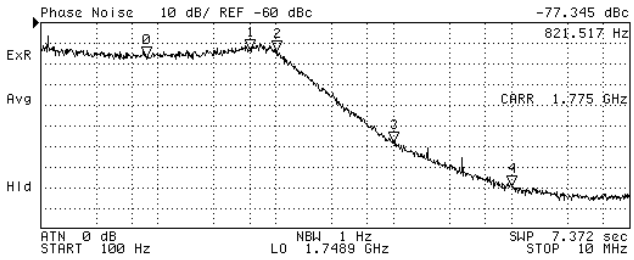


Typical plots measured with test circuit are shown below. The plots show lock up time, phase noise and reference leakage.

RF PLL Reference Leakage
@ 200 kHz offset = -85 dBc

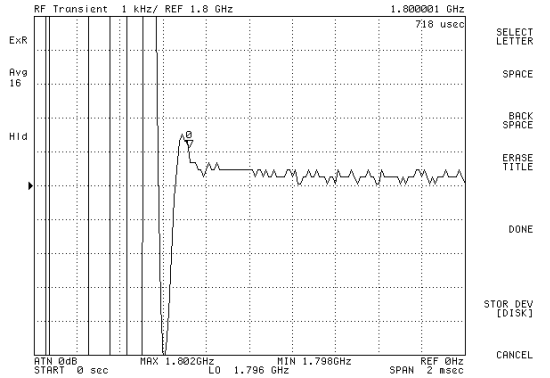


RF PLL Phase Noise
@ max within loop band = -73 dBc/Hz

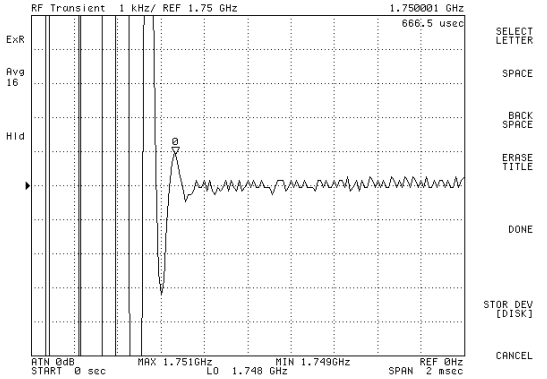


N	SWP PARAM	VAL
0	821.517 Hz	-77.345 dBc
1	6.051814 kHz	-73.711 dBc
2	10 kHz	-73.917 dBc
3	100 kHz	-118.37 dBc
4	1 MHz	-139.94 dBc

RF PLL Lock Up Time = 718µs
1750.000 MHz → 1800.000 MHz, within ± 1kHz)

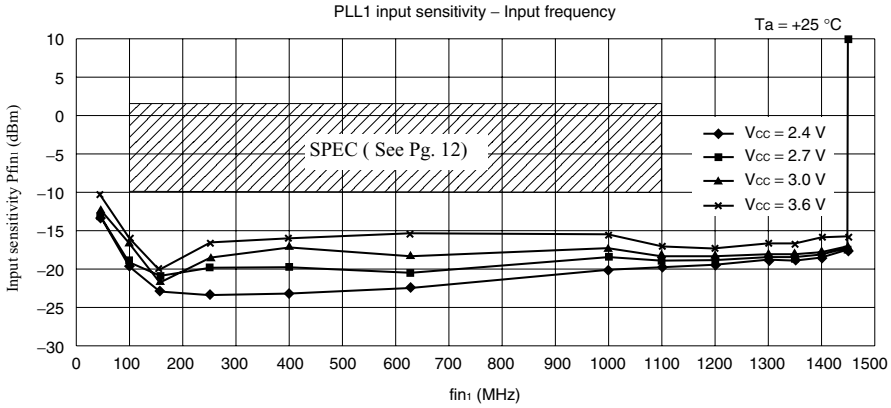


RF PLL Lock Up Time = 667µs
(1800.000 MHz → 1750.000 MHz, within ± 1kHz)

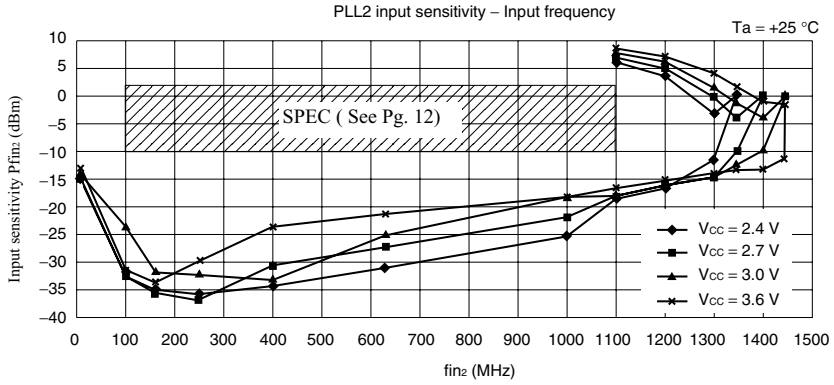


Typical Electrical Characteristics: MB15F07SL

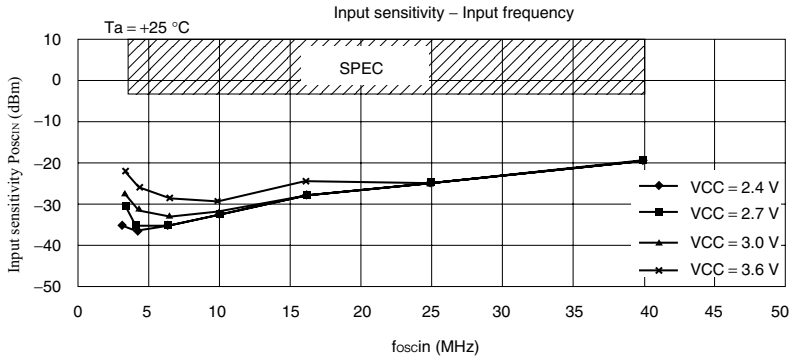
Input Sensivity of f_{IN} PLL1 Versus Input Frequency
(Prescaler set at 64/65, CP in 6.0mA mode)



Input Sensivity of f_{IN} PLL2 Versus Input Frequency
(Prescaler set at 64/65, CP in 6.0mA mode)



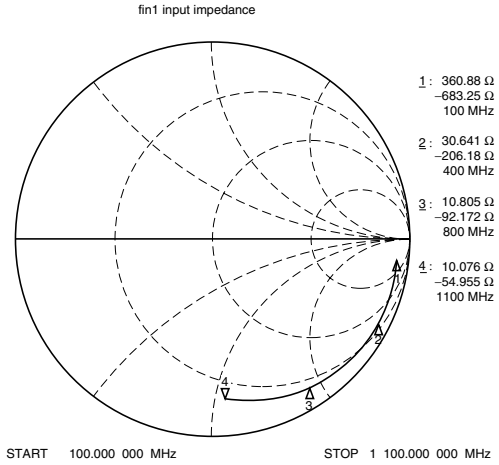
Input Sensivity of OSC_{IN} Versus Input Frequency



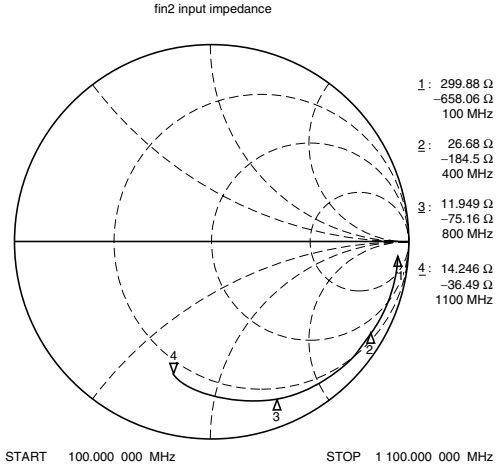
Typical Electrical Characteristics: MB15F07SL

Input Impedance

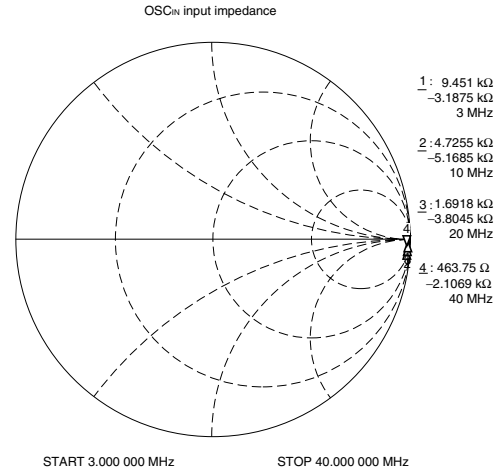
fin_{PLL1} Pin



fin_{PLL2} Pin



OSC_{IN} Pin

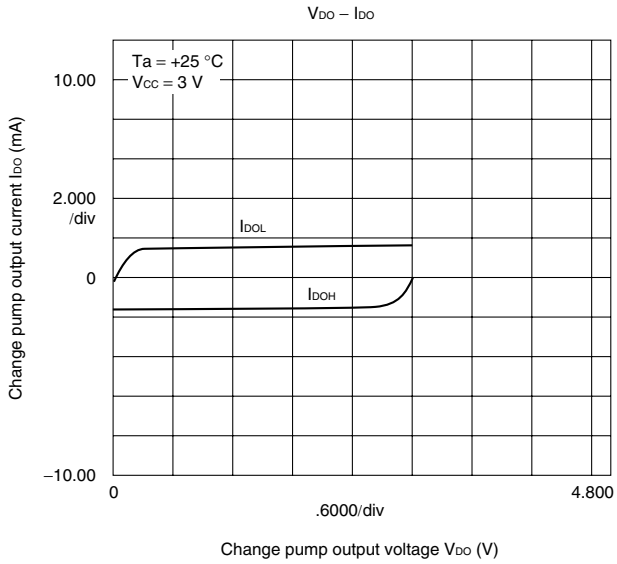


Typical Electrical Characteristics: MB15F07SL

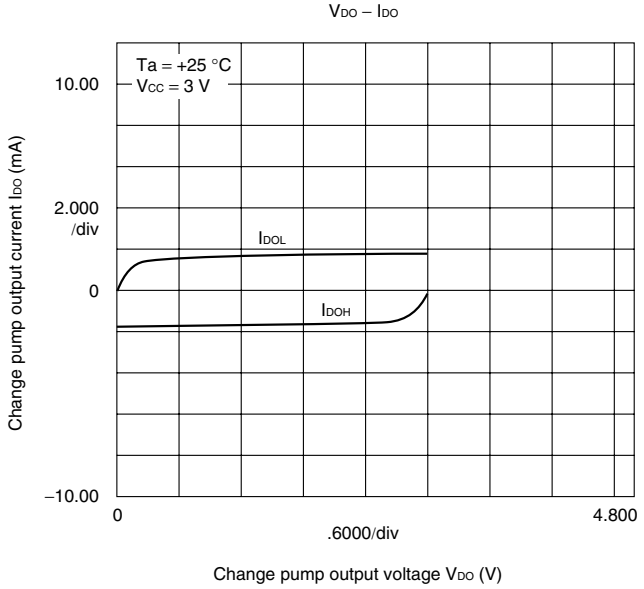
Conditions: Ta = +25°C
V_{CC}= 3.0V

Do output current: 1.5 mA mode

PLL1

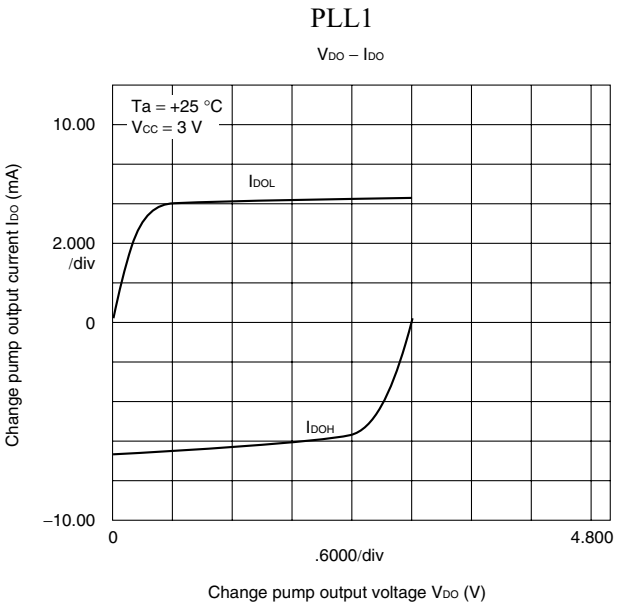


PLL2

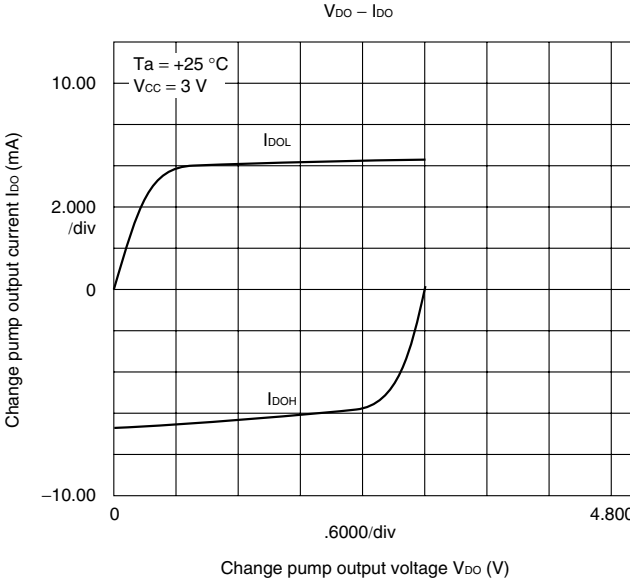


Do output current: 6.0 mA mode

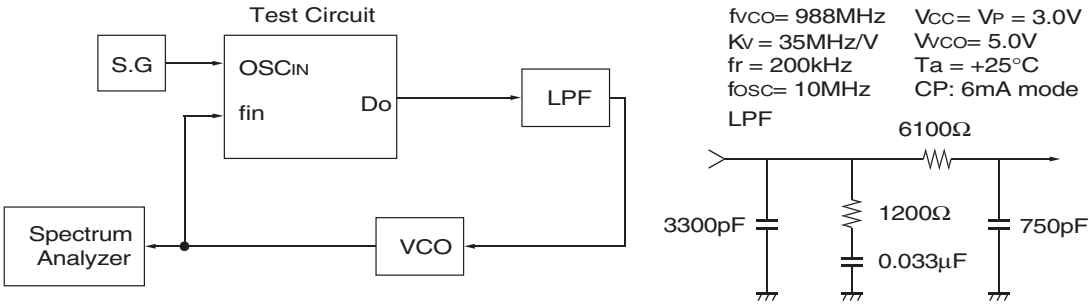
PLL1



PLL2

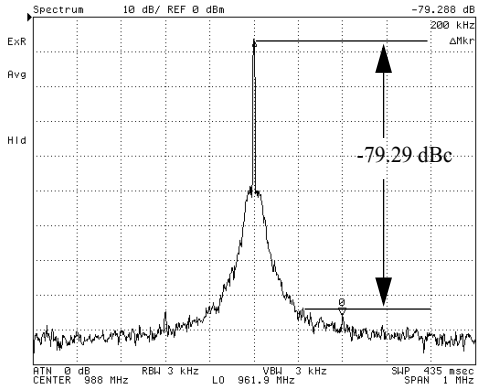


Reference Information: MB15F07SL

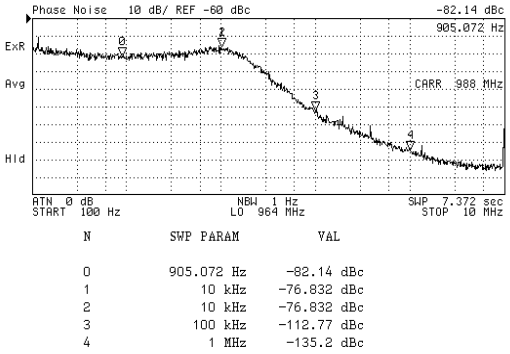


Typical plots measured with test circuit are shown below. The plots show lock up time, phase noise and reference leakage.

PLL1, PLL2 Reference Leakage
@ 200 kHz offset = -79.3 dBc

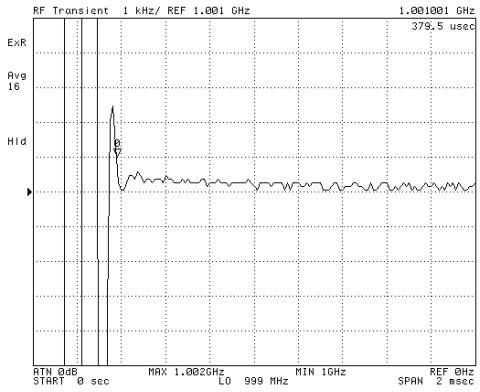


PLL1, PLL2 Phase Noise
@ max within loop band = -76.8 dBc/Hz

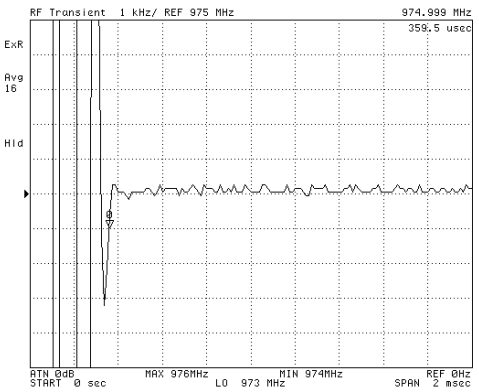


N	SWP PARAM	VAL
0	905.072 Hz	-82.14 dBc
1	10 kHz	-76.832 dBc
2	10 kHz	-76.832 dBc
3	100 kHz	-112.77 dBc
4	1 MHz	-135.2 dBc

RF PLL Lock Up Time = 380µs
(975.000 MHz → 1001.000 MHz, within ± 1kHz)

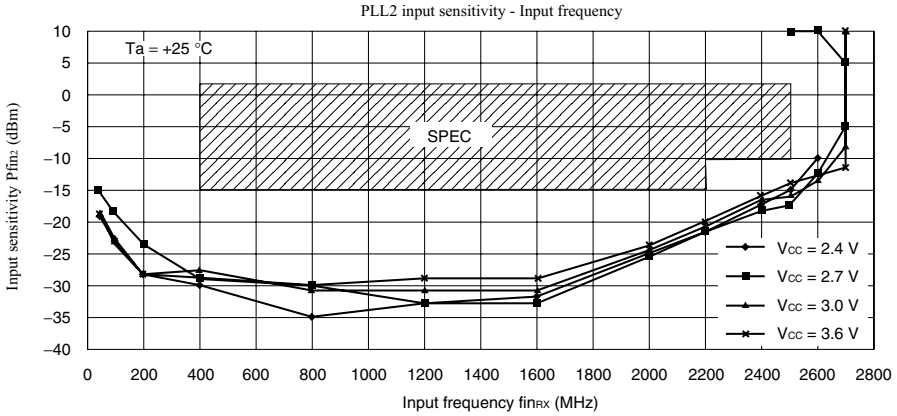


RF PLL Lock Up Time = 360µs
(1001.000 MHz → 975.000 MHz, within ± 1kHz)

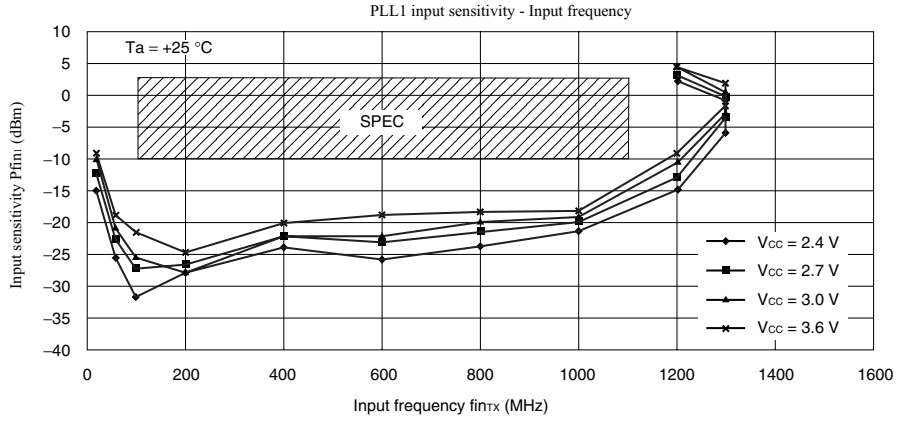


Typical Electrical Characteristics: MB15F08SL

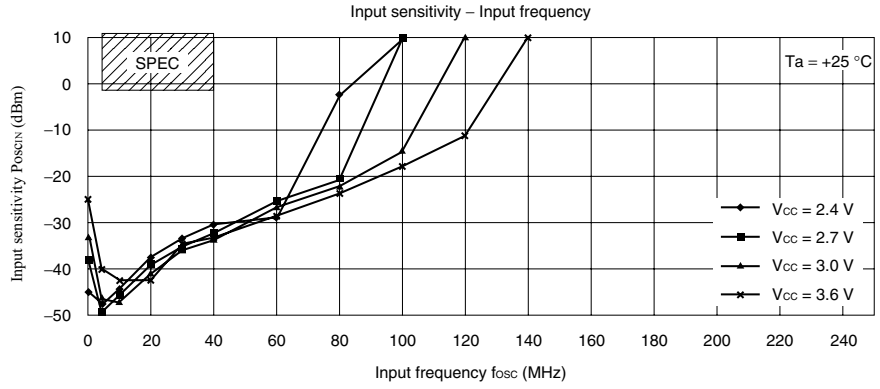
Input Sensivity of f_{IN} PLL2 Versus Input Frequency



Input Sensivity of f_{IN} PLL1 Versus Input Frequency



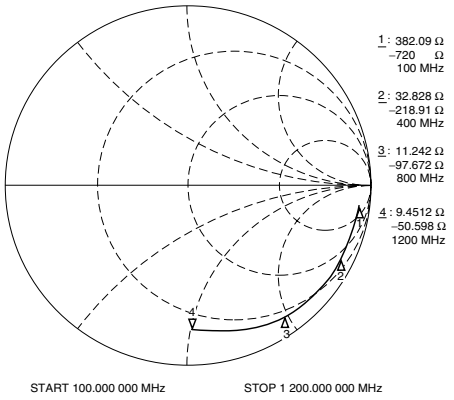
Input Sensivity of OSC_{IN} Versus Input Frequency



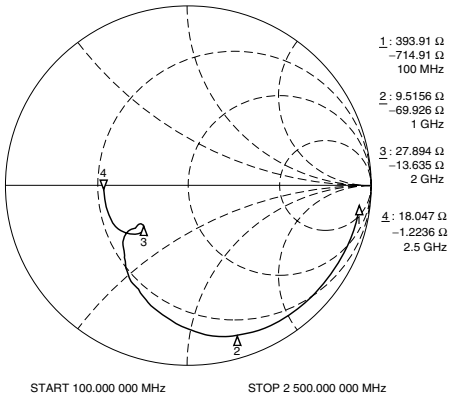
Typical Electrical Characteristics: MB15F08SL

Input Impedance

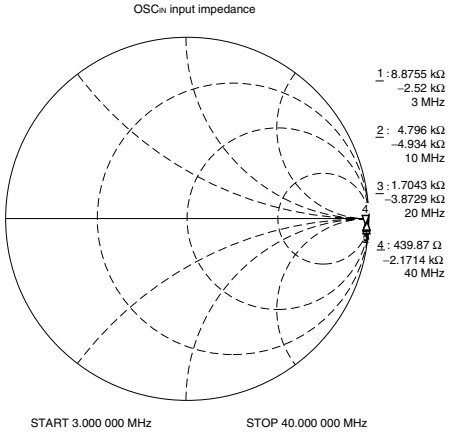
fin_{PLL2} Pin



fin_{PLL1} Pin



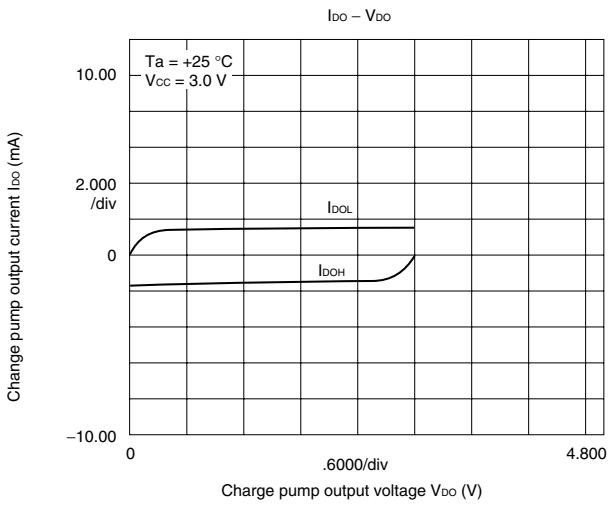
OSC_{IN} Pin



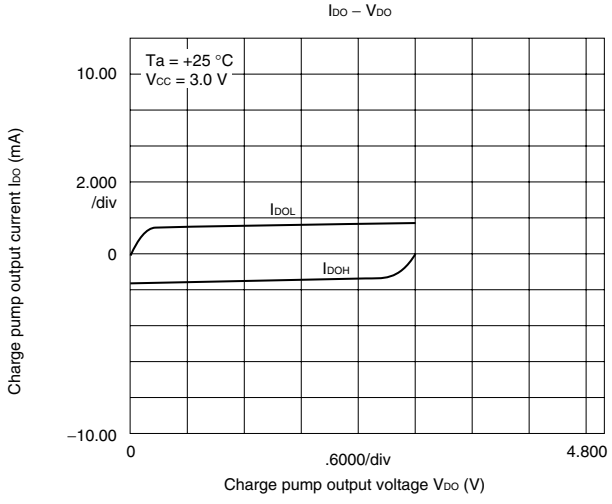
Typical Electrical Characteristics: MB15F08SL

Do output current: 1.5 mA

PLL1

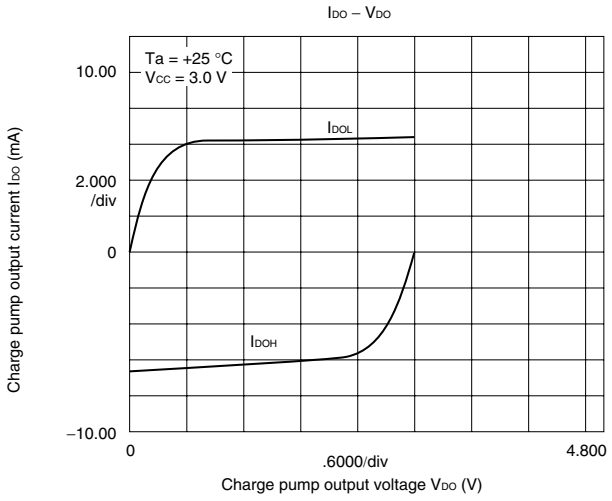


PLL2

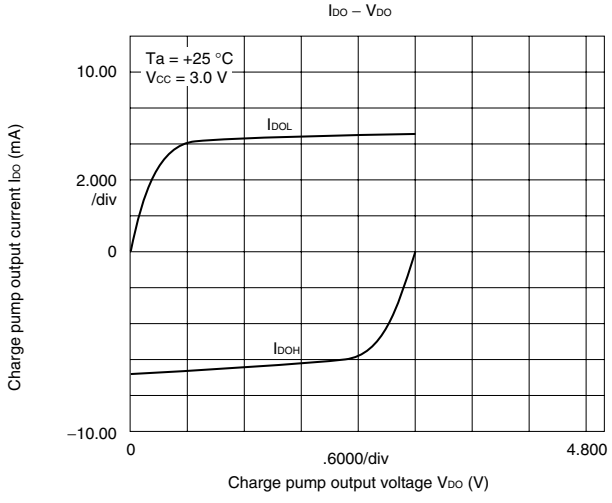


Do output current: 6.0 mA mode

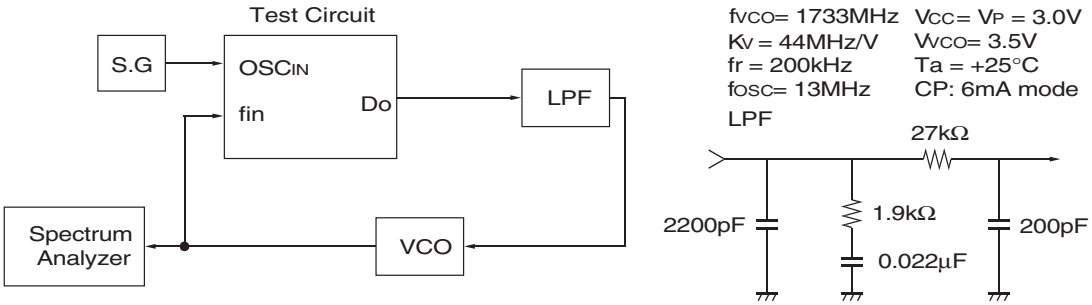
PLL1



PLL2



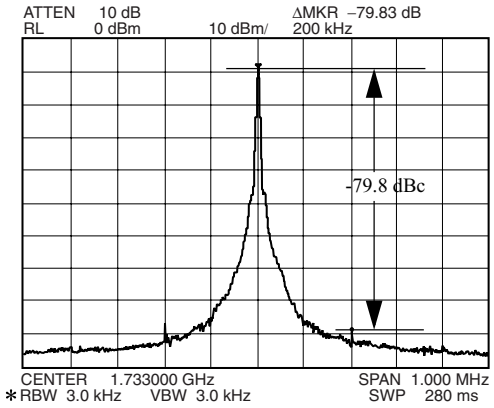
Reference Information: MB15F08SL



Typical plots measured with test circuit are shown below. The plots show lock up time, phase noise and reference leakage.

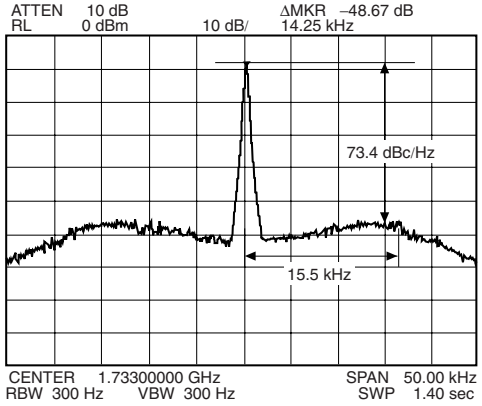
PLL2 Reference Leakage

@ 200 kHz offset = -79.8 dBc



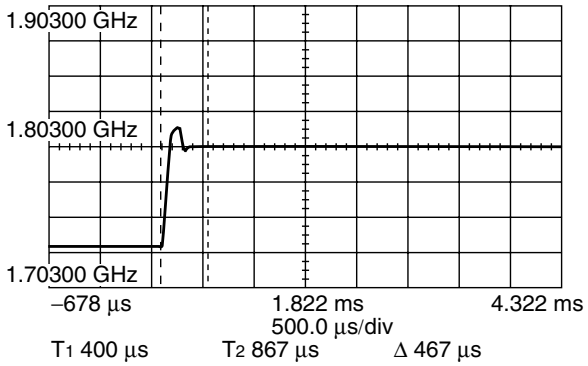
PLL2 Phase Noise

@ max within loop band = -73.4 dBc/Hz



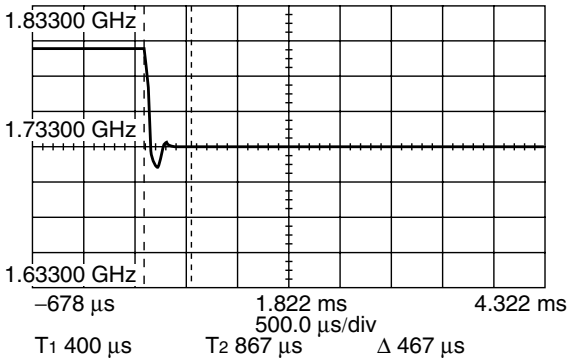
PLL2 Lock Up Time = 467 s

(1733.000 MHz → 1803.000 MHz, within ± 1kHz)



PLL2 Lock Up Time = 467 s

(1803.000 MHz → 1733.000 MHz, within ± 1kHz)



Functional Descriptions

The VCO output frequency can be calculated using the following equation:

$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} \div R \; (A < N)$

f_{VCO} Output frequency of external voltage controlled ocillator (VCO)
M Preset divide ratio of dual modulus prescaler (8, 16, 32, 64 or 128 for IF PLL or PLL1) (32, 64 or 128 for RF PLL or PLL2)
N Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
f_{OSC} Reference oscillation frequency
R Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

Serial Data Input

The serial data is entered using the Data, Clock and LE pins. The serial data controls the programmable reference counters and the programmable counters separately.

The binary serial data is entered through the Data pin when the LE pin is held low. One bit of data is shifted into the shift register on the rising edge of the Clock. When the LE signal pin is taken high, entered data is latched into the appropriate counters according to the control bit settings as follows:

Table 1. Control Bits

Control bit		Destination of serial data
CN1	CN2	
L	L	Programmable reference counter for IF-PLL or PLL1, Tx
H	L	Programmable reference counter for RF-PLL or PLL2, Rx
L	H	Programmable counter and swallow counter for IF-PLL or PLL1, Tx
H	H	Programmable counter and swallow counter for RF-PLL or PLL2, Rx

Shift Register Configuration

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	CS	X	X	X	X

CNT1, 2 Control bits [Table 1]
R1 to R14 Divide ratio setting bits for the programmable reference counter (3 to 16,383) [Table 2]
T1, 2 Test purpose bits [Table 3]
CS Charge pump current select bit [Table. 9]
X Dummy bits(set “0” or “1”)
Note: Input Data with MSB first.

Functional Descriptions

Programmable Counter

LSB ← Data Flow → MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	SW	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CNT1, 2	Control bits	[Table 1]
N1 to N14	Divide ratio setting bits for the programmable counter (3 to 2,047)	[Table 4]
A1 to A7	Divide ratio setting bits for the swallow counter (0 to 127)	[Table 5]
MB15F02SL, MB15F03SL:		[Table 6]
$SW_{IF/RF}$	Divide ratio setting bit for the prescaler (8/9 or 16/17 for the IF-PLL, 64/65 or 128/129 for the RF-PLL)	
MB15F07SL:		
$SW_{PLL1/PLL2}$	Divide ratio setting bit for the prescaler (64/65 or 128/129 for PLL1 and PLL2)	
MB15F08SL:		
$SW_{Tx/Rx}$	Divide ratio setting bit for the prescaler (16/17or 32/33 for PLL1, 32/33 or 64/65 for PLL2)	
FC	Phase control bit for the phase detector ($FC_{IF/PLL1}$, $FC_{RF/PLL2}$)	[Table 7]
LDS	LD/f_{OUT} signal select bit	[Table 8]

Note: Input Data with MSB first.

Table 2. Binary 14-Bit Programmable Reference Counter Data Setting

Divide ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 3. Test Purpose Bit Setting

T1	T2	LD/f_{OUT} Pin State
L	L	Outputs $fr_{IF/PLL1/Tx}$
H	L	Outputs $fr_{RF/PLL2/Rx}$
L	H	Outputs $fp_{IF/PLL1/Tx}$
H	H	Outputs $fp_{RF/PLL2/Rx}$

Functional Descriptions

Table 4. Binary 11-Bit Programmable Counter Data Setting

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 5. Binary 7-Bit Swallow Counter Data Setting

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

Table 6. Prescaler Data Setting for MB15F02SL, MB15F03SL

Prescaler Divide Ratio	SW = "H"	SW = "L"
IF-PLL	8/9	16/17
RF-PLL	64/65	128/129

Prescaler Data Setting for MB15F07SL

Prescaler Divide Ratio	SW = "H"	SW = "L"
PLL1	64/65	128/129
PLL2	64/65	128/129

Prescaler Data Setting for MB15F08SL

Prescaler Divide Ratio	SW = "H"	SW = "L"
PLL Tx	16/17	32/33
PLL Rx	32/33	64/65

Functional Descriptions

Table 7. Phase Comparator Phase Switching Data Setting

	$FC_{IF/PLL1,RF/PLL2}$ = H	$FC_{IF/PLL1,RF/PLL2}$ = L
	$Do_{IF/PLL1,RF/PLL2}$	
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO polarity	(1)	(2)

Notes: Z = High-impedance
FC bit should be set depending upon VCO and LPF polarity

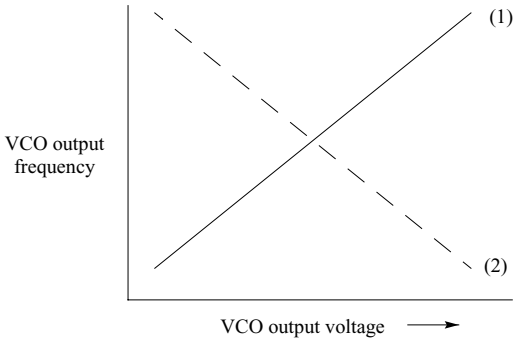


Table 8. LD/f_{OUT} Output Select Data Setting

LDS	LD/f_{OUT} Output Signal
H	f_{OUT} signals
L	LD signals

Table 9. Charge Pump Current Setting

CS	Current Value
H	± 6.0 mA
L	± 1.5 mA

Power-Saving Mode (Intermittent Mode Control)

The Intermittent Mode Control circuit greatly reduces the PLL power consumption by shutting down various internal functions, as shown in Table 11, depending upon the settings of the power-save (PS) pins. (See the Electrical Characteristics chart for the specific value of current when in the power-saving mode.)

The phase detector output, Do, becomes high impedance.

The lock detector output, LD, is as shown in Table 13.

Setting the PS pin high releases the power-saving mode returning the selected PLL to normal operation.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation, at which time, the phase comparator output signal is unpredictable due to the unknown relationship between the comparison frequency (fp) and the reference frequency (fr). This can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lock-up time.

To prevent a major VCO frequency jump, the Intermittent Mode Control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

Note: When power (V_{CC}) is first applied, the device must be in standby mode, PS = Low, for at least 1 µs.

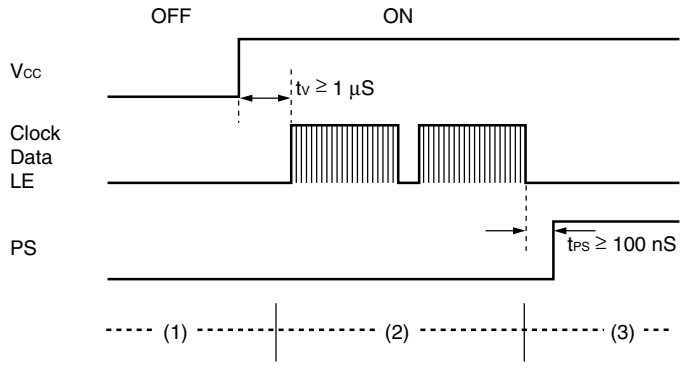
Table 10. Power-Save Pin Setting

PS Pins	Status
H	Normal mode
L	Power-saving mode

Table 11. Power-Save Internal Shutdown Logic

PS_{IF}	PS_{RF}	IF (TX)-PLL counters	RF (RX)-PLL counters	OSC input buffer
L	L	OFF	OFF	OFF
H	L	ON	OFF	ON
L	H	OFF	ON	ON
H	H	ON	ON	ON

Power-ON Timing



(1) PS = L (power-saving mode) at Power ON

(2) Set serial data 1 µs later after power supply remains stable ($V_{CC} \geq 2.2V$).

(3) Release power-saving mode (PS: L → H) 100 ns later after setting serial data.

Serial Data Input Timing

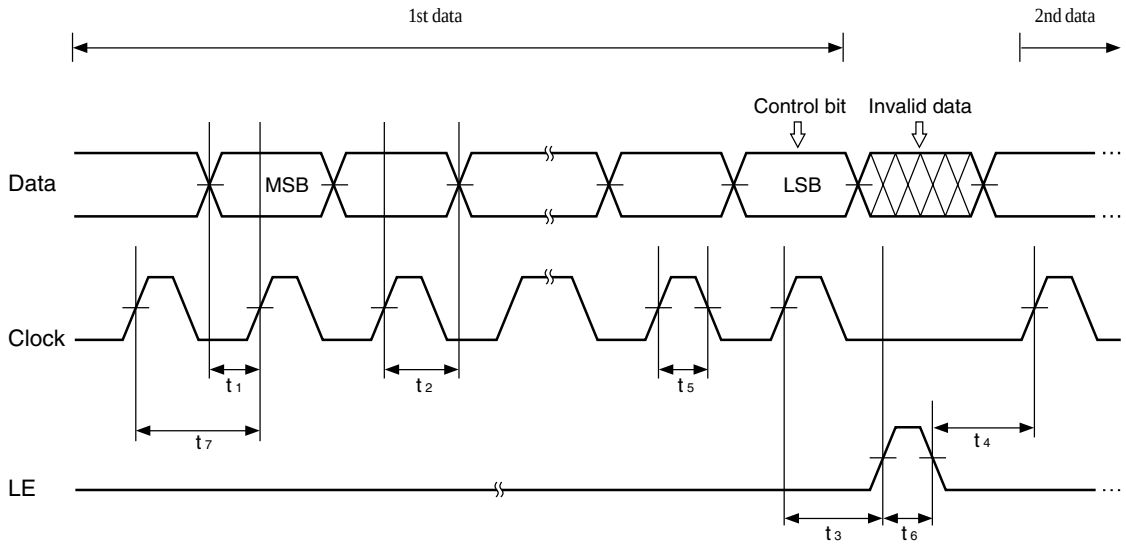


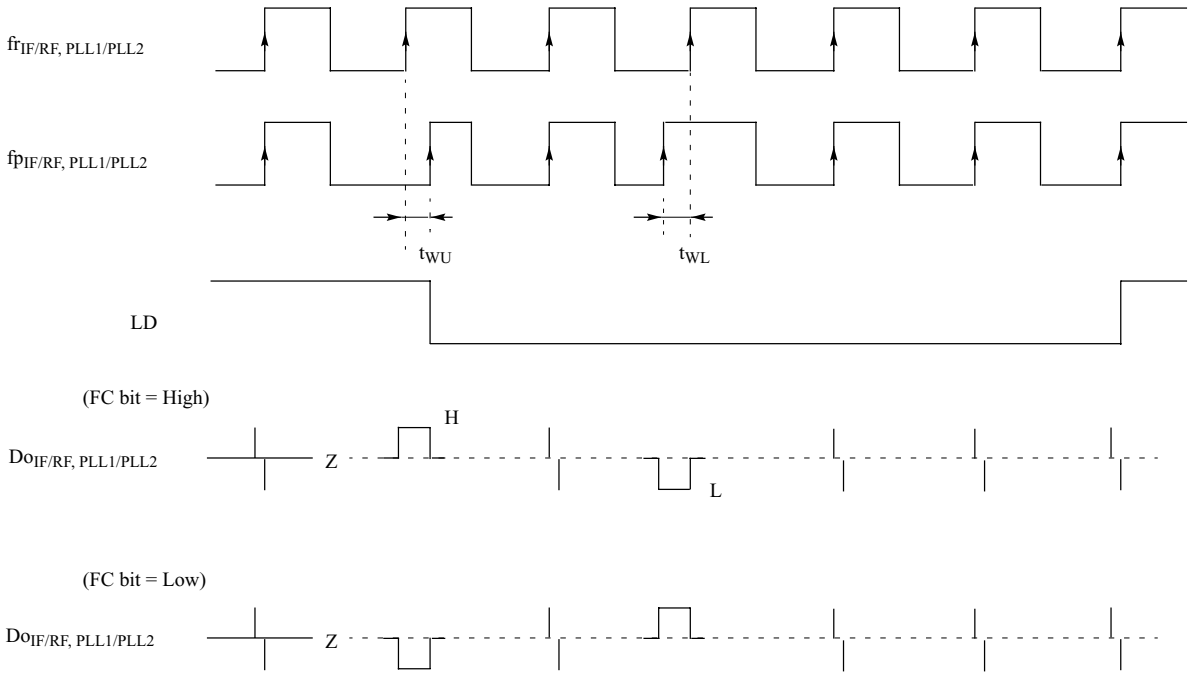
Table 12. Timing Parameters

Parameter	Min.	Typ.	Max.	Unit	Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns	t5	100	–	–	ns
t2	20	–	–	ns	t6	20	–	–	ns
t3	30	–	–	ns	t7	100	–	–	ns
t4	30	–	–	ns					

Notes: 1) On the rising edge of the clock, one bit of the data is transferred into the shift register.

2) LE should be “L” when the data is transferred into the shift register.

Phase Detector Output Waveform

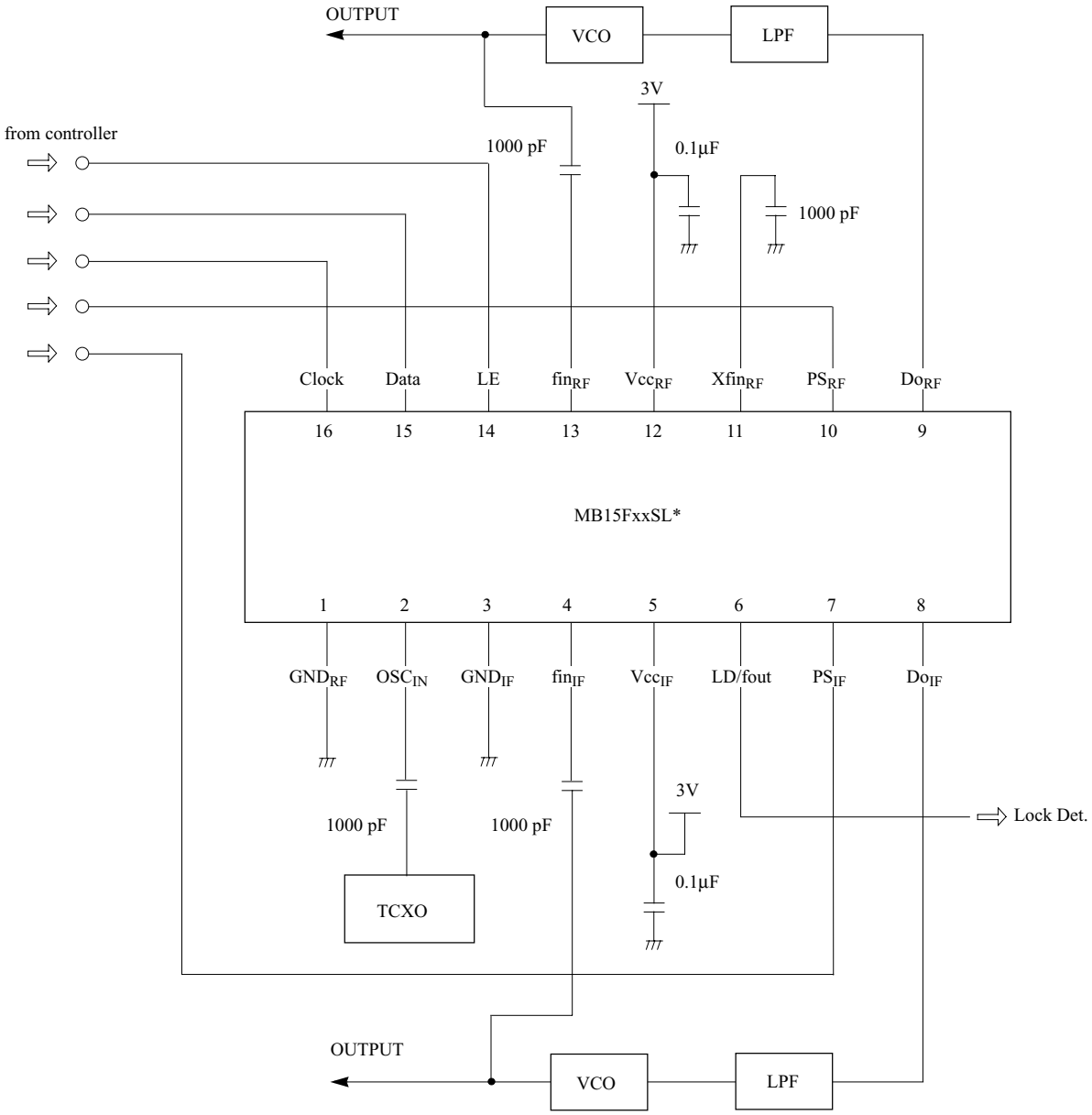


Notes:
1) Phase error detection range: -2π to $+2\pi$
2) Pulses on Do signal during locked state are output to prevent dead zone.
3) LD output becomes low when phase is t_{WU} or more. LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
4) t_{WU} and t_{WL} depend on OSC_{IN} input frequency.
   $t_{WU} \geq 2/fosc$ (s) (e. g. $t_{WU} \geq 156.3$ns, fosc = 12.8MHz)
   $t_{WU} \leq 4/fosc$ (s) (e. g. $t_{WL} \leq 312.5$ns, fosc = 12.8MHz)
5) LD becomes high during the power-saving mode (PS = "L").

Table 13. LD Output Logic Table

IF/PLL1 Section	RF/PLL2 Section	LD Output
Locked state / Power-saving state	Locked state / Power-saving state	H
Locked state / Power-saving state	Unlocked state	L
Unlocked state	Locked state / Power-saving state	L
Unlocked state	Unlocked state	L

Application Example



Notes: 1) Clock, Data, LE: Schmitt trigger circuit is provided (insert a pull-down or pull-up resistor to prevent oscillation)

2) *MB15F07SL uses PLL designators PLL1 and PLL2 in place of IF and RF in the pin signal callouts. MB15F08SL uses Tx and Rx in place of IF and RF.

3) Package type: 16-pin SSOP

Usage Precautions

$Vcc_{RF/PLL2}$ must equal $Vcc_{IF/PLL1}$:

- Even if either the RF/PLL2 or IF/PLL1 is not used, power must be supplied to both $Vcc_{RF/PLL2}$ and $Vcc_{IF/PLL1}$ to keep them equal. It is recommended that the unused PLL be controlled by the power-saving function.

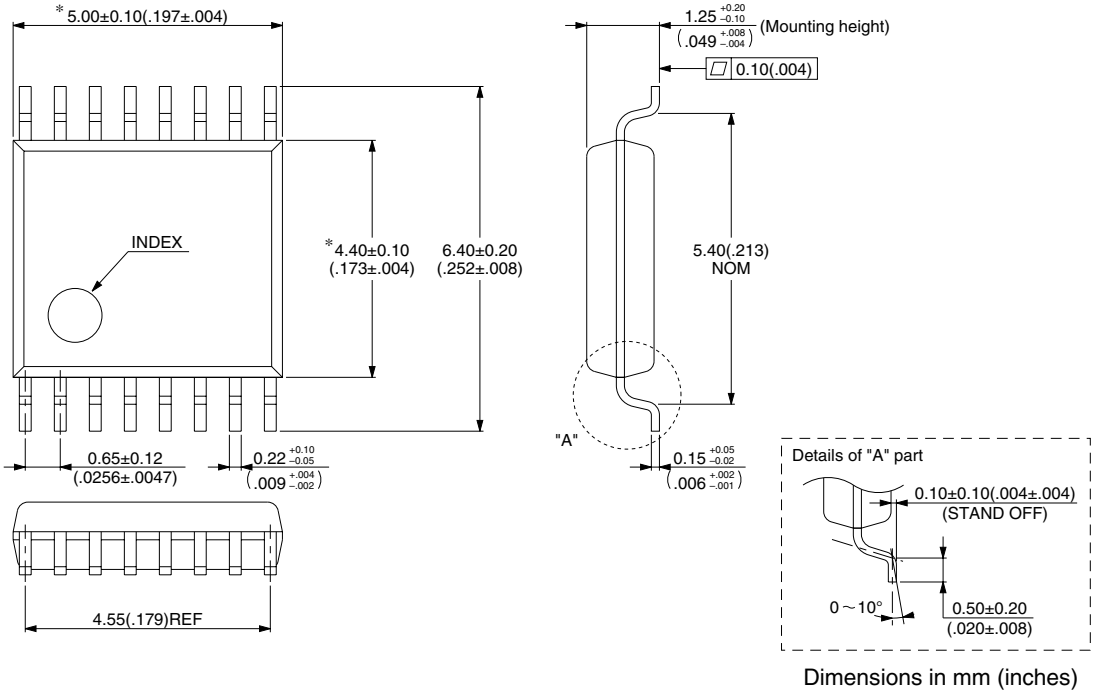
To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet when transporting a board mounted device.

Ordering Information

Part Number	Package
MB15FxxSLPFV1	16 pin, Plastic SSOP (FPT-16P-M05)
MB15FxxSLPV1	16 pin, Plastic BCC (LCC-16P-M04)

Package Dimensions

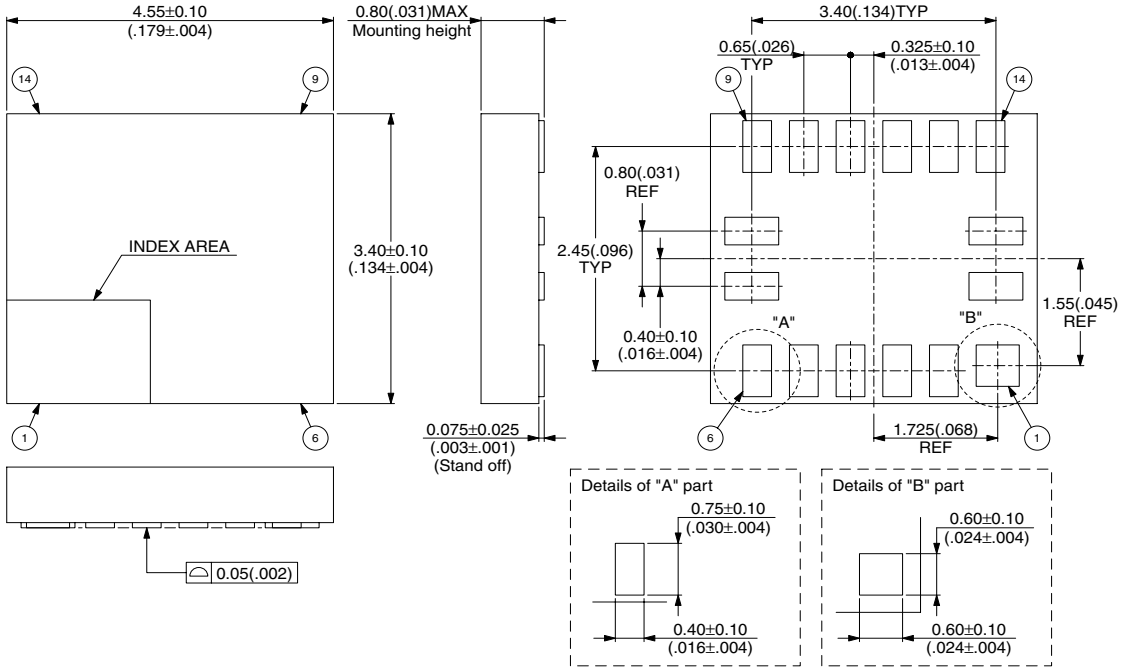


Dimensions in mm (inches)

Note: 16-pin, Plastic SSOP (FPT-16P-M05)

* These dimensions do not include resin protrusion.

Package Dimensions



Note: 16-pin, Plastic BCC (LCC-16P-M06)

Dimensions in mm (inches)

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