FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16704-1E

32-bit Microcontroller

CMOS

FR60 Lite MB91345 Series

MB91F345B/F346B

■ DESCRIPTION

The MB91345 series is the microcontrollers based on 32-bit high-perform RISC-CPU while integrating a variety of I/O resources for embedded control applications which require high-performance, high-speed CPU processing.

It is suitable for the embedded control in digital home appliances or audio visual equipment, requiring high-performance CPU processing power.

This product compactly integrates a variety of peripheral functions for single chip and is FR60 applicable to faster-speed application.

Note : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Limited.

■ FEATURE

- FR CPU
  - 32-bit RISC, load/store architecture, with a five-stage pipeline
  - Maximum operating frequency : 50 MHz [PLL used : original oscillation 12.5 MHz]
  - 16-bit fixed length instruction (basic instructions) ; 1 instruction per cycle
  - Instruction set optimized for embedded applications : Memory-to-Memory transfer, bit manipulation, barrel shift instructions
  - Instructions adapted for high-level programming languages : Function entry/exit instructions, multiple-register load/store instructions
  - Register interlock function : Facilitating coding in assembles

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Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

FUJITSU

- On-chip multiplier supported at instruction level
  Signed 32-bit multiplication : 5 cycles
  Signed 16-bit multiplication : 3 cycles
- Interrupt (PC, PS save) : 6 cycles, 16 priority levels
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instruction set compatible with FR family

• External bus interface
- Operating frequency : Max 25 MHz
- 24-bit address full output (16 Mbytes area)
- 8/16-bit data output
- Capable of chip-select signal output for completely independent four areas settable in 64 Kbytes minimum
- Support for various memory interfaces : SRAM and ROM/Flash
- Basic bus cycle : 2 cycles
- Programmable automatic wait cycle generator capable of inserting wait cycles for each area
- External wait cycles generated by RDY input
- Unused data/address pins can serve for general-purpose I/O

• Internal memory

	Flash	D-bus RAM	F-bus RAM
MB91F345B	512 Kbytes	24 Kbytes	8 Kbytes
MB91F346B	1 Mbyte	24 Kbytes	8 Kbytes

• DMAC (DMA Controller)
- 5 channels
- Two transfer factors (internal peripheral / software)
- Addressing mode : 20/24-bit full-address selection (increment/decrement/fixed)
- Transfer modes (burst transfer/step transfer/and block transfer)
- Selectable transfer data sizes : 8, 16, or 32 bits

• Bit search module (for REALOS)

Search for the position of the bit I/O-changed first in one word from the MSB

• Reload timer : 3 channels (including 1channel for REALOS)
- 16-bit timer
- The internal clock is optional from 2/8/32 division

• Multi function serial interface
- 11 channels
- Full duplex double buffer
- 2 channels out of 11 channels with 16-byte FIFO
- Capable of selecting communication mode : asynchronous (Start-Stop synchronous) communication, clock synchronous communication (Max 8.25 Mbps) , I^2C* standard mode (Max 100 kbps) , high-speed mode (Max 400 kbps)
- Parity on/off selectable
- Baud rate generator per channel
- Abundant error detection functions are provided (Parity, frame, and overrun)
- External clock can be used as transfer clock
- ch.0, ch.1, ch.2, and ch.10 is tolerant of 5 V

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- Interrupt controller
  - A total of 24 external interrupt lines (external interrupt pins INT23 to INT0)
  - Interrupt from internal peripheral
  - Programmable 16 priority levels
  - Available for wakeup from STOP mode

- A/D converter :
  - 10-bit resolution, 8 channels + 8 channels 2unit
  - Successive approximation type : Conversion time : min. 1.2 µs (at 16 MHz)
  - Conversion mode (Shingle-shot conversion mode, scan conversion mode)
  - Startup source (software/external trigger)

- PPG timer : up to 16 channels (at 8 bits)
  - 8/16-bit PPG timer : 8 bits × 16 channels or 16 bits × 8 channels
  - The internal clock is optional from 1/4/16/64 division

- PWC timer : 1 channel
  16-bit up counter 1 channel (1 input)

- Input capture and output compare : up to 8 channels (ch.0 to ch.3; 16-bit ICU, OCU, ch.4 to ch.7; 32-bit ICU, OCU)
  - 16-bit free-run counter × 1 channel + 16-bit input capture × 4 channels + 16-bit output compare × 4 channels
  - 32-bit free-run counter × 1 channel + 32-bit input capture × 4 channels + 32-bit output compare × 4 channels

- MIN/MAX/ABS
  - MIN/MAX/ABS is performed and the result is accumulated and added.

- Other interval timer and counter
  - 8/16-bit up down counter :
    8-bit × 4 channels or 16-bit × 2 channels
  - 16-bit timebase timer/watchdog timer

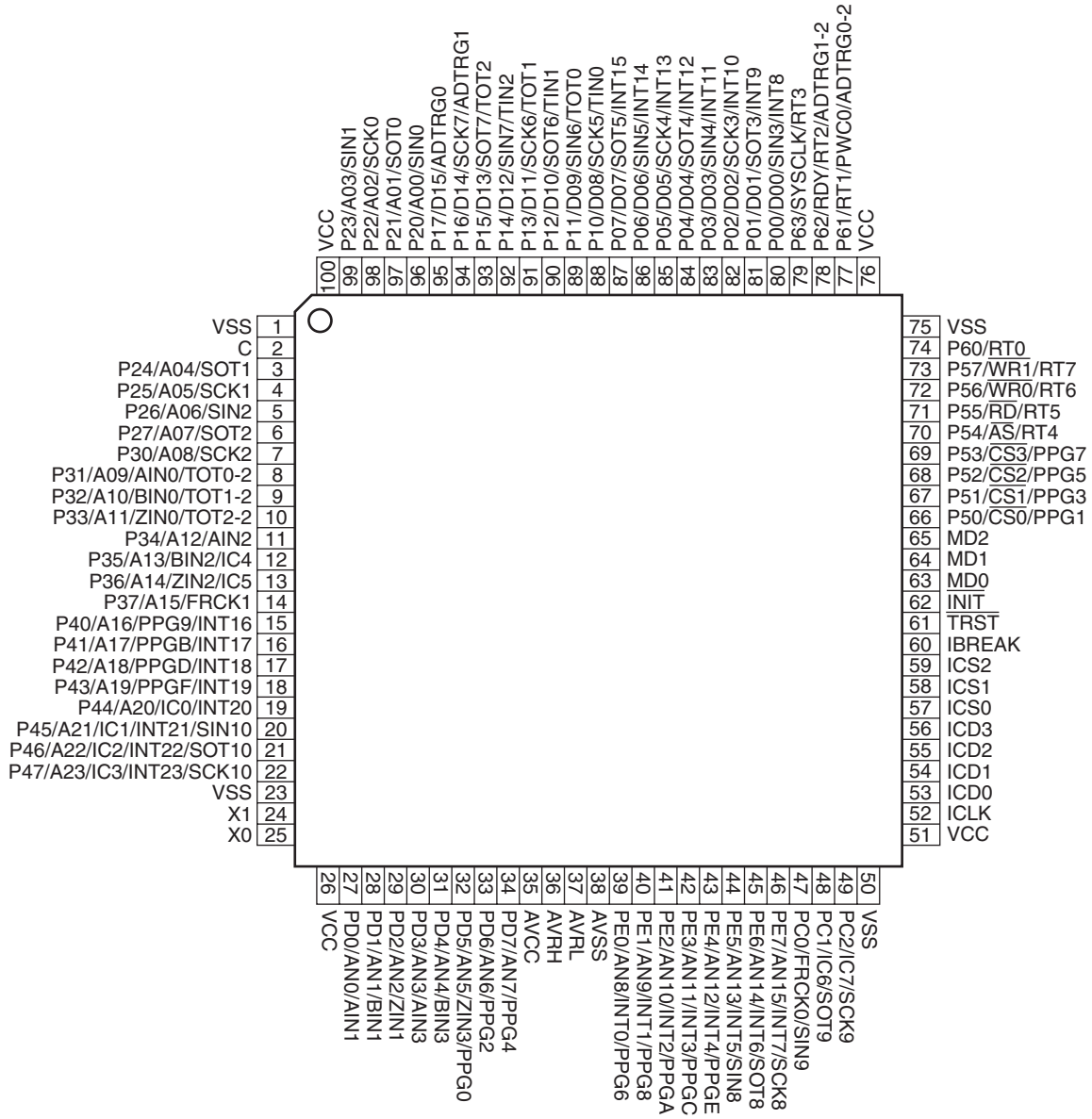
- I/O port
  - Max 71 ports

- Other features
  - Internal oscillation circuit as a clock source and PLL multiplier
  - $\overline{\text{INIT}}$ is prepared as a reset terminal
  - Watchdog timer reset and software reset are also available
  - Stop and sleep mode supported as low-power-consumption modes
  - Gear function
  - Built-in time base timer
  - Memory patch function
  - Package : TQFP-100
  - CMOS technology (0.18 µm)
  - Power supply voltage : 3.3 V ± 0.3 V (single power supply)

* : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-100P-M18)

Note : TOTx and TOTx-2 have same function. Also ADTRGx and ADTRGx-2 have same function. Use either of the two depending on the combined resource.

■ PIN DESCRIPTION

Pin No.	Pin name	I/O Circuit type*	Function
1	VSS	—	GND pin
2	C	—	Power stabilization capacitance pin
3	P24	B	General-purpose I/O port
	A04		Bit 4 of external address bus output pin. Enabled when external bus is effective.
	SOT1		Multi function serial 1 serial data output pin
4	P25	B	General-purpose I/O port. Enabled in single-chip mode.
	A05		Bit 5 of external address bus output pin. Enabled when external bus is effective.
	SCK1		Multi function serial 1 clock I/O pin
5	P26	B	General-purpose I/O port. Enabled in single-chip mode.
	A06		Bit 6 of external address bus output pin. Enabled when external bus is effective.
	SIN2		Multi function serial 2 serial data input pin
6	P27	B	General-purpose I/O port. Enabled in single-chip mode.
	A07		Bit 7 of external address bus output pin. Enabled when external bus is effective.
	SOT2		Multi function serial 2 serial data output pin
7	P30	B	General-purpose I/O port. Enabled in single-chip mode.
	A08		Bit 8 of external address bus output pin. Enabled when external bus is effective.
	SCK2		Multi function serial 2 clock I/O pin
8	P31	B	General-purpose I/O port. Enabled in single-chip mode.
	A09		Bit 9 of external address bus output pin. Enabled when external bus is effective.
	AIN0		Up down counter input pin
	TOT0-2		Reload timer output pin
9	P32	B	General-purpose I/O port. Enabled in single-chip mode.
	A10		Bit 10 of external address bus output pin. Enabled when external bus is effective.
	BIN0		Up down counter input pin
	TOT1-2		Reload timer output pin

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Pin No.	Pin name	I/O Circuit type*	Function
10	P33	B	General-purpose I/O port. Enabled in single-chip mode.
	A11		Bit 11 of external address bus output pin. Enabled when external bus is effective.
	ZIN0		Up down counter input pin
	TOT2-2		Reload timer output pin
11	P34	B	General-purpose I/O port. Enabled in single-chip mode.
	A12		Bit 12 of external address bus output pin. Enabled when external bus is effective.
	AIN2		Up down counter input pin
12	P35	B	General-purpose I/O port. Enabled in single-chip mode.
	A13		Bit 13 of external address bus output pin. Enabled when external bus is effective.
	BIN2		Up down counter input pin
	IC4		Input capture ICU 4 data sample input pin
13	P36	B	General-purpose I/O port. Enabled in single-chip mode.
	A14		Bit 14 of external address bus output pin. Enabled when external bus is effective.
	ZIN2		Up down counter input pin
	IC5		Input capture ICU 5 data sample input pin
14	P37	B	General-purpose I/O port. Enabled in single-chip mode.
	A15		Bit 15 of external address bus output pin. Enabled when external bus is effective.
	FRCK1		16-bit free-run timer input pin
15	P40	B	General-purpose I/O port
	A16		Bit 16 of external address bus output pin. Enabled when external bus is effective.
	PPG9		PPG output pin
	INT16		External interrupt request 16 input pin
16	P41	B	General-purpose I/O port
	A17		Bit 17 of external address bus output pin. Enabled when external bus is effective.
	PPGB		PPG output pin
	INT17		External interrupt request 17 input pin

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Pin No.	Pin name	I/O Circuit type*	Function
17	P42	B	General-purpose I/O port
	A18		Bit 18 of external address bus output pin. Enabled when external bus is effective.
	PPGD		PPG output pin
	INT18		External interrupt request 18 input pin
18	P43	B	General-purpose I/O port
	A19		Bit 19 of external address bus output pin. Enabled when external bus is effective.
	PPGF		PPG output pin
	INT19		External interrupt request 19 input pin
19	P44	B	General-purpose I/O port
	A20		Bit 20 of external address bus output pin. Enabled when external bus is effective.
	IC0		Input capture ICU0 data sample input pin
	INT20		External interrupt request 20 input pin
20	P45	B	General-purpose I/O port
	A21		Bit 21 of external address bus output pin. Enabled when external bus is effective.
	IC1		Input capture ICU1 data sample input pin
	INT21		External interrupt request 21 input pin
	SIN10		Multi function serial 10 serial data input pin
21	P46	B	General-purpose I/O port
	A22		Bit 22 of external address bus output pin. Enabled when external bus is effective.
	IC2		Input capture ICU2 data sample input pin
	INT22		External interrupt request 22 input pin
	SOT10		Multi function serial 10 serial data output pin
22	P47	B	General-purpose I/O port
	A23		Bit 23 of external address bus output pin. Enabled when external bus is effective.
	IC3		Input capture ICU3 data sample input pin
	INT23		External interrupt request 10 input pin
	SCK10		Multi function serial 10 clock I/O pin

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Pin No.	Pin name	I/O Circuit type*	Function
23	VSS	—	GND pin
24	X1	A	Main clock I/O pin
25	X0	A	Main clock input pin
26	VCC	—	Power supply input pin (3.3 V)
27	PD0	E	General-purpose I/O port
	AN0		A/D converter analog input pin
	AIN1		Up down counter input pin
28	PD1	E	General-purpose I/O port
	AN1		A/D converter analog input pin
	BIN1		Up down counter input pin
29	PD2	E	General-purpose I/O port
	AN2		A/D converter analog input pin
	ZIN1		Up down counter input pin
30	PD3	E	General-purpose I/O port
	AN3		A/D converter analog input pin
	AIN3		Up down counter input pin
31	PD4	E	General-purpose I/O port
	AN4		A/D converter analog input pin
	BIN3		Up down counter input pin
32	PD5	E	General-purpose I/O port
	AN5		A/D converter analog input pin
	ZIN3		Up down counter input pin
	PPG0		PPG output pin
33	PD6	E	General-purpose I/O port
	AN6		A/D converter analog input pin
	PPG2		PPG output pin
34	PD7	E	General-purpose I/O port
	AN7		A/D converter analog input pin
	PPG4		PPG output pin

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Pin No.	Pin name	I/O Circuit type*	Function
35	AVCC	—	A/D converter analog power supply input pin
36	AVRH	—	A/D converter standard voltage input pin Be sure to turn on/off this power supply when potential of AVRH or more is applied to AVCC.
37	AVRL	—	A/D converter standard low voltage input pin
38	AVSS	—	A/D converter analog GND pin
39	PE0	E	General-purpose I/O port
	AN8		A/D converter analog input pin
	INT0		External interrupt request 0 input pin
	PPG6		PPG output pin
40	PE1	E	General-purpose I/O port
	AN9		A/D converter analog input pin
	INT1		External interrupt request 1 input pin
	PPG8		PPG output pin
41	PE2	E	General-purpose I/O port
	AN10		A/D converter analog input pin
	INT2		External interrupt request 2 input pin
	PPGA		PPG output pin
42	PE3	E	General-purpose I/O port
	AN11		A/D converter analog input pin
	INT3		External interrupt request 3 input pin
	PPGC		PPG output pin
43	PE4	E	General-purpose I/O port
	AN12		A/D converter analog input pin
	INT4		External interrupt request 4 input pin
	PPGE		PPG output pin
44	PE5	E	General-purpose I/O port
	AN13		A/D converter analog input pin
	INT5		External interrupt request 5 input pin
	SIN8		Multi function serial 8 serial data input pin

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Pin No.	Pin name	I/O Circuit type*	Function
45	PE6	E	General-purpose I/O port
	AN14		A/D converter analog input pin
	INT6		External interrupt request 6 input pin
	SOT8		Multi function serial 8 serial data output pin
46	PE7	E	General-purpose I/O port
	AN15		A/D converter analog input pin
	INT7		External interrupt request 7 input pin
	SCK8		Multi function serial 8 clock I/O pin
47	PC0	C	General-purpose I/O port
	FRCK0		16-bit free-run timer input pin
	SIN9		Multi function serial 9 serial data input pin
48	PC1	C	General-purpose I/O port
	IC6		Input capture ICU6 data sample input pin
	SOT9		Multi function serial 9 serial data output pin
49	PC2	C	General-purpose I/O port
	IC7		Input capture ICU7 data sample input pin
	SCK9		Multi function serial 9 clock I/O pin
50	VSS	—	GND pin
51	VCC	—	Power supply input pin (3.3 V)
52	ICLK	H	Development tool clock pin
53	ICD0	K	Development tool data pin
54	ICD1	K	Development tool data pin
55	ICD2	K	Development tool data pin
56	ICD3	K	Development tool data pin
57	ICS0	J	Development tool status pin
58	ICS1	J	Development tool status pin
59	ICS2	J	Development tool status pin
60	IBREAK	I	Development tool break pin
61	$\overline{\text{TRST}}$	G	Development tool reset pin
62	$\overline{\text{INIT}}$	G	Initial reset pin

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Pin No.	Pin name	I/O Circuit type*	Function
63	MD0	F	Mode input pin
64	MD1	F	Mode input pin
65	MD2	F	Mode input pin
66	P50	C	General-purpose I/O port
	$\overline{CS0}$		External chip select 0. Enabled when external bus is effective.
	PPG1		PPG output pin
67	P51	C	General-purpose I/O port
	$\overline{CS1}$		External chip select pin. Enabled when external bus is effective.
	PPG3		PPG output pin
68	P52	C	General-purpose I/O port
	$\overline{CS2}$		External chip select pin. Enabled when external bus is effective.
	PPG5		PPG output pin
69	P53	C	General-purpose I/O port
	$\overline{CS3}$		External chip select pin. Enabled when external bus is effective.
	PPG7		PPG output pin
70	P54	C	General-purpose I/O port
	$\overline{AS}$		External address strobe output pin. Enabled when external bus is effective.
	RT4		Output compare OCU4 waveform output pin
71	P55	C	General-purpose I/O port
	$\overline{RD}$		External read strobe output pin. Enabled when external bus is effective.
	RT5		Output compare OCU5 waveform output pin
72	P56	D	General-purpose I/O port
	$\overline{WR0}$		External data bus upper 8-bit write strobe output pin. When external bus is effective, high 8 bits of data during 16-bit access or 8 bits of data during 8-bit access is used as write strobe.
	RT6		Output compare OCU6 waveform output pin

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Pin No.	Pin name	I/O Circuit type*	Function
73	P57	D	General-purpose I/O port
	$\overline{WR1}$		External data bus lower 8-bit write strobe output pin. Enabled when external bus is effective and external bus 16-bit mode is selected.
	RT7		Output compare OCU7 waveform output pin
74	P60	C	General-purpose I/O port
	RT0		Output compare OCU0 waveform output pin
75	VSS	—	GND pin
76	VCC	—	Power supply input pin (3.3 V)
77	P61	C	General-purpose I/O port
	RT1		Output compare OCU1 waveform output pin
	PWC0		PWC input pin
	ADTRG0-2		A/D converter trigger input pin
78	P62	C	General-purpose I/O port
	RDY		External ready input pin. Enabled when both external bus and bus request are effective.
	RT2		Output compare OCU2 waveform output pin
	ADTRG1-2		A/D converter trigger input pin
79	P63	C	General-purpose I/O port
	SYSCLK		External clock output pin. Enabled when external bus is effective.
	RT3		Output compare OCU3 waveform output pin
80	P00	C	General-purpose I/O port
	D00		Bit 0 of external address/data bus I/O pin. Enabled when external bus is effective.
	SIN3		Multi function serial 3 serial data input pin
	INT8		External interrupt request 8 input pin
81	P01	C	General-purpose I/O port
	D01		Bit 1 of external address/data bus I/O pin. Enabled when external bus is effective.
	SOT3		Multi function serial 3 serial data output pin
	INT9		External interrupt request 9 input pin

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Pin No.	Pin name	I/O Circuit type*	Function
82	P02	C	General-purpose I/O port
	D02		Bit 2 of external address/data bus I/O pin. Enabled when external bus is effective.
	SCK3		Multi function serial 3 clock I/O pin
	INT10		External interrupt request 10 input pin
83	P03	C	General-purpose I/O port
	D03		Bit 3 of external address/data bus I/O pin. Enabled when external bus is effective.
	SIN4		Multi function serial 4 serial data input pin
	INT11		External interrupt request 11 input pin
84	P04	C	General-purpose I/O port
	D04		Bit 4 of external address/data bus I/O pin. Enabled when external bus is effective.
	SOT4		Multi function serial 4 serial data output pin
	INT12		External interrupt request 12 input pin
85	P05	C	General-purpose I/O port
	D05		Bit 5 of external address/data bus I/O pin. Enabled when external bus is effective.
	SCK4		Multi function serial 4 clock I/O pin
	INT13		External interrupt request 13 input pin
86	P06	C	General-purpose I/O port
	D06		Bit 6 of external address/data bus I/O pin. Enabled when external bus is effective.
	SIN5		Multi function serial 5 serial data input pin
	INT14		External interrupt request 14 input pin
87	P07	C	General-purpose I/O port
	D07		Bit 7 of external address/data bus I/O pin. Enabled when external bus is effective.
	SOT5		Multi function serial 5 serial data output pin
	INT15		External interrupt request 12 input pin
88	P10	C	General-purpose I/O port
	D08		Bit 8 of external address/data bus I/O pin. Enabled when external bus is effective.
	SCK5		Multi function serial 5 clock I/O pin
	TIN0		Reload timer event input pin

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Pin No.	Pin name	I/O Circuit type*	Function
89	P11	C	General-purpose I/O port
	D09		Bit 9 of external address/data bus I/O pin. Enabled when external bus is effective.
	SIN6		Multi function serial 6 serial data input pin
	TOT0		Reload timer output pin
90	P12	C	General-purpose I/O port
	D10		Bit 10 of external address/data bus I/O pin. Enabled when external bus is effective.
	SOT6		Multi function serial 6 serial data output pin
	TIN1		Reload timer event input pin
91	P13	C	General-purpose I/O port
	D11		Bit 11 of external address/data bus I/O pin. Enabled when external bus is effective.
	SCK6		Multi function serial 6 clock I/O pin
	TOT1		Reload timer output pin
92	P14	C	General-purpose I/O port
	D12		Bit 12 of external address/data bus I/O pin. Enabled when external bus is effective.
	SIN7		Multi function serial 7 serial data input pin
	TIN2		Reload timer event input pin
93	P15	C	General-purpose I/O port
	D13		Bit 13 of external address/data bus I/O pin. Enabled when external bus is effective.
	SOT7		Multi function serial 7 serial data output pin
	TOT2		Reload timer output pin
94	P16	C	General-purpose I/O port
	D14		Bit 14 of external address/data bus I/O pin. Enabled when external bus is effective.
	SCK7		Multi function serial 7 clock I/O pin
	ADTRG1		A/D converter trigger input pin
95	P17	C	General-purpose I/O port
	D15		Bit 15 of external address/data bus I/O pin. Enabled when external bus is effective.
	ADTRG0		A/D converter trigger input pin

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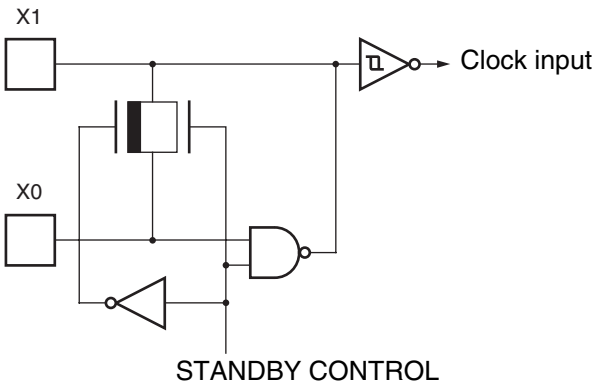
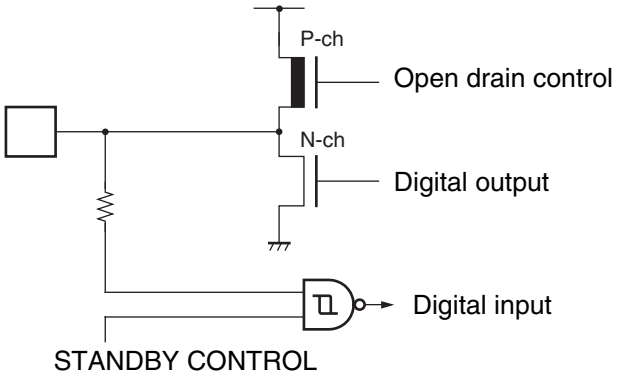
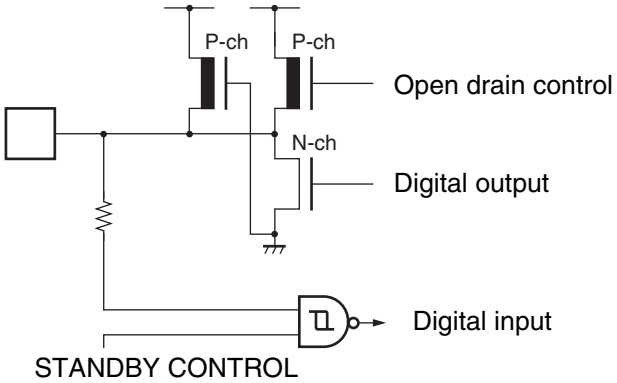
Pin No.	Pin name	I/O Circuit type*	Function
96	P20	C	General-purpose I/O port
	A00		Bit 0 of external address bus output pin. Enabled when external bus is effective.
	SIN0		Multi function serial 0 serial data input pin
97	P21	C	General-purpose I/O port
	A01		Bit 1 of external address bus output pin. Enabled when external bus is effective.
	SOT0		Multi function serial 0 serial data output pin
98	P22	C	General-purpose I/O port
	A02		Bit 2 of external address bus output pin. Enabled when external bus is effective.
	SCK0		Multi function serial 0 clock I/O pin
99	P23	C	General-purpose I/O port
	A03		Bit 3 of external address bus output pin. Enabled when external bus is effective.
	SIN1		Multi function serial 1 serial data input pin
100	VCC	—	Power supply input pin (3.3 V)

* : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Classification	Circuit type	Remarks
A		Oscillation circuit Feedback resistor X0 : 1 MΩ
B		• CMOS level output I_{OH} = 4 mA • With open drain output control • CMOS level hysteresis input $V_{IH} = 0.7 \times V_{CC}$ • With standby control • 5V tolerance
C		• CMOS level output I_{OH} = 4 mA • With open drain output control • CMOS level hysteresis input $V_{IH} = 0.8 \times V_{CC}$ • With standby control • With pull-up resistor (33 kΩ)

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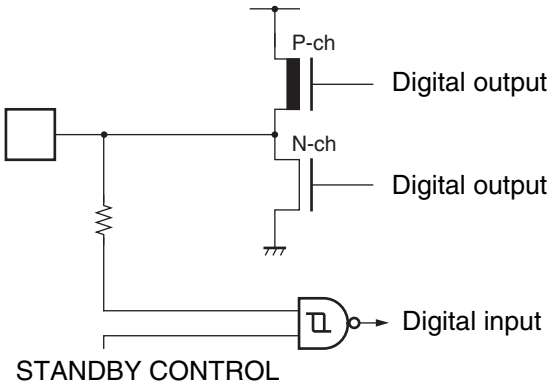
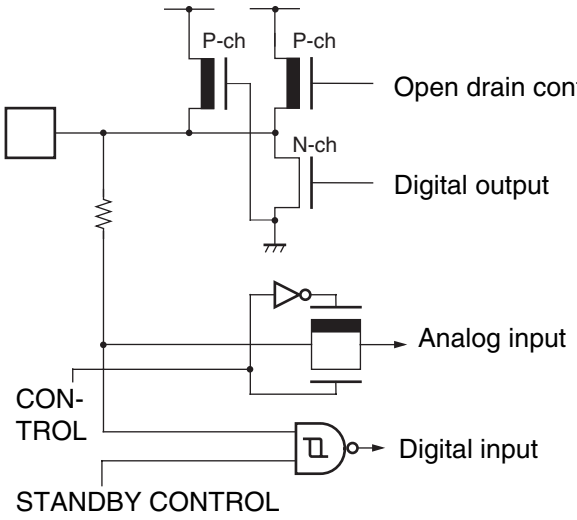
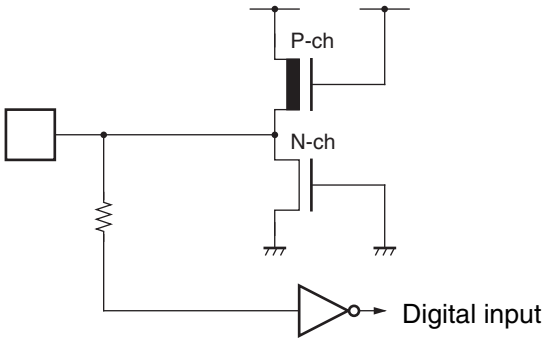
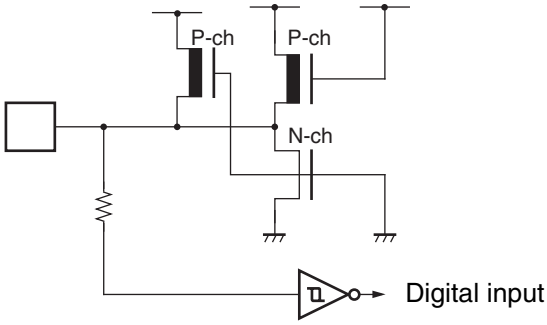
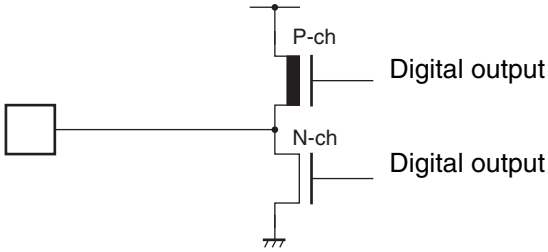
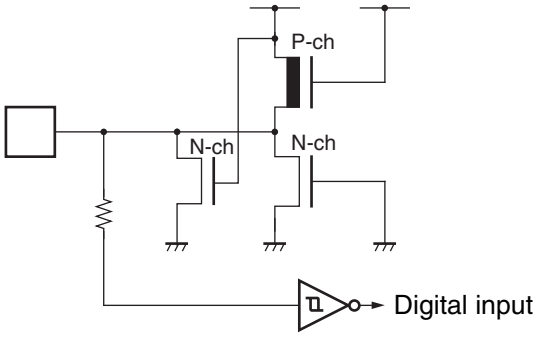
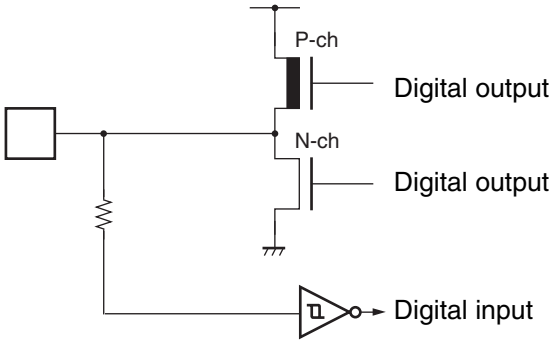
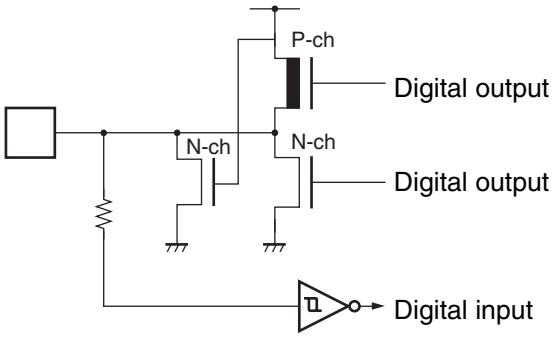
Classification	Circuit type	Remarks
D		• CMOS level output I_{OH} = 4 mA • CMOS level hysteresis input $V_{IH} = 0.8 \times V_{CC}$ Standby control provided Without pull-up resistor
E		• CMOS level output I_{OH} = 4 mA • With open drain output control • CMOS level hysteresis input $V_{IH} = 0.8 \times V_{CC}$ With standby control • With analog input switch • With pull-up resistor (33 kΩ)
F		• CMOS level input • Without standby control

(Continued)

Classification	Circuit type	Remarks
G		• CMOS hysteresis input • With pull-up resistor
H		CMOS level output
I		• CMOS hysteresis input • With pull-down resistor • Without standby control
J		• CMOS level output • CMOS level hysteresis input • Without standby control

(Continued)

(Continued)

Classification	Circuit type	Remarks
K		• CMOS level output • CMOS level hysteresis input • Without standby control • With pull-down resistor

■ HANDLING DEVICES

• Preventing Latch-up

Latch-up may occur in a COMS IC if a voltage greater than VCC pin, or less than VSS pin is applied to input and output pins, or if an above-rating voltage is applied between VCC pin and VSS pin. If the latch-up occurs, the significantly increases the power supply current and may cause thermal destruction of an element. Thus, When you use a CMOS IC, be very careful not to exceed maximum voltage rating.

• Treatment of Unused input pins

Do not leave an unused input pin open, since it may cause a malfunction. Thus, use pull-up or pull-down resistor.

• About power supply pins

If there are multiple VCC pin or VSS pin, from the point of view of device design, pins to be of the same level are connected the inside of the device to prevent such malfunctioning as latch-up. Be sure to connect all of them to the power supply and ground externally for reducing unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the total output current standard. In addition, consideration should be given to connecting VCC/VSS of this device with as low an impedance as possible from the current supply source. Also, we recommend connecting a ceramic capacitor of about 0.1 µF as a bypass capacitor between VCC and VSS near this device.

• About crystal oscillator circuit

Noise near the X0 and X1 pins can cause this device to malfunction. Design the PC board such that X0 and X1 pins, crystal oscillator (or ceramic oscillator) , and bypass capacitor to the ground are placed as near one another as possible. It is strongly recommended to design the PC board artwork with the X0/X1 pins surrounded by a ground plane, as it expects stable operations.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

• About mode pins (MD0 to MD2)

These pins should be connected directly to VCC or VSS pins. To prevent the device erroneously switching to test mode due to noise, design the PC board such that the distance between the mode pins and VCC or VSS pins is as short as possible and the connection impedance is low.

• About operation at power-on

Be sure to set initialized reset (INIT) with $\overline{\text{INIT}}$ pin immediately after power-on.
Immediately after turning on the power, be sure to continue connecting the Low level input to the $\overline{\text{INIT}}$ pin for the stabilization wait time required for oscillator circuit, to secure the stabilization wait time of the oscillator and regulator (For INIT via the $\overline{\text{INIT}}$ pin, the oscillation stabilization wait time setting is initialized to the minimum value) .

• About oscillation input at power on

When turning on the power, be sure that clock input is maintained until the device is released from the oscillation stabilization wait state.

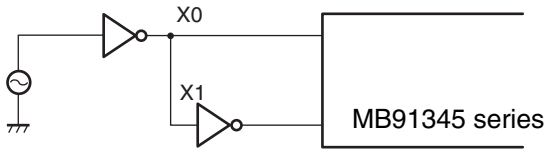
• Note on power-on/off sequences

When turning on the power, the output pin may be indeterminate until the internal power supply stabilizes.

• Note when using external clock

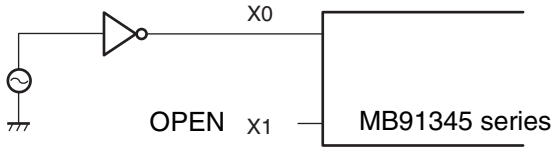
In principle, when using external clock, supply a clock to the X0 pin and an opposite-phase clock signal to the X1 pin simultaneously. However in this case, the STOP mode (oscillator stop mode) must not be used, because the X1 pin stops with the “H” output in the STOP mode. At 12.5 MHz or less, the device can be used with the clock signal supplied only to the X0 pin.

Using an External Clock (Normal Method)



[The STOP mode (oscillation stop mode) cannot be used.]

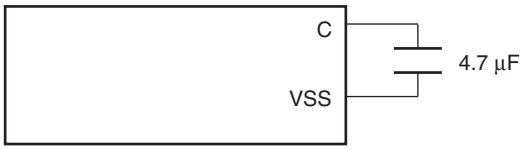
Using an External (enabled at 12.5 MHz or lower)



Note : The X1 pin must be designed to have a delay within 15 ns, at 10 MHz, from the signal to the X0 pin.

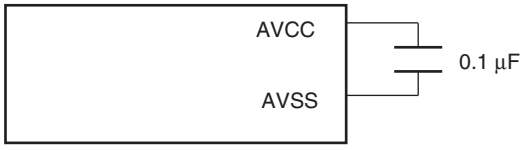
• About C pin

MB91345 series has an internal regulator. A bus condenser of 4.7 µF or above should be connected to the C pin for the regulator.



• About AVCC pin

MB91345 series has an internal A/D converter. A condenser of approximately 0.1 µF should be connected between the AVCC pin and AVSS pin.



• Treatment of NC pin and OPEN pin

The NC and OPEN pins should always be open.

- Note when not using emulator

  If evaluation MCU on user system is operated without emulator, each input pin on evaluation MCU connected to the emulator interface on the user system should be handled, as described in the following table. Note that the switch circuit or other function may be required on user system when designing the MCU.

Emulator Interface Pin Treatment

Evaluation MCU pin name	Pin processing
$\overline{\text{TRST}}$	Connect to the reset output circuit on the user system.
$\overline{\text{INIT}}$	Connect to the reset output circuit on the user system.
Others	Open.

■ RESTRICTIONS

- **Common in the series**
  - Clock control block
    Take the oscillation stabilization wait time during Low level input to $\overline{\text{INIT}}$ pin.

  - Bit search module
    The bit search data register for 0-detection (BSD0) , and bit search data register for 1-detection (BSD1) , and bit search data register for change point detection (BSDC) are only word-accessible.

  - I/O port
    Ports are accessed only in bytes.

  - Low power consumption mode

  - To enter the standby mode, use the synchronous standby mode (set with the SYNCS bit as bit8 in TBCR, or timebase counter control register) and be sure to use the following sequence :

```
 (ldi      #value_of_standby, r0)
 (ldi      #_STCR, r12)
stb        r0, @r12        // set STOP/SLEEP bit
ldub       @r12, r0        // Must read STCR
ldub       @r12, r0        // after reading, go into standby mode
nop                        // Must insert NOP *5
nop
nop
nop
nop
```

  - Please do not do the following when the monitor debugger is used
    - Setting of the break point to the above instructions.
    - Execution of the single-stepping for the above instructions.

- Notes on the PS register
  As the PS register is processed by some instructions in advance, exception handling below may cause the interrupt handling routine to break when the debugger is used or the display contents of flags in the PS register to be updated. In either case, the operations before and after an EIT are performed as specified as the device is designed such that the recovery from the EIT is followed by correct re-processing.
- The instruction just before the DIV0U/DIV0S instruction may cause the following operation, if a user interrupt or NMI occurs, single-stepping is performed or a break is caused by a data event or emulator menu :

  (1) The D0 and D1 flags are updated in advance.

  (2) An EIT handling routine (user interrupt, NMI, or emulator) is executed.

  (3) Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as shown in (1) .
- If the ORCCR/STILM/MOV Ri and PS instructions are executed to enable interruptions when a user interrupt or NMI trigger even has occurred, the following operations are performed.

  (1) The PS register is updated in advance.

  (2) An EIT handling routine (user interrupt, NMI, or emulator) is executed.

  (3) Upon returning from the EIT, the instructions shown above are executed and the PS register is updated to the same value as shown in (1) .

- About watchdog timer
  MB91345 series has an internal function called “watchdog timer”. This function monitors a program to perform the reset defer operation within a certain period of time. The watchdog timer resets the CPU if the program runs out of controls and the reset defer operation is not executed. Thus, once enabled, the watchdog timer will be up and running until it resets the CPU. However, with one exception, the watchdog timer automatically defers a reset timing under the condition in which the CPU stops program execution. Refer to the section describing the watchdog timer functions for the exceptional condition. If the system runs out of control and develops the above condition, a watchdog reset may not be generated. In that case, please reset (INIT) from external $\overline{\text{INIT}}$ terminal.

- Note on using the A/D converter
  MB91345 series has an internal A/D converter. The AVCC pin should not be supplied with higher voltage than VCC pin.

- Software reset in synchronous mode
  When using the software reset in the synchronous mode, the following two conditions should be satisfied before setting “0” to the SRST bit in STCR (Standby control register) .
  - Set the interrupt enable flag (I-Flag) to interrupt disable (I-Flag = 0) .
  - Do not use NMI.

- Debug control when using ICE
  - Single-stepping of the RETI instruction
    If an interrupt occurs frequently during single stepping, only the relevant interrupt processing routine is executed repeatedly after single-stepping RETI. This will prevent the main routine and low-interrupt-level programs from being executed. Do not single-step the RETI instruction for escape. When the debugging of the relevant interrupt routine no longer requires, perform debugging with that interrupt disabled.

  - About operand break
    Do not apply a data event break to access to the area containing the address of a stack pointer.

- Execution of an unused area of Flash memory
  Accidently if an unused area (data at 0XFFFF) of Flash memory is executed in an instruction, no break can be accepted. To avoid this, it is recommended to use the code event address mask feature of the debugger to break at instruction access to the unused area.

- Interrupt handler for NMI request (tool)
  Add the following program to the interrupt handler to prevent the device from malfunctioning when the source flag is set accidentlly with no ICE connected, for example, due to noise to the DSU pin, which is to be set only at the break request of the ICE. can be used normally with this program added.

  Add place :

    Next interrupt handler

    Interrupt source : NMI request (tool)

    Interrupt number : 13 (decimal) , 0D (hexadecimal)

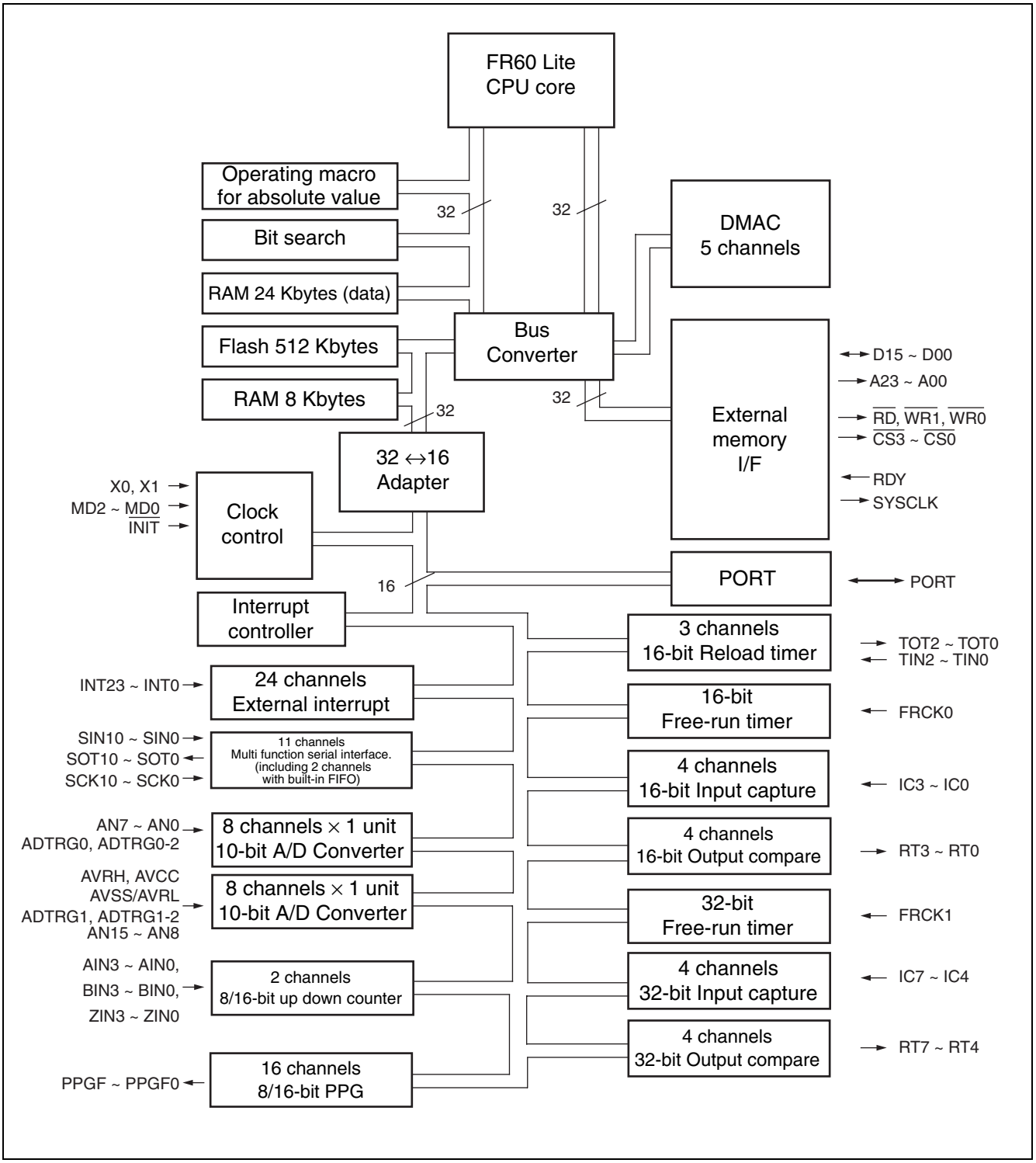
    Offset : 3C8H

  TBR default address : $000FFFC8_H$

  Add program

```
STM (R0, R1)
LDI #0B00H, R0    ; 0B00H is the address of DSU break source register
LDI #0, R1
STB R1, @R0       ; Clear the break source register
LDM (R0, R1)
RETI
```

■ BLOCK DIAGRAM



■ CPU AND CONTROL UNIT

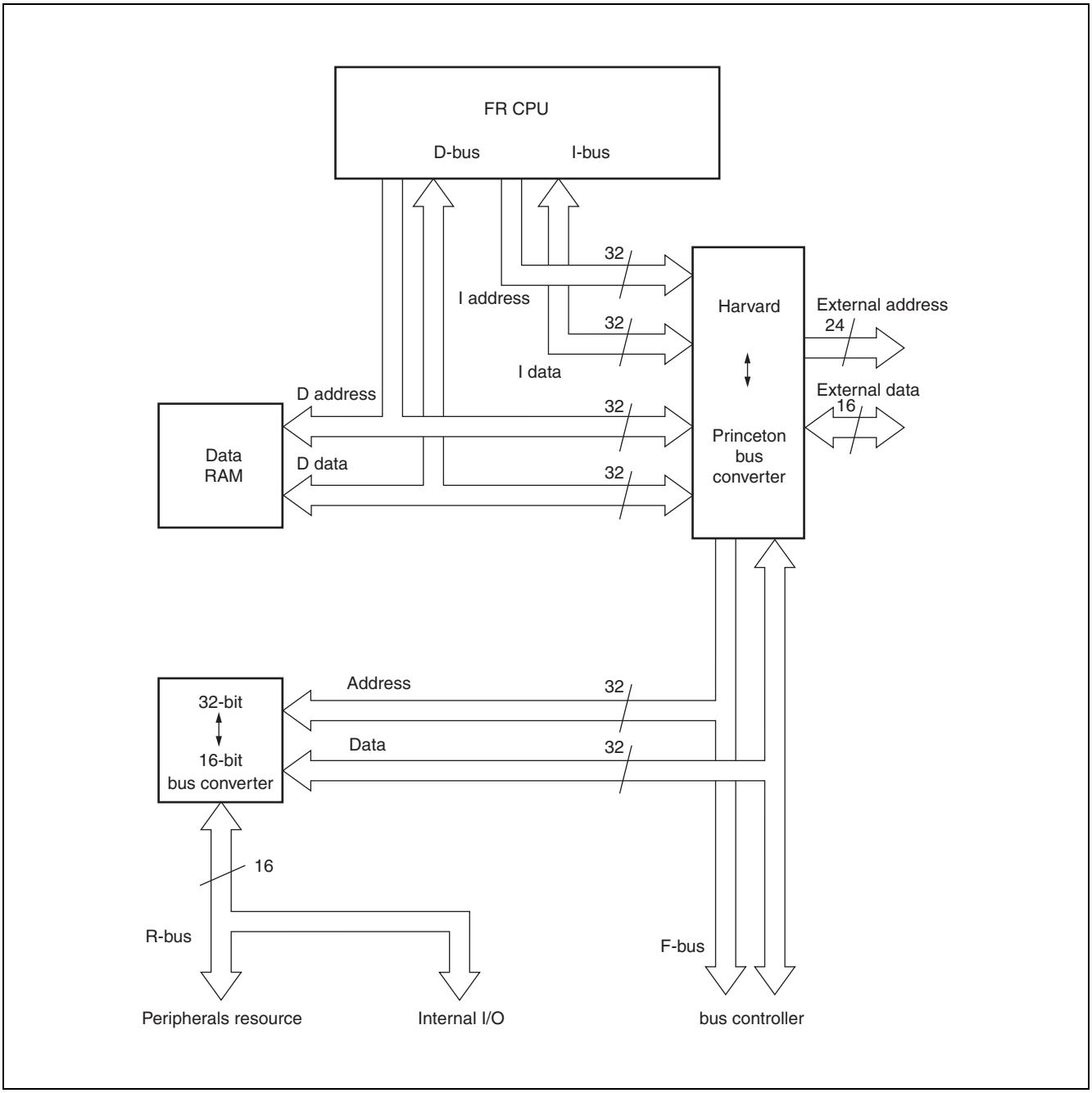
The FR family CPU is a line of high-performance cores based on a RISC architecture while incorporating advanced instructions for embedded controller applications.

1. Features

- RISC architecture adopted.
  Basic instructions : Executed at 1 instruction per cycle
- 32-bit architecture
  General purpose registers : 32 bit × 16
- 4G bytes of linear memory space
- Multiplier integrated.
  32-bit × 32-bit multiplication : 5 cycles.
  16-bit × 16-bit multiplication : 3 cycles
- Enhanced interrupt servicing.
  High-speed response (6 cycles) .
  Multi-level interrupts support.
  Level mask feature (16 levels)
- Enhanced I/O manipulation instructions.
  Memory-to-memory transfer instructions
  Bit manipulation instructions
- High code efficiency. Basic instruction word length : 16-bit
- Low-power consumption.
  Sleep mode / stop mode
- Gear function

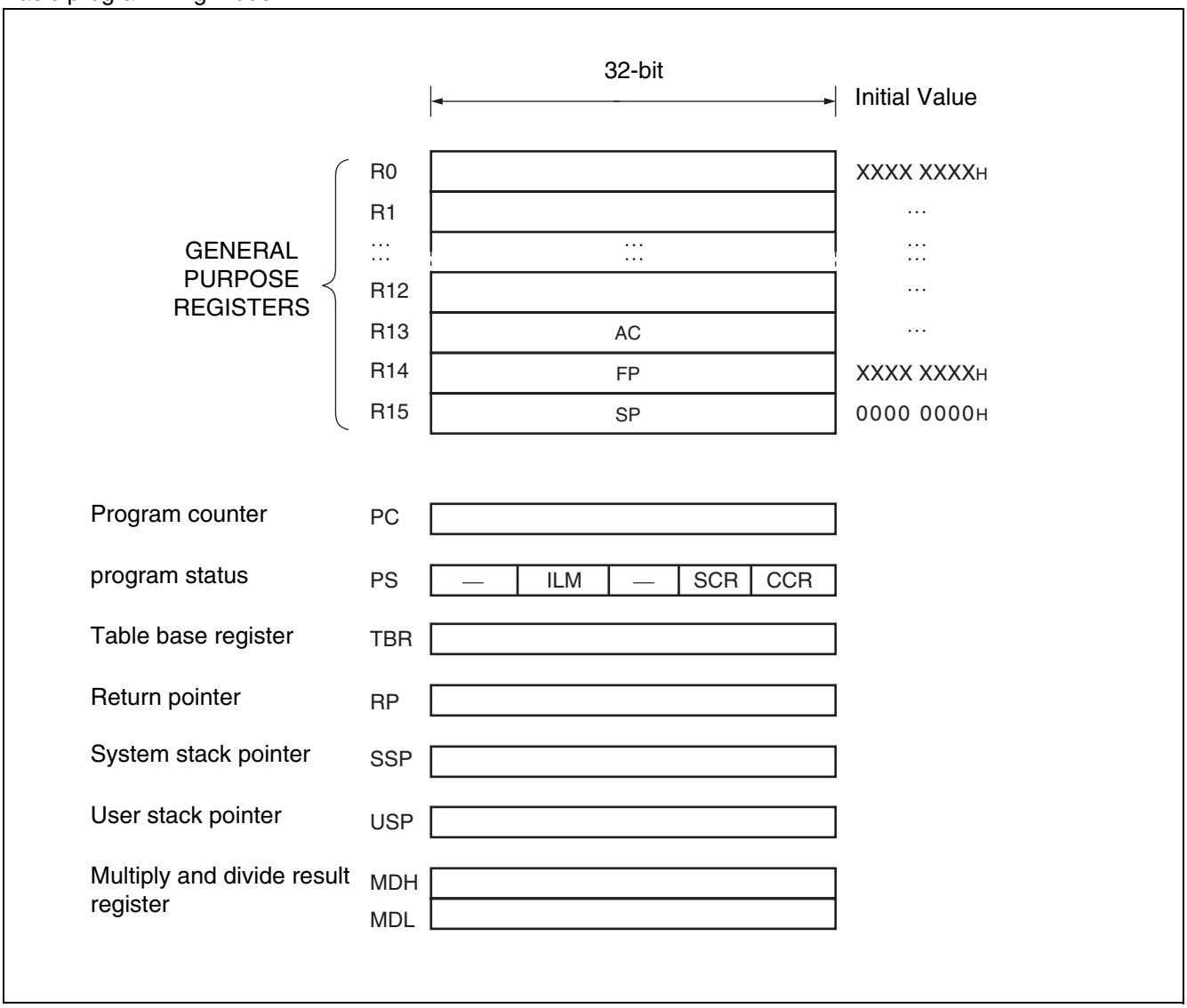
2. Internal architecture

The FR-family CPU has a Harvard architecture in which the instruction bus and data buses are separated. The 32-bit←→16-bit bus converter is connected to a 32-bit bus (F-bus) , providing an interface between the CPU and peripheral resources. The Harvard←→Princeton bus converter is connected to both of the I-bus and D-bus, providing an interface between the CPU and the bus controller.



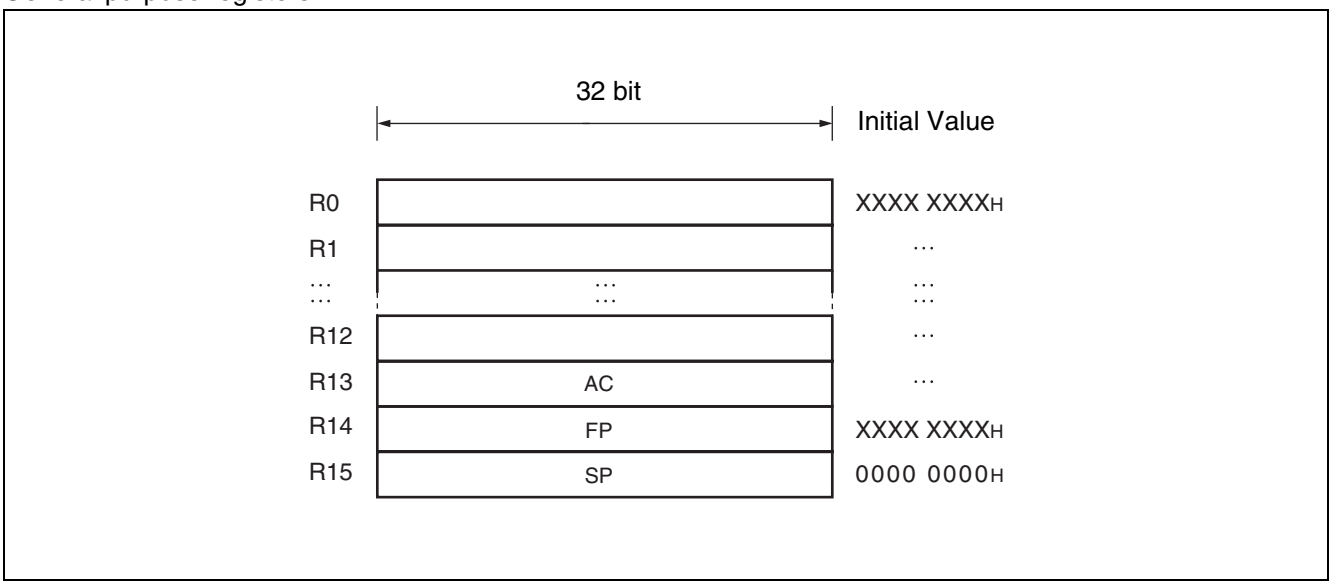
3. Programming model

Basic programming model



4. Register

General purpose registers



Registers R0 to R15 are general purpose registers. The registers are used as the accumulator and memory access pointers for CPU operations.

Of these 16 registers, the registers listed below are intended for special applications, for which some instructions are enhanced.

R13 : Virtual accumulator
R14 : Frame pointer
R15 : Stack pointer

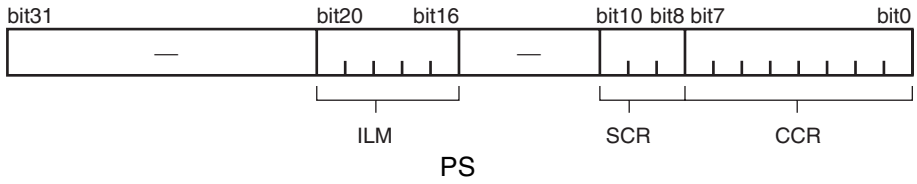
The initial values of R0 to R14 after a reset are indeterminate. R15 is initialized to 00000000H (SSP value) .

• PS (Program Status)

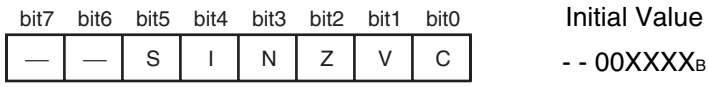
This register holds the program status and is divided into the ILM, SCR, and CCR.

All of undefined bits are reserved bits. Reading these bits always returns “0”.

Writing to them has no effect.



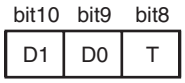
• CCR (Condition Code Register)



S : Stack flag. Cleared to “0” at a reset.

I : Interrupt Enable flag. Cleared to “0” at a reset.
N : Negative flag. Initial State at a reset is unspecified.
Z : Zero flag. Initial State at a reset is unspecified.
V : Overflow flag. Initial State at a reset is unspecified.
C : Carry flag. Initial State at a reset is unspecified.

• SCR (System Condition code Register)



Initial Value
$XX0_B$

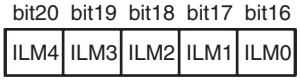
Flag for step dividing

Stores intermediate data for stepwise multiplication operations.

Step trace trap flag

A flag specifying whether the step trace trap function is enabled or not.
Emulator uses step trace trap function. The function cannot be used by the user program when using the emulator.

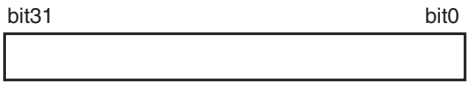
• ILM (Interrupt Level Mask Register)



Initial Value
01111_B

This register stores the interrupt level mask value. The value in the ILM register is used as the level mask.
Initialized to “15” (01111_B) by a reset.

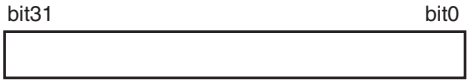
• PC (Program Counter)



Initial Value
$XXXXXXXX_H$

The program counter contains the address of the instruction currently being executed.
The initial value after a reset is indeterminate.

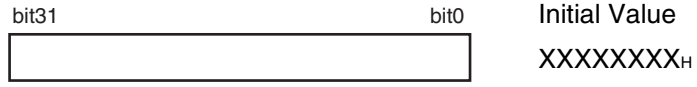
• TBR (Table Base Register)



Initial Value
$000FFC00_H$

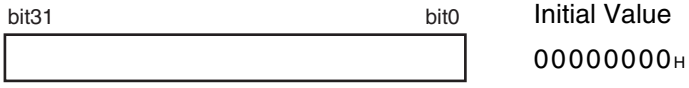
The table base register contains the start address of the vector table used for servicing EIT events.
The initial value after a reset is $000FFC00_H$.

• RP (Return Pointer)



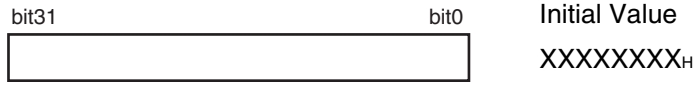
The return pointer contains the address to which to return from a subroutine.
When the CALL instruction is executed, the value in the PC is transferred to the RP.
When the RET instruction is executed, the value in the RP is transferred to the PC.
The initial value after a reset is indeterminate.

• SSP (System Stack Pointer)



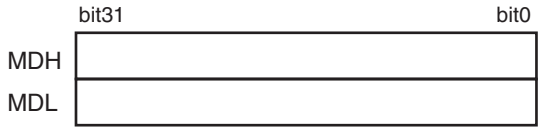
The SSP is the system stack pointer and functions as R15 when the S flag is “0”.
The SSP can be explicitly specified.
The SSP is also used as the stack pointer that specifies the stack for saving the PS and PC when an EIT event occurs.
The initial value after a reset is 00000000H.

• USP (User Stack Pointer)



The USP is the user stack pointer and functions as R15 when the S flag is “1”.
The USP can be explicitly specified.
The initial value after a reset is indeterminate.
This pointer cannot be used by the RETI instruction.

• MDH, MDL (Multiply and Divide register)



Multiplication and division result register

These registers hold the results of a multiplication or division. Each of them is 32-bit long.
The initial value after a reset is indeterminate.

■ MODE SETTING

In the FR family, operation mode is set by the mode setting pins (MD2, MD1, MD0) and the mode register (MODR) .

1. Mode pins

They are three pins of MD2, MD1 and MD0, and specify the contents of the mode vector fetch.

Mode pins			Mode name	Reset vector Access area
MD2	MD1	MD0		
0	0	0	Internal ROM mode vector	Internal

Note : In the FR family, external mode vector fetch by multiplex bus is not supported.

2. Mode register (MODR)

The data that are written in the mode register by mode vector fetch is called mode data.

After the mode register (MODR) is set, it operates in the operation mode set by this register.

The mode register is set by all reset source. And Mode data is not written in by the user program.

Note : Conventionally, the address (0000 07FF$_H$) of the mode register for the FR family holds nothing.

Details of the mode register

MODR 0007FD$_H$

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	ROMA	WTH1	WTH0

Operation mode setting bits

Initial Value XXXXXXXX$_B$

[bit7 to bit3] Reserved bits

Be sure to set these bits to “00000$_B$”.

Setting the bits to any value other than “00000$_B$” may result in an unpredictable operation .

[bit2] ROMA (Internal ROM enable bit)

This bit sets to make internal F-bus RAM and F-bus ROM areas valid or not.

ROMA	Function	Remarks
0	External ROM mode	Embedded F-bus RAM becomes valid, and internal ROM area (50000$_H$ to 100000$_H$) becomes external area.
1	Internal ROM mode	Embedded F-bus RAM and F-bus ROM become valid.

[bit1, bit0] WTH1, WTH0 (Bus width specifying bits)

These bits specify bus widths for the external bus mode.

In case of the external bus mode, this value is set in the DBW0 bit of ACR0 (CS0 area) .

WTH1	WTH0	Function	Remarks
0	0	8-bit bus width	External bus mode
0	1	16-bit bus width	External bus mode
1	0	—	Setting disabled
1	1	Single chip mode	Single chip mode

■ MEMORY SPACE

1. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) linearly accessible to the CPU .

• Direct Addressing Areas

The following address space areas are used as I/O areas.

These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.

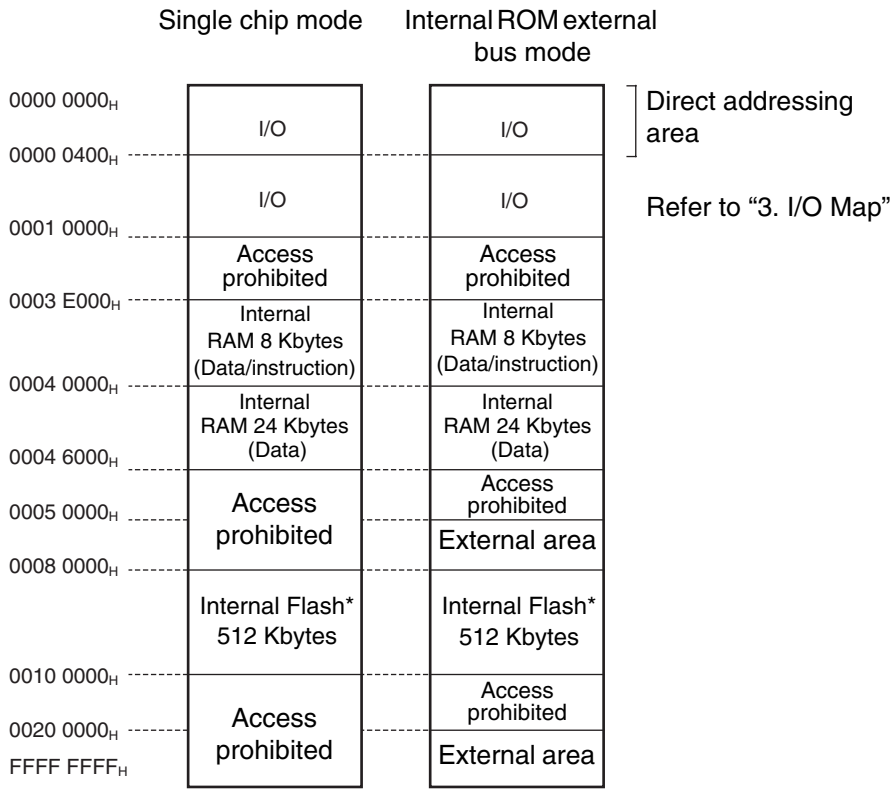
The direct area varies depending on the size of data to be accessed as follows :

→ byte data access : 000_H to $0FF_H$

→ half word data access : 000_H to $1FF_H$

→ word data access : 000_H to $3FF_H$

2. Memory Map (MB91F345B/F346B)



* : Internal Flash area of MB91F346B is 0008 0000_H to 0018 0000_H (1 Mbyte.)

■ I/O MAP

The following table shows the correspondence between the memory space area and each register of the peripheral resource.

[How to read the table]

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H	PDR0 [R/W] B XXXXXXXX	PDR1 [R/W] B XXXXXXXX	PDR2 [R/W] B XXXXXXXX	PDR3 [R/W] B XXXXXXXX	T-unit Port Data Register

Read/write attribute, Access unit
(B : Byte, H : Half Word, W : Word)
Initial value after a reset
Register name (First-column register at address 4n; second-column register at address 4n + 1...)
Location of left-most register (When using word access, the register in column 1 is in the MSB side of the data.)

Note : Initial values of register bits are represented as follows :

"1" : Initial value is "1".
"0" : Initial value is "0".
"X" : Initial value is "indeterminate".
"–" : No physical register at this location

Access is barred with an undefined data access attribute.

Address	Register				Block
	0	1	2	3	
000000H	PDR0 [R/W] B, H XXXXXXXX	PDR1 [R/W] B, H XXXXXXXX	PDR2 [R/W] B, H XXXXXXXX	PDR3 [R/W] B, H XXXXXXXX	Port Data Registers
000004H	PDR4 [R/W] B, H XXXXXXXX	PDR5 [R/W] B, H XXXXXXXX	PDR6 [R/W] B, H ----XXXX	—	
000008H	—				
00000CH	PDRC [R/W] B, H -----XXX	PDRD [R/W] B, H XXXXXXXX	PDRE [R/W] B, H XXXXXXXX	—	
000010H to 00001CH	—				Reserved
000020H	—			ADERH0 [R/W] 11111111	A/D converter 0
000024H	ADCS01 [R/W] 00000000	ADCS00 [R, R/W] 00000000	ADCR0 [R] ------XX XXXXXXXX		
000028H	ADCT0 [R/W] 00010000 00101100		ADSCH0 [R/W] 0---0000	ADECH0 [R/W] ----0000	
00002CH	ADCR0M [R] ------XX XXXXXXXX		ADCR1M [R] ------XX XXXXXXXX		AD mirror data register
000030H	—			ADERH1 [R/W] 11111111	A/D converter 1
000034H	ADCS11 [R/W] 00000000	ADCS10 [R, R/W] 00000000	ADCR1 [R] ------XX XXXXXXXX		
000038H	ADCT1 [R/W] 00010000 00101100		ADSCH1 [R/W] 0----000	ADECH1 [R/W] -----000	
00003CH	—				Reserved
000040H	EIRR0 [R/W] 00000000	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt INT 0 to INT7
000044H	DICR [R/W] 00000000	HRCL [R, R/W] 0--11111	—		DLY / I-unit
000048H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
00004CH	—		TMCSR0 [R, RW] 00000000 00000000		
000050H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054H	—		TMCSR1 [R, RW] 00000000 00000000		

(Continued)

Address	Register				Block
	0	1	2	3	
000058H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
00005CH	—		TMCSR2 [R, RW] 00000000 00000000		
000060H	SCR0/IBCR0 [R, R/W] *	SMR0 [W, R/W] *	SSR0 [R, R/W] *	ESCR0/IBSR0 [R/W] *	Multi function Serial Interface 0 FIFO 0
000064H	RDR0/TDR0 [R/W] *		BGR01 [R/W] *	BGR00 [R/W] *	
000068H	ISMK0 [R/W] *	IBSA [R/W] *	FCR01 [R/W] *	FCR00 [R/W] *	
00006CH	FBYTE02 [R/W] *	FBYTE01 [R/W] *	—		
000070H	SCR1/IBCR1 [R, R/W] *	SMR1 [W, R/W] *	SSR1 [R, R/W] *	ESCR1/IBSR1 [R/W] *	Multi function Serial Interface 1 FIFO 1
000074H	RDR1/TDR1 [R/W] *		BGR11 [R/W] *	BGR10 [R/W] *	
000078H	ISMK1 [R/W] *	IBSA1 [R/W] *	FCR11 [R/W] *	FCR10 [R/W] *	
00007CH	FBYTE12 [R/W] *	FBYTE11 [R/W] *	—		
000080H	SCR2/IBCR2 [R, R/W] *	SMR2 [W, R/W] *	SSR2 [R, R/W] *	ESCR2/IBSR2 [R/W] *	Multi function Serial Interface 2
000084H	RDR2/TDR2 [R/W] *		BGR21 [R/W] *	BGR20 [R/W] *	
000088H	ISMK2 [R/W] *	IBSA2 [R/W] *	—		
00008CH	—				
000090H	SCR3/IBCR3 [R, R/W] *	SMR3 [W, R/W] *	SSR3 [R, R/W] *	ESCR3/IBSR3 [R/W] *	Multi function Serial Interface 3
000094H	RDR3/TDR3 [R/W] *		BGR31 [R/W] *	BGR30 [R/W] *	
000098H	ISMK3 [R/W] *	IBSA3 [R/W] *	—		
00009CH	—				

(Continued)

Address	Register				Block
	0	1	2	3	
0000A0H	SCR4/IBCR4 [R, R/W] *	SMR4 [W, R/W] *	SSR4 [R, R/W] *	ESCR4/IBSR4 [R/W] *	Multi function Serial Interface 4
0000A4H	RDR4/TDR4 [R/W] *		BGR41 [R/W] *	BGR40 [R/W] *	
0000A8H	ISMK4 [R/W] *	IBSA4 [R/W] *	—		
0000ACH	—				
0000B0H	SCR5/IBCR5 [R, R/W] *	SMR5 [W, R/W] *	SSR5 [R, R/W] *	ESCR5/IBSR5 [R/W] *	Multi function Serial Interface 5
0000B4H	RDR5/TDR5 [R/W] *		BGR51 [R/W] *	BGR50 [R/W] *	
0000B8H	ISMK5 [R/W] *	IBSA5 [R/W] *	—		
0000BCH	—				
0000C0H	EIRR1 [R/W] 00000000	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt INT 8 to INT15
0000C4H	EIRR2 [R/W] 00000000	ENIR2 [R/W] 00000000	ELVR2 [R/W] 00000000 00000000		External interrupt INT 16 to INT 23
0000C8H to 0000CCH	—				Reserved
0000D0H	CPCLRB/CPCLR [R/W] H 11111111 11111111		TCDT [R/W] H 00000000 00000000		16-bit Free Run Timer 0
0000D4H	TCCSH [R/W] B 00000000	TCCSL [R/W] B 01000000	—		
0000D8H	—				Reserved
0000DCH	IPCPH0/IPCPL0 [R] XXXXXXXX XXXXXXXX		IPCPH1/IPCPL1 [R] XXXXXXXX XXXXXXXX		16-bit Input Capture
0000E0H	IPCPH2/IPCPL2 [R] XXXXXXXX XXXXXXXX		IPCPH3/IPCPL3 [R] XXXXXXXX XXXXXXXX		
0000E4H	ICSH01 [R/W] ------00	ICSL01 [R/W] 00000000	ICSH23 [R/W] ------00	ICSL23 [R/W] 00000000	
0000E8H	OCCPH0/OCCPL0 [R/W] XXXXXXXX XXXXXXXX		OCCPH1/OCCPL1 [R/W] XXXXXXXX XXXXXXXX		Output Compare 0, 1
0000ECH	OCCPH2/OCCPL2 [R/W] XXXXXXXX XXXXXXXX		OCCPH3/OCCPL3 [R/W] XXXXXXXX XXXXXXXX		Output Compare 2, 3
0000F0H	OCS01 [R/W] 11101100 00001100		OCS23 [R/W] 11101100 00001100		Output Compare 0 to 3 Control

(Continued)

Address	Register				Block
	0	1	2	3	
0000F4H	OCMOD [R/W] B 00000000	—			Output Compare Mode Select
0000F8H	PWCSR0 [R/W, R] B, H, W 0000000X 00000000		PWCR0 [R] H, W 00000000 00000000		PWC
0000FCH	—	PDIVR0 [R/W] B, H, W XXXXX000	—		
000100H	PRLH0 [R/W] B, H, W XXXXXXXX	PRLL0 [R/W] B, H, W XXXXXXXX	PRLH1 [R/W] B, H, W XXXXXXXX	PRLL1 [R/W] B, H, W XXXXXXXX	PPG 0 to PPG F
000104H	PRLH2 [R/W] B, H, W XXXXXXXX	PRLL2 [R/W] B, H, W XXXXXXXX	PRLH3 [R/W] B, H, W XXXXXXXX	PRLL3 [R/W] B, H, W XXXXXXXX	
000108H	PPGC0 [R/W] B, H, W 0000000X	PPGC1 [R/W] B, H, W 0000000X	PPGC2 [R/W] B, H, W 0000000X	PPGC3 [R/W] B, H, W 0000000X	
00010CH	PRLH4 [R/W] B, H, W XXXXXXXX	PRLL4 [R/W] B, H, W XXXXXXXX	PRLH5 [R/W] B, H, W XXXXXXXX	PRLL5 [R/W] B, H, W XXXXXXXX	
000110H	PRLH6 [R/W] B, H, W XXXXXXXX	PRLL6 [R/W] B, H, W XXXXXXXX	PRLH7 [R/W] B, H, W XXXXXXXX	PRLL7 [R/W] B, H, W XXXXXXXX	
000114H	PPGC4 [R/W] B, H, W 0000000X	PPGC5 [R/W] B, H, W 0000000X	PPGC6 [R/W] B, H, W 0000000X	PPGC7 [R/W] B, H, W 0000000X	
000118H	PRLH8 [R/W] B, H, W XXXXXXXX	PRLL8 [R/W] B, H, W XXXXXXXX	PRLH9 [R/W] B, H, W XXXXXXXX	PRLL9 [R/W] B, H, W XXXXXXXX	
00011CH	PRLHA [R/W] B, H, W XXXXXXXX	PRLLA [R/W] B, H, W XXXXXXXX	PRLHB [R/W] B, H, W XXXXXXXX	PRLLB [R/W] B, H, W XXXXXXXX	
000120H	PPGC8 [R/W] B, H, W 0000000X	PPGC9 [R/W] B, H, W 0000000X	PPGCA [R/W] B, H, W 0000000X	PPGCB [R/W] B, H, W 0000000X	
000124H	PRLHC [R/W] B, H, W XXXXXXXX	PRLLC [R/W] B, H, W XXXXXXXX	PRLHD [R/W] B, H, W XXXXXXXX	PRLLD [R/W] B, H, W XXXXXXXX	
000128H	PRLHE [R/W] B, H, W XXXXXXXX	PRLLE [R/W] B, H, W XXXXXXXX	PRLHF [R/W] B, H, W XXXXXXXX	PRLLF [R/W] B, H, W XXXXXXXX	
00012CH	PPGCC [R/W] B, H, W 0000000X	PPGCD [R/W] B, H, W 0000000X	PPGCE [R/W] B, H, W 0000000X	PPGCF [R/W] B, H, W 0000000X	

(Continued)

Address	Register				Block
	0	1	2	3	
000130H	PPGTRG [R/W] B, H, W 00000000 00000000		—	PPGGATEC [R/W] B XXXXXX00	PPG 0-F
000134H	PPGREVC [R/W] B, H, W 00000000 00000000		—		
000138H to 00014CH	—				Reserved
000150H	CPCLRB/CPCLR [R/W] W 11111111 11111111 11111111 11111111				32 bit Free Run Timer 0
000154H	TCDT [R/W] W 00000000 00000000 00000000 00000000				
000158H	TCCSH [R/W] B 00000000	TCCSL [R/W] B 01000000	—		32 bit Input Capture Unit 4 to 7
00015CH	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000160H	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000164H	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000168H	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00016CH	—	ICS45 [R/W] 00000000	—	ICS67 [R/W] 00000000	
000170H	OCCP4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				32 bit Output Compare 4 to 7
000174H	OCCP5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000178H	OCCP6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00017CH	OCCP7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000180H	OCS45 [R/W] 11101100 00001100		OCS67 [R/W] 11101100 00001100		
000184H	RCRH1 [W] B, H 00000000	RCRL0 [W] B, H 00000000	UDCR1 [R] B, H 00000000	UDCR0 [R] B, H 00000000	Up/Down Counter 0, 1
000188H	CCRH0 [R/W] B, H 00000000	CCRL0 [R/W] B, H 00000000	—	CSR0 [R/W] B 00000000	
00018CH	CCRH1 [R/W] B, H 00000000	CCRL1 [R/W] B, H 00000000	—	CSR1 [R/W] B 00000000	

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Address	Register				Block
	0	1	2	3	
000190H	—				Reserved
000194H	RCRH3 [W] B, H 00000000	RCRL2 [W] B, H 00000000	UDCR3 [R] B, H 00000000	UDCR2 [R] B, H 00000000	Up/Down Counter 2, 3
000198H	CCRH2 [R/W] B, H 00000000	CCRL2 [R/W] B, H 00000000	—	CSR2 [R/W] B 00000000	
00019CH	CCRH3 [R/W] B, H 00000000	CCRL3 [R/W] B, H 00000000	—	CSR3 [R/W] B 00000000	
0001A0H to 0001ACH	—				Reserved
0001B0H	SCR6/IBCR6 [R, R/W] *	SMR6 [W, R/W] *	SSR6 [R, R/W] *	ESCR6/IBSR6 [R/W] *	Multi function Serial Interface 6
0001B4H	RDR6/TDR6 [R/W] *		BGR61 [R/W] *	BGR60 [R/W] *	
0001B8H	ISMK6 [R/W] *	IBSA6 [R/W] *	—		
0001BCH	—				
0001C0H	SCR7/IBCR7 [R, R/W] *	SMR7 [W, R/W] *	SSR7 [R, R/W] *	ESCR7/IBSR7 [R/W] *	Multi function Serial Interface 7
0001C4H	RDR7/TDR7 [R/W] *		BGR71 [R/W] *	BGR70 [R/W] *	
0001C8H	ISMK7 [R/W] *	IBSA7 [R/W] *	—		
0001CCH	—				
0001D0H	SCR8/IBCR8 [R, R/W] *	SMR8 [W, R/W] *	SSR8 [R, R/W] *	ESCR8/IBSR8 [R/W] *	Multi function Serial Interface 8
0001D4H	RDR8/TDR8 [R/W] *		BGR81 [R/W] *	BGR80 [R/W] *	
0001D8H	ISMK8 [R/W] *	IBSA8 [R/W] *	—		
0001DCH	—				

(Continued)

Address	Register				Block
	0	1	2	3	
0001E0H	SCR9/IBCR9 [R, R/W] *	SMR9 [W, R/W] *	SSR9 [R, R/W] *	ESCR9/IBSR9 [R/W] *	Multi function Serial Interface 9
0001E4H	RDR9/TDR9 [R/W] *		BGR91 [R/W] *	BGR90 [R/W] *	
0001E8H	ISMK9 [R/W] *	IBSA9 [R/W] *	—		
0001ECH	—				
0001F0H	SCRA/IBCRA [R, R/W] *	SMRA [W, R/W] *	SSRA [R, R/W] *	ESCRA/IBSRA [R/W] *	Multi function Serial Interface 10
0001F4H	RDRA/TDRA [R/W] *		BGRA1 [R/W] *	BGRA0 [R/W] *	
0001F8H	ISMKA [R/W] *	IBSAA [R/W] *	—		
0001FCH	—				
000200H	DMACA0 [R/W] 00000000 00000000 00000000 00000000				DMAC
000204H	DMACB0 [R/W] 00000000 00000000 00000000 00000000				
000208H	DMACA1 [R/W] 00000000 00000000 00000000 00000000				
00020CH	DMACB1 [R/W] 00000000 00000000 00000000 00000000				
000210H	DMACA2 [R/W] 00000000 00000000 00000000 00000000				
000214H	DMACB2 [R/W] 00000000 00000000 00000000 00000000				
000218H	DMACA3 [R/W] 00000000 00000000 00000000 00000000				
00021CH	DMACB3 [R/W] 00000000 00000000 00000000 00000000				
000220H	DMACA4 [R/W] 00000000 00000000 00000000 00000000				
000224H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000228H to 00023CH	—				Reserved
000240H	DMACR [R/W] 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC

(Continued)

Address	Register				Block
	0	1	2	3	
000244H to 0003BCH	—				Reserved
0003A0H	DATA_A [-/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				MIN/MAX/ABS
0003A4H	DATA_B [-/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003A8H	MIN [R/W] 00000000 00000000 00000000 00000000				
0003ACH	MAX [R/W] 00000000 00000000 00000000 00000000				
0003B0H	ABS [R/W] 00000000 00000000 00000000 00000000				
0003B4H to 0003ECH	—				Reserved
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	DDR0 [R/W] B, H 00000000	DDR1 [R/W] B, H 00000000	DDR2 [R/W] B, H 00000000	DDR3 [R/W] B, H 00000000	Data Direction Registers
000404H	DDR4 [R/W] B, H 00000000	DDR5 [R/W] B, H 00000000	DDR6 [R/W] B, H ----0000	—	
000408H	—				
00040CH	DDRC [R/W] B, H -----000	DDRD [R/W] B, H 00000000	DDRE [R/W] B, H 00000000	—	
000410H	—				
000414H to 00041CH	—				Reserved

(Continued)

Address	Register				Block
	0	1	2	3	
000420H	PFR0 [R/W] B, H 00000000	PFR1 [R/W] B, H 00000000	PFR2 [R/W] B, H 00000000	PFR3 [R/W] B, H 00000000	Registers
000424H	PFR4 [R/W] B, H 00000000	PFR5 [R/W] B, H 00000000	PFR6 [R/W] B, H ----0000	—	
000428H	—				
00042CH	PFRC [R/W] B, H -----000	PFRD [R/W] B, H 00000000	PFRE [R/W] B, H 00000000	—	
000430H	—				
000434H to 00043CH	—				Reserved
000440H	ICR00 [R, R/W] ---11111	ICR01 [R, R/W] ---11111	ICR02 [R, R/W] ---11111	ICR03 [R, R/W] ---11111	Interrupt Control Unit
000444H	ICR04 [R, R/W] ---11111	ICR05 [R, R/W] ---11111	ICR06 [R, R/W] ---11111	ICR07 [R, R/W] ---11111	
000448H	ICR08 [R, R/W] ---11111	ICR09 [R, R/W] ---11111	ICR10 [R, R/W] ---11111	ICR11 [R, R/W] ---11111	
00044CH	ICR12 [R, R/W] ---11111	ICR13 [R, R/W] ---11111	ICR14 [R, R/W] ---11111	ICR15 [R, R/W] ---11111	
000450H	ICR16 [R, R/W] ---11111	ICR17 [R, R/W] ---11111	ICR18 [R, R/W] ---11111	ICR19 [R, R/W] ---11111	
000454H	ICR20 [R, R/W] ---11111	ICR21 [R, R/W] ---11111	ICR22 [R, R/W] ---11111	ICR23 [R, R/W] ---11111	
000458H	ICR24 [R, R/W] ---11111	ICR25 [R, R/W] ---11111	ICR26 [R, R/W] ---11111	ICR27 [R, R/W] ---11111	
00045CH	ICR28 [R, R/W] ---11111	ICR29 [R, R/W] ---11111	ICR30 [R, R/W] ---11111	ICR31 [R, R/W] ---11111	
000460H	ICR32 [R, R/W] ---11111	ICR33 [R, R/W] ---11111	ICR34 [R, R/W] ---11111	ICR35 [R, R/W] ---11111	
000464H	ICR36 [R, R/W] ---11111	ICR37 [R, R/W] ---11111	ICR38 [R, R/W] ---11111	ICR39 [R, R/W] ---11111	
000468H	ICR40 [R, R/W] ---11111	ICR41 [R, R/W] ---11111	ICR42 [R, R/W] ---11111	ICR43 [R, R/W] ---11111	
00046CH	ICR44 [R, R/W] ---11111	ICR45 [R, R/W] ---11111	ICR46 [R, R/W] ---11111	ICR47 [R, R/W] ---11111	
000470H to 00047CH	—				Reserved

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Address	Register				Block
	0	1	2	3	
000480H	RSRR [R, R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXX	Clock Control Unit
000484H	CLKR [R/W] 00000000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488H	—		OSCCR [R/W] XXXXXXXX	—	
00048CH	—				Reserved
000490H	OSCR [R/W] 00000000	OSCT [R/W] XXXXXXXX	—		Stb. Wait Timer
000494H to 0004FCH	—				Reserved
000500H	PCR0 [R/W] B, H 00000000	PCR1 [R/W] B, H 00000000	—		Port Pull-up Control Registers
000504H	—	PCR5 [R/W] B, H 00000000	PCR6 [R/W] B, H ----0000	—	
000508H	—				
00050CH	PCRC [R/W] B, H -----000	PCRD [R/W] B, H 00000000	PCRE [R/W] B, H 00000000	—	
000510H	—				
000514H to 00051CH	—				Reserved
000520H	EPFR0 [R/W] B, H 00000000	EPFR1 [R/W] B, H 00000000	EPFR2 [R/W] B, H 11111111	EPFR3 [R/W] B, H 11111111	Extra Port Function Registers
000524H	EPFR4 [R/W] B, H 11111111	EPFR5 [R/W] B, H 11111111	EPFR6 [R/W] B, H ----1000	—	
000528H	—				
00052CH	EPFRC [R/W] B, H -----000	EPFRD [R/W] B, H 00000000	EPFRE [R/W] B, H 00000000	—	
000530H	—				
000534H to 000550H	—				Reserved

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Address	Register				Block
	0	1	2	3	
000554H	TTCR0 [R/W] B, H, W 11110000	—		TSTPR0 [R] B, H, W 00000000	Timing Generator
000558H	COMP0 [R/W] B, H, W 00000000	COMP2 [R/W] B, H, W 00000000	COMP4 [R/W] B, H, W 00000000	COMP6 [R/W] B, H, W 00000000	
00055CH	TTCR1 [R/W] B, H, W 11110000	—		TSTPR1 [R] B, H, W 00000000	
000560H	COMP8 [R/W] B, H, W 00000000	COMP10 [R/W] B, H, W 00000000	COMP12 [R/W] B, H, W 00000000	COMP14 [R/W] B, H, W 00000000	
000564H to 000574H	—				Reserved
000578H	ADTGS [R/W] B ------00	—			AD Trigger Select
00057CH to 00063CH	—				Reserved
000640H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 00110X00 00000000		T-Unit
000644H	ASR1 [R/W] 00000000 XXXXXXXX		ACR1 [R/W] 0XXX0X00 00X0XXXX		
000648H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXX0X00 00X0XXXX		
00064CH	ASR3 [R/W] 00000000 XXXXXXXX		ACR3 [R/W] 01XX0X00 00X0XXXX		
000650H	—				
000654H to 00065CH	—				
000660H	AWR0 [R/W] B, H, W 01111111 11111111		AWR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000664H	AWR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		AWR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000668H to 00067CH	—				
000680H	CSER [R/W] B, H, W 00000001	—		TCR [W] B, H, W 0000XXXX	
000684H	—				
000688H to 0007F8H	—				Not Used

(Continued)

Address	Register				Block
	0	1	2	3	
0007FC$_H$	—	MODR [W] XXXXXXXX	—		—
000800$_H$ to 000AFC$_H$	—				Not Used
000B00$_H$	ESTS0 [R/W] B X0000000	ESTS1 [R/W] B XXXXXXXX	ESTS2 [R] B 1XXXXXXX	—	DSU (Evaluation Chip Only)
000B04$_H$	ECTL0 [R/W] B 0X000000	ECTL1 [R/W] B 00000000	ECTL2 [W] B 000X0000	ECTL3 [R/W] B 00X00X11	
000B08$_H$	ECNT0 [W] B XXXXXXXX	ECNT1 [W] B XXXXXXXX	EUSA [W] B XXX00000	EDTC [W] B 0000XXXX	
000B0C$_H$	EWPT [R] H 00000000 00000000		ECTL4 [R] ([R/W]) B -0X00000	ECTL5 [R] ([R/W]) B ----000X	
000B10$_H$	EDTR0 [W] H XXXXXXXX XXXXXXXX		EDTR1 [W] H XXXXXXXX XXXXXXXX		
000B14$_H$ to 000B1C$_H$	—				
000B20$_H$	EIA0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24$_H$	EIA1 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B28$_H$	EIA2 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B2C$_H$	EIA3 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B30$_H$	EIA4 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B34$_H$	EIA5 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B38$_H$	EIA6 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B3C$_H$	EIA7 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B40$_H$	EDTA [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B44$_H$	EDTM [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B48$_H$	EOA0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	0	1	2	3	
000B4C$_H$	EOA1 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU (Evaluation Chip Only)
000B50$_H$	EPCR [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B54$_H$	EPSR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B58$_H$	EIAM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B5C$_H$	EIAM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B60$_H$	EOAM0/EODM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B64$_H$	EOAM1/EODM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B68$_H$	EOD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B6C$_H$	EOD1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B70$_H$ to 000FFC$_H$	—				Reserved
001000$_H$	DMASA0 [R/W] 00000000 00000000 00000000 00000000				DMAC
001004$_H$	DMADA0 [R/W] 00000000 00000000 00000000 00000000				
001008$_H$	DMASA1 [R/W] 00000000 00000000 00000000 00000000				
00100C$_H$	DMADA1 [R/W] 00000000 00000000 00000000 00000000				
001010$_H$	DMASA2 [R/W] 00000000 00000000 00000000 00000000				
001014$_H$	DMADA2 [R/W] 00000000 00000000 00000000 00000000				
001018$_H$	DMASA3 [R/W] 00000000 00000000 00000000 00000000				
00101C$_H$	DMADA3 [R/W] 00000000 00000000 00000000 00000000				
001020$_H$	DMASA4 [R/W] 00000000 00000000 00000000 00000000				
001024$_H$	DMADA4 [R/W] 00000000 00000000 00000000 00000000				
001028$_H$ to 006FFC$_H$	—				Reserved

(Continued)

(Continued)

Address	Register				Block
	0	1	2	3	
007000H	FLCR [R/W] 01101000	—			Flash Interface
007004H	FLWC [R/W] 00110011	—			
007008H to 007019H	—				Reserved
007020H	WREN [R/W] 00000000	—			
007024H to 00702CH	—				
007030H	WA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Flash Interface
007034H	WD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007038H	WA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00703CH	WD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007040H	WA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007044H	WD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007048H	WA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Flash Interface
00704CH	WD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007050H	WA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007054H	WD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007058H	WA5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00705CH	WD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007060H	WA6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007064H	WD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007068H	WA7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00706CH	WD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

* : Refer to “Hardware manual” for initial value.

■ VECTOR TABLE

Interrupt factor	Interrupt No.		Interrupt level	Offset	Address of TBR default	DMA transfer	DMAC STOP factor
	Decimal	Hexa-decimal					
Reset	0	00	—	3FC$_H$	000FFFFC$_H$	—	
Mode vector	1	01	—	3F8$_H$	000FFFF8$_H$	—	
System reserved	2	02	—	3F4$_H$	000FFFF4$_H$	—	
System reserved	3	03	—	3F0$_H$	000FFFF0$_H$	—	
System reserved	4	04	—	3EC$_H$	000FFFEC$_H$	—	
System reserved	5	05	—	3E8$_H$	000FFFE8$_H$	—	
System reserved	6	06	—	3E4$_H$	000FFFE4$_H$	—	
Coprocessor absent trap	7	07	—	3E0$_H$	000FFFE0$_H$	—	
Coprocessor error trap	8	08	—	3DC$_H$	000FFFDC$_H$	—	
INTE instruction	9	09	—	3D8$_H$	000FFFD8$_H$	—	
Instruction break exception	10	0A	—	3D4$_H$	000FFFD4$_H$	—	
Operand break trap	11	0B	—	3D0$_H$	000FFFD0$_H$	—	
Step trace trap	12	0C	—	3CC$_H$	000FFFCC$_H$	—	
NMI request (tool)	13	0D	—	3C8$_H$	000FFFC8$_H$	—	
Undefined instruction exception	14	0E	—	3C4$_H$	000FFFC4$_H$	—	
NMI request	15	0F	15 (F$_H$) fixed	3C0$_H$	000FFFC0$_H$	—	
External interrupt 0	16	10	ICR00	3BC$_H$	000FFFBC$_H$	—	
External interrupt 1	17	11	ICR01	3B8$_H$	000FFFB8$_H$	—	
External interrupt 2	18	12	ICR02	3B4$_H$	000FFFB4$_H$	—	
External interrupt 3	19	13	ICR03	3B0$_H$	000FFFB0$_H$	—	
External interrupt 4	20	14	ICR04	3AC$_H$	000FFFAC$_H$	—	
External interrupt 5	21	15	ICR05	3A8$_H$	000FFFA8$_H$	—	
External interrupt 6	22	16	ICR06	3A4$_H$	000FFFA4$_H$	—	
External interrupt 7	23	17	ICR07	3A0$_H$	000FFFA0$_H$	—	
Reload timer 0	24	18	ICR08	39C$_H$	000FFF9C$_H$	○	
Reload timer 1	25	19	ICR09	398$_H$	000FFF98$_H$	○	
Reload timer 2	26	1A	ICR10	394$_H$	000FFF94$_H$	○	
UART0 RX/I^{2}C0 status	27	1B	ICR11	390$_H$	000FFF90$_H$	○	STOP
UART0 TX	28	1C	ICR12	38C$_H$	000FFF8C$_H$	○	
UART1 RX/I^{2}C1 status	29	1D	ICR13	388$_H$	000FFF88$_H$	○	STOP
UART1 TX	30	1E	ICR14	384$_H$	000FFF84$_H$	○	
UART2 RX/I^{2}C2 status	31	1F	ICR15	380$_H$	000FFF80$_H$	○	STOP
UART2 TX	32	20	ICR16	37C$_H$	000FFF7C$_H$	○	

(Continued)

Interrupt factor	Interrupt No.		Interrupt level	Offset	Address of TBR default	DMA transfer	DMAC STOP factor
	Decimal	Hexa-decimal					
UART3 RX/TX/SX	33	21	ICR17	378H	000FFF78H	—	
UART4 RX/TX/SX	34	22	ICR18	374H	000FFF74H	—	
UART5 RX/TX/SX	35	23	ICR19	370H	000FFF70H	—	
UART6 RX/TX/SX	36	24	ICR20	36CH	000FFF6CH	—	
UART7 RX/TX/SX	37	25	ICR21	368H	000FFF68H	—	
UART8 RX/TX/SX	38	26	ICR22	364H	000FFF64H	—	
UART9 RX/TX/SX	39	27	ICR23	360H	000FFF60H	—	
UART10 RX/TX/SX	40	28	ICR24	35CH	000FFF5CH	—	
A/D Converter 0	41	29	ICR25	358H	000FFF58H	◯	
A/D Converter 1	42	2A	ICR26	354H	000FFF54H	◯	
PWC (measurement completed, overflow)	43	2B	ICR27	350H	000FFF50H	—	
System reserved	44	2C	ICR28	34CH	000FFF4CH	—	
Up/Down Counter 1	45	2D	ICR29	348H	000FFF48H	—	
Up/Down Counter 2, 3	46	2E	ICR30	344H	000FFF44H	—	
Timebase Timer Overflow	47	2F	ICR31	340H	000FFF40H	—	
PPG 0/PPG 1/PPG 4/PPG 5	48	30	ICR32	33CH	000FFF3CH	—	
PPG 2/PPG 3/PPG 6/PPG 7	49	31	ICR33	338H	000FFF38H	—	
PPG 8/PPG 9/PPG C/PPG D	50	32	ICR34	334H	000FFF34H	—	
PPG A/PPG B/PPG E/PPG F	51	33	ICR35	330H	000FFF30H	—	
Free Running Timer 0	52	34	ICR36	32CH	000FFF2CH	—	
Free Running Timer 1	53	35	ICR37	328H	000FFF28H	—	
Input Capture 0/ Input Capture 1/ Input Capture 2/ Input Capture 3	54	36	ICR38	324H	000FFF24H	—	
Input Capture 4/ Input Capture 5/ Input Capture 6/ Input Capture 7	55	37	ICR39	320H	000FFF20H	—	
Output Compare 0/ Output Compare 1/ Output Compare 2/ Output Compare 3	56	38	ICR40	31CH	000FFF1CH	—	
Output Compare 4/ Output Compare 5/ Output Compare 6/ Output Compare 7	57	39	ICR41	318H	000FFF18H	—	

(Continued)

(Continued)

Interrupt factor	Interrupt No.		Interrupt level	Offset	Address of TBR default	DMA transfer	DMAC STOP factor
	Decimal	Hexadecimal					
System reserved	58	3A	ICR42	314H	000FFF14H	—	
External interrupt 8 to External interrupt 15	59	3B	ICR43	310H	000FFF10H	—	
External interrupt 16 to External interrupt 23	60	3C	ICR44	30CH	000FFF0CH	—	
Up/Down Counter 0	61	3D	ICR45	308H	000FFF08H	—	
DMA (0 channel to 4 channels)	62	3E	ICR46	304H	000FFF04H	—	
Delayed interrupt activation	63	3F	ICR47	300H	000FFF00H	—	
System reserved (Used by REALOS)	64	40	—	2FCH	000FFEFCH	—	
System reserved (Used by REALOS)	65	41	—	2F8H	000FFEF8H	—	
System reserved	66	42	—	2F4H	000FFEF4H	—	
System reserved	67	43	—	2F0H	000FFEF0H	—	
System reserved	68	44	—	2ECH	000FFEECH	—	
System reserved	69	45	—	2E8H	000FFEE8H	—	
System reserved	70	46	—	2E4H	000FFEE4H	—	
System reserved	71	47	—	2E0H	000FFEE0H	—	
System reserved	72	48	—	2DCH	000FFEDCH	—	
System reserved	73	49	—	2D8H	000FFED8H	—	
System reserved	74	4A	—	2D4H	000FFED4H	—	
System reserved	75	4B	—	2D0H	000FFED0H	—	
System reserved	76	4C	—	2CCH	000FFECCH	—	
System reserved	77	4D	—	2C8H	000FFEC8H	—	
System reserved	78	4E	—	2C4H	000FFEC4H	—	
System reserved	79	4F	—	2C0H	000FFEC0H	—	
Used by INT instruction	80 to 255	50 to FF	—	2BCH to 000H	000FFEBCH to 000FFC00H	—	

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage *	V_{CC}	V_{SS}–0.5	V_{SS} + 4.0	V
Analog power supply voltage *	AV_{CC}	V_{SS}–0.3	V_{SS} + 4.0	V
Input voltage *	V_I	V_{SS}–0.3	V_{SS} + 4.0	V
Analog pin input voltage *	V_{IA}	V_{SS}–0.3	AVcc + 0.5	V
Storage temperature	Tstg	–40	+125	°C

* : The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0$)

Parameter	Symbol	Value		Unit
		Min	Max	
Operating temperature	Ta	– 40	+ 85	°C
Power supply voltage	V_{CC}	3.0	3.6	V
Analog power supply voltage	AV_{CC}	3.0	V_{CC}	V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Sym-bol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	VCC	During normal operation Ta = + 25 °C fcp = 50 MHz, fcpp = 25 MHz	—	65	80	mA	
	I_{CCS}		SLEEP mode during normal operation Ta = + 25 °C fcp = 50 MHz, fcpp = 25 MHz	—	30	35	mA	
	I_{CCH}		In STOP mode Ta = + 25 °C, fclk = 0	—	66	390	µA	
			In STOP mode Ta = + 45 °C, fclk = 0	—	140	760	µA	
“H” level input voltage	V_{IH}	—	—	$V_{CC} \times 0.7$	—	V_{CC}	V	P20 to P27, P30 to P37, P40 to P47
“L” level input voltage	V_{IL}	—	—	V_{SS}	—	$V_{CC} \times 0.3$	V	P20 to P27, P30 to P37, P40 to P47
“H” level input voltage	V_{IH}	—	—	$V_{CC} \times 0.8$	—	V_{CC}	V	
“L” level input voltage	V_{IL}	—	—	V_{SS}	—	$V_{CC} \times 0.2$	V	
“H” level output voltage	V_{OH}	—	I_{OH} = –4 mA	V_{CC} – 0.5	—	V_{CC}	V	
“L” level output voltage	V_{OL}	—	I_{OL} = 4 mA	V_{SS}	—	0.4	V	
Input leak current	I_{IL}	—	—	–5	—	+ 5	µA	
A/D power supply current (analog + digital)	—	—	—	—	7.2	—	mA	At operating A/D 2 unit
	—	—	—	—	—	5	µA	At power down operation*
A/D reference power supply current (AVRH to V_{SS})	—	—	—	—	940	—	µA	At operating A/D 2 unit AVRH = 3.0 V, VSS = 0.0 V
	—	—	—	—	—	10	µA	At power down operation*

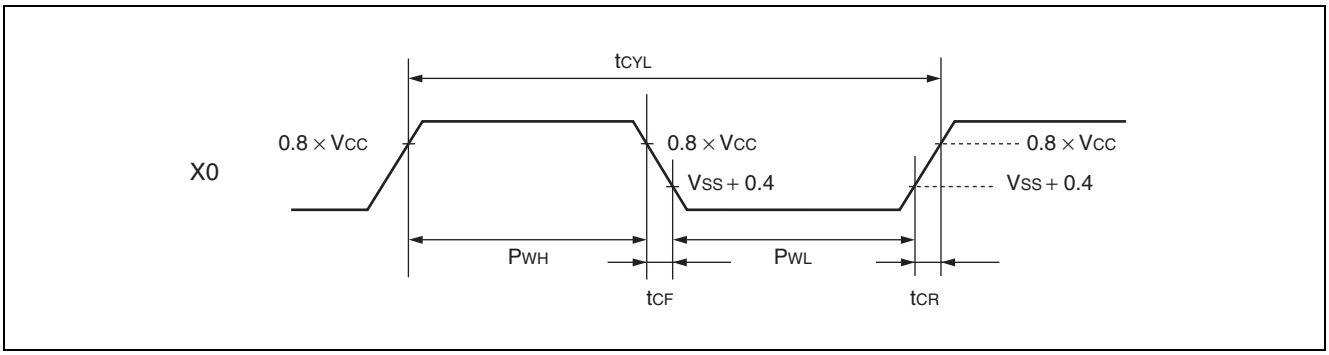
* : Current when A/D converter is not operating and the CPU is in stop mode.

4. AC Characteristics

(1) Main Clock Input Standard

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_C	X0	—		12.5		MHz	
Input clock cycle	t_{CYL}		—	—	80	—	ns	
Input clock pulse width	—		P_{WH}/t_{CYL} P_{WL}/t_{CYL}	40	—	60	%	
Input clock rise time and fall time	t_{CF} t_{CR}		—	—	—	5	ns	In external clock
Internal operating clock frequency	f_{CP}	—	—	—	—	50	MHz	CPU core operation clock
Peripheral clock cycle time	t_{CYCP}	—	—	30	—	—	ns	Peripheral clock is derived from internal operating clock divided by 1/1 to 1/16.



(2) PLL Oscillation Stabilization Wait Time (LOCK UP Time)

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to + 85 °C)

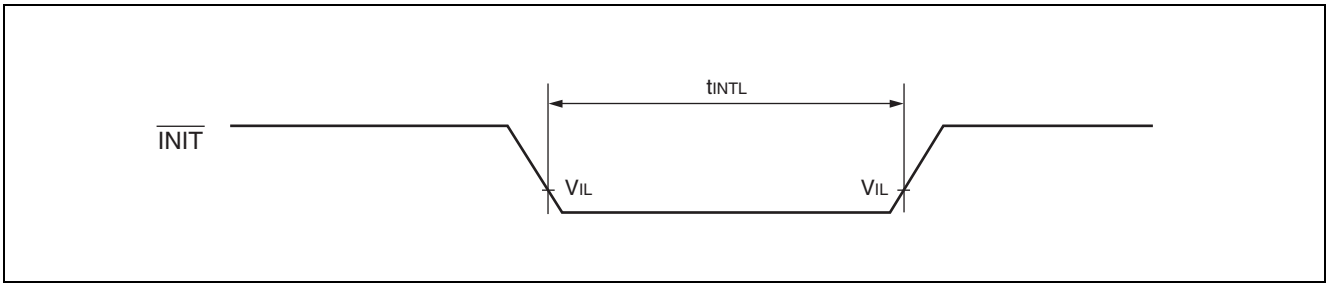
Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
PLL oscillation stabilization wait time (LOCK UP time)	t_{LOCK}	500	—	µs	Wait time until the PLL oscillation is stable.

(3) Reset Input Standard

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Pin	Condi-tions	Value		Unit	Remarks
				Min	Max		
Reset input time (except power-on)	t_{INTL}	$\overline{INIT}$	—	$t_{CP} \times 10$	—	ns	

Notes :
- t_{CP} is cycle time for CPU operation clock (CLKB) .
- For power-on, input $\overline{INIT}$ = “L” more than regulator voltage stabilization wait time. If the oscillation stabilization wait time of used oscillator takes more time than regulator voltage stabilization wait time, input $\overline{INIT}$ = “L” until the oscillation is stable.



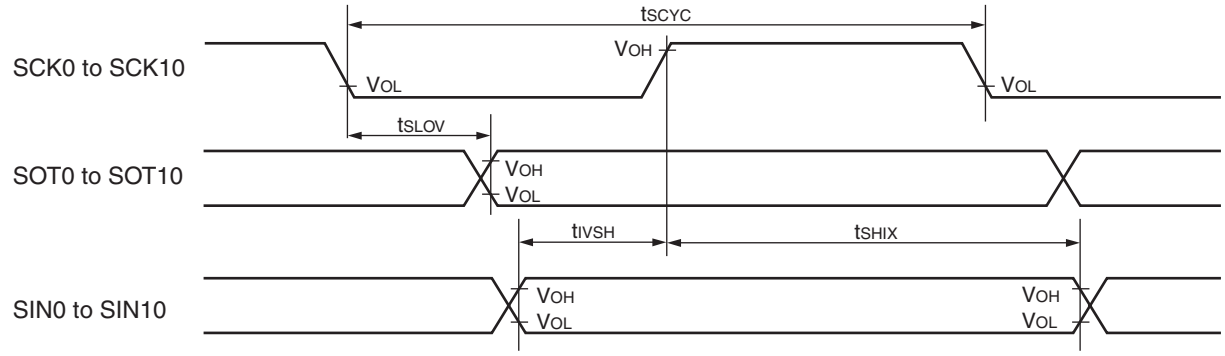
(4) UART Timing

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to + 85 °C)

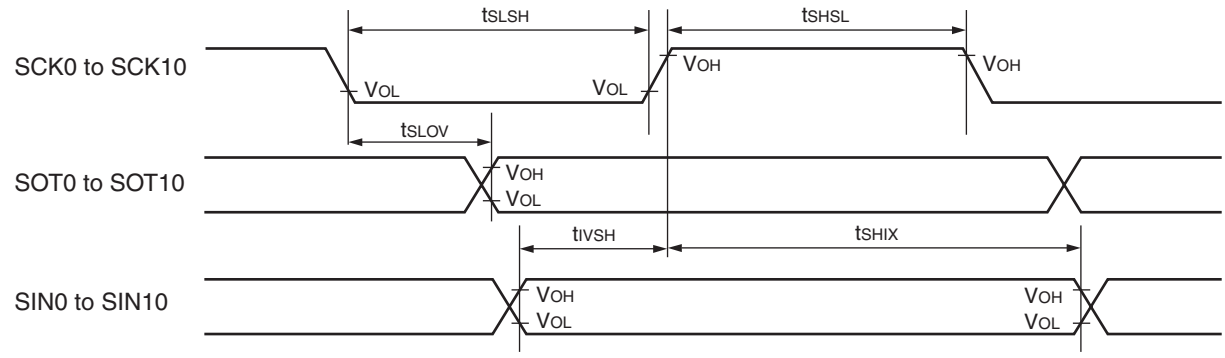
Parameter	Symbol	Pin	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK10	Internal shift clock operation	4 t_{CYCP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK10, SOT0 to SOT10		– 20	+ 20	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK10, SIN0 to SIN10		30	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK10, SIN0 to SIN10		20	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK10	External shift clock operation	2 t_{CYCP}	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK10		2 t_{CYCP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK10, SOT0 to SOT10		—	30	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK10, SIN0 to SIN10		20	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK10, SIN0 to SIN10		20	—	ns

Notes : • AC rating in CLK synchronous mode
• t_{CYCP} is the peripheral clock cycle time.

- Internal shift clock mode



- External shift clock mode



(5) Free-run timer clock, Reload timer event Input , up down counter Input , Input capture Input, Interrupt Input Timing

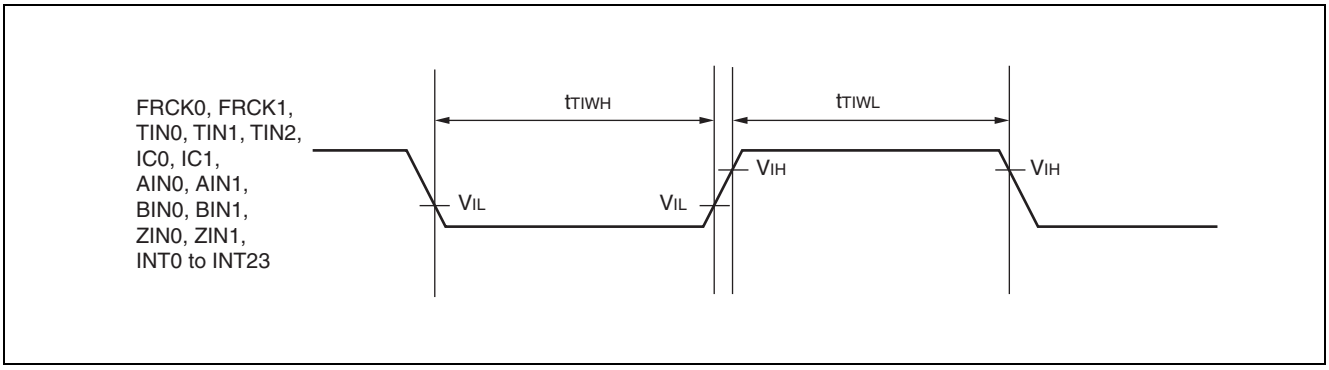
(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	FRCK0, FRCK1, TIN0, TIN1, TIN2, IC0, IC1, AIN0, AIN1, BIN0, BIN1, ZIN0, ZIN1	—	$t_{CYCP} \times 2$	—	ns	*1
		INT0 to INT23		$t_{CYCP} \times 3$	—	ns	*2
				1.0	—	µs	*3

*1 : t_{CYCP} is cycle time for peripheral clock.

*2 : Except in stop time

*3 : In stop time

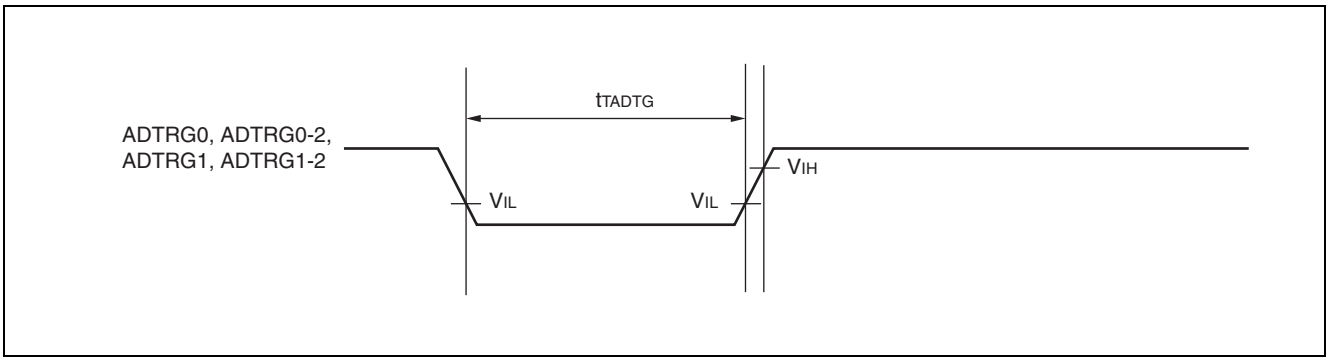


(6) A/D Trigger Input Timing

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
A/D trigger input (falling time)	t_{TADTG}	ADTRG0, ADTRG0-2, ADTRG1, ADTRG1-2	—	$t_{CYCP} \times 2$	—	ns	*

* : t_{CYCP} is the peripheral clock cycle time.



(7) I²C timing

• At master mode operating

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*3		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	R = 1 kΩ C = 50 pF*4	0	100	0	400	kHz	
"L" period of SCL clock	t_{LOW}		4.7	—	1.3	—	µs	
"H" period of SCL clock	t_{HIGH}		4.0	—	0.6	—	µs	
SCL↓ → SDA output delay time	t_{DLDAT}		—	5 × M*1	—	5 × M*1	ns	
Bus free time between [STOP condition] and [START condition]	t_{BUS}		4.7	—	1.3	—	µs	
SDA data input hold time (vs. SCL↓)	t_{HDDAT}		2 × M*1	—	2 × M*1	—	µs	
SDA data input setup time (vs. SCL↑)	t_{SUDAT}		250	—	100*2	—	ns	
Setup time of [repeat START condition] SCL↑ → SDA↓	t_{SUSTA}		4.7	—	0.6	—	µs	
Hold time of [repeat START condition] SDA↓ → SCL↓	t_{HDSTA}		4.0	—	0.6	—	µs	After that, the first clock pulse is generated.
Setup time of [STOP condition] SCL↑ → SDA↑	t_{SUSTO}		4.0	—	0.6	—	µs	

*1 : M = Resource clock cycle (ns)

*2 : A high-speed mode I²C bus device can be used for a typical mode I²C bus system as long as the device satisfies a requirement of "$t_{SUDAT} \geq 250$ ns".
When a device does not extend the "L" period of the SCL signal, the next data must be outputted to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDAT}) in which the SCL line is released.

*3 : For use at over 100 kHz, set the resource clock to at least 6 MHz.

*4 : R and C represent the pull-up resistor and load capacitor of the SCL and SDA output lines, respectively.

• At slave mode operating

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*3		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	R = 1 kΩ C = 50 pF*4	0	100	0	400	kHz	
"L" period of SCL clock	t_{LOW}		4.7	—	1.3	—	µs	
"H" period of SCL clock	t_{HIGH}		4.0	—	0.6	—	µs	
SCL ↓ → SDA output delay time	t_{DLDAT}		—	5 × M*1	—	5 × M*1	ns	
Bus free time between [STOP condition and START condition]	t_{BUS}		4.7	—	1.3	—	µs	
SDA data input hold time (vs. SCL↓)	t_{HDDAT}		2 × M*1	—	2 × M*1	—	µs	
SDA data input setup time (vs. SCL↑)	t_{SUDAT}		250	—	100*2	—	ns	
Setup time of [repeat START condition] SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	0.6	—	µs	
Hold time of [repeat START condition] SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	0.6	—	µs	After that, the first clock pulse is generated.
Setup time of [STOP condition] SCL ↑ → SDA ↑	t_{SUSTO}		4.0	—	0.6	—	µs	

*1 : M = Resource clock cycle (ns)

*2 : A high-speed mode I^2C bus device can be used for a typical mode I^2C bus system as long as the device satisfies a requirement of "$t_{SUDAT} \geq 250$ ns".
When the device does not extend the "L" period of the SCL signal, the next data must be outputted to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDAT}) in which the SCL line is released.

*3 : For use at over 100 kHz, set the resource clock to at least 6 MHz.

*4 : R and C represent the pull-up resistor and load capacitor of the SCL and SDA output lines, respectively.

(8) Regulator Voltage Wait Time

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Regulator voltage wait time	t_{REG}	250	—	µs	Wait time until the regulator voltage is stable

5. Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, AVRH = 3.0 V to 3.6 V, Ta = –40 °C to + 85 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Resolution	—	—	10	bit	
Total error*1	–3.0	—	+3.0	LSB	AV_{CC} = 3.3 V, AVRH = 3.3 V
Nonlinear error*1	–2.5	—	+2.5	LSB	
Differential linear error*1	–1.9	—	+1.9	LSB	
Zero transition voltage*1	–1.5	+0.5	+2.5	LSB	
Full transition voltage*1	AVRH–3.5	AVRH–1.5	AVRH+0.5	LSB	
Minimum comparison time*2	0.6	—	—	µs	Not including sampling time
Minimum sampling time*2	0.3*3	—	—	µs	
Conversion time	0.9*3	1.1	—	µs	
Power supply current (analog + digital)	—	7.2	—	mA	At operating A/D 2 unit
	—	—	5	µA	At power down operation*4
Reference power supply current (between AVRH and AVRL)	—	940	—	µA	At operating A/D 2 unit AVRH = 3.0 V, AVRL = 0.0 V
	—	—	10	µA	At power down operation*4
Analog input capacitance	—	—	20	pF	
Interchannel disparity	—	—	4	LSB	

*1 : Measured in the CPU sleep state.

*2 : Depends on the clock cycle supplied to the peripheral resource.

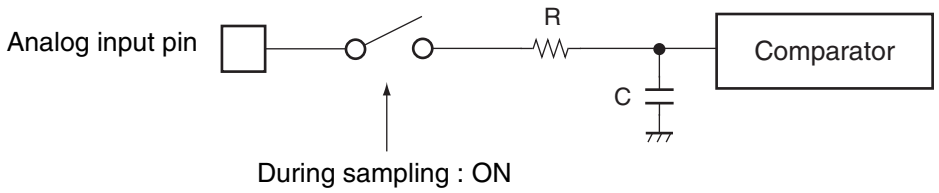
*3 : No external load

*4 : Current when the A/D converter is not operating and the CPU is in stop mode

• About the external impedance of the analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sampling and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input circuit model

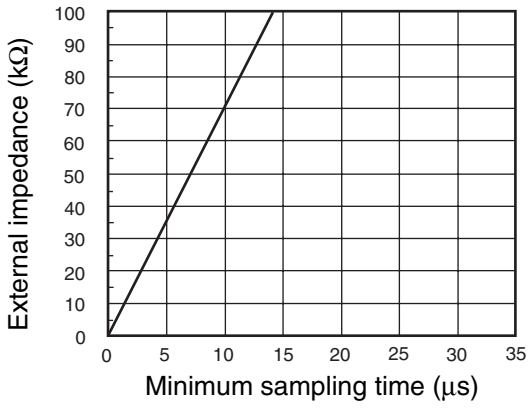


	R	C
MB91F345B/F346B	1.5 kΩ (Max)	20.0 pF (Max)

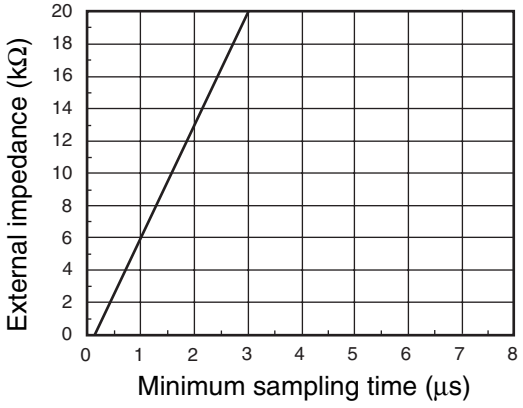
Note : The values are reference values.

- The relationship between the external impedance and minimum sampling time

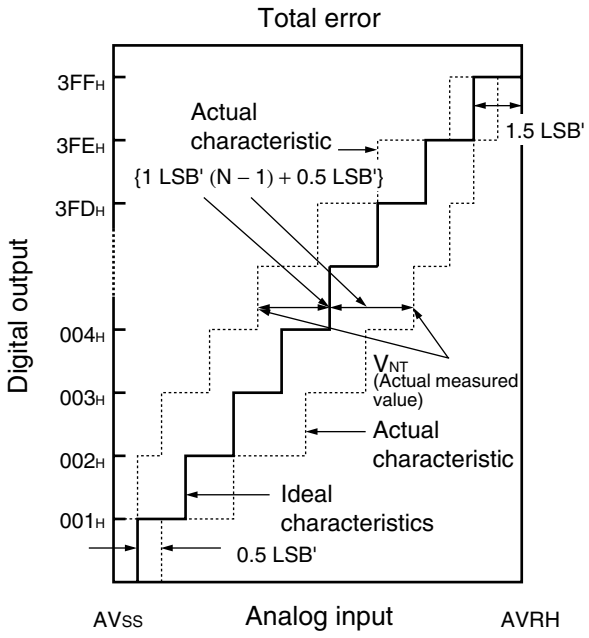
[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]



- **A/D Converter Block Electrical Characteristics**
  - Resolution
    Analog variations recognized by an A/D converter.
  - Linearity error
    Deviation of actual conversion characteristics from an ideal line, which is across zero-transition point (“00 0000 0000” ←→ “00 0000 0001”) and full-scale transition point (“11 1111 1110” ←→ “11 1111 1111”).
  - Differential linearity error
    Deviation from ideal value of input voltage, which is required for changing output code by 1 LSB.
  - Total error
    Difference between actual value and ideal value. The error includes zero-transition error, full-scale transition error, and linearity error.



$$1\ \text{LSB'}\ (\text{ideal value}) = \frac{\text{AVRH} - \text{AV}_{SS}}{1024}\ [\text{V}]$$

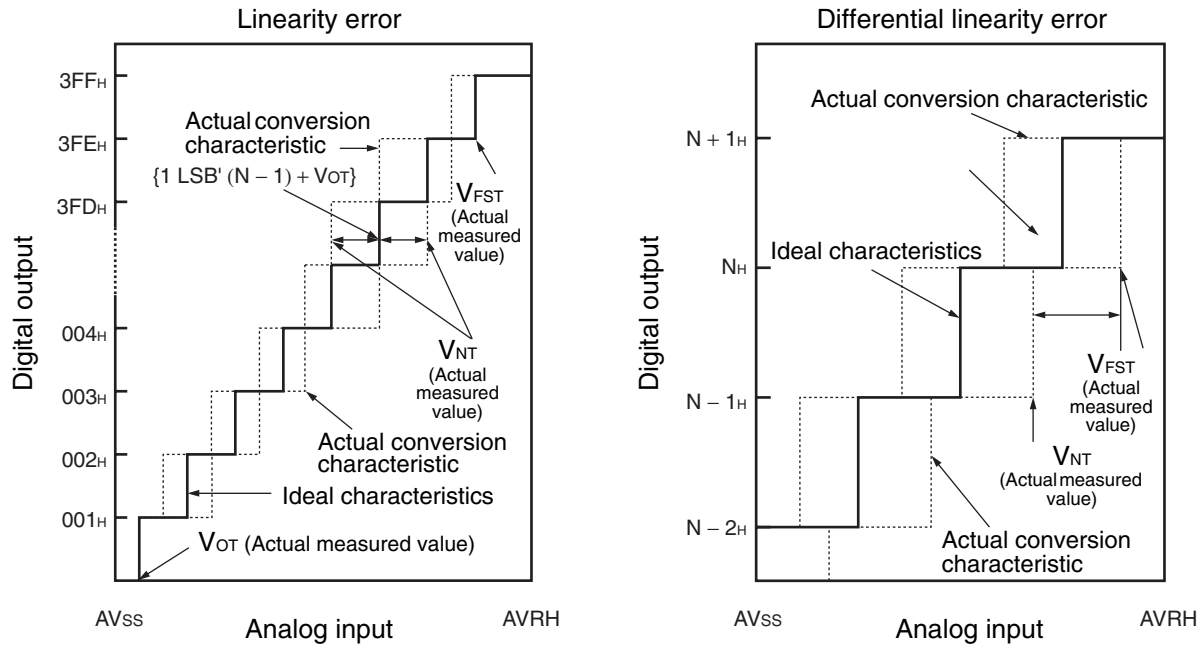
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB'} \times (\text{N} - 1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB'}}$$

V_{NT} : Transition voltage for digital output to change from (N + 1) H to N_H.

V_{OT}' (ideal value) = AV_{SS} + 0.5 LSB' [V]
V_{FST}' (ideal value) = AVRH – 1.5 LSB' [V]

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + V_{OT}\}}{1\ LSB'}\ [LSB]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB'} - 1[LSB]$$

$$1\ LSB = \frac{V_{FST} - V_{OT}}{1022}\ [V]$$

V_{OT} : Transition voltage for digital output to change from $(000)_H$ to $(001)_H$.
V_{FST} : Transition voltage for digital output to change from $(3FE)_H$ to $(3FF)_H$.

• About errors

- As |AVRH – AV_{SS}| becomes smaller, values of relative errors grow larger.

6. Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

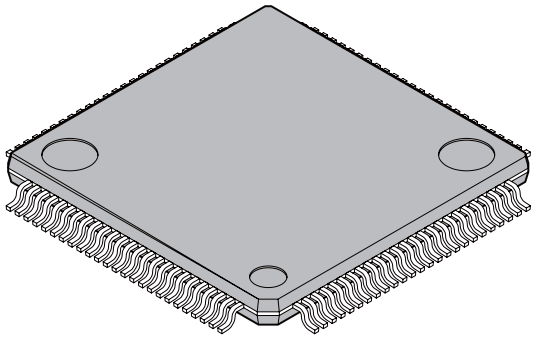
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	—	—	1	15	s	Excludes 00_H programming prior erasure
Byte write time	—	—	6	100	µs	Not including system-level overhead time
Chip write time	—	—	3.4	56	s	Not including system-level overhead time
Erase/write cycle	—	10000	—	—	cycle	
Flash memory data retain period	Average Ta = + 55 °C	10	—	—	year	*

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 55 °C) .

■ ORDERING INFORMATION

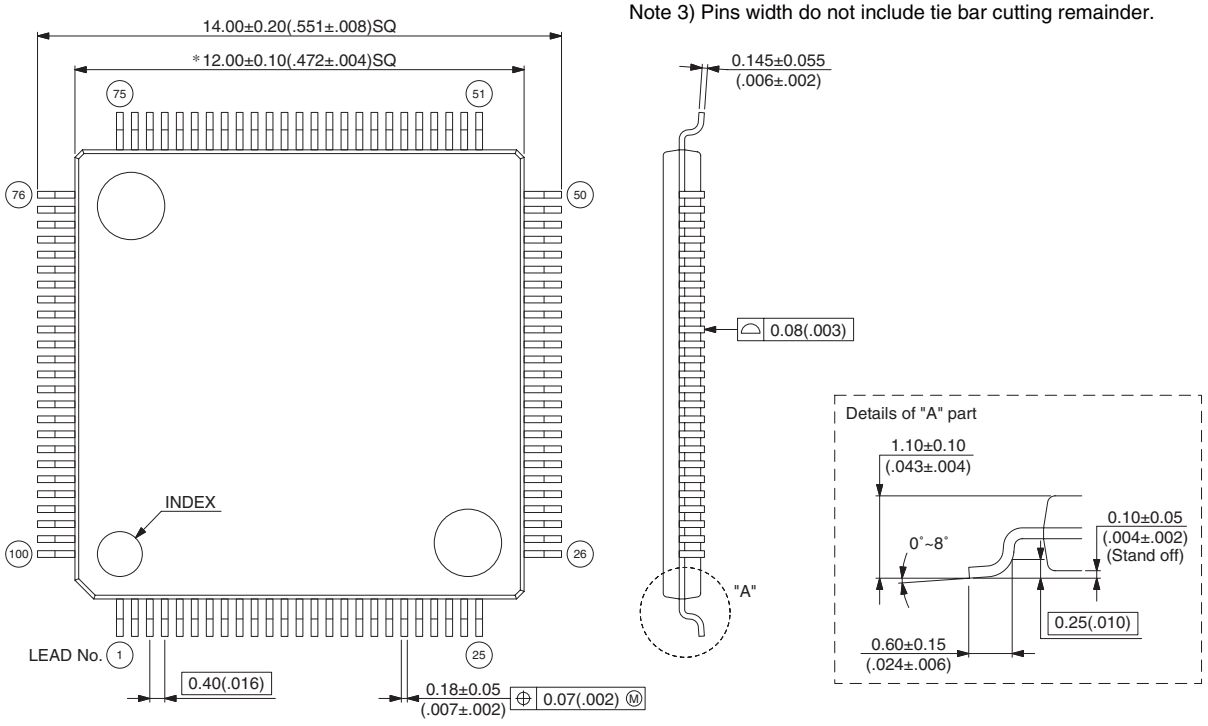
Part number	Package
MB91F345BPFT-GE1 MB91F346BPFT-GE1	100-pin plastic TQFP (FPT-100P-M18)

■ PACKAGE DIMENSIONS

100-pin plastic TQFP		
	Lead pitch	0.40 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.40g
(FPT-100P-M18)	Code(Reference)	P-TFQFP100-12 × 12-0.40

100-pin plastic TQFP
(FPT-100P-M18)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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