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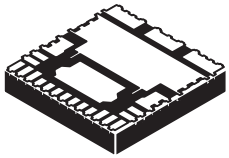
RoHS

Smart High Side Switch Module (Triple 6.0 mΩ and Dual 17 mΩ)

06XS3517

HIGH SIDE SWITCH



Bottom View

FKSUFFIX
98ART10511D
24-PIN PQFN

PB FREE

The 06XS3517 device is a five channel 12 V high side switch module with integrated control and a high number of protective and diagnostic functions. It is designed for automotive lighting and industrial applications. The low $R_{DS(ON)}$ channels (three 6.0 mΩ, two 17 mΩ) can control different types of lighting applications; bulbs, Xenon-HID lights, and LEDs. Control, device configuration, and diagnostics are performed through a 16-bit SPI interface (3.3 V or 5.0 V). When communication with the external microcontroller or VDD is lost, the device enters a fail-safe operation mode, but remains operational, controllable, and protected.

The channels are controlled by an external clock signal and allow staggered switch-on delay, to improve EMC performances. Programmable output voltage slew rates (individually programmable) further helps improve EMC performance. To avoid shutting off the device upon inrush current while still being able to closely track the load current, a dynamic over-current threshold profile is featured. Load current in each channel can be sensed. The duty cycle of the channels can be controlled independently and the switching frequency of each of them can be doubled. The 06XS3517 is housed in a non-leaded Power QFN package with an exposed pad.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC06XS3517AFK	-40°C to 125°C	24 PQFN

Features

- Three 6.0 mΩ and Two 17 mΩ protected high side switches
- Optional sixth channel with an external SMART MOSFET
- 16-bit SPI communication interface with daisy chain capability
- Accurate temperature & current sensing
- Fail-safe mode including autorestart
- PWM module with programmable switch-on delay and frequency prescaler
- Over-voltage, under-voltage, over-current, over-temperature, and reverse battery protections
- Dedicated bulb over-current protection with inrush current handling
- Sleep mode with low current consumption
- Normal operating range 7.0 V to 20 V, extended operating range 6.0 V - 28 V

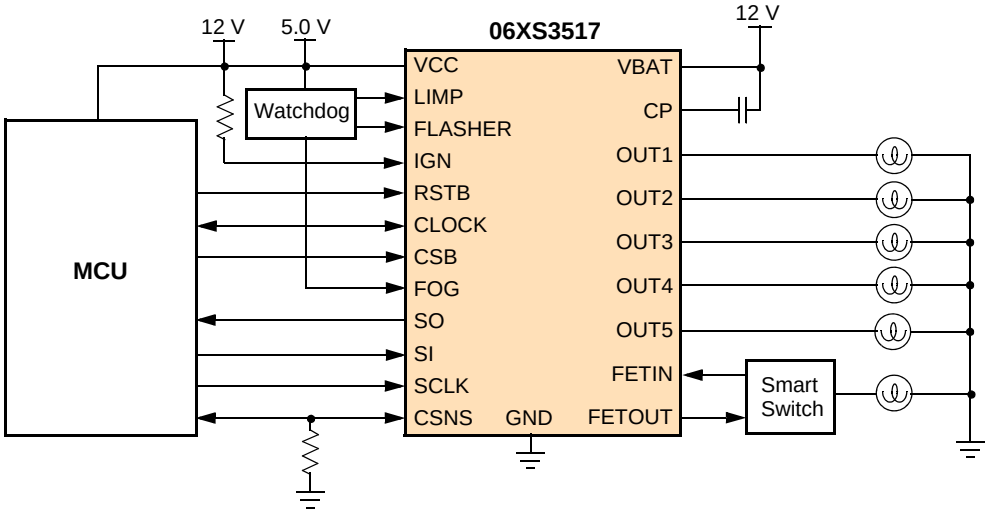


Figure 1. 06XS3517 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

freescale

INTERNAL BLOCK DIAGRAM

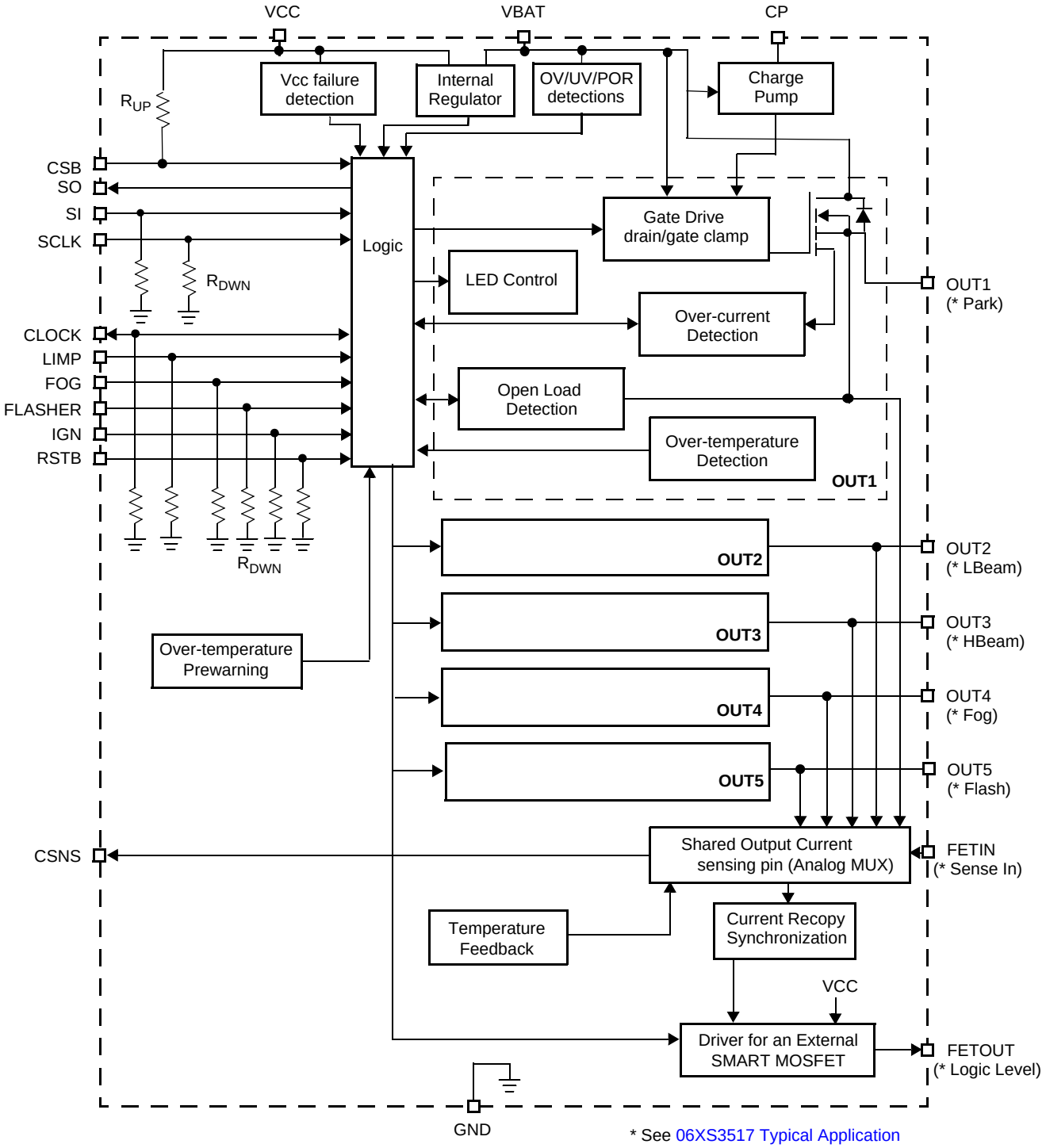


Figure 2. 06XS3517 Simplified Internal Block Diagram

PIN CONNECTIONS

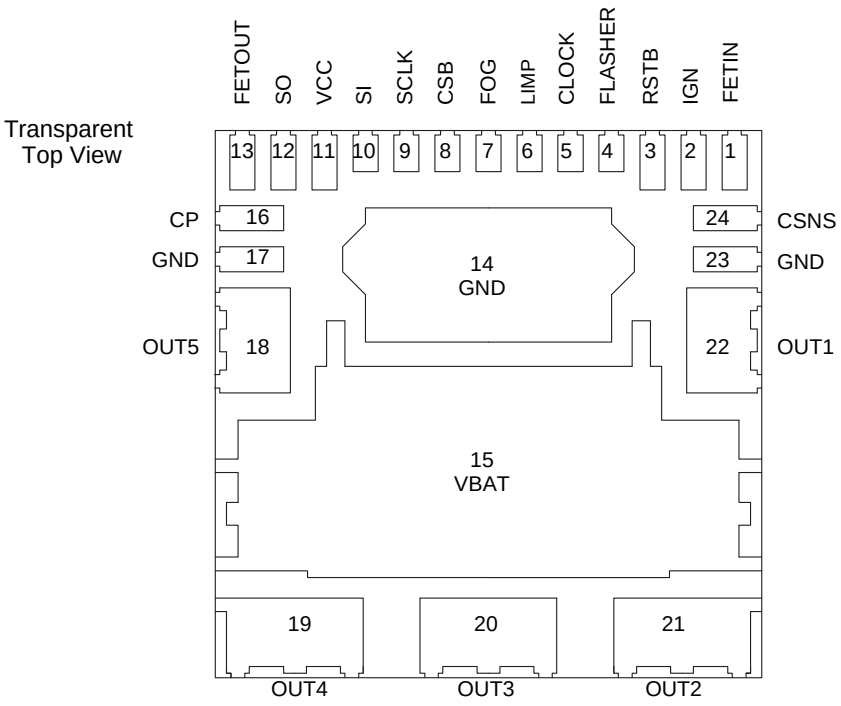


Figure 3. 06XS3517 Pin Connections

Table 1. 06XS3517 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on Page 17.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	FETIN	Input	External FET Input	This pin receives the current sense signal of the external SMART MOSFET.
2	IGN	Input	Ignition Input (Active High)	This input wakes the device. It also controls the Outputs 1 and 2 in case of Fail mode activation. This pin has an internal pull-down resistor.
3	RSTB	Input	Reset	This input wakes the device. It is also used to initialize the device configuration and fault registers through SPI. This digital pin has a passive internal pull-down.
4	FLASHER	Input	Flasher Input (Active High)	This input wakes the device and allows control over channel 5. (FLASHER) This pin has an internal pull-down resistor.
5	CLOCK	Input/Output	Clock Input	This pin state depends on RSTB logic level. As long as RSTB input pin is set to logic [0], this pin is pulled up to report wake events. Otherwise, the PWM frequency and timing are generated from this digital clock input by the PWM module. This pin has a passive internal pull-down.
6	LIMP	Input	Limp Home Input (Active High)	The Fail mode can be activated by this digital input. This pin has a passive internal pull-down.
7	FOG	Input	FOG Input (Active high)	This input wakes the device. This pin has a passive internal pull-down.
8	CSB	Input	Chip Select (Active Low)	When this digital signal is high, SPI signals are ignored. Asserting this pin low starts a SPI transaction. The transaction is signaled as completed when this signal returns high. This pin has a passive internal pull-up resistance.

Table 1. 06XS3517 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on Page 17.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
9	SCLK	Input	SPI Clock Input	This digital input pin is connected to the master microcontroller providing the required bit shift clock for SPI communication. This pin has a passive internal pull-down resistance.
10	SI	Input	Master-Out Slave-In	This data input is sampled on the positive edge of the SCLK. This pin has a passive internal pull-down resistance.
11	VCC	Power	Logic Supply	SPI logic power supply.
12	SO	Output	Master-In Slave-Out	SPI data is sent to the MCU by this pin. This data output changes on the negative edge of SCLK and when CSB is high, this pin is high-impedance.
13	FETOUT	Output	External FET Gate	This pin outputs a logic level that can be used to control an external SMART MOSFET. This output is also called OUT6. If OUT6 is not used in the application, this output pin is set to logic high when the current sense output becomes valid when CSNS sync SPI bit is set to logic [1].
14,17,23	GND	Ground	Ground	This pin is the ground for the logic and analog circuitry of the device.
15	VBAT	Power	Battery Input	Power supply pin.
16	CP	Output	Charge Pump	This pin is the connection for an external tank capacitor (for internal use only).
22 18	OUT1 OUT5	Output	Output 1 Output 5	Protected 17 mΩ high side switch output terminals.
21 20 19	OUT2 OUT3 OUT4	Output	Output 2 Output 3 Output 4	Protected 6.0 mΩ high side switch output terminals
24	CSNS	Output	Current Sense Output	This pin is outputs the current sense signal of OUT1:OUT5, FETIN current, and it is used externally to generate a ground-referenced voltage for the microcontroller to monitor output current. If desired, this pin can also report a voltage proportional to the temperature on the GND flag. OUT1:OUT5, FETin current sensing and temperature sensing are activated through the SPI interface.

Notes

1. The pins 14, 17, and 23 must be shorted on the board.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground, unless mentioned otherwise. Exceeding these ratings may cause malfunction or permanent device damage.

Parameter	Symbol	Value	Unit
ELECTRICAL RATINGS			
Over-voltage Test Range (all OUT[1:5] ON with nominal DC current) Maximum operating voltage Load dump (400 ms) @ 25 °C	V_{BAT}	 28 40	V
Reverse Polarity Voltage Range (all OUT[1:5] ON with nominal DC current) 2.0 Min @ 25°C	V_{BAT}	 -18	V
VCC Supply Voltage	V_{CC}	-0.3 to 5.5	V
OUT[1:5] Voltage Positive Negative (ground disconnected)	V_{OUT}	 40 -16	V
Digital Current in Clamping Mode (SI, SCLK, CSB, RSTB, IGN, FLASHER, LIMP, and FOG)	I_{IN}	±1.0	mA
FETIN Input Current	I_{FETIN}	+10 -1.0	mA
SO, FETOUT, CLOCK, and CSNS Outputs Voltage	V_{SO}	-0.3 to V_{CC}+0.3	V
Outputs Clamp Energy Using Single Pulse Method (L = 2.0 mH; R = 0.0 Ω; V_{BAT} = 14 V @150 °C initial) OUT[1,5] OUT[2:4]	 $E_{1,5}$ $E_{2,3,4}$	 30 100	mJ
ESD Voltage[(2)] Human Body Model (HBM) Human Body Model (HBM) OUT [1:5], VPWR, and GND Charge Device Model (CDM) Corner Pins (1, 13, 19, 21) All Other Pins (2-12, 14-18, 20, 22-24)	V_{ESD}	 ±2000 ±8000 ±750 ±500	V

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model.

Table 2. Maximum Ratings *(continued)*

All voltages are with respect to ground, unless mentioned otherwise. Exceeding these ratings may cause malfunction or permanent device damage.

Parameter	Symbol	Value	Unit
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Peak Package Reflow Temperature During Reflow[3]	T_{PPRT}	260	°C
Storage Temperature	T_{STG}	-55 to 150	°C
THERMAL RESISTANCE			
Thermal Resistance, Junction to Case[4]	$R_{\theta JC}$	1.0	°K/W

Notes

3. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. Typical value guaranteed per design.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUTS (VBAT, VCC)					
Battery Supply Voltage Range	V_{BAT}				V
Full performance & short-circuit		7.0	–	20.0	
Extended voltage range[5]		6.0	–	28.0	
Battery Supply Under-voltage (UV flag is set ON)	V_{BATUV}	5.0	5.5	6.0	V
Battery Supply Over-voltage (OV flag is set ON)	V_{BATOV}	27.5	30	32.5	V
Battery Voltage Clamp[6]	$V_{BATCLAMP}$	40	–	48	V
Battery Supply Power on Reset					V
If V_{BAT} < 5.5 V, V_{BAT} = V_{CC}	$V_{BATPOR1}$	2.0	–	3.0	
If V_{BAT} < 5.5 V, V_{CC} = 0	$V_{BATPOR2}$	2.0	–	4.0	
VBAT Supply Current @ 25 °C and V_{BAT} = 12 V and V_{CC} = 5.0 V					
Sleep state current, outputs opened	$I_{BATSLEEP1}$	–	0.5	5.0	µA
Sleep state current, outputs grounded	$I_{BATSLEEP2}$	–	0.5	5.0	µA
Normal mode, IGN = 5.0 V, RSTB = 5.0 V, outputs open	I_{BAT}	–	10.0	20.0	mA
Digital Supply Voltage Range, Full Performance	V_{CC}	3.0	–	5.5	V
Digital Supply Under-voltage (VCC Failure)	V_{CCUV}	2.2	2.5	2.8	V
Sleep Current Consumption on V_{CC} @ 25 °C and V_{BAT} = 12 V	$I_{CCSLEEP}$				µA
Output OFF		–	0.2	5.0	
Supply Current Consumption on V_{CC} and V_{BAT} = 12 V	I_{CC}				mA
No SPI		–	–	2.6	
3.0 MHz SPI communication		–	–	5.0	
LOGIC INPUT/OUTPUT (IGN, $\overline{CS}$, CSNS, SI, SCLK, CLOCK, SO, FLASHER, $\overline{RST}$, LIMP, FOG)					
Input High Logic Level[7]	V_{IH}	2.0	–	–	V
Input Low Logic Level[7]	V_{IL}	–	–	0.8	V
Voltage Threshold for Wake-up (IGN, FLASHER, FOG, $\overline{RST}$)	V_{IGNTH}	1.0	–	2.2	V
Input Clamp Voltage (IGN, FLASHER, LIMP, FOG, $\overline{CS}$, SCLK, SI, $\overline{RST}$)	V_{CL_POS}				V
I = 1.0 mA		7.5	–	13	
Input Forward Voltage (IGN, FLASHER, LIMP, FOG, $\overline{CS}$, SCLK, SI, $\overline{RST}$)	V_{CL_NEG}				V
I = -1.0 mA		-2.0	–	-0.3	
Input Passive Pull-up Resistance on $\overline{CS}$ Input[8]	R_{UP}	100	200	400	kΩ
Input Passive Pull-down Resistance on SI, SCLK, FLASHER, IGN, FOG, CLOCK, LIMP, $\overline{RST}$ pins[8]	R_{DWN}	100	200	400	kΩ

Notes

5. In extended mode, the functionality is guaranteed but not the electrical parameters.
6. Outputs shorted to ground, I_{OUT} = + 500 mA and I_{OUT} = OCHI (guaranteed by design).
7. Valid for $\overline{RST}$, SI, SCLK, $\overline{CS}$, CLOCK, IGN, FLASHER, FOG, and LIMP pins.
8. Valid for the following input voltage range: -0.3 V to VCC +0.3 V.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUT/OUTPUT (IGN, $\overline{CS}$, CSNS, SI, SCLK, CLOCK, SO, FLASHER, $\overline{RST}$, LIMP, FOG) (CONTINUED)					
SO High-state Output Voltage I_{OH} = 1.0 mA	V_{SOH}	0.8	0.95	–	V_{CC}
SO Low-state Output Voltage I_{OL} = -1.6 mA	V_{SOL}	–	0.2	0.4	V
CLOCK Output Voltage Reporting Wake-up Event (I_{CLOCK}=1.0mA)	V_{CLOCKH}	0.8	0.95	–	V_{CC}
SO and CSNS Tri-state Leakage Current	I_{SOLEAK}	-1.0	0.0	1.0	µA
Current Sense Output Clamp Voltage CSNS open and $I_{OUT[1:5]}$ = I_{FSR}	V_{CSNS}	5.0	6.0	7.0	V
OUTPUTS (OUT 1-5)					
Output Negative Clamp Voltage I_{OUT} = - 500 mA, Outputs OFF	V_{OUT}	-22.0	–	-16.0	V
Output Leakage Current in OFF State	$I_{LEAK(OFF)}$				µA
Sleep mode, outputs grounded, T_A = 25 °C		–	0.0	2.0	
Sleep mode, outputs grounded, T_A = 125 °C		–	0.0	3.0	
Normal mode, outputs grounded		–	20	25	
Current Sense Error[9] over the Full Voltage and Temperature Range	$\Delta I_{CS}/I_{CS}$				%
%Full Scale Range (FSR), LED Control bit = 0, Channels 1,5 (17 mΩ)					
point @ 0.75 FSR		-14	0.0	14	
point @ 0.50 FSR		-15	0.0	15	
point @ 0.25 FSR		-17	0.0	17	
point @ 0.1 FS		-25	0.0	25	
point @ 0.05FSR		-40	0.0	40	
% Full-Scale Range (FSR), LED Control bit =0, Channels 2,3,4 (6.0 mΩ)		-14	0.0	14	
point @ 0.75 FSR		-15	0.0	15	
point @ 0.50 FSR		-17	0.0	17	
point @ 0.25 FSR		-34	0.0	34	
point @ 0.1 FSR					
Current Sense error with one calibration point (50% FSR, V_{BAT} = 13.5 at 25 °C[10]		-6.0	–	6.0	%
Current Sense error with one calibration point (50% FSR_{LED}, V_{BAT} = 13.5 at 25 °C[10]		-6.0	–	6.0	%
Temperature Drift of Current Sense Output[11] V_{BAT} = 13.5 V, $I_{OUT1,5}$ = 2.8 A, I_{OUT2-4} = 5.5 A, reference taken at T_A=25 °C	$\Delta I_{CS}/\Delta T$	–	±280	±400	ppm/°C
Over-temperature Shutdown	T_{OTS}	155	175	195	°C

Notes

9. 10 V < V_{BAT} < 16 V. $\Delta I_{CS}/I_{CS}$ = (measured I_{CS} - targeted I_{CS})/ targeted I_{CS} with targeted I_{CS} = 5.0 mA. Test conditions of accuracy measurement of point I(HS[1]) @ 0.05*FSR: I(HS[5]) = 0, I(HS[2]) = I(HS[3]) = I(HS[4]) =8.0 A
10. Based on statistical analysis covering 99.74% of parts, except 10% of FSR. Refer to Current Sense section for more details.
11. Based on statistical data. Not production tested. $\Delta I_{CS}/\Delta T$=[(measured I_{CS} at T_1 - measured I_{CS} at T_2) / measured I_{CS} at room] / (T_1 -T_2)

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS (OUT 1-5) (CONTINUED)					
Thermal Prewarning[12]	$T_{OTSWARN}$	110	125	140	°C
Output Voltage Threshold	V_{OUT_TH}	0.475	0.5	0.525	VBAT
CHANNEL 1 - PARKING LIGHT (17 mΩ CHANNEL)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 17 26.7	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150 °C)[12]	$R_{DS(ON)150}$	–	–	28.9	mΩ
Reverse Output ON Resistance (I_{OUT} = -2.8 A, T_A = 25 °C)[13] V_{BAT} = -12 V	$R_{SD(ON)}$	–	–	34	mΩ
High Over-current Shutdown Threshold 1, V_{BAT} = 16 V	I_{OCHI1}	48	56.2	72	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	21.0	25.8	30.5	A
Low Over-current Shutdown Threshold	I_{OCLO}	9.0	11.5	14	A
Open Load-current Threshold in ON State[14]	I_{OL}	0.08	0.3	0.77	A
Open Load-current Threshold in ON State with LED[15] V_{OUT} = V_{BAT} - 0.8 V	I_{OLLED}	4.0	10.0	20.0	mA
Current Sense Full-scale Range[16]	$I_{CS\ FSR}$	–	9.5	–	A
Severe Short-circuit Impedance Range[17]	$R_{SC1(OUT1)}$	225	–	–	mΩ
CHANNEL 2 - LOW BEAM (6.0 mΩ CHANNEL)					
Output Drain-to-Source ON Resistance (I_{OUT} = 5.5 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 6.0 9.0	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 5.5 A, V_{BAT} = 13.5 V, T_A = 150 °C)[17]	$R_{DS(ON)150}$	–	–	10.2	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -5.5 A, T_A = 25 °C)[18] V_{BAT} = -12 V	$R_{SD(ON)}$	–	–	12.0	mΩ
High Over-current Shutdown Threshold 1, V_{BAT} = 16 V	I_{OCHI1}	96	123	150	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	40	50.5	61	A

Notes

12. Parameter guaranteed by design, however, it is not production tested.
13. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
14. OLLED1, bit D0 in SI data is set to [0].
15. OLLED1, bit D0 in SI data is set to [1].
16. For typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA.
17. Parameter guaranteed by design; however, it is not production tested.
18. Source-to-Drain ON resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CHANNEL 2 - LOW BEAM (6.0 mΩ CHANNEL) (CONTINUED)					
Low Over-current Shutdown Threshold Optional Xenon lamp Optional H7 bulb	I_{OCLO}	 28 17	 35 22.5	 42 28	A
Open Load Current Threshold in ON State[19]	I_{OL}	0.15	0.62	1.55	A
Open Load Current Threshold in ON State with LED[20] V_{OL} = V_{BAT} - 0.8 V	I_{OLLED}	 4.0	 10.0	 20.0	mA
Current Sense Full-scale Range[21] Optional Xenon bulb Optional H7 bulb	$I_{CS\ FSR}$	 – –	 30 19	 – –	A
Severe Short-circuit Impedance Range[22]	$R_{SC1(OUT2)}$	65	–	–	mΩ
CHANNEL 3- HIGH BEAM (6.0 mΩ CHANNEL)					
Output Drain-to-Source ON Resistance (I_{OUT} = 5.5 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 6.0 9.0	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 5.5 A, V_{BAT} = 13.5 V, T_A = 150 °C)[22]	$R_{DS(ON)150}$	 –	 –	 10.2	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -5.5 A, T_A = 25 °C)[23] V_{BAT} = -12 V	$R_{SD(ON)25}$	 –	 –	 12	mΩ
High Over-current Shutdown Threshold 1, V_{BAT} = 16 V	I_{OCHI1}	96	123	150	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	40	50.5	61	A
Low Over-current Shutdown Threshold H7 Bulb	I_{OCLO}	 17	 22.5	 28	A
Open Load Current Threshold in ON State[24]	I_{OL}	0.15	0.62	1.55	A
Open Load Current Threshold in ON State with LED[25] V_{OL} = V_{BAT} - 0.8 V	I_{OLLED}	 4.0	 10.0	 20.0	mA
Current Sense Full-scale Range [21]	$I_{CS\ FSR}$	–	19	–	A
Severe Short-circuit Impedance Range[22]	$R_{SC1(OUT3)}$	65	–	–	mΩ

Notes

19. OLLED2, bit D1 in SI data is set to [0].
20. OLLED2, bit D1 in SI data is set to [1].
21. For typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0mA.
22. Parameter guaranteed by design; however, it is not production tested.
23. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
24. OLLED3, bit D2 in SI data is set to [0].
25. OLLED3, bit D2 in SI data is set to [1].

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CHANNEL 4 - FOG LIGHT(6.0 mΩ CHANNEL)					
Output Drain-to-Source ON Resistance (I_{OUT} = 5.5 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 6.0 9.0	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 5.5 A, V_{BAT} = 13.5 V, T_A = 150 °C)(26)	$R_{DS(ON)150}$	–	–	10.2	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -5.5 A, T_A = 25 °C)(27) V_{BAT} = -12 V	$R_{SD(ON)25}$	–	–	12	mΩ
High Over-current Shutdown Threshold 1, V_{BAT} = 16 V	I_{OCHI1}	96	123	150	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	40	50.5	61	A
Low Over-current Shutdown Threshold H7 Bulb	I_{OCLO}	 17	 22.5	 28	A
Open Load Current Threshold in ON State(28)	I_{OL}	0.15	0.62	1.5	A
Open Load Current Threshold in ON State with LED(29) V_{OL} = V_{BAT} - 0.8 V	I_{OLLED}	 4.0	 10.0	 20.0	mA
Current Sense Full Scale Range(30)	$I_{CS\ FSR}$	–	19	–	A
Severe Short-circuit Impedance Range(26)	$R_{SC1(OUT4)}$	65	–	–	mΩ
CHANNEL 5 - FLASHER (17 mΩ CHANNEL)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 17 26.7	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150 °C)(31)	$R_{DS(ON)150}$	–	–	18.9	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -2.8A, T_J = 25°C)(32) V_{BAT} = -12V	$R_{SD(ON)25}$	–	–	34	mΩ
High Over-current Shutdown Threshold 1,	I_{OCHI1}	48	56.2	72	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	21.0	25.8	30.5	A
Low Over-current Shutdown Threshold	I_{OCLO}	9.0	11.5	14	A

Notes

26. Parameter guaranteed by design; however, it is not production tested.
27. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
28. OLLED4, bit D3 in SI data is set to [0].
29. OLLED4, bit D3 in SI data is set to [1].
30. For typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA.
31. Parameter guaranteed by design; however, it is not production tested.
32. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CHANNEL 5 - FLASHER (17 mΩ CHANNEL) (CONTINUED)					
Open Load Current Threshold in ON State[33]	I_{OL}	0.08	0.3	0.77	A
Open Load Current Threshold in ON State with LED[34] V_{OL} = V_{BAT} - 0.8 V	I_{OLLED}	4.0	10.0	20.0	mA
Current Sense Full Scale Range[35]	$I_{CS\ FSR}$	–	8.8	–	A
Severe Short-circuit Impedance Range[36]	$R_{SC1(OUT5)}$	225	–	–	mΩ
SPARE FETOUT(OUT6) / FETIN (OUT1)					
FETOUT Output High Level @ I = 1.0 mA	$V_{H\ MAX}$	0.8	–	–	V_{CC}
FETOUT Output Low Level @ I = -1.0 mA	$V_{H\ MIN}$	–	0.2	0.4	V
FETIN Input Full Scale Range Current	I_{FETIN}	–	5.0	–	mA
FETIN Input Clamp Voltage $I_{FET\ IN}$ = 5.0 mA, CSNS open	V_{CLIN}	5.3	–	13	V
Drop Voltage on FETIN (FETIN - CSNS) I_{FETIN} = 5.0 mA, 5.5 V > CSNS > 3.0 V	V_{DRIN}	0.0	–	0.4	V
FETIN Leakage Current When External Current Switch Sense Is Enabled 5.5 V > V_{FETIN} > 0.0 V, CSNS open	$I_{FETINLEAK}$	-1.0	–	6.0	μA
TEMPERATURE OF GND FLAG					
Analog Temperature Feedback Range	T_{FEED_RANGE}	-40	–	150	°C
Analog Temperature Feedback at T_A = 25 °C with 5.0 kΩ > R_{CSNS} > 500 Ω	V_{T_FEED}	925	1000	1075	mV
Analog Temperature Feedback Derating with 5.0 kΩ > R_{CSNS} > 500 Ω [36]	V_{DT_FEED}	10.9	11.3	11.7	mV/°C
Analog Temperature Feedback Precision [36]	V_{DT_ACC}	-15	–	15	°C
Analog Temperature Feedback Precision with calibration point at 25 °C [36]	$V_{DT\_ACC\_CAL}$	-5.0	–	5.0	°C

Notes
33. OLLED5, bit D4 in SI data is set to [0].
34. OLLED5, bit D4 in SI data is set to [1].
35. For typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA.
36. Parameter guaranteed by design; however, it is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUTS TIMING (OUT1 TO OUT5)					
Current Sense Valid Time (valid for resistive loads only),(37)	$t_{CSNS(VAL)}$				µs
SR bit = 0		0	100	200	
SR bit = 1		0	50	100	
Current Sense Settling Time on Resistive Load Only(37)	$t_{CSNS(SET)}$	–	10	30	µs
Current Sense Synchronization signal - typical validation time	$t_{SYNC(val)}$				
SR bit = 0		0	90	180	
SR bit = 1		0	45	90	
Driver Output Positive Slew Rate (30% to 70% @ V_{BAT} = 14 V)	SR_R				V/µs
SR bit = 0					
I_{OUT} = 2.8 A for OUT1 and OUT5		0.14	0.4	0.8	
I_{OUT} = 5.5 A for OUT2, OUT3, and OUT4		0.2	0.4	0.8	
SR bit = 1					
I_{OUT} =0.7 A for OUT1 and OUT5		0.28	0.8	1.6	
I_{OUT} = 1.4 A for OUT2, OUT3, and OUT4		0.4	0.8	1.6	
Driver Output Negative Slew Rate (70% to 30% @ V_{BAT} = 14 V)	SR_F				V/µs
SR bit = 0					
I_{OUT} = 2.8 A for OUT1 and OUT5		0.14	0.4	0.8	
I_{OUT} = 5.5 A for OUT2, OUT3, and OUT4		0.2	0.4	0.8	
SR bit = 1					
I_{OUT} = 0.7 A for OUT1 and OUT5		0.28	0.8	1.6	
I_{OUT} = 1.4 A for OUT2, OUT3, and OUT4		0.4	0.8	1.6	
Driver Output Matching Slew Rate (SR_R /SR_F) (70% to 30% @ V_{BAT} = 14 V @25 °C)	ΔSR				
SR bit = 0: I_{OUT} = 2.8 A for OUT1 and OUT5 and I_{OUT} = 5.5 A for OUT2/3/4		0.8	1.0	1.2	
SR bit = 1: I_{OUT} = 0.7 A for OUT1 and OUT5 and I_{OUT} = 1.4 A for OUT2/3/4		0.8	1.0	1.2	
Driver Output Turn-ON Delay (SPI ON Command [No PWM, $\overline{CS}$ Positive Edge] to Output = 50% V_{BAT} @ V_{BAT} = 14 V) (see Figure 6)	t_{DLYON}				µs
SR bit = 0: I_{OUT} = 2.8 A for OUT1 and OUT5 and I_{OUT} = 5.5 A for OUT2/3/4		65	–	300	
SR bit = 1: I_{OUT} = 0.7 A for OUT1 and OUT5 and I_{OUT} = 1.4 A for OUT2/3/4		35	–	120	
Driver Output Turn-OFF Delay (SPI OFF command [$\overline{CS}$ Positive Edge] to Output = 50% V_{BAT} @ V_{BAT} = 14 V) (see Figure 6)	t_{DLYOFF}				µs
SR bit = 0: I_{OUT} = 2.8 A for OUT1 and OUT5 and I_{OUT} = 5.5 A for OUT2/3/4		40	–	110	
SR bit = 1: I_{OUT} = 0.7 A for OUT1 and OUT5 and I_{OUT} = 1.4 A for OUT2/3/4		15	–	80	

Notes

37. Not production tested. See Figure 7, Current Sensing Time Delays.

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUTS TIMING (OUT1 TO OUT5) (CONTINUED)					
Driver Output Matching Time ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) @ Output = 50% V_{BAT} with V_{BAT} = 14 V, f_{PWM} = 240 Hz, δ_{PWM} = 50%, @25 °C SR bit = 0: I_{OUT} = 2.8 A for OUT1 and OUT5 and I_{OUT} = 5.5 A for OUT2/3/4 SR bit = 1: I_{OUT} = 0.7 A for OUT1 and OUT5 and I_{OUT} = 1.4 A for OUT2/3/4	Δt_{RF}	 10 5.0	 – –	 200 70	µs
PWM MODULE					
PWM Frequency Range	f_{PWM}	60.0	–	400	Hz
Clock Input Frequency Range	f_{CLK}	7.68	–	51.2	kHz
Output PWM Duty Cycle maximum range for 11 V<V_{BAT}<18 V[38], [39]	PWM_MAX	4.0	–	96	%
Output PWM Duty Cycle linear range for 11 V<V_{BAT}<18 V[40]	PWM_LIN	5.5	–	96	%
WATCHDOG TIMING					
Watchdog Timeout (SPI Failure)	t_{WDTO}	50	75	100	ms
I/O PLAUSIBILITY CHECK TIMING					
Fault Shutdown Delay Time (from Over-temperature or OCHI1 or OCHI2 or OCLO or UV Fault Detection to Output = 50%V_{BAT} without round shaping feature for turn off)	t_{SD}	–	7.0	30	µs
High Over-current Threshold Time 1 for OUT1 and OUT5 for OUT2, OUT3, and OUT4	t_1	 7.0 14	 10 20	 13.5 26	ms
High Over-current Threshold Time 2 for OUT1 and OUT5 for OUT2, OUT3, and OUT4	t_2	 52.5 105	 75 150	 97.5 195	ms
Autorestart Period for OUT1 and OUT5 for OUT2, OUT3, and OUT4	$t_{AUTORST}$	 52.5 105	 75 150	 97.5 195	ms
Autorestart Over-current Shutdown Delay Time for OUT1 and OUT5 for OUT2, OUT3, and OUT4	t_{OCHI_AUTO}	 3.5 7.0	 5.0 10.0	 6.5 13.0	ms
Limp Home Input pin Deglicher Time	t_{LIMP}	7.0	10.0	13.0	ms
Cyclic Open Load Detection Timing with LED[41]	t_{OLLED}	105	150	195	ms
Flasher Toggle Timeout	$t_{FLASHER}$	1.4	2.3	3.0	s
Fog Toggle Timeout	t_{FOG}	1.4	2.3	3.0	s

Notes

38. Not production tested. See Figure 7, Current Sensing Time Delays.
39. The PWM ratio is measured at V_{OUT} = 50% of V_{BAT} in nominal range of PWM frequency (from 60 Hz to 400 Hz). It is possible to put the device fully on (PWM duty cycle = 100%) and fully off (PWM duty cycle = 0%). Between 4%-96%, $OCHI_{1,2}$, OCLO and open load are available in ON state. See Figure 6, Output Slew Rate and Time Delays.
40. Linear range is defined by output duty cycle to SPI duty cycle configuration +/-1 LSB. For values outside linear duty cycle range, a calibration curve is available.
41. IOLLEDn bit (where “n” corresponds to respective outputs 1 through 5) in SI data is set to logic [1]. Refer to Table 8, Serial Input Address and Configuration Bit Map, page 25.

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
I/O PLAUSIBILITY CHECK TIMING (CONTINUED)					
Ignition Toggle Timeout	$t_{IGNITION}$	1.4	2.3	3.0	s
Clock Input Low Frequency Detection Range	$f_{LCLK\ DET}$	1.0	2.0	4.0	kHz
Clock Input High Frequency Detection Range	$f_{HCLK\ DET}$	100	200	400	kHz
SPI INTERFACE CHARACTERISTICS					
Maximum Frequency of SPI Operation	f_{SPI}	–	–	3.0	MHz
Rising Edge of CSB to Falling Edge of CSB (Required Setup Time)(42)	t_{CSB}	–	–	1.0	us
Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time)(42)	t_{LEAD}	–	–	500	ns
Required High State Duration of SCLK (Required Setup Time)(42)	t_{WSCLKH}	–	–	167	ns
Required Low State Duration of SCLK (Required Setup Time)(42)	t_{WSCLKL}	–	–	167	ns
Falling Edge of SCLK to Rising Edge of CSB (Required Setup Time)(42)	t_{LAG}	–	50	167	ns
SI to Falling Edge of SCLK (Required Setup Time)(43)	$t_{SI(SU}$	–	25	83	ns
Falling Edge of SCLK to SI (Required Setup Time)(43)	t_{SIHOLD}	–	25	83	ns
SO Rise Time C_L = 80 pF	t_{RSO}	–	25	50	ns
SO Fall Time C_L = 80 pF	t_{FSO}	–	25	50	ns
SI, CSB, SCLK Incoming Signal Rise Time(43)	t_{RSI}	–	–	50	ns
SI, CSB, SCLK Incoming Signal Fall Time(43)	t_{FSI}	–	–	50	ns
Time from Falling Edge of SCLK to SO Low-impedance(44)	$t_{SO(EN)}$	–	–	145	ns
Time from Rising Edge of SCLK to SO High-impedance(45)	$t_{SO(DIS)}$	–	65	145	ns

Notes

42. Maximum setup time required for the 06XS3517 is the minimum guaranteed time needed from the microcontroller.
43. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
44. Time required for output status data to be available for use at SO. 1.0 kΩ on pull-up on CSB.
45. Time required for output status data to be terminated at SO. 1.0 kΩ on pull-up on CSB.

TIMING DIAGRAMS

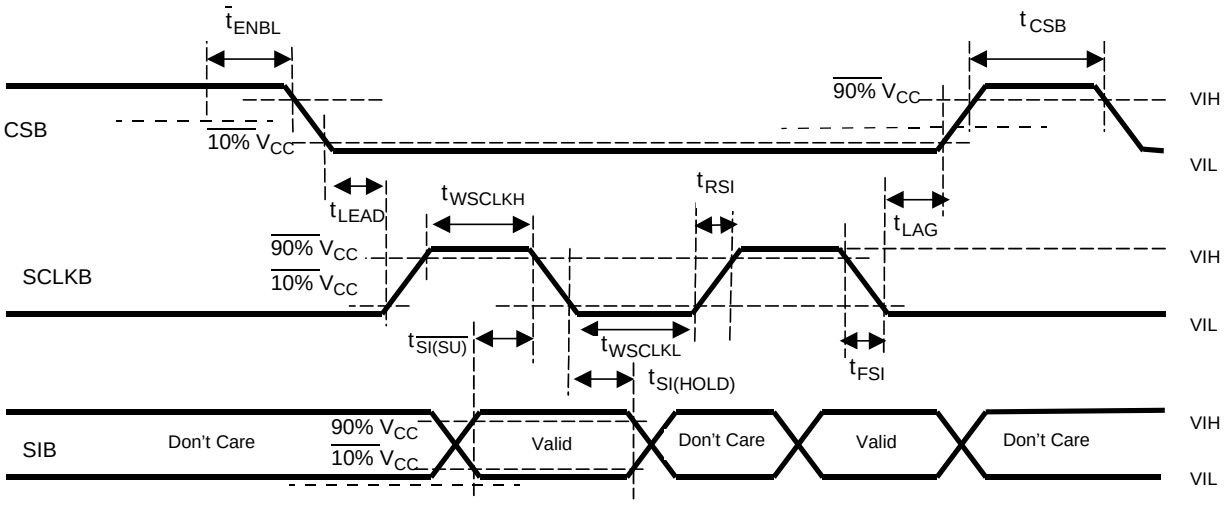


Figure 4. Input Timing Switching Characteristics

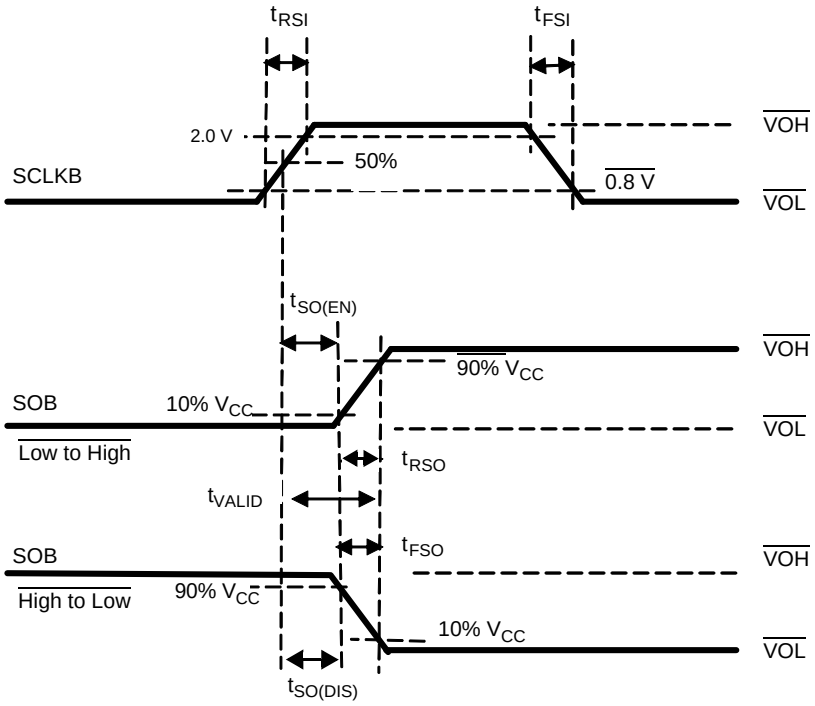


Figure 5. SCLK Waveform and Valid SO Data Delay Time

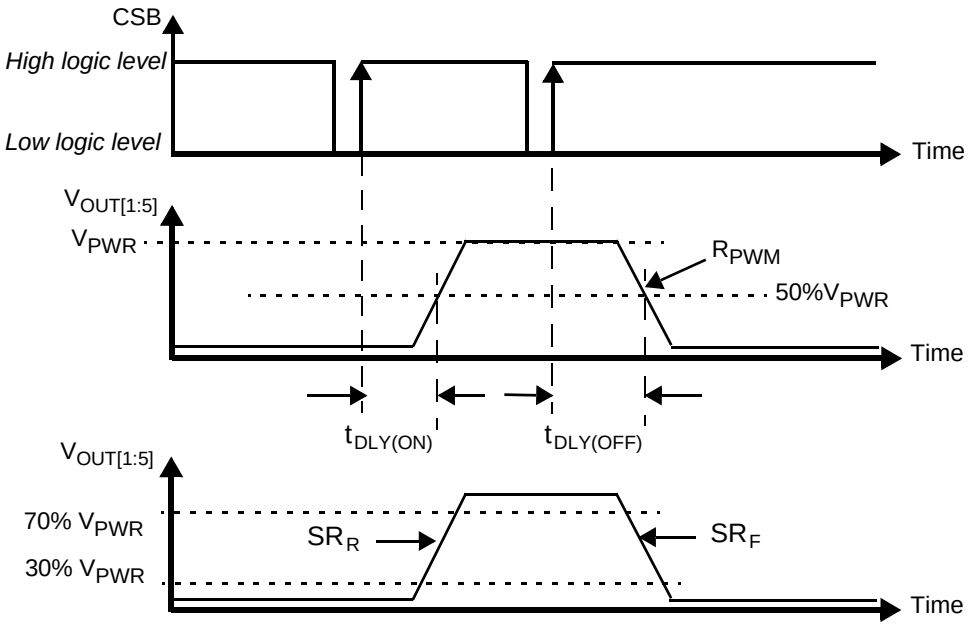


Figure 6. Output Slew Rate and Time Delays

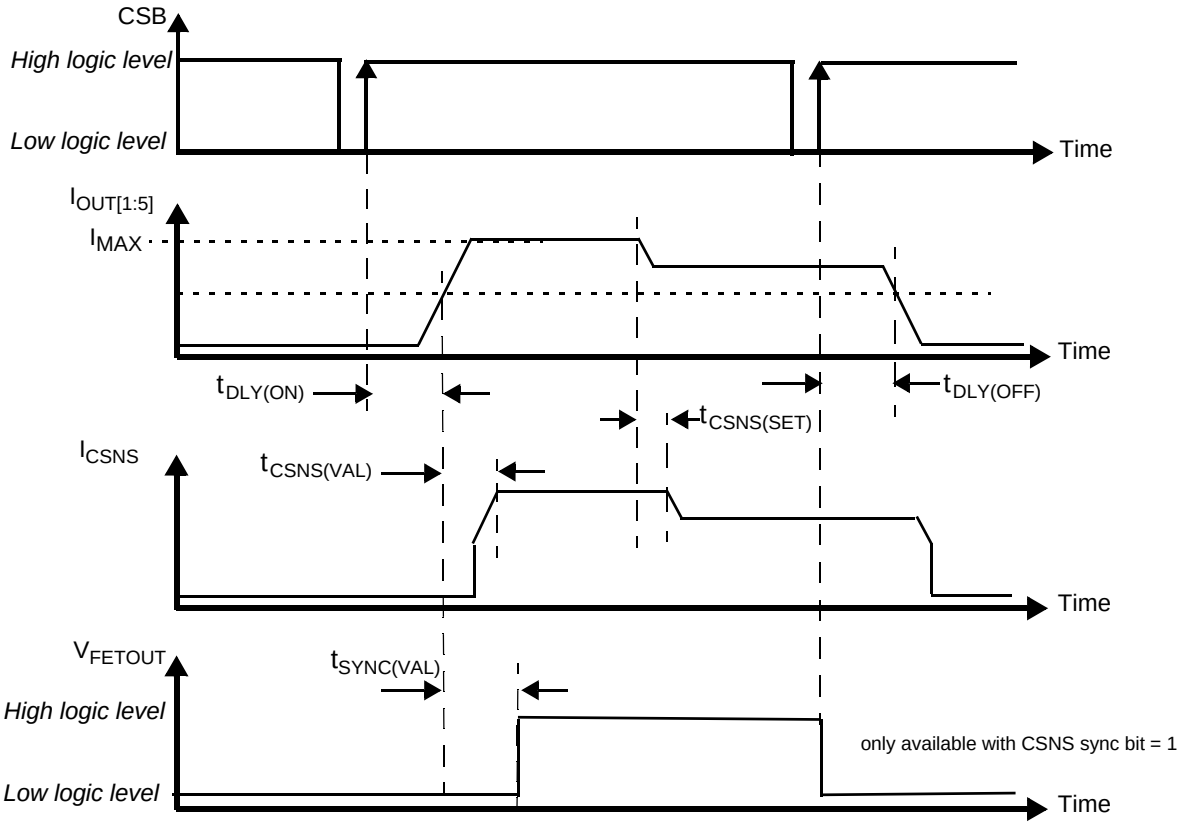


Figure 7. Current Sensing Time Delays

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 06XS3517 is designed for low-voltage automotive and industrial lighting applications. Its five low $R_{DS(ON)}$ MOSFETs (three 6.0 mΩ and two 16 mΩ) can control the high sides of five separate resistive loads (bulbs). Programming, control, and diagnostics are accomplished using a 16-bit SPI interface.

FUNCTIONAL PIN DESCRIPTION

SUPPLY VOLTAGE (VBAT)

The VBAT pin of the 06XS3517 is the power supply of the device. In addition to its supply function, this tab contributes to the thermal behavior of the device by conducting the heat from the switching MOSFETs to the printed circuit board.

SUPPLY VOLTAGE (VCC)

This is an external voltage input pin used to supply the digital portion of the circuit and the gate driver of the external SMART MOSFET.

GROUND (GND)

This pin is the ground of the device.

CLOCK INPUT / WAKE-UP OUTPUT (CLOCK)

When the part is in Normal mode ($\overline{RST}$=1), the PWM frequency and timing are generated from the rising edge of clock input by the PWM module. The clock input frequency is the selectable factor 2^7 = 128 or 2^8 = 256 of the PWM frequency per output, depending PR bit value.

The OUT1:6 can be controlled in the range of 4% to 96% with a resolution of 7 bits of the duty cycle (bits D[6:0]).

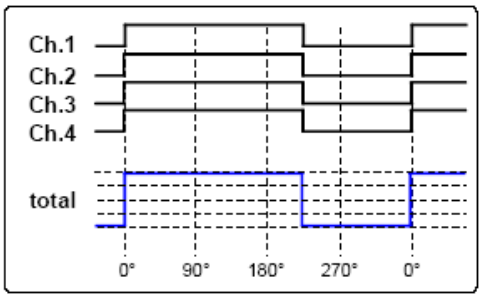
Figure 5 describes the PWM resolution.

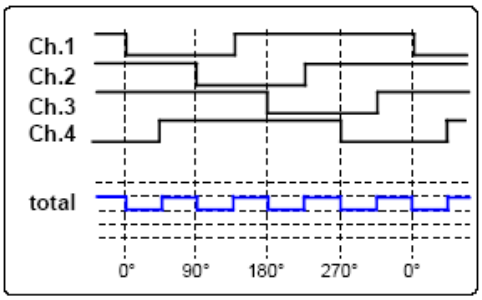
Table 5. PWM Resolution

On/Off (Bit D7)	Duty cycle (7 bits resolution)	Output state
0	**X**	**OFF**
1	0000000	PWM (1/128 duty cycle)
1	0000001	PWM (2/128 duty cycle)
1	0000010	PWM (3/128 duty cycle)
1	1111111	fully ON

The timing includes four programmable PWM switching phases (0°, 90°, 180°, and 270°) to improve overall EMC behavior of the light module.

As an example: When the load currents have equal amplitude, the amplitude of the input current is divided by four, while the ripple frequency is 4 times the original. The two following pictures illustrate this behavior.





The synchronization of the switching phases between different IC is provided by an SPI command in combination with the CSB input. The bit in the SPI is called PWM sync (initialization register).

In Normal mode, no PWM feature (100% duty cycle) is provided in the following instances:

- With the following SPI configuration: D7:D0=FF.
- In case of clock input signal failure (out of $_{fPWM}$), the outputs state depends of D7 bit value (D7=1=ON) in Normal mode.

In Fail mode, the ouputs state depend on IGN, FLASHER, and FOG pins.

If RSTB=0, this pin reports the wake-up event for wake=1 when VBAT and VCC are in operational voltage range.

IGNITION INPUT (IGN)

The ignition input wakes the device. It also controls the Fail mode activation. The signal is “high active”, meaning the component is active in case of a logic high at the input.

LIMP HOME INPUT (LIMP)

The Fail mode of the component can be activated by this digital input port. The signal is “high active”, meaning the Fail mode can be activated by a logic high signal at the input.

FLASHER INPUT (FLASHER)

The flasher input wakes the device. It also controls the Fail Mode activation. The signal is “high active”, meaning the component is active in case of a logic high at the input.

FOG INPUT (FOG)

The fog input wakes the device. It also controls the Fail Mode activation. The signal is “high active”, meaning the component is active in case of a logic high at the input.

RESET INPUT (RSTB)

This input wakes the device when the RSTB pin is at logic [1]. It is also used to initialize the device configuration and the SPI faults registers when the signal is low. All SI/SO registers described Table 8 and Table are reset. The fault management is not affected by RSTB (see Figure 2).

CURRENT SENSE OUTPUT (CSNS)

The current sense output pin is an analog current output or a voltage proportional to the temperature on the GND flag. The routing to the external resistor is SPI programmable.

This current sense monitoring may be synchronized in case of the OUT6 is not used. The CSNS output is valid after a rising edge on the FETOUT pin (after $t_{sync(val)}$ s.) if the CSNS sync SPI bit was set to logic [0] and remains valid till a falling edge is generated. Connection of the FETOUT pin to a MCU input pin allows the MCU to sample the CSNS pin during a valid time slot. Since this falling edge is generated at the end of this time slot, upon a switch-off command, this feature may be used to implement maximum current control.

CHARGE PUMP (CP)

An external capacitor must be connected between the CP and the VBAT pin. It is used as a tank for the internal charge pump. Its value is 100 nF ±20%, 25 V maximum.

FETOUT OUTPUT (FETOUT)

This output pin can be used to control an external SMART MOSFET (OUT6) at a logic level (1=ON, 0=OFF).

The high level of the FETOUT Output is V_{CC}, if V_{BAT} and V_{CC} are available, in case FETOUT is a controlled ON.

FETOUT is not protected if there is a short-circuit or under-voltage on VBAT.

In case of a reverse battery, OUT6 is OFF.

FETIN INPUT (FETIN)

This input pin receives the current recopy from an external SMART MOSFET. It can be routed on CSNS output by a SPI command.

SPI PROTOCOL DESCRIPTION

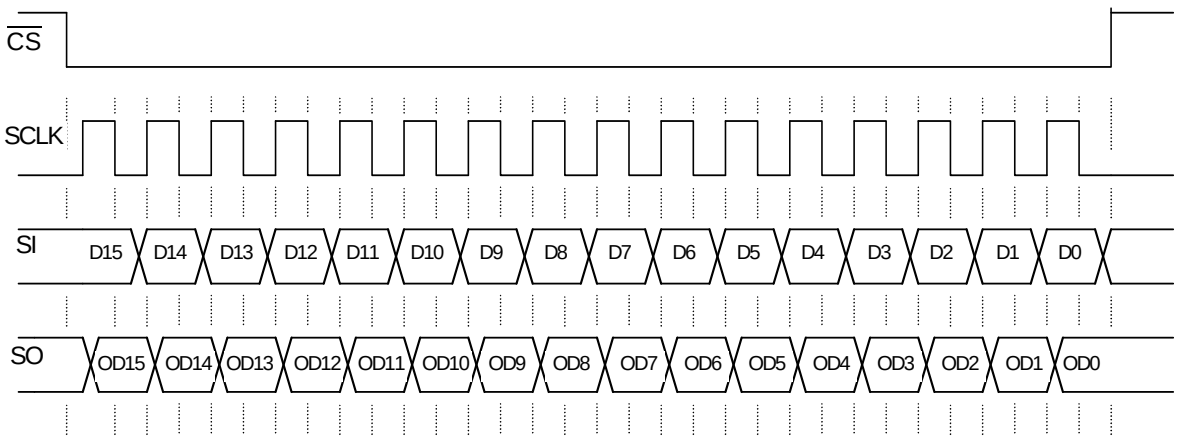
The SPI interface has a full-duplex, three-wire, synchronous data transfer with four I/O lines associated with it: Serial Clock (SCLK), Serial Input (SI), Serial Output (SO), and Chip Select (CSB).

The SI/SO pins of the 06XS3517 device follow a first-in, first-out (D15 to D0) protocol, with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 3.3 V and 5.0 V CMOS logic levels, supplied by V_{CC}.

The SPI lines perform the following functions:

SERIAL CLOCK (SCLK)

The SCLK pin clocks the internal shift registers of the 06XS3517 device. The SI pin accepts data into the input shift register on the falling edge of the SCLK signal, while the SO pin shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important that the SCLK pin be in a logic low state whenever CSB makes any transition. For this reason, it is recommended the SCLK pin be in a logic [0] whenever the device is not accessed (CSB logic [1] state). SCLK has a passive pull-down, R_{DWN}. When CSB is logic [1], signals at the SCLK and SI pins are ignored, and SO is tri-stated (high-impedance) (see Figure 8).



Notes
1. D15 : D0 relate to the most recent ordered entry of data into the device.
2. OD15 : OD0 relate to the first 16 bits of ordered fault and status data out of the device.

Figure 8. Single 16-Bit Word SPI Communication

SERIAL INPUT (SI)

The SI pin is a serial interface command data input pin. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, starting with D15 to D0. SI has a passive pull-down, R_{DOWN}.

SERIAL OUTPUT (SO)

The SO data pin is a tri-stateable output from the shift register. The SO pin remains in a high-impedance state until the CSB pin is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, and the state of the key inputs. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK.

CHIP SELECT ($\overline{CS}$)

The CSB pin enables communication with the master device. When this pin is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the master device. The 06XS3517 device latches in data from the Input Shift registers to the addressed registers on the rising edge of CSB. The device transfers status information from the power output to the Shift register on the falling edge of CSB. The SO output driver is enabled when CSB is logic [0]. CSB should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. CSB has a passive pull-up, R_{UP}.

FUNCTIONAL DEVICE OPERATION

OPERATION MODES

SLEEP MODE

The Sleep mode is the default mode of the 06XS3517. This is the state of the device after first applying battery voltage (V_{BAT}) and prior to any I/O transitions. This is also the state of the device when IGN, FOG, FLASHER, and RSTB are logic [0] (wake=0). In the Sleep mode, the outputs and all internal circuitry are OFF to minimize current draw. In addition, all SPI-configurable features of the device are reset. The 06XS3517 will transit to two modes (Normal and Fail) depending on wake and fail signals (see Fig13).

The transition to the other modes is according following signals:

- Wake = IGN or IGN_ON or FLASHER or FLASHER_ON or RSTB or FOG or FOG_ON
- Fail = VCC fail or SPI fail or External limp

NORMAL MODE

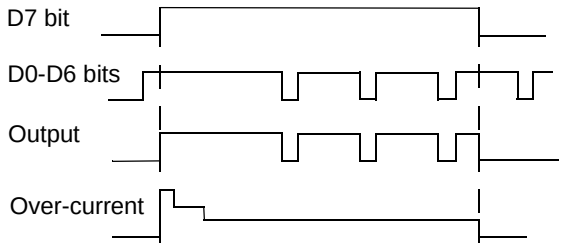
The 06XS3517 is in Normal mode when:

- Wake = 1
- Fail = 0

In Normal operating mode the power outputs are under full control of the SPI as follows:

- The outputs 1 to 6, including multiphase timing and selectable slew-rate, are controlled by the programmable PWM module.
- The outputs 1 to 5 are switched OFF in case of an under-voltage on VBAT.
- The outputs 1 to 5 are protected by the selectable over-current double window and over-temperature shutdown circuit.
- The digital diagnosis feature transfers status of the smart outputs via SPI.
- The analog current sense output (current recopy feature) can be routed by SPI.
- The outputs 1 and 5 can be configured to control LED loads.
- The SPI reports NM=1 in this mode.

The figure below describes the PWM, outputs and over-current behavior in Normal mode.



FAIL MODE

The 06XS3517 is in Fail mode when:

- Wake = 1
- Fail = 1.

In Fail mode:

- The outputs are under control of external pins (see Table 6)
- The outputs are fully protected in case of an overload, over-temperature and under-voltage (on VBAT or on VCC).
- The SPI reports continuously the content of address 11 (Initialization register), regardless previously requested output data word.
- Analog current sense is not available.
- Output 2 is configured in Xenon mode.
- In case of an overload (OCHI2 or OCLO) conditions or under-voltage on VBAT, the outputs are under control of autorestart feature.
- In case of serious overload condition (OCHI1 or OT) the corresponding output is latched OFF until a new wake-up event (wake=0 then 1).

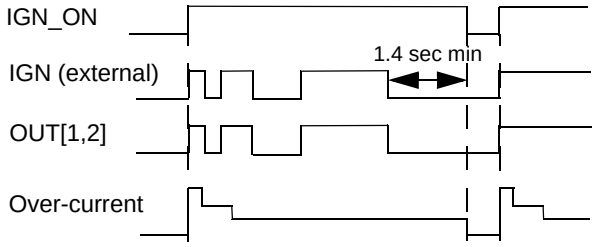


Table 6. Output States During Limp Home

Output 1 Parking Light	Output 2 Low Beam	Output 3 High Beam	Output 4 Fog Light	Output 5 Flasher	External Switch Spare
IGN Pin	IGN Pin	OFF	FOG Pin	FLASHER Pin	OFF

AUTORESTART STRATEGY

The autorestart circuitry is used to supervise the outputs and reactivate high side switches in cases of overload or under-voltage failure conditions, to provide a high availability of the outputs.

Autorestart feature is available in Fail mode (after loss of SPI communication). Autorestart is activated in case of overload condition (OCHI2 or OCLO) or under-voltage condition on VBAT (see Figure 12).

The autorestart periodically switches ON the outputs. During ON state of the switch OCHI1 window is enabled for tochi_Auto, then after the output is protected by OCLO.

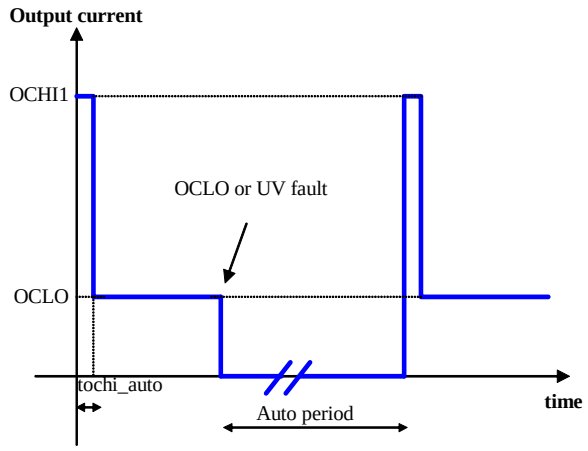


Figure 9. Over-current window in case of Autorestart

In case of OCHI1 or OT, the channel is latched OFF until wake-up (wake=0 then 1).

In case of OCLO or under-voltage, the output is switched OFF and turned On again automatically after the autorestart period (150 ms for 6.0 mOhm channels or 75 ms for 17 mOhm channels).

In case of an under-voltage in Fail mode, the outputs 1 to 5 will be latched off. The corresponding output is switched on only after the autorestart period ($t_{AUTORST-T1}$ or $t_{AUTORST-T2}$).

The Autorestart is not limited in time.

TRANSITION FAIL TO NORMAL MODE

To leave Fail mode, the fail condition must be removed (fail=0). The microcontroller has to toggle the SPI D10 bit (0 to 1) to reset the watchdog bit (WD); the other bits are not considered. The previous latched faults are reset by the transition into Normal mode.

TRANSITION NORMAL TO FAIL MODE

To leave the Normal mode, a fail condition must occur (fail=1). The previous latched faults are reset by the transition into Fail mode.

If the SI is shorted to VDD, the device transmits to Fail Safe mode until the WD bit toggles through the SPI (from [0] to [1]).

All settings are according to predefined values (all bits set to logic [0]).

START-UP SEQUENCE

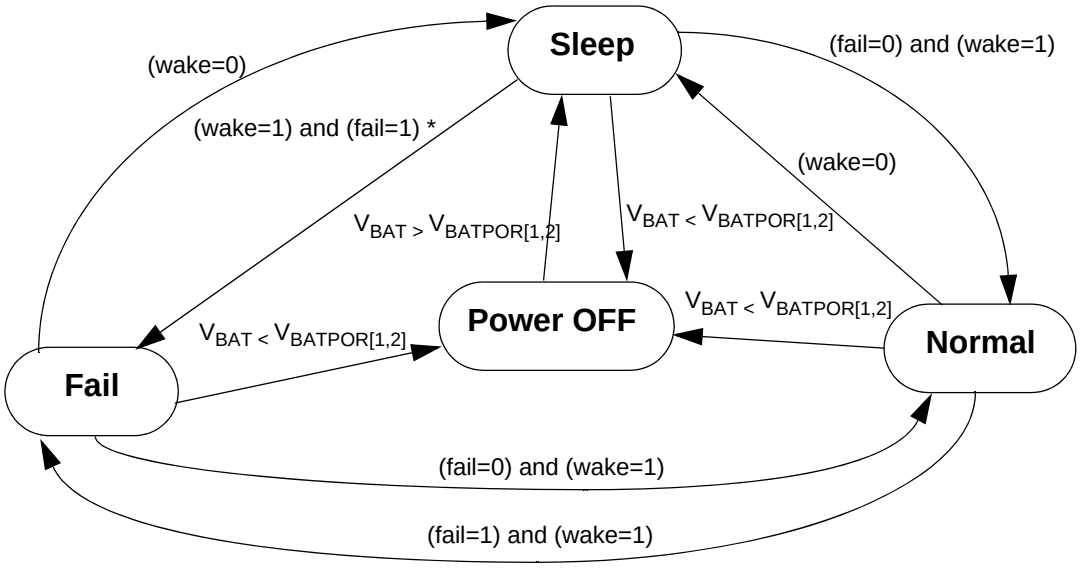
The 06XS3517 enters in Normal mode after start-up if following sequence is provided:

- VBAT and VCC power supplies must be above their under-voltage thresholds (Sleep mode).
- generate wake up event (wake=1) from 0 to 1 on RSTB**.** The device switches to Normal mode.
- apply PWM clock after maximum 200 µs (min 50 µs).
- send SPI command to the Device status register to clear the clock fail flag to enable the PWM module to start.

Figure 10 describes the wake-up block diagram.

POWER OFF MODE

The 06XS3517 is in Power OFF mode when the battery voltage is below $V_{BATPOR[1,2]}$ thresholds. For more details, refer to Loss of VBAT.



Notes:

* only available in case of a Vcc fail condition

wake = (RSTB = 1) OR (IGN_ON = 1) OR (Flasher_ON = 1) OR (FOG_ON = 1)

fail = (VCC_fail = 1) OR (SPI_fail = 1) OR (ext_limp = 1)

Figure 10. Operating Modes State Machine

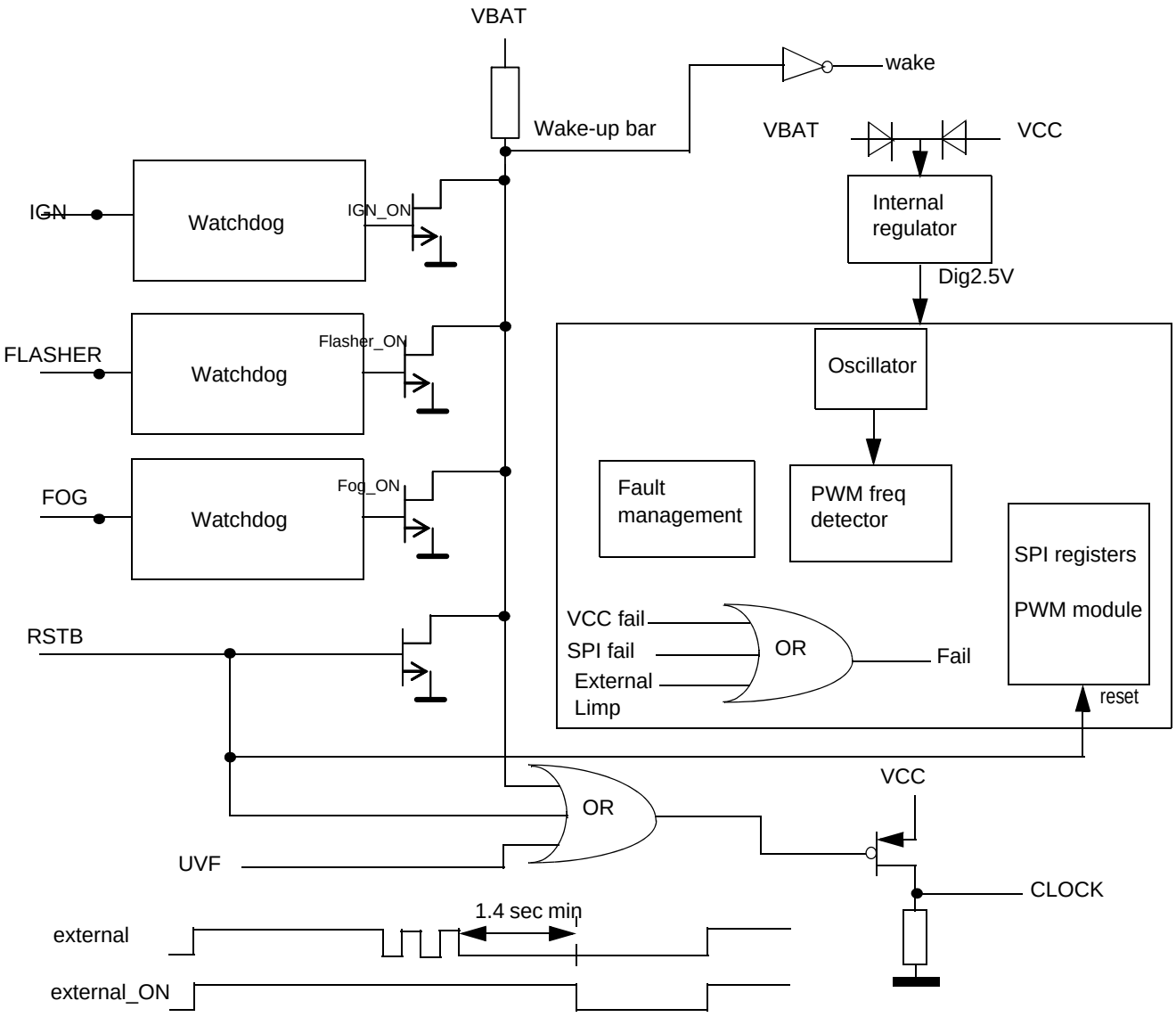


Figure 11. Wake-up Block Diagram

LOGIC COMMANDS AND REGISTERS

SERIAL INPUT COMMUNICATION

SPI communication compliant to 3.3 V and 5.0 V is accomplished using 16-bit messages. A message is transmitted by the master starting with the MSB, D15, and ending with the LSB, D0. Each incoming command message on the SI pin can be interpreted using the bit assignment described in Table 7. The 5 bits D15:D11, called register address bits, are used to select the command register. Bit D10 is the watchdog bit. The remaining 10 bits, D9:D0, are used to configure and control the output and its protection features. Multiple messages can be transmitted in succession to accommodate those applications where daisy chaining is desirable or to confirm transmitted data as long as the messages are all multiples of 16 bits. Any attempt made to latch in a message that is not 16 bits will be ignored.

All SPI registers are reset (all bit equal 0) in case of RSTB equal 0 or fail mode (Fail=1).

Table 7. SI Message Bit Assignment

Bit Sig	SI Msg Bit	Message Bit Description
MSB	D15:D11	Register address bits.
	D10	Watchdog in: toggled to satisfy watchdog requirements.
LSB	D9:D0	Used to configure inputs, outputs, device protection features, and SO status content.

DEVICE REGISTER ADDRESSING

The register addresses (D15:D11) and the impact of the serial input registers on device operation are described in this section. Table 8 summarizes the SI registers.

Table 8. Serial Input Address and Configuration Bit Map

SI Register	SI Address					SI Data										
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Initialization	0	0	0	0	0	WD	0	0	FOGen	PWM sync	Xenon	MUX2	MUX1	MUX0	SOA1	SOA0
Config OL	0	0	0	0	1	WD	05	0	0	0	0	OLLED5	OLLED4	OLLED3	OLLED2	OLLED1
Config Prescaler	0	0	0	1	0	WD	0	PR1	PR2	PR3	0	0	0	PR4	PR5	PR6
Config SR	0	0	0	1	0	WD	1	SR1	SR2	SR3	0	0	0	SR4	SR5	0
Config CSNS	0	0	0	1	1	WD	CSNS sync	0	0	0	0	NO_OC HI5	NO_OC HI4	NO_OC HI3	NO_OC HI2	NO_OC HI1
Control OUT1	0	1	0	0	1	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control OUT2	0	1	0	1	0	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control OUT3	0	1	0	1	1	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control OUT4	0	1	1	0	0	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control OUT5	0	1	1	0	1	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control External Switch	0	1	1	1	0	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
RESET	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0

Note: testmode address used only by FSL is D[15:11]=01111 with RSTB pin voltage higher than 8.0 V typ.
X = Don't care and 0 = need to rewrite logic "0"

ADDRESS 00000—INITIALIZATION

The Initialization register is used to read the various statuses, choose one of the six outputs current recopy, load the H7 bulbs profile for OUT2 only, enable the FOG pin and synchronize the switching phases between different devices. The register bits D1 and D0 determine the content of the 16 bits of the next SO data. (Refer Serial Output Communication (Device Status Return Data)) Table describes the register of initialization.

The watchdog timeout is specified by $_{tWDTO}$ parameter. As long as the WD bit (D10) of an incoming SPI message is toggled within the minimum watchdog timeout period (WDTO), the device will operate normally. If an internal watchdog timeout occurs before the WD bit is toggled, the device will revert to Fail mode. All registers are cleared. To exit the Fail mode, send valid SPI communication with WD bit = 1.

Table 9. Initialization Register

SI Address					SI Data										
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	WD	0	0	FOGen	PWM sync	Xenon	MUX2	MUX1	MUX0	SOA1	SOA0

D6 (PWM sync) = 0, No synchronization

D6 (PWM sync) = 1, Synchronization on CSB positive edge

D5 ($\overline{\text{Xenon}}$) = 0, Xenon

D5 ($\overline{\text{Xenon}}$) = 1, H7 Bulb

D7 (FOGen) = 0, FOG pin does not control the output 4

D7 (FOGen) = 1, FOG input controls the output 4

D4, D3, D2 (MUX2, MUX1, MUX0) = 000, No current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 001, OUT1 current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 010, OUT2 current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 011, OUT3 current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 100, OUT4 current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 101, OUT5 current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 110, External Switch current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 111, Temperature analog feedback

ADDRESS 00001—CONFIGURATION OL

The Configuration OL register is used to enable the open load detection for LEDs in Normal mode (OLLEDn in Table 8) and to active the LED Control.

When bit D0 is set to logic [1], the open load detection circuit for LED is activated for output 1. When bit D0 is set to logic [0], open load detection circuit for standard bulbs is activated for output 1.

When bit D5 is set to logic [1], the LED Control is activated for output 1.

ADDRESS 00010—CONFIGURATION PRESCALER AND SR

Two configuration registers are available at this address. The Configuration Prescaler when D9 bit is set to logic [0] and Configuration SR when D9 bit is set to logic [1].

The Configuration Prescaler register is used to enable the PWM clock prescaler per output. When the corresponding PR bit is set to logic [1], the clock prescaler (reference clock divided by 2) is activated for the dedicated output.

The SR Prescaler register is used to increase the output slew rate by a factor of 2. When the corresponding SR bit is set to logic [1], the output switching time is divided by 2 for the dedicated output.

ADDRESS 00011—CONFIGURATION CSNS

The Configuration Current Sense register is used to disable the high over-current shutdown phase (OCHI1 and OCHI2 dynamic levels) in order to activate immediately the current sense analog feedback.

When bit D9 is set to logic [1], the current sense synchronization signal is reported on FETOUT output pin.

When the corresponding NO_OCHI bit is set to logic [1], the output is only protected with OCLO level. The current sense is immediately available if it is selected through SPI, as described in Figures 13. The NO_OCHI bit per output is automatically reset at each corresponding ON/OFF bit transition from logic [1] to [0], and in case of over-temperature or over-current fault. All NO_OCHI bits are also reset in case of under-voltage fault detection.

ADDRESS 01001—CONTROL OUT1

Bits D9 and D8 control the switching phases as shown in Table 10.

Table 10. Switching Phases

D9:D8	PWM Phase
00	0°
01	90°
10	180°
11	270°

Bit D7 at logic [1] turns ON OUT1. OUT1 is turned OFF with bit D7 at logic [0]. This register allows the master to control the duty cycle and the switching phases of OUT1. The duty cycle resolution is given by bits D6:D0.

D7 = 0, D6:D0 = XX output OFF.

D7 = 1, D6:D0 = 00 output ON during 1/128.

D7 = 1, D6:D0 = 1A output ON during 27/128 on PWM period.

D7 = 1, D6:D0 = 7F output continuous ON (no PWM).

ADDRESS 01010—CONTROL OUT2

Same description as OUT1.

ADDRESS 01011—CONTROL OUT3

Same description as OUT1.

ADDRESS 01100—CONTROL OUT4

Same description as OUT1.

ADDRESS 01101—CONTROL OUT5

Same description as OUT1.

ADDRESS 01110—CONTROL EXTERNAL SWITCH

Same description as OUT1.

ADDRESS 01111 —TEST MODE

This register is reserved for test and is not available with SPI during normal operation.

SERIAL OUTPUT COMMUNICATION (DEVICE STATUS RETURN DATA)

When the CSB pin is pulled low, the output register is loaded. Meanwhile, the data is clocked out MSB first as the new message data is clocked into the SI pin. The first 16 bits of data clocking out of the SO, and following a CSB transition, is dependant upon the previously written SPI word (SOA1 and SOA0 defined in the last SPI initialization word).

Any bits clocked out of the SO pin after the first 16 will be representative of the initial message bits clocked into the SI pin since the CSB pin first transitioned to a logic [0]. This feature is useful for daisy chaining devices.

A valid message length is determined following a CSB transition of logic [0] to logic [1]. If the message length is valid, the data is latched into the appropriate registers. A valid message length is a multiple of 16 bits. At this time, the SO pin is tri-stated and the fault status register is now able to accept new fault status information.

The output status register correctly reflects the status of the Initialization-selected register data at the time that the CSB is pulled to a logic [0] during SPI communication and/or for the period of time since the last valid SPI communication, with the following exceptions:

- The previous SPI communication was determined to be invalid. In this case, the status will be reported as though the invalid SPI communication never occurred.
- Battery transients below 6.0 V, resulting in an under-voltage shutdown of the outputs, may result in incorrect data loaded into the status register.

SERIAL OUTPUT BIT ASSIGNMENT

The contents of bits OD15:OD0 depend on bits D1:D0 from the most recent initialization command SOA[1:0] (refer to Table 8), and as explained in the paragraphs that follow.

The register bits are reset by a read operation and also if the fault is removed.

Table 11 summarizes the SO register content. Bit OD10 reflects Normal mode (NM).

Table 11. Serial Output Bit Map Description

Status/ Mode	Previous SI Data		SO Data															
	SOA1	SOA0	OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
Fault Status	0	0	0	0	UVF	OTW	OTS	NM	OL5	OVL5	OL4	OVL4	OL3	OVL3	OL2	OVL2	OL1	OVL1
Overload Status	0	1	0	1	UVF	OTW	OTS	NM	OC5	OTS5	OC4	OTS4	OC3	OTS3	OC2	OTS2	OC1	OTS1
Device Status	1	0	1	0	UVF	OTW	OTS	NM	0	OV	X	X	X	RC	FOG pin	FLASHER pin	IGN pin	CLOCK fail
Output Status	1	1	1	1	UVF	OTW	OTS	NM	0	0	0	0	0	OUT5	OUT4	OUT3	OUT2	OUT1
Reset	X	X	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

X = Don't care

PREVIOUS ADDRESS SOA[1:0]=00

If the previous two LSBs are 00, bits OD15:OD0 reflect the fault status (Table 11).

Table 12. Fault Status

OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
0	0	UVF	OTW	OTS	NM	OL5	OVL5	OL4	OVL4	OL3	OVL3	OL2	OVL2	OL1	OVL1

OD13 (UVF) = Under-voltage Flag on V_{BAT}

OD12 (OTW) = Over-temperature Prewarning Flag

OD11 (OTS) = Over-temperature Flag for all outputs

OD10 (NM) = Normal mode

OD9, OD7, OD5, OD3, OD1 (OL5, OL4, OL3, OL2, OL1) = Open Load Flag at Outputs 5 through 1, respectively.

OD8, OD6, OD4, OD2, OD0 (OVL5, OVL4, OVL3, OVL2, OVL1) = Overload Flag for Outputs 5 through 1, respectively.This corresponds to OCHI or OCLO faults.

Note

A logic [1] at bits OD9:OD0 indicates a fault. If there is no fault, bits OD9:OD0 are logic [0].

OVL=OCHI1+OCHI2+OCLO

PREVIOUS ADDRESS SOA[1:0]=01

If the previous two LSBs are 01, bits OD15:OD0 reflect the temperature status (Table 13).

Table 13. Overload Status

OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
0	1	UVF	OTW	OTS	NM	OC5	OTS5	OC4	OTS4	OC3	OTS3	OC2	OTS2	OC1	OTS1

OD13 (UVF) = Under-voltage Flag on V_{BAT}

OD12 (OTW) = Over-temperature Prewarning Flag

OD11 (OTS) = Over-temperature Flag for all outputs

OD10 (NM) = Normal mode

OD9, OD7, OD5, OD3, OD1 (OC5, OC4, OC3, OC2, OC1) = High Over-current Shutdown Flag for Outputs 5 through 1, respectively

OD8, OD6, OD4, OD2, OD0 (OTS5, OTS4, OTS3, OTS2, OTS1) = Over-temperature Flag for Outputs 5 through 1, respectively

Note

A logic [1] at bits OD9:OD0 indicates a fault. If there is no fault, bits OD9:OD0 are logic [0].

OC=OCHI1+OCHI2

PREVIOUS ADDRESS SOA[1:0]=10

If the previous two LSBs are 10, bits OD15:OD0 reflect the status of the 06XS3517 (Table 14).

Table 14. Device Status

OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
1	0	UVF	OTW	OTS	NM	0	0V	X	X	X	RC	FOG pin	FLASHER pin	IGN pin	CLOCK fail

OD13 (UVF) = Under-voltage Flag on V_{BAT}

OD12 (OTW) = Over-temperature Prewarning Flag

OD11 (OTS) = Over-temperature Flag for all outputs

OD10 (NM) = Normal mode

OD8 (Overvoltage) = Over-voltage Flag on V_{BAT} in real time

OD4 (RC) = Logic [0] indicates a Front Penta Device. Logic [1] indicates a Rear Penta Device

OD3 (FOG pin) = indicates the FOG pin state

OD2 (FLASHER pin) = Indicates the FLASHER pin state in real time

OD1 (IGN pin) = Indicates the IGN pin state in real time

OD0 (CLOCK fail) = Logic [1], which indicates a clock failure. The content of this bit is reset by read operation.

PREVIOUS ADDRESS SOA[1:0]=11

If the previous two LSBs are 11, bits OD15:OD0 reflect the status of the 06XS3517 (Table 14).

Table 15. Output Status

OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
1	0	UVF	OTW	OTS	NM	0	0	0	0	0	OUT5	OUT4	OUT3	OUT2	OUT1

OD13 (UVF) = Under-voltage Flag on V_{BAT}

OD12 (OTW) = Over-temperature Prewarning Flag

OD11 (OTS) = Over-temperature Flag for all outputs

OD10 (NM) = Normal mode

OD4 (OUT5) = Logic [0] indicates the OUT5 voltage is lower than V_{OUT_TH}. Logic [1] indicates the OUT5 voltage is higher than V_{OUT_TH}

OD3 (OUT4) = Logic [0] indicates the OUT4 voltage is lower than V_{OUT_TH}. Logic [1] indicates the OUT4 voltage is higher than V_{OUT_TH}

OD2 (OUT3) = Logic [0] indicates the OUT3 voltage is lower than V_{OUT_TH}. Logic [1] indicates the OUT3 voltage is higher than V_{OUT_TH}

OD1 (OUT2) = Logic [0] indicates the OUT2 voltage is lower than V_{OUT_TH}. Logic [1] indicates the OUT2 voltage is higher than V_{OUT_TH}

OD0 (OUT1) = Logic [0] indicates the OUT5 voltage is lower than V_{OUT_TH}. Logic [1] indicates the OUT1 voltage is higher than V_{OUT_TH}

PROTECTION AND DIAGNOSIS FEATURES

OUTPUT PROTECTION FEATURES

The 06XS3517 provides the following protection features:

- Protection against transients on V_{BAT} supply line (per ISO 7637)
- Active clamp, including protection against negative transients on output line
- Over-temperature
- Severe and resistive over-current
- Open Load during ON state

These protections are provided for each output (OUT1:5).

Over-temperature Detection

The 06XS3517 provides over-temperature shutdown for each output (OUT1:OUT5). It can occur when the output pin is in the ON or OFF state. An over-temperature fault condition results in turning OFF the corresponding output. The fault is latched and reported via SPI. To delatch the fault and be able to turn ON again the outputs, the failure condition must be removed (T< 175 °C, typically) and:

- if the device was in Normal mode, the output corresponding register (bit D7) must be rewritten. Application of complete OCHI window (OCHI1+OCHI2 during t2) depends on toggling or not toggling the D7 bit.
- if the device was in Fail mode, the corresponding output is locked until restart of the device: wake-up from Sleep mode or $V_{BATPOR1}$.

The corresponding SPI fault report (OTS bit) is removed after a read operation.

Over-current Detections

The 06XS3517 provides a dynamic over-current shutdown protection (see Figure 12) in order to protect the internal power transistors and the harness in the event of overload (fuse characteristic).

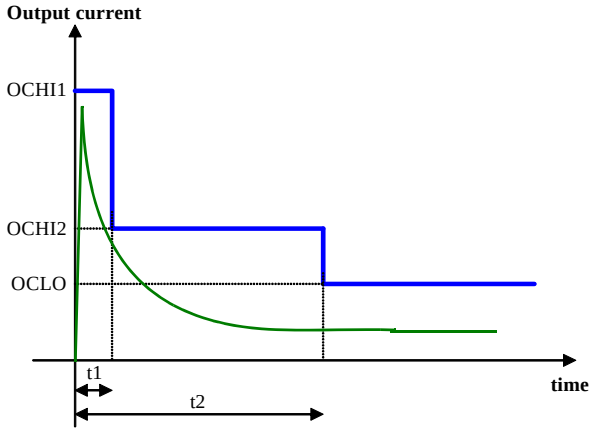


Figure 12. Two-segment Over-current Window in Normal Mode

OCHI (I_{OCHI1} and then I_{OCHI2}) is only activated after toggling D7 bit of the corresponding Control Out registers in Normal Mode. During switch-on, a severe short-circuit condition at the output is reported as an OCHI fault. In Fail Mode, the control of OCHI window is provided by the toggles: IGN_ON, Flasher_ON, and FOG_ON. The current thresholds (I_{OCHI1}, I_{OCHI2} and I_{OCLO}) and the time (t_1 and t_2) are fixed numbers for each channel. After t_2, the OCLO current threshold is activated to protect in steady state. t_1 and t_2 times are compared to “on” state duration (t_{ON}) of the output. In case of the output is controlled in PWM mode during the inrush period, the t_{ON} corresponds to the sum of each “on” state duration in order to only account for times the channel was actually in the ON state.

OUT2 is default loaded with the Xenon profile. The use of H7 bulbs at this output requires SPI programming (Xenon bit).

In case of overload (OCHI1 or OCHI2 or OCLO detection), the corresponding output is disabled immediately. The fault is

latched and the status is reported via SPI. To delatch the fault, the failure condition must be removed and:

For OCHI1:

- if the device was in Normal mode: the channel's associated on/off bit (bit D7) must be rewritten D7=1. Application of complete OCHI window depends on toggling or not toggling D7 bit.
- if the device was in Fail mode, the failure is locked until restart of the device: wake-up from Sleep mode or $V_{BATPOR1}$.

For OCHI2 and OCLO:

- if the device was in Normal mode: channel's associated on/off bit (bit D7) must be rewritten D7=1. Application of complete OCHI window depends on toggling or not toggling D7 bit.
- if the device was in Fail mode, Autorestart is activated. The device Autorestart feature opens a fixed window width and restarts at a fixed period with OCHI1 window. Autorestart feature resets OCHI2 or OCLO fault after corresponding Autorestart period.

The SPI fault reports are removed together after a read operation:

- OC bit=(OCHI1) or (OCHI2) fault
- OVL bit=(OCHI1) or (OCHI2) or (OCLO) fault

Over-voltage detection and active clamp

The 06XS3517 possesses an active gate clamp circuit in order to limit the maximum drain to source voltage.

In case of overload on an output the corresponding switch (OUT[1 to 5]) is turned off which leads to high-voltage at VBAT with an inductive VBAT line. The maximum VBAT voltage is limited at $V_{BATCLAMP}$ by automatically turning on the channel. In case of open load condition, the positive transient pulses (ISO 7637 pulse 2 and inductive battery line) shall also be handled by the application.

Figures 13 and 14 describe the faults management in Normal mode and Fail mode.

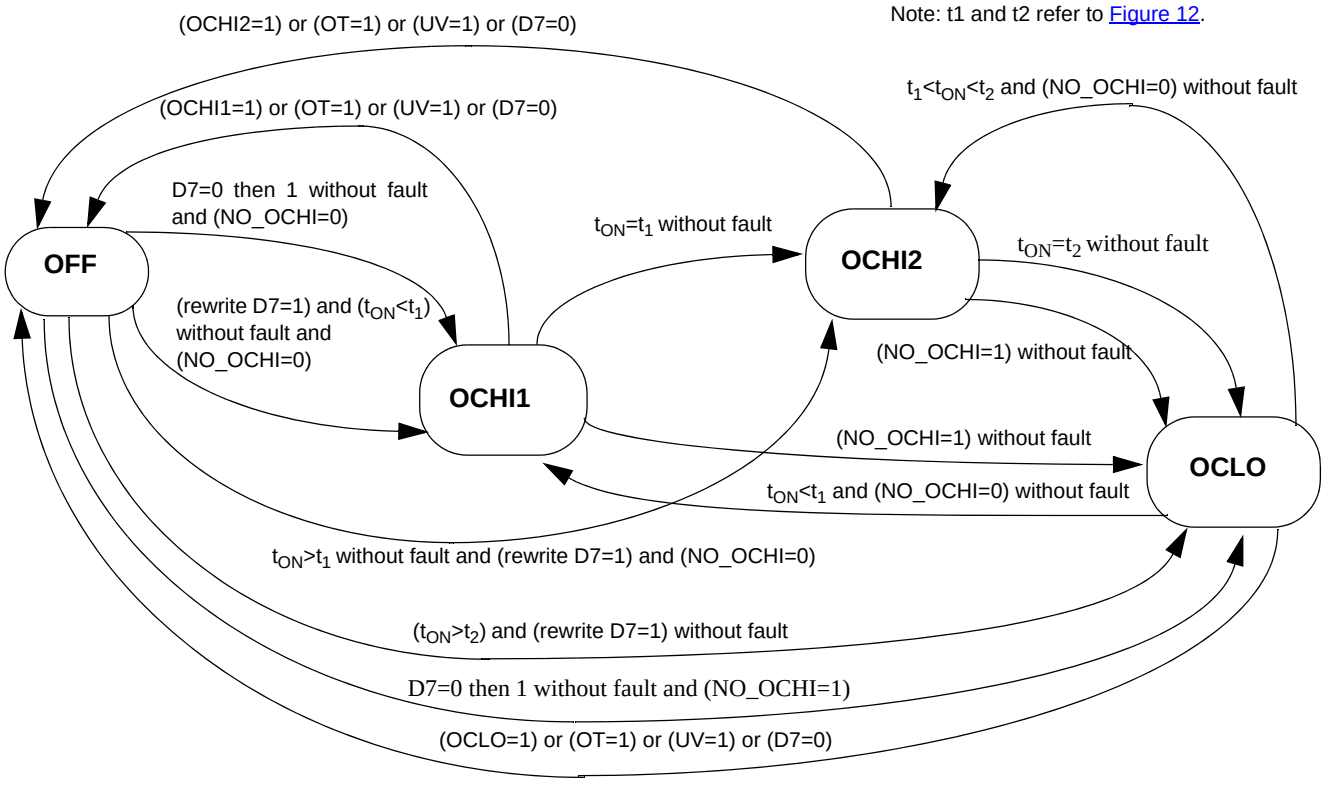
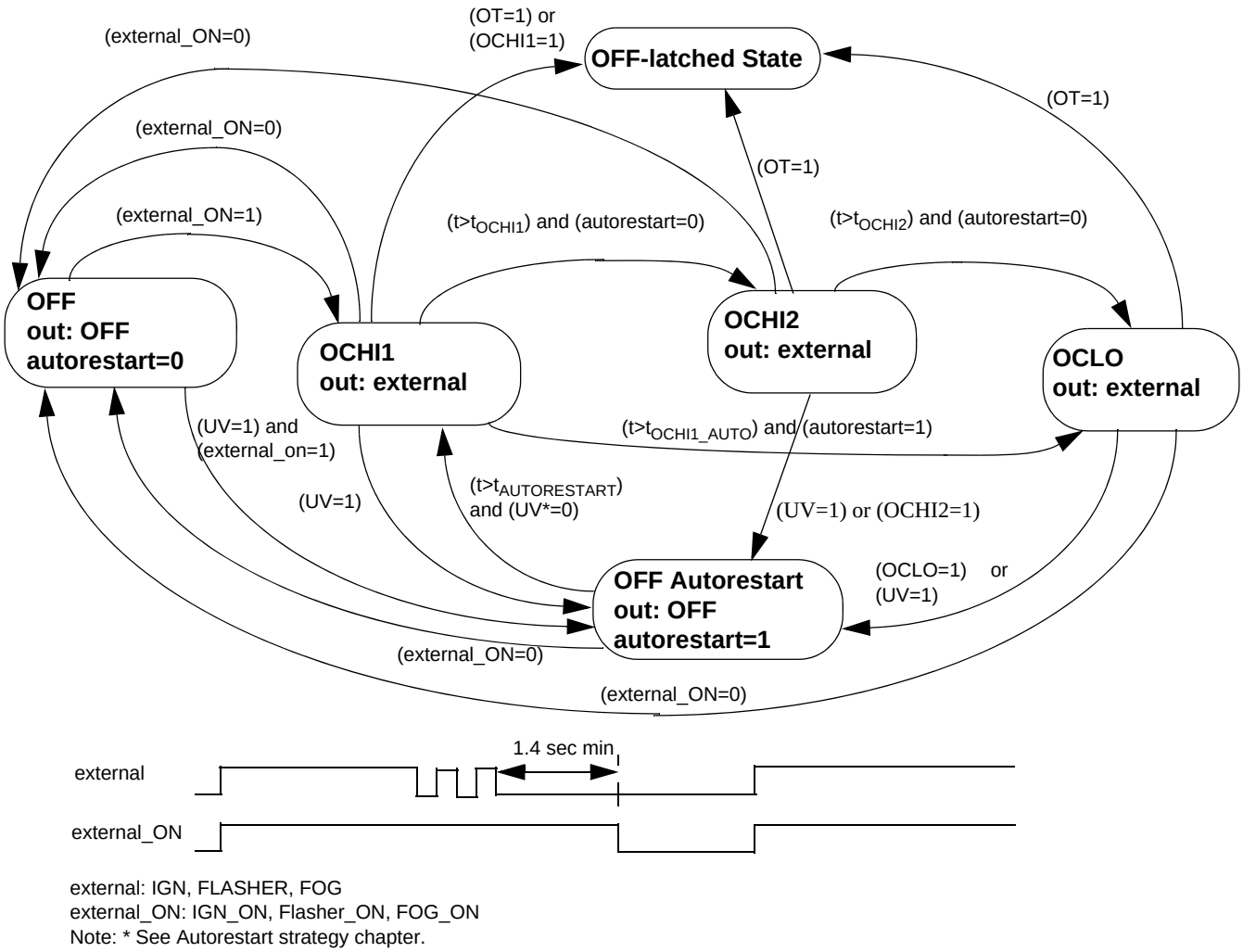


Figure 13. Faults Management in Normal Mode (for OUT[1:5] Only)



external: IGN, FLASHER, FOG
external_ON: IGN_ON, Flasher_ON, FOG_ON
Note: * See Autorestart strategy chapter.

Figure 14. Faults Management in Fail Mode (for OUT[1:5] Only)

DIAGNOSTIC Functions

Open Load

The 06XS3517 provides open load detection for each output (OUT1:OUT5) when the output pin is in the ON state. Open load detection levels can be chosen by SPI to detect a standard bulb, a Xenon bulb for OUT2 only, or LEDs (OLLED bit). Open load for LEDs only is detected during each regular switch-off state or periodically each t_{OLLED} (fully-on, D[6:0]=7F). To detect OLLED in fully on state, the output must be on at least t_{OLLED}. When an open load has been detected, the output stays ON.

To delatch the fault bit, the condition should be removed and the SPI read operation is needed (OL bit). In case of a Power on Reset on VBAT, the fault will be reset.

Current Sense

The 06XS3517 diagnosis for load current (OUT1:6) is done using the current sense (CSNS) pin connected to an external resistor. The CSNS resistance value is defined in function to V_{CC} voltage value. It is recommended to use resistor 500 Ω < R_{CSNS} < 5.0 kΩ. Typical value is 1.0 kΩ for 5.0 V application. The channel the current of which is sensed is addressed through bits MUX[4,2] bits of the Initialization register.

The current recopy feature for OUT1:5 is disabled during a high over-current shutdown phase (t_2) and is only enabled during low over-current shutdown thresholds. The current recopy output delivers current only during ON time of the output switch without overshoot (aperiodic settling).

The current recopy is not active in Fail mode.

With a calibration strategy, the output current sensing precision can be improved significantly. One calibration point at 25 °C for 50% of FSR allows removing part to part contribution. So, the calibrated part precision goes down to ±6.0% over [20% - 75%] output current FSR, over-voltage range (10 V to 16 V) and temperature range (-40 to 125 °C).

Board Temperature Feedback

The 06XS3517 provides a voltage proportional to the temperature on the GND flag, often representative for the temperature of the underlaying PCB land. This voltage is available at the CSNS output pin when the associated UX[2,0] bits are set to “111”. Figure 15 shows the output voltage over temperature.

.

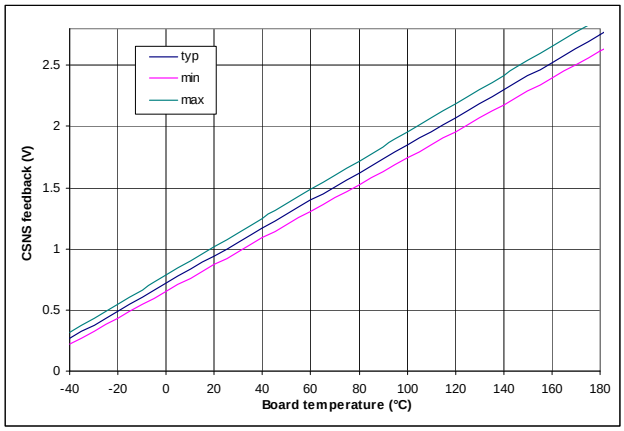


Figure 15. Temperature sensing voltage

The board temperature feedback is not active in Fail mode.

With a calibration strategy, the temperature monitoring precision can be improved. So, one calibration point at 25 °C allows removing part to part contribution, as presented in Figure 16.

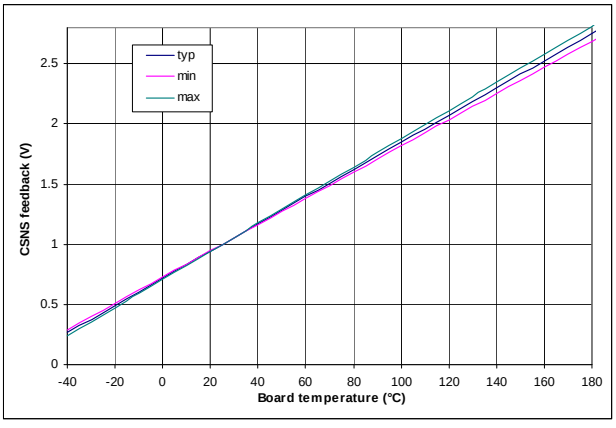


Figure 16. Analog Temperature Precision with Calibration Strategy

Output Voltage Status

The 06XS3517 provides the state of OUT1:OUT5 outputs in real time through SPI. The OUT bit is set to logic [1] when the corresponding output voltage is higher or equal then half of the supply voltage. This bit allows synchronizing current sense and diagnosing short-circuit between OUT and VBAT terminals.

TEMPERATURE PREWARNING

The 06XS3517 provides a temperature prewarning reported via the SPI (OTW bit) in Normal mode. The information is latched. To delatch, a read SPI command is needed. In case of a Power on Reset, the fault will be reset.

EXTERNAL PIN STATUS

The 06XS3517 provides the status of the FLASHER, FOG, and IGN pins via the SPI in real time and in Normal mode.

FAILURE HANDLING STRATEGY

A highly sophisticated fault handling strategy allows guaranteeing the various lighting functions even in case of failures inside the component or the light module. Components are protected against:

- Reverse Polarity
- Loss of Supply Lines
- Fatal Mistreatment of Logic I/O Pins

REVERSE POLARITY PROTECTION ON VBAT

In case of a permanently reverse voltage operation, the channels are turned ON (R_{SD} Ohm) in order to prevent thermal overloads. No protections are available.

An external diode on VCC is necessary in order to protect the 06XS3517 in cases from reverse polarity.

In case of negative transients on the VBAT line (per ISO 7637), the V_{CC} supplied functions are still available operating, while the VBAT line is negative. Without loads on OUT1:5 pin, an external clamp between V_{BAT} and GND is mandatory to avoid exceeding maximum ratings. The maximum external clamp voltage shall be between the reverse battery condition and -20 V.

Therefore, the device is protected against latch-up with or without load on OUT outputs.

LOSS OF SUPPLY LINES

The 06XS3517 is protected against the loss of any supply line. The detection of the supply line failure is provided inside the device itself.

LOSS OF VBAT

During an under-voltage of V_{BAT} ($V_{BATPOR1} < V_{BAT} < V_{BATUV}$), the outputs [1-5] are switched off immediately. No current path from VBAT to VCC exists. The external MOSFET (OUT6) can be controlled in Normal mode by the SPI if VCC is above V_{CCUV}. The fault is reported to the UVF bit (OD13). To delatch the fault, the under-voltage condition should be removed and:

- To turn-on the output, the corresponding D7 bit must be rewritten to logic [1] in Normal mode. Application of the OCHI window depends on toggling or not toggling the D7 bit.
- If the device was in Fail mode, the fault will be delatched by the Autorestart feature periodically.

In case of $V_{BAT} < V_{BATPOR1}$ (Power OFF mode), the behavior depends on V_{CC}:

- all latched faults are reset if VCC < V_{CCUV},
- all latched faults are maintained under V_{CC} in nominal conditions. In case V_{BAT} is disconnected, OUT[1:5] outputs are OFF. OUT6 output state depends on the previous SPI configuration. The SPI configuration, reporting, and daisy-chain features are provided for RST is set to logic [1]. The SPI pull-up and pull-down current resistors are available. This fault condition can be diagnosed with UVF fault in OD13 reporting bit. The previous device configuration is maintained. No current is conducted from V_{CC} to V_{BAT}.

LOSS OF V_{CC} (DIGITAL LOGIC SUPPLY LINE)

During loss of V_{CC} ($V_{CC} < V_{CCUV}$) and with wake=1, the 06XS3517 is switched automatically into Fail mode. The external SMART MOSFET is turned OFF. All SPI registers are reset and must be reprogrammed when V_{CC} goes above V_{CCUV}. The device will transit in OFF mode if $V_{BAT} < V_{BATPOR2}$.

LOSS OF V_{CC} AND VBAT

If the external V_{BAT} and V_{CC} supplies are disconnected (or not within specification: (V_{CC} and V_{BAT}) < $V_{BATPOR1}$), all SPI register contents are reset with default values corresponding to all SPI bits are set to logic [0] and all latched faults are also reset.

LOSS OF GROUND (GND)

During loss of ground, the 06XS3517 cannot drive the loads (the outputs (1:5) are switched OFF), but is not destroyed by the operating condition. Current limit resistors in the digital input lines protect the digital supply against excessive current (1.0 kOhm typical). The state of the external smart power switch controlled by FETOUT is not guaranteed, and the state of external smart MOS is defined with an external termination resistor.

FATAL MISTREATMENT OF LOGIC I/O PINS

The digital I/Os are protected against fatal mistreatment by signal plausibility check according to Table 16.

Table 16. Logic I/O Plausibility Check

Input/Output	Signal Check Strategy
LIMP	Debounce for 10 ms
(PWM) CLOCK	Frequency range (bandpass filter)
SPI (MOSI, SCLK, CS)	WD, D10 bit internal toggle

In case the LIMP input is set to logic [1] for a delay longer than 10 ms typical, the 06XS3517 is switched into Fail mode. In case of a (PWM) Clock failure, no PWM feature is provided and the bit D7 defines the outputs state. In case of SPI failure, the 06XS3517 is switched into Fail mode (see Figure 17)

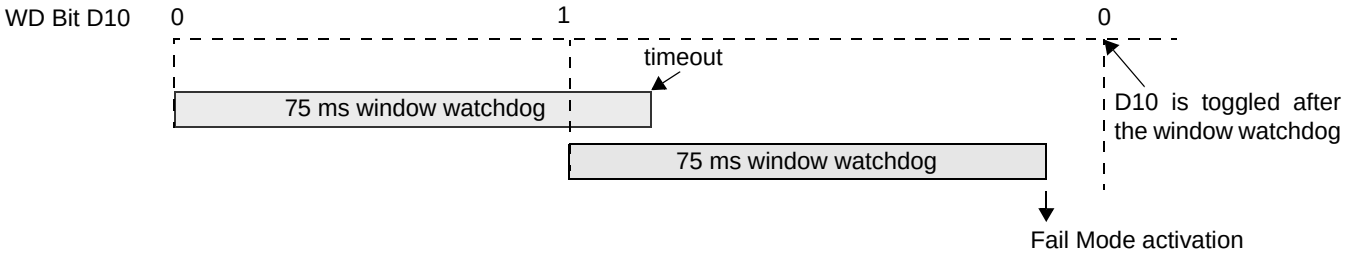


Figure 17. Watchdog window

TYPICAL APPLICATIONS

Figure 18 gives the architecture of a vehicle lighting system, including fog lights, battery redundancy concept, light substitution mode, and Fail mode.

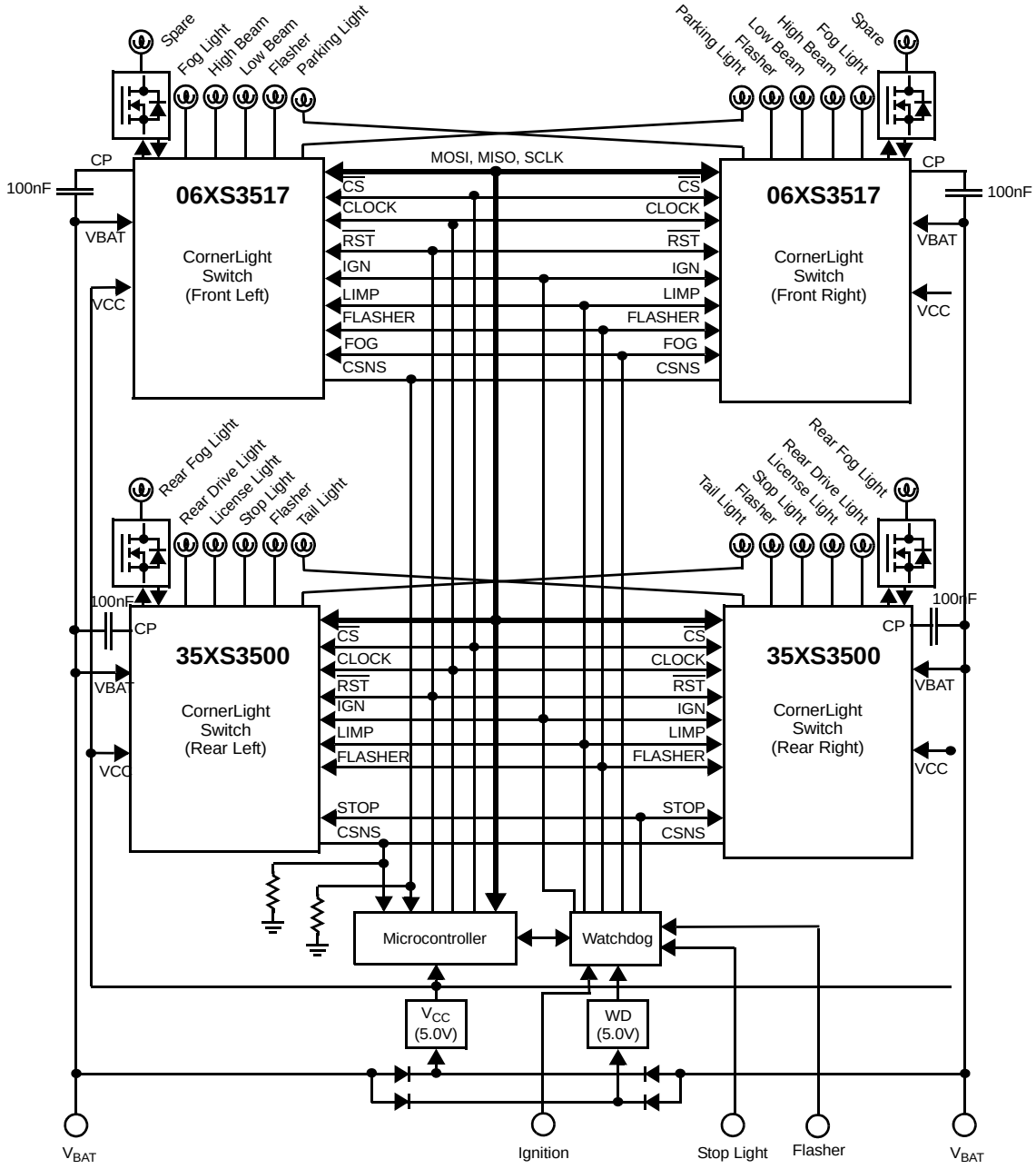


Figure 18. 06XS3517 Typical Application

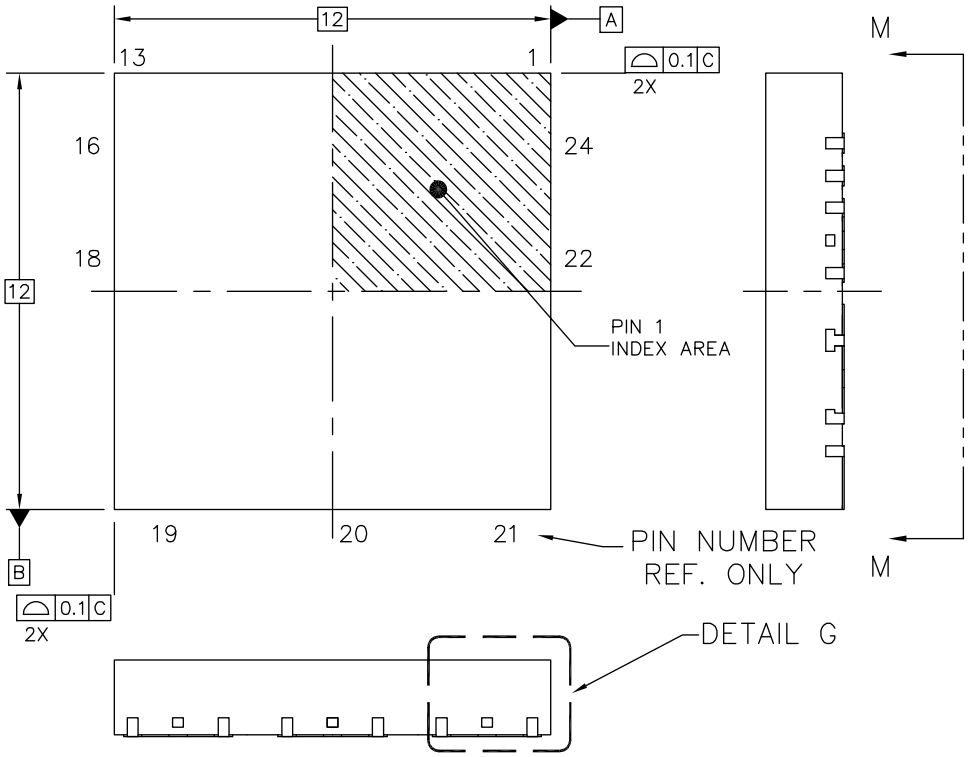
EMC PERFORMANCES

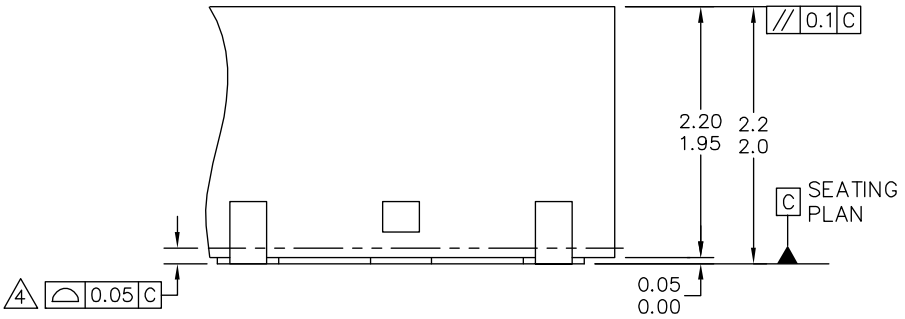
The 06XS3517 will be compliant to CISPR25 Class5 in the Standby mode with 22 nF decoupling capacitor on OUT[1:5].

PACKAGING

PACKAGING DIMENSIONS

For the most current package revision, visit www.freescale.com and perform a keyword search using the “98A” listed below.





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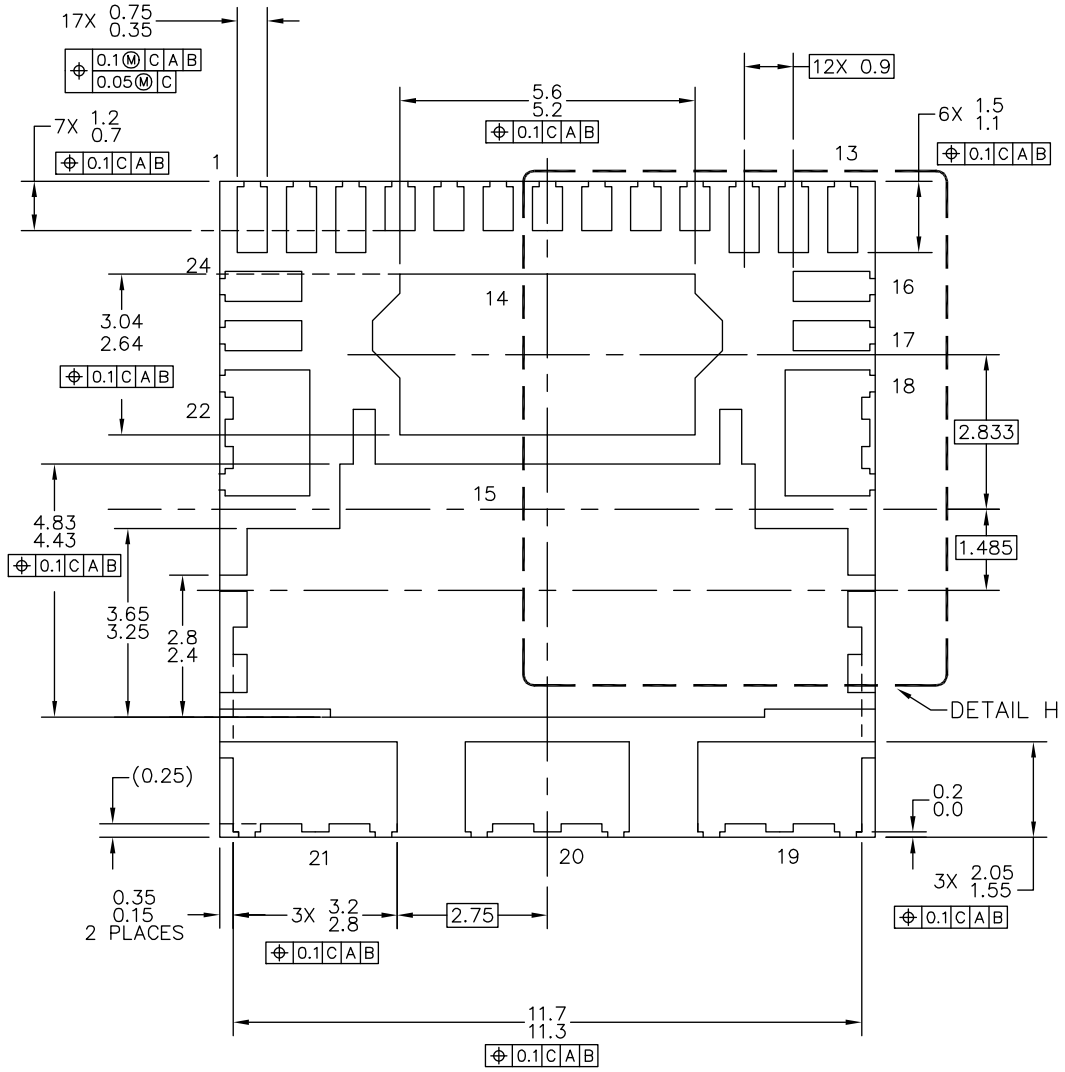

VIEW M–M

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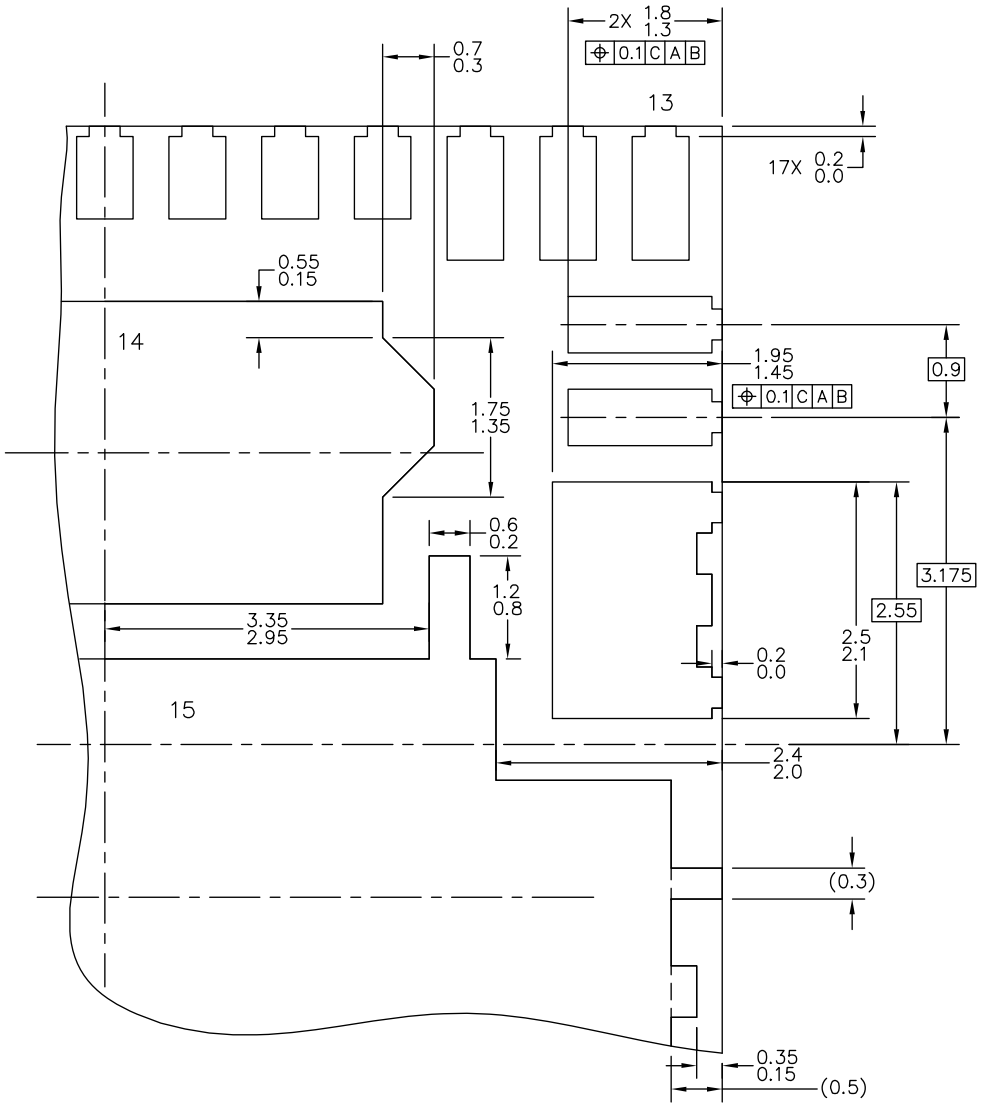

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ISSUE 0

06XS3517

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFP–N.
4. COPLANARITY APPLIES TO LEADS AND CORNER LEADS.
5. MINIMUM METAL GAP IS GUARANTEED TO BE 0.25MM.

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	CASE NUMBER: 1951–01	14 MAR 2007
	STANDARD: NON–JEDEC	

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ISSUE 0

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	2/2012	• Initial release
2.0	2/2012	• Corrected ordering information from MC06XS3517FK to MC06XS3517AFK • Updated 98A package drawing

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