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Application Note

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HC908QY4/QT4 Microcontroller (MCU) Application Hints

by: Arthur Oliveira
Brazil Semiconductor Technology Center
Brazil, SP

1 Introduction

This application note describes how to develop a robust application circuit using the MC68HC908QY4/QT4 family of microcontrollers (MCUs) by:

- Exploring characteristics of this MCU family
- Suggesting good practices and hints related to noise filtering, circuit and printed-circuit board design.

NOTE

A typical MC68HC908QT4 application circuit is shown, which presents good noise immunity and reliable operation.

MC68HC908QY4/QY2/QY1/QT4/QT2/QT1 microcontrollers, and other members of this family of MCUs (like MC68HLC908QY4/QT4 and MC68HC908QL4), have features and characteristics that need to be understood to achieve their best performance and avoid common application issues and pitfalls. Most techniques described here are useful for

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most of the microcontroller devices available in the market and are good application development practices. These techniques and hints are aimed at avoiding EMI, noise, and marginal designs that may disturb circuit operation and cause system malfunctions.

A robust application circuit design is achieved by detailed definition of product operation environment, good knowledge of MCU characteristics, careful device selection and PCB layout, good filtering, decoupling and termination techniques, complemented by good software development techniques. Those items are detailed in the next sections.

2 QY4 MCU Features and Characteristics

MC68HC908QY4/QT4 are members of the M68HC08 family of low-cost, high performance microcontrollers with a variety of modules, memory sizes, types, and package types. The HC08 central processor unit (CPU08), with Von Neumann architecture, is a complex instruction set computer (CISC) type.

Main features of the QY family MCUs are:

- Easy to use high-performance HC08 CPU
- 4 Kbytes or 1.5 Kbytes of in-application programmable flash
- 128 bytes of random-access memory (RAM)
- 2-channel 16-bit timer with selectable input capture, output compare, and pulse width modulator (PWM)
- Selectable crystal, RC or trimmable internal oscillator with ±5% accuracy
- 4-channel 8-bit analog-to-digital converter (ADC)
- Selectable trip-point low-voltage inhibit module (LVI), with flag or reset generation
- Computer operating properly (COP) watchdog timer
- Auto wakeup from stop mode capability
- Flexible high-current input/output (I/O) ports with programmable pullups
  — 13 or 5 bidirectional I/O
  — 1 input only
  — Keyboard interrupt inputs, shared with I/O pins
  — Asynchronous $\overline{\text{IRQ}}$ input, shared with I/O pin
  — Asynchronous $\overline{\text{RST}}$ input/output signal, shared with I/O pin
- QY family MCUs are available in these packages:
  — 16-pin plastic dual in-line package (PDIP)
  — 16-pin small outline integrated circuit (SOIC) package
  — 16-pin thin shrink small outline package (TSSOP)
- QT family MCUs are available in these packages:
  — 8-pin PDIP
  — 8-pin SOIC
  — 8-pin dual flat no lead (DFN) package

Remarkable characteristics of the QY family of MCUs are:

- Internal oscillator, RC oscillator (with external resistor), crystal oscillator, or external clock source, selectable by CONFIG register or user/monitor mode
- Due to low pin-count, many functional signals share pins with the port I/O signals. For example, ADC inputs, KBI inputs, timer signals, OSC signals, $\overline{IRQ}$, and $\overline{RST}$
- Monitor, programming, and test modes are entered by applying a voltage above V_{DD} (V_{HI}) at the $\overline{IRQ}$ pin and applying a reset signal to the $\overline{RST}$ pin

Shared pins, required to achieve low pin-count, require a careful selection of pin allocation on the application circuit. Proper termination and filtering at critical pins, like $\overline{IRQ}$ and $\overline{RST}$, is also required to avoid operation issues or an inadvertent mode change. Clock source selection (external or internal oscillator type) may also be changed (for example, when switching from user mode to monitor mode).

The PTA2/$\overline{IRQ}$/KBI2 pin is particularly sensitive to noise above the V_{DD} level, as this may be recognized as V_{HI} at the $\overline{IRQ}$ line (test voltage) which would force the $\overline{RST}$ pin to be an input. In this case, if a low level is applied to the shared PTA3/$\overline{RST}$/KBI3 pin, it is recognized as a reset. In the worst case, causing the MCU to enter monitor or test modes causes a system failure, until another reset is applied (power-on reset (POR), LVI reset, or external reset).

$\overline{IRQ}$ and $\overline{RST}$ pins should ideally be used on shared functions with short connection lines far away from noisy circuitry. Careful port-to-function allocation is recommended. See Figure 1.

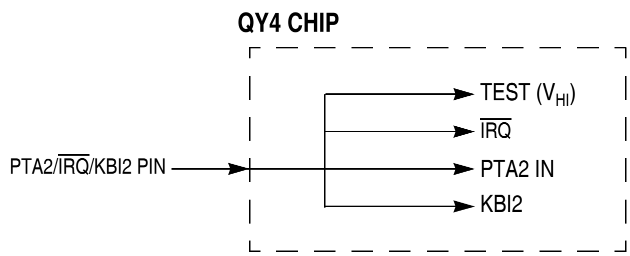
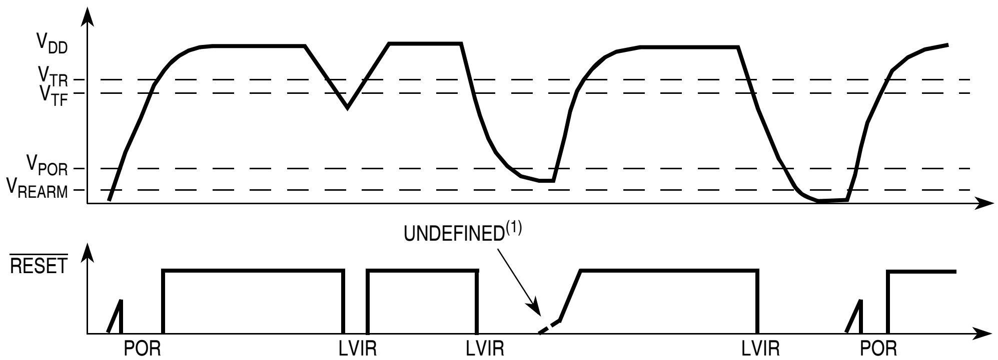


Figure 1. Shared Function Example

The internal POR module generates a reset when V_{DD} falls to roughly 1 V. However, POR rearm voltage is below 0.1 V when the module is ready to generate a POR again as V_{DD} rises. If the application circuit does not discharge V_{DD} below 0.1 V in a power-down sequence, POR may not be generated on the next power up. In this case, internal logic states are not initialized to guaranteed levels and may cause a malfunction. To guarantee circuit initialization, the POR pulse actually depends on the V_{DD} voltage level and a number of clock cycles.

A minimum POR rise time ramp rate is specified in the device data sheet. This ramp rate translates to maximum V_{DD} rise time for proper circuit initialization (roughly, from 0 V to 5 V in less than 150 ms). Slow V_{DD} ramp up should be avoided by using adequate current compliance in the power supply design. Do this by considering the MCU run mode V_{DD} supply current (RI_{DD}) plus pullups, pulldowns, sensors, LEDs, and other loads.

The low-voltage inhibit module (LVI) sets a flag bit or generates a reset if properly programmed at the configuration (CONFIG) register when V_{DD} falls below trip-falling level (selectable by CONFIG for 3-V or 5-V operation). The reset signal is deactivated when V_{DD} rises above the trip rising level (falling threshold level + hysteresis). LVI module active, LVI reset generation, and 3-V trip-points are selected by default upon resets.



1. Undefined state when POR is not rearmed

Figure 2. Supply Voltage Variation and Reset Generation

Due to characteristics mentioned before, at the initialization sequence, the application software has to take care of:

- Shared pin functionality selection
- Clock source selection
- LVI selection

NOTE

Different microcontroller families available in the market present other characteristics and limitations, which should be considered when designing application circuits.

For more detailed information on these topics and electrical specifications, refer to the MC68HC908QY4 Data Sheet (Freescale document order number MC68HC908QY4).

3 Application Hints

Good design practices must be used when developing application circuits, some of which are briefly described here. A detailed description of these techniques and hints may be found in Section 5, "References," and in other noise reduction, EMC, and PCB design bibliography.

3.1 Supply Circuit

- Analyze current consumption, power-up, and power-down sequences
- Determine noise filtering and add appropriate transient suppressor and decoupling capacitors
- Many voltage regulators require a ceramic capacitor near input pins as well as a low equivalent series resistance (ESR) capacitors plus decoupling capacitors on output pins
- Electrolytic or tantalum capacitors, with adequate capacitance to provide charge during supply voltage drops, and ceramic capacitors should be placed near regulator output pins

- In specifically noisy environments, like an automotive battery network, zener diodes, or varistors and series resistors may be required to filter extreme, high-energy, high-voltage transients
- Supply derived from AC mains should be of the preferred resistive type, which is a low-pass filter, instead of the capacitive type which is a high-pass filter and allows line transients to reach the V_{DD} network

3.2 Noise Filtering and Decoupling

- Small capacitors with high resonant frequency, or even RC filters, may be added to critical signal pins (like $\overline{IRQ}$, $\overline{RST}$, and ADC inputs)
- Good decoupling for internal and external noise, generally combining 0.1 μF and 0.01 μF ceramic or multilayer capacitors, are used as close as possible to V_{DD} and V_{SS} pins of the MCUs
- Pins, leads, and track inductance may degrade decoupling efficiency

For additional information, refer to Figure 3, Table 1, application note titled Designing for Board Level Electromagnetic Compatibility (Freescale document order number AN2321), and the technical articles listed in Section 5, “References.”

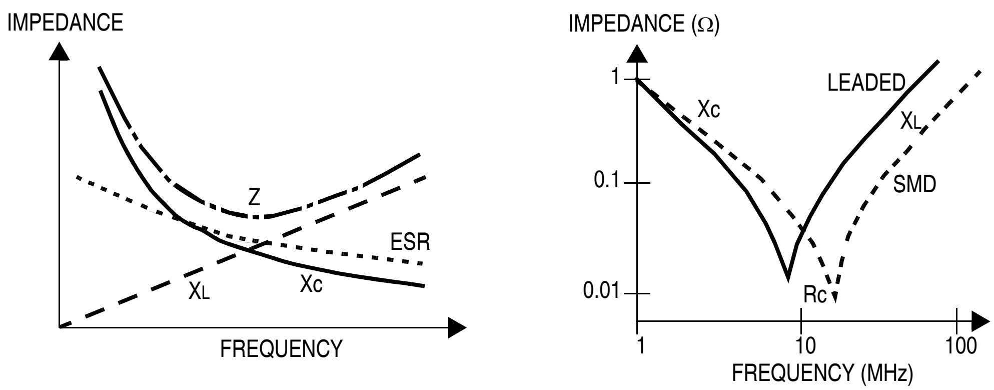


Figure 3. Typical Capacitor Parameters with Frequency

Table 1. Typical Electronic Device Characteristics

	Capacitance	Inductance	ESR	Self-Resonant Frequency
Leaded devices	4 pF per pin	1 nH/mm	—	—
Leadless devices	0.3 pF per pin	0.5 nH	—	—
Ceramic Z5U through-hole capacitor	For example, 0.1 μF	3.5 nH	—	8 MHz
Multilayer NPO through-hole capacitor	For example, 1 nF	3 nH	—	80 MHz
Ceramic Z5U SMD capacitor	For example, 0.1 μF	1 nH	—	16 MHz
Multilayer NPO SMD capacitor	For example, 1nF	0.5 nH	—	160 MHz
Aluminum electrolytic capacitor	For example, 10 μF	—	20 Ω	—
Aluminum electrolytic capacitor	For example, 1000 μF	—	0.5 Ω	—
Tantalum capacitor	For example, 10 μF	—	3 Ω	—
Tantalum capacitor	For example, 100 μF	—	0.8 Ω	—

3.3 Line Termination and Pullup/Pulldown Resistors

- Line termination and pullup/pulldown resistors may be required to guarantee voltage levels at high impedance or unused pins (do not tie directly to V_{DD}/V_{SS})
- Floating input pins may store intermediate voltage levels that would cause current drain on internal logic gates
- Floating pins are also prone to pick up noise and suffer electrostatic discharge stress (ESD)

In the specific case of QY4 MCUs, $\overline{IRQ}$ and $\overline{RST}$ pins should have decoupling capacitors to V_{DD} close to the MCU pins. If possible, pullup resistors and short connections should be far from high-noise circuitry.

3.4 POR and LVI Modules

- Internal POR circuits and LVI modules are efficient ways to protect MCUs from V_{DD} voltage drops (brown-out) and power-up/power-down events
- To check for proper operation with the power supply (within operating ranges), threshold levels and response times can be obtained from the MCU electrical specifications
- POR requires a number of clock cycles to release internal reset signals and oscillators may take some time to achieve adequate oscillating amplitude levels (for example, the internal oscillator is ready in a few cycles, crystal oscillators may require a thousand cycles to stabilize, and ceramic resonators may take even more to achieve full swing)

For more detailed information, refer to application note titled Resetting Microcontrollers During Power Transitions (Freescale document order number AN1744).

3.5 Protection Devices

Protection devices should be added to cancel spikes and to clamp voltages such as:

- Free-wheel diodes on relay coils and inductors
- Clamp diodes to V_{DD} or V_{SS} on critical pins subject to high energy noise,
- Reverse diodes on power switches to avoid arcs
- Zener diodes to limit voltage excursion at some critical circuit points

3.6 Printed Circuit Board

Printed circuit boards should be designed following good common practices such as:

- Maximizing ground plan or ground mesh (small ground loops to avoid high-frequency induced currents)
- Single-point ground connection for low-frequency signals
- Multi-point ground connection for high-frequency signals
- Signal layers inside V_{DD} and V_{SS} planes on multilayer PCBs
- Separate analog and digital power lines
- Large V_{DD} and V_{SS} tracks
- Narrow signal tracks to minimize inductance

- Short tracks on critical signals like clocks, oscillators, $\overline{\text{IRQ}}$, and $\overline{\text{RST}}$
- Ground shielding parallel to critical lines and around critical circuit areas (oscillators, analog circuitry, power circuitry, relays, etc.)
- Shielding around whole PCB

For more detailed information, refer to the application note titled Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers (Freescale document order number AN1050).

3.7 Noise Reduction Checklist

To control use of the most important techniques and be sure the design was thoroughly reviewed, use a noise reduction checklist. For more detailed information, refer to the application titled System Design and Layout Techniques for Noise Reduction in MCU-Based Systems (Freescale document order number AN1259).

3.8 Software Coding Practices

Incorporate software coding practices such as:

- Sanity checking routines or token pass routines on main flow
- Port or flag polling to control execution flow
- Filling empty memory with NOPs and JUMPs to allow recovery from wrong addressing

All of these may help to avoid code runaway or being lost on a bad loop, making the application more robust.

4 Typical Application Circuit

The circuit shown in Figure 4 is an application example of a microcontroller system in an automotive environment (a similar concept could be used for an appliance controller at the AC line).

The MC68HC908QT4 MCU:

- Reads a switch and one analog input
- Controls a light-emitting diode (LED) and a relay through a bipolar driver

Such a circuit presents good noise immunity and is the basis for reliable microcontroller system operation.

Some of the points recommended in this application note have been implemented in the circuit shown in Figure 4. They are:

- Series resistor and zener diode at +Bat for high voltage protection
- Ceramic decoupling capacitors close to regulator in and out pins
- Low ESR tantalum capacitor at regulator output
- Decoupling capacitor (multilayer suggested) close to MCU V_{DD}/V_{SS} pins
- Pullup resistors (internal or external) and noise filtering capacitors (multilayer suggested) at $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ pins, which deserve special attention at PCB layout (far from noise sources)
- PTA3/$\overline{\text{RST}}$ pin used for on-board jumper reading, not for external signal

- CN1 is the system connector, which may have long and noisy lines
- Optional CN2 connector may be used for in-circuit programming of MCU flash
- RC low-pass filter at analog sensor input for noise filtering
- Noise filtering capacitor at KBI pin, with internal pullup resistor enabled
- Relay with protection diodes and noise filtering capacitor at load line

NOTE

To filter incoming noise and high-voltage pulses, ideally 1 nF decoupling capacitor should be added right at the system connector pins in automotive applications.

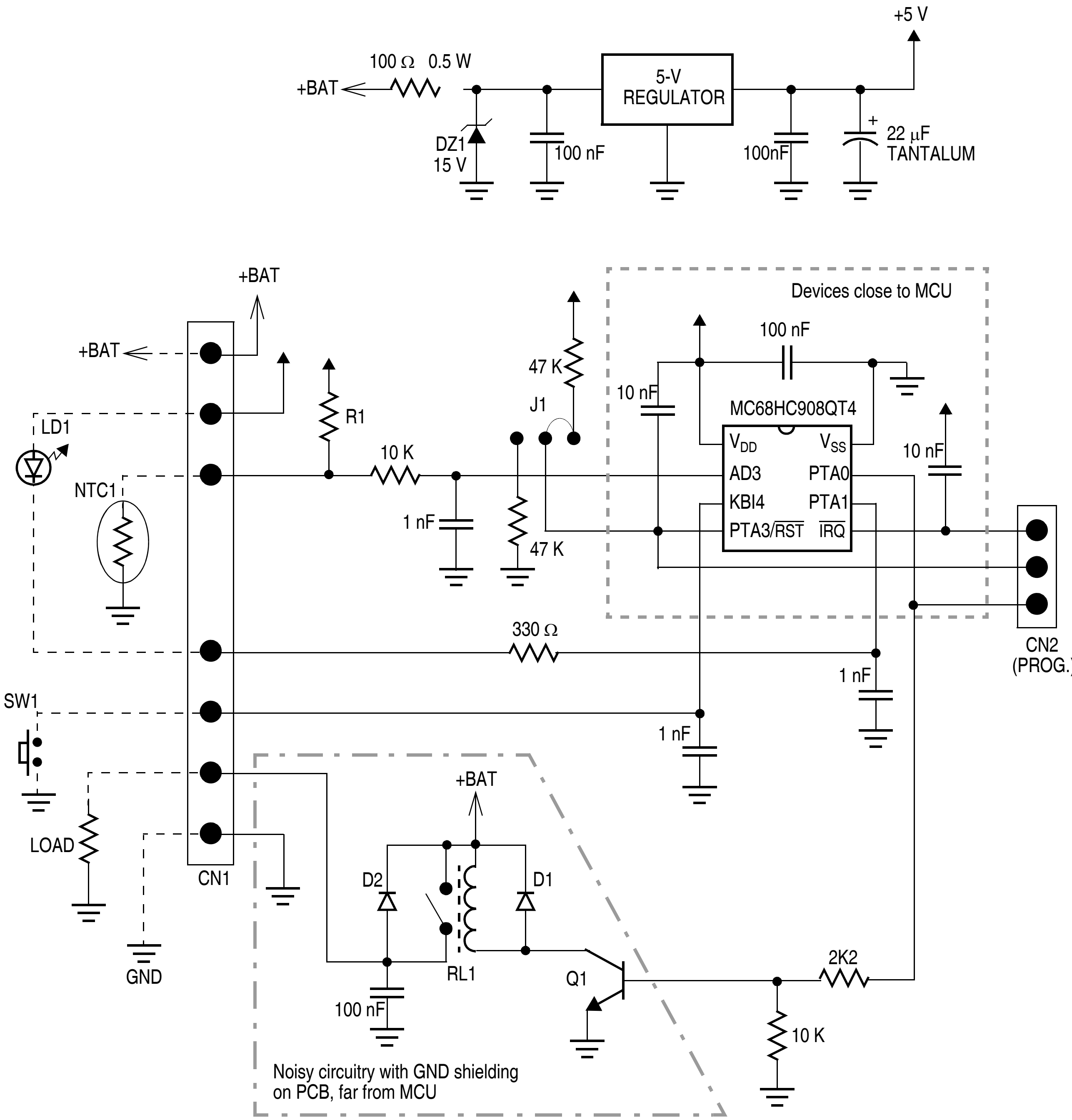


Figure 4. Typical Automotive Application Circuit using the MC68HC908QT4 MCU

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Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
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+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
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