MCP2021A/2A

LIN Transceiver with Voltage Regulator

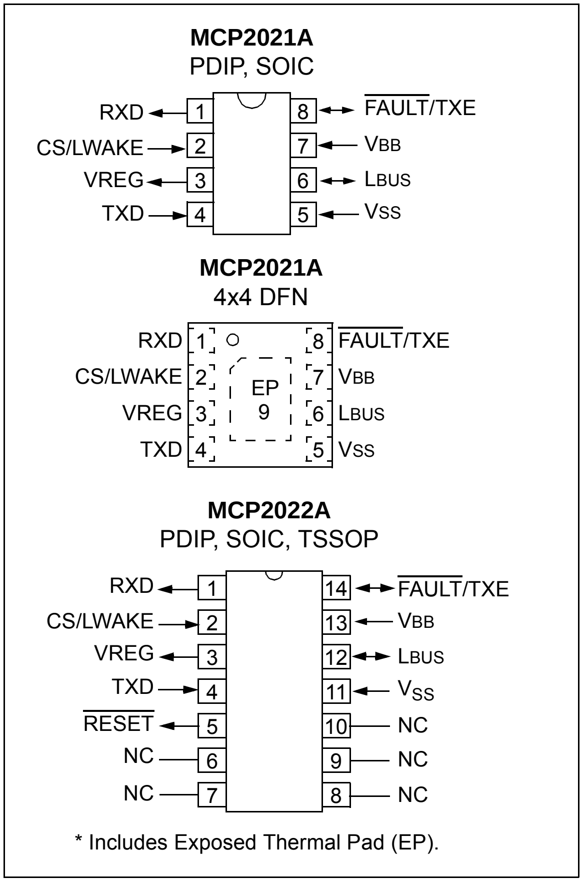
Features:

- The MCP2021A/2A is compliant with:
  - LIN Bus Specifications Version 1.3, and 2.x.
  - SAE J2602-2
- Support Baud Rates up to 20 kBaud
- 43V Load Dump Protected
- Maximum Continuous Input Voltage of 30V
- Wide LIN Compliant Supply Voltage, 6.0 - 18.0V
- Extended Temperature Range: -40 to +125°C
- Interface to PIC® EUSART and Standard USARTs
- Wake-up on LIN Bus Activity or Local Wake Input
- LIN Bus Pin
  - Internal Pull-up Termination Resistor and Diode for Slave Node
  - Protected Against VBAT Shorts
  - Protected Against Loss of Ground
  - High-Current Drive
- TXD and LIN Bus Dominant Time-out Function
- Two Low-Power Modes
  - TRANSMITTER OFF Mode: 90 µA (typical)
  - POWER DOWN Mode: 4.5 µA (typical)
- Output Indicating Internal RESET State (POR or SLEEP Wake)
- MCP2021A/2A On-chip Voltage Regulator
  - Output Voltage of 5.0V or 3.3V 70 mA Capability with Tolerances of ±3% Over Temperature Range
  - Internal Short Circuit Current Limit
  - Only External Filter and Load Capacitors Needed
- Automatic Thermal Shutdown
- High Electromagnetic Immunity (EMI), Low Electromagnetic Emission (EME)
- Robust ESD Performance: ±15 kV for LBUS and VBB pin (IEC61000-4-2)
- Transient Protection for LBUS and VBB Pins in Automotive Environment (ISO7637)
- Meets Stringent Automotive Design Requirements Including “OEM Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications”, Version 1.2, March 2011
- Multiple Package Options Including Small 4x4 mm DFN

Description

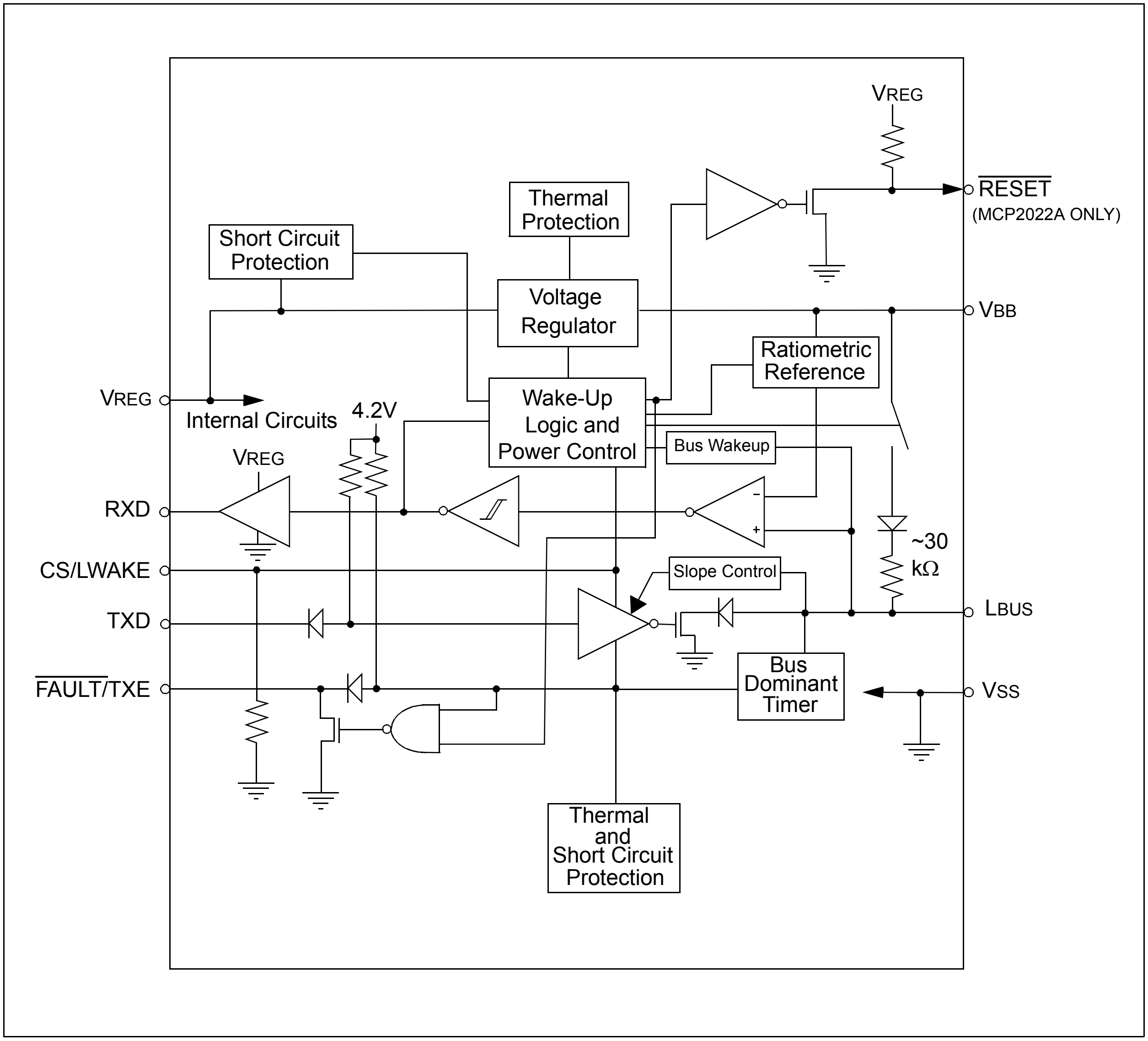
The MCP2021A/2A provides a bidirectional, half-duplex communication physical interface to meet the LIN bus specification Revision 2.1 and SAE J2602-2. The device incorporates a voltage regulator with 5V or 3.3V 70 mA regulated power supply output. The device has been designed to meet the stringent quiescent current requirements of the automotive industry and will survive +43V load dump transients, and double battery jumps.

Package Types (Top View)


MCP2021A
PDIP, SOIC
RXD 1
CS/LWAKE 2
VREG 3
TXD 4
8 FAULT/TXE
7 VBB
6 LBUS
5 VSS
MCP2021A
4x4 DFN
RXD 1
CS/LWAKE 2
VREG 3
TXD 4
EP 9
8 FAULT/TXE
7 VBB
6 LBUS
5 VSS
MCP2022A
PDIP, SOIC, TSSOP
RXD 1
CS/LWAKE 2
VREG 3
TXD 4
RESET 5
NC 6
NC 7
14 FAULT/TXE
13 VBB
12 LBUS
11 VSS
10 NC
9 NC
8 NC

* Includes Exposed Thermal Pad (EP).

Block Diagram


VREG
RESET
(MCP2022A ONLY)
Thermal Protection
Short Circuit Protection
Voltage Regulator
VBB
Ratiometric Reference
VREG
Internal Circuits
4.2V
Wake-Up Logic and Power Control
Bus Wakeup
VREG
RXD
-
+
~30 kΩ
CS/LWAKE
Slope Control
TXD
LBUS
FAULT/TXE
Bus Dominant Timer
VSS
Thermal and Short Circuit Protection

MCP2021A/2A Family Members

Device	Package	Regulator Output Voltage	$\overline{\text{RESET}}$ Pin
MCP2021A-500	8-PIN DFN, SOIC, PDIP	5.0V	No
MCP2021A-330	8-PIN DFN, SOIC, PDIP	3.3V	No
MCP2022A-500	14-PIN SOIC, TSSOP, PDIP	5.0V	Yes
MCP2022A-330	14-PIN SOIC, TSSOP, PDIP	3.3V	Yes

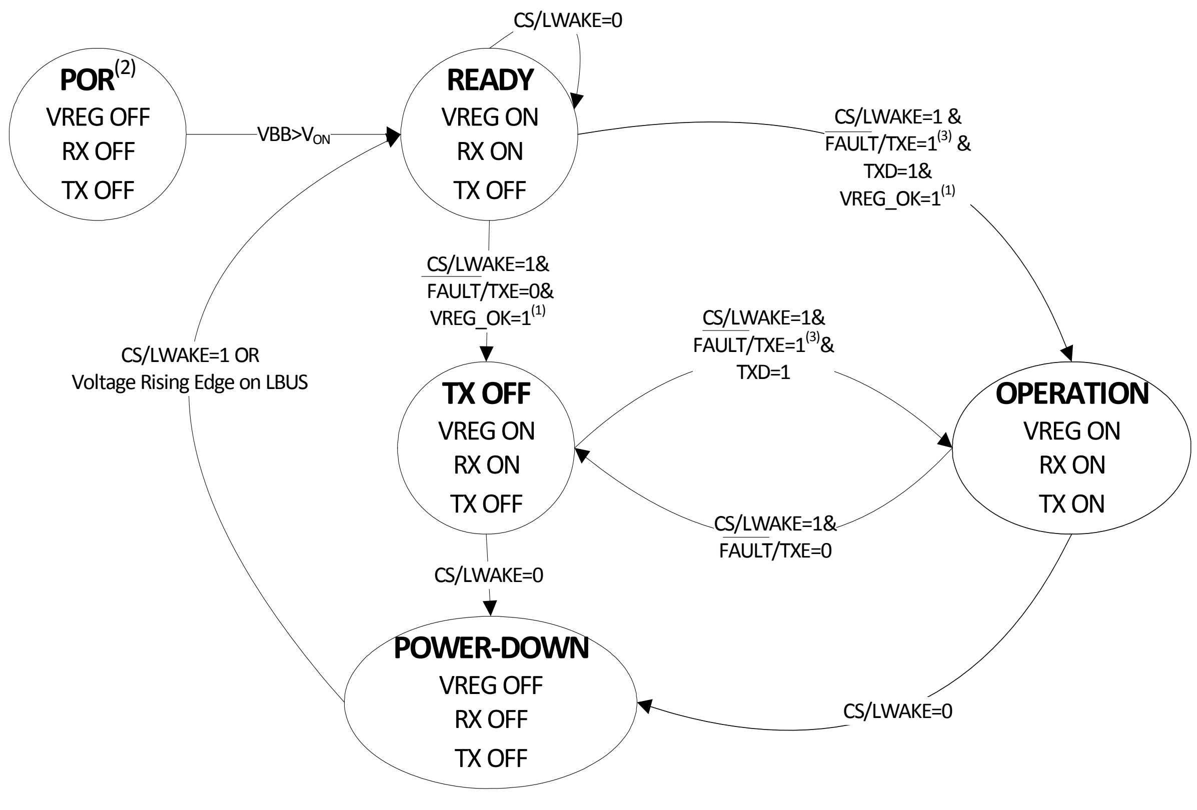
1.0 FUNCTION DESCRIPTION

The MCP2021A/2A provides a physical interface between a microcontroller and a LIN half-duplex bus. It is intended for automotive and industrial applications with serial bus baud rates up to 20 k Baud. This device will translate the CMOS/TTL logic levels to LIN logic levels, and vice versa. The device offers optimum EMI and ESD performance; it can withstand high voltage on the LIN bus. The device supports two low-power modes to meet automotive industry power consumption requirements. The MCP2021A/2A also provides a +5V or 3.3V 70 mA regulated power output.

1.1 Modes of Operation

The MCP2021A/2A works in five modes: POWER-ON-RESET mode, POWER-DOWN mode, READY mode, OPERATION mode, and TRANSMITTER OFF mode. For an overview of all operational modes, please refer to Table 1-1. For the operational mode transition, please refer to Figure 1-1.

FIGURE 1-1: STATE DIAGRAM


CS/LWAKE=0
POR(2)
VREG OFF
RX OFF
TX OFF
VBB>VON
READY
VREG ON
RX ON
TX OFF
CS/LWAKE=1 &
FAULT/TXE=1(3) &
TXD=1&
VREG_OK=1(1)
CS/LWAKE=1&
FAULT/TXE=0&
VREG_OK=1(1)
CS/LWAKE=1 OR
Voltage Rising Edge on LBUS
CS/LWAKE=1&
FAULT/TXE=1(3)&
TXD=1
TX OFF
VREG ON
RX ON
TX OFF
OPERATION
VREG ON
RX ON
TX ON
CS/LWAKE=1&
FAULT/TXE=0
CS/LWAKE=0
POWER-DOWN
VREG OFF
RX OFF
TX OFF
CS/LWAKE=0

Note 1: VREG_OK : Regulator Output Voltage > 0.8VREG_NOM.

2: If the voltage on pin VBB falls below V_{OFF}, the device will enter POWER-ON-RESET mode from all other modes, which is not shown in the figure.

3: FAULT/TXE = `1` represents input high and no fault conditions. FAULT/TXE = `0` represents input low or a fault condition, refer to Table 1-3.

1.1.1 POWER-ON-RESET MODE

Upon application of VBB, or whenever the voltage on VBB is below the threshold of regulator turn off voltage VOFF (typically 4.50V), the device enters POWER-ON-RESET mode (POR). During this mode, the device maintains the digital section in a reset mode and waits until the voltage on VBB pin rises above the threshold of regulator turn on voltage VON (typically 5.75V) to enter to READY mode. In POWER-ON-RESET mode, the LIN physical layer and voltage regulator are disabled, and RESET output (MCP2022A only) is forced to LOW.

1.1.2 READY MODE

The device enters READY mode from POR mode after the voltage on VBB rises above the threshold of regulator turn on voltage V_{ON} or from POWER-DOWN mode when a remote or local wake-up event happens.

Upon entering READY mode, the voltage regulator and receiver section of the transceiver are powered up. The transmitter remains in an off state. The device is ready to receive data but not to transmit. In order to minimize the power consumption, the regulator operates in a reduced-power mode. It has a lower GBW product and thus is slower. However, the 70 mA drive capability is unchanged.

The device stays in READY mode until the output of the voltage regulator has stabilized and the CS/LWAKE pin is HIGH (‘1’).

1.1.3 OPERATION MODE

If VREG is OK (VREG>0.8VREG_NORM), and the CS/LWAKE pin, FAULT/TXE pin and TXD pin are HIGH, the part enters OPERATION mode from either READY or TRANSMITTER OFF mode.

In this mode, all internal modules are operational. The internal pull-up resistor between LBUS and VBB is connected only in this mode.

The device goes into POWER-DOWN mode at the falling edge on CS/LWAKE; or to the TRANSMITTER OFF mode at the falling on FAULT/TXE while CS/LWAKE stays HIGH.

1.1.4 TRANSMITTER OFF MODE

In TRANSMITTER OFF mode, the receiver is enabled but the LBUS transmitter is off. It is a lower power mode.

In order to minimize power consumption, the regulator operates in a reduced power mode. It has a lower GBW product and thus is slower. However the 70 mA drive capability is unchanged.

The transmitter may be re-enabled whenever the FAULT/TXE signal returns high, by removing the internal fault condition and the CPU returning the FAULT/TXE high. The transmitter will not be enabled even if the FAULT/TXE pin is brought high externally, when the internal fault is still present. However, externally forcing the FAULT/TXE high while internal fault is still present should be avoided, since this will induce high current and power dissipation in the FAULT/TXE pin.

The transmitter is also turned off whenever the voltage regulator is unstable or recovering from a fault. This prevents unwanted disruption of the bus during times of uncertain operation.

1.1.5 POWER-DOWN MODE

In POWER-DOWN mode, the transceiver and the voltage regulator are both off. Only the Bus Wake-up section and the CS/LWAKE pin wake-up circuits are in operation. This is the lowest power mode.

If any bus activity (e.g. a BREAK character) occurs during POWER-DOWN mode, the device will immediately enter READY mode and enable the voltage regulator. Then, once the regulator output has stabilized (approximately 0.3 ms to 1.2 ms), it goes to OPERATION mode. Refer to **Section 1.1.6 “Remote Wake-up”**.

The part will also enter READY mode from POWER-DOWN mode, followed by the OPERATION mode, if the CS/LWAKE pin becomes active HIGH (‘1’).

1.1.6 REMOTE WAKE-UP

The remote wake-up sub module observes the LBUS in order to detect bus activity. In POWER DOWN mode, normal LIN recessive/dominant threshold is disabled, and the LIN bus Wake-Up Voltage Threshold $V_{WK(LBUS)}$ is used to detect bus activities. Bus activity is detected when the voltage on the LBUS falls below the LIN bus Wake-Up Voltage Threshold $V_{WK(LBUS)}$ (approximately 3.5V) for at least t_{BDB} (a typical duration of 80 µs) followed by a rising edge. Such a condition causes the device to leave POWER-DOWN mode.

TABLE 1-1: OVERVIEW OF OPERATIONAL MODES

State	Transmitter	Receiver	Internal Wake Module	Voltage Regulator	Operation	Comments
POR	OFF	OFF	OFF	OFF	Transfer to READY mode after VBB>V_{ON}	
READY	OFF	ON	OFF	ON	If CS/LWAKE high, then proceed to OPERATION or TRANSMITTER OFF mode.	Bus Off state
OPERATION	ON	ON	OFF	ON	If CS/LWAKE low level, then Power down If FAULT/TXE low level, then TRANSMITTER-OFF mode	Normal Operation mode
POWER DOWN	OFF	OFF	ON Activity Detect	OFF	On LIN bus rising edge or CS/LWAKE high level, go to READY mode.	Lowest Power mode
TRANSMITTER-OFF	OFF	ON	OFF	ON	If CS/LWAKE low level, then Power down If FAULT/TXE high, then OPERATION mode	Bus Off state, Lower Power mode

1.2 Pin Descriptions

Please refer to Table 1-2 for the pinout overview.

1.2.1 VBB

Battery Positive Supply Voltage pin. An external diode is connected in series to prevent the device from being reversely powered (refer to **FIGURE 1-9: "Typical Application Circuit"**).

1.2.2 VREG

Positive Supply Voltage Regulator Output pin. An on-chip LDO gives +5.0 or +3.3V 70 mA regulated voltage on this pin.

1.2.3 VSS

Ground pin.

1.2.4 TXD

Transmit data input pin (TTL level, HV compliant, adaptive pull-up). The transmitter reads the data stream on TXD pin and sends it to LIN bus. The LBUS pin is low (dominant) when TXD is low, and high (recessive) when TXD is high.

The Transmit Data Input pin has an internal adaptive pull-up to an internally-generated 4.2V (approximately). When TXD is '0', a weak pull-up (~900 kΩ) is used to reduce current. When TXD is '1', a stronger pull-up (~300 kΩ) is used to maintain the logic level. A series reverse-blocking diode allows applying TXD input voltages greater than the internally generated 4.2V and renders TXD pin HV compliant up to 30V (see block diagram).

1.2.5 RXD

Receive Data Output pin. The RXD pin is a standard CMOS output pin and it follows the state of the LBUS pin.

1.2.6 LBUS

LIN Bus pin. LBUS is a bidirectional LIN bus Interface pin and is controlled by the signal TXD. It has an open collector output with a current limitation. To reduce electromagnetic emission, the slopes during signal changes are controlled, and the LBUS pin has corner-rounding control for both falling and rising edges.

The internal LIN receiver observes the activities on the LIN bus, and generates the output signal RXD that follows the state of the LBUS. A 1st degree 160 kHz, low-pass input filter optimizes electromagnetic immunity.

1.2.7 CS/LWAKE

Chip Select and Local Wake-up Input pin (TTL level, high voltage tolerant). This pin controls the device state transition. Refer to **FIGURE 1-1: "State Diagram"**.

If CS/LWAKE = 1, the device can work in OPERATION mode ($\overline{\text{FAULT}}$/TXE = 1) or TRANSMITTER OFF mode ($\overline{\text{FAULT}}$/TXE = 0).

If CS/LWAKE = 0, the device can work in POWER-DOWN mode or READY mode.

An internal pull-down resistor will keep the CS/LWAKE pin low to ensure that no disruptive data will be present on the bus while the microcontroller is executing a Power-on Reset and I/O initialization sequence. When CS/LWAKE is '1', a weak pull-down (~600 kΩ) is used to reduce current. When CS/LWAKE is '0' a stronger pull-down (~300 kΩ) is used to maintain the logic level.

This pin may also be used as a local wake-up input (see **FIGURE 1-9: "Typical Application Circuit"**). The microcontroller will set the I/O pin to control the CS/LWAKE. An external switch, or other source, can then wake-up both the transceiver and the microcontroller.

Note:	CS/LWAKE should NOT be tied directly to the VREG pin as this could force the MCP2021A/2A into Operation mode before the microcontroller is initialized.

1.2.8 $\overline{\text{FAULT}}$/TXE

Fault Detect Output/Transmitter Enable Input pin. The output section is HV tolerant open drain (up to 30V). The input section is identical with the TXD section (TTL level, HV compliant, adaptive pull-up). The internal pull-up resistor may be too weak for some applications. We recommend to add a 10 k ohm external pull-up resistor to ensure a logic high level. Its state is defined as shown in **TABLE 1-3: "FAULT/TXE Truth Table"**. The device is placed in TRANSMITTER OFF mode whenever this pin is LOW ('0'), either from an internal fault condition or by external drive.

If CS/LWAKE is HIGH ('1'), the $\overline{\text{FAULT}}$/TXE signals a mismatch between the TXD input and the LBUS level. This can be used to detect a bus contention. Since the bus exhibits a propagation delay, the sampling of the internal compare is debounced to eliminate false faults.

After the device wakes up, the $\overline{\text{FAULT}}$/TXE indicates what wakes the device if CS/LWAKE remains LOW ('0') (refer Table 1-3).

The $\overline{\text{FAULT}}$/TXE pin sampled at a rate faster than every 10 µs.

1.2.9 $\overline{\text{RESET}}$ (MCP2022A ONLY)

RESET OUTPUT pin. This pin is open drain with ~90 kΩ pull-up to VREG. It indicates the internal voltage has reached a valid, stable level. As long as the internal voltage is valid (above 0.8 VREG), this pin will remain HIGH ('1'); otherwise the $\overline{\text{RESET}}$ pin switches to LOW ('0').

TABLE 1-2: PINOUT OVERVIEW

PIN Name	PIN Number		PIN Type	Function
	MCP2021A	MCP2022A		
VREG	3	3	Output	Voltage Regulator Output
VSS	5	11	Power	Ground
VBB	7	13	Power	Battery
TXD	4	4	Input, HV-tolerant	Transmit Data Input
RXD	1	1	Output	Receive Data Output
LBUS	6	12	I/O, HV	LIN Bus
CS/LWAKE	2	2	TTL Input, HV-tolerant	Chip Select and Local Wake-up Input
FAULT/TXE	8	14	I/O, HV-tolerant	Fault Detect Output/Transmitter Enable Input
RESET	-	5	Output	Reset Output

TABLE 1-3: FAULT/TXE TRUTH TABLE

TXD In	RXD Out	LIN BUS I/O	Thermal Override	FAULT/TXE		Definition
				External Input	Driven Output	
CS = 1						
L	H	VBB	OFF	H	L	**FAULT**, TXD driven low, LIN BUS shorted to VBB **(Note 1),** or LBUS/TXD permanent dominant detected, and Transmit time-out shutdown.
H	H	VBB	OFF	H	H	**OK**
L	L	GND	OFF	H	H	**OK**
H	L	GND	OFF	H	H	**OK**, data is being received from the LIN BUS
x	x	VBB	ON	H	L	**FAULT**, Transceiver in thermal shutdown
x	x	VBB	x	L	x	**NO FAULT**, the CPU is commanding the transceiver to turn off the transmitter driver
CS = `0` after a wake-up						
x	x	x	x	x	L	**Wake-up from LIN bus activity**
x	x	x	x	x	H	**Wake-up from POR**

Legend: x = don't care

Note 1: The FAULT/TXE is valid after approximately 25 µs after TXD falling edge. This is to eliminate false fault reporting during bus propagation delays.

1.3 Fail-Safe Features

1.3.1 GENERAL FAIL-SAFE FEATURES

- An internal pull-down resistor on CS/LWAKE pin disables the transmitter if the pin is floating.
- An internal pull-up resistor on the TXD pin places TXD in HIGH thus the LBUS in recessive if TXD pin is floating.
- High-impedance and low-leakage current on LBUS during loss of power or ground.
- The current limit on LBUS protects the transceiver from being damaged if the pin is shorted to VBB.

1.3.2 THERMAL PROTECTION

The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter and voltage regulator.

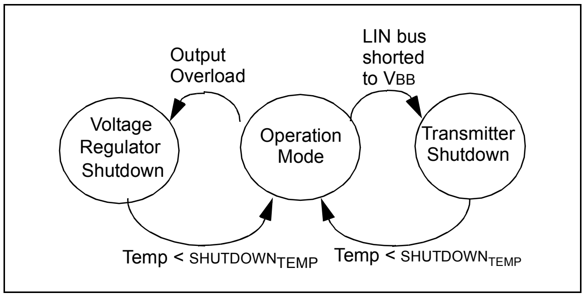
There are three causes for a thermal overload. A thermal shut down can be triggered by any one, or a combination of, the following thermal overload conditions.

- Voltage regulator overload
- LIN bus output overload
- Increase in die temperature due to increase in environment temperature

The recovery time from the thermal shutdown is equal to adequate cooling time.

Driving the TXD and checking the RXD pin make it possible to determine whether there is a bus contention (TXD = high, RXD = low) or a thermal overload condition (TXD = low, RXD = high).

FIGURE 1-2: THERMAL SHUTDOWN STATE DIAGRAMS



1.3.3 TXD/LBUS TIME-OUT TIMER

The LIN bus can be driven to a dominant level either from the TXD pin or externally. An internal timer deactivates the LBUS transmitter if a dominant status (LOW) on the LIN bus lasts longer than Bus Dominant Time-out Time $t_{TO(LIN)}$ (approximately 20 milliseconds). At the same time, RXD output is put in recessive (HIGH), $\overline{\text{FAULT}}$/TXE is also driven to LOW, and the internal LIN pull-up resistor is disconnected. The timer is reset on any recessive LBUS status or POR mode. The recessive status on LBUS can be caused either by the bus being externally pulled up or by the TXD pin being returned high.

1.4 Internal Voltage Regulator

The MCP2021A/2A has a positive regulator capable of supplying +5.00 or +3.30 VDC ±3% at up to 70 mA of load current over the entire operating temperature range of -40°C to +125°C. The regulator uses a LDO design, is short-circuit-protected and will turn the regulator output off if its output falls below the Shutdown Voltage Threshold V_{SD}.

With a load current of 70 mA, the minimum input to output voltage differential required for the output to remain in regulation is typically +0.5V (+1V maximum over the full operating temperature range). Quiescent current is less than 100 µA with a full 70 mA load current when the input to output voltage differential is greater than +3.00V.

Regarding the correlation between VBB, VREG and IDD, please refer to Figure 1-6 and Figure 1-7. When the input voltage (VBB) drops below the differential needed to provide stable regulation, the voltage regulator output VREG will track the input down to approximately VOFF. The regulator will turn off the output at this point. This will allow PIC® microcontrollers, with internal POR circuits, to generate a clean arming of the Power-on Reset trip point. The MCP2021A/2A will then monitor VBB and turn on the regulator when VBB is above the threshold of regulator turn on voltage V_{ON}.

In Power-down mode, the VBB monitor is turned off.

Under a specific ambient temperature and battery voltage range, the voltage regulator can output as high as 150mA current. For current load capability of the voltage regulator, refer Figure 1-4 and Figure 1-5.

> **Note:** The regulator overload current limit is approximately 250 mA. The regulator output voltage V_{REG} is monitored. If output voltage V_{REG} is lower than V_{SD}, the voltage regulator will turn off. After a recovery time of about 3mS, the V_{REG} will be checked again. If there is no short circuit ($V_{REG} > V_{SD}$), then the voltage regulator remains on.

The regulator requires an external output bypass capacitor for stability. See Figure 2-1 for correct capacity and ESR for stable operation.

> **Note:** A ceramic capacitor of at least 10 uF, or a tantalum capacitor of at least 2.2 uF is recommended for stability.

> **Warning:** A ceramic capacitor may worst case derate 50%, based on tolerance, voltage and temperature. Therefore, in order to ensure stability, ceramic capacitors smaller than 10 uF may require a small series resistance to meet the ESR requirements. We recommend 1 Ohm in series with a 1 uF capacitor, 0.47 Ohm in series with a 2.2 uF capacitor, 0.22 Ohm in series with a 4.7 uF capacitor and 0.1 Ohm in series with a 6.8 uF capacitor.

FIGURE 1-3: VOLTAGE REGULATOR BLOCK DIAGRAM

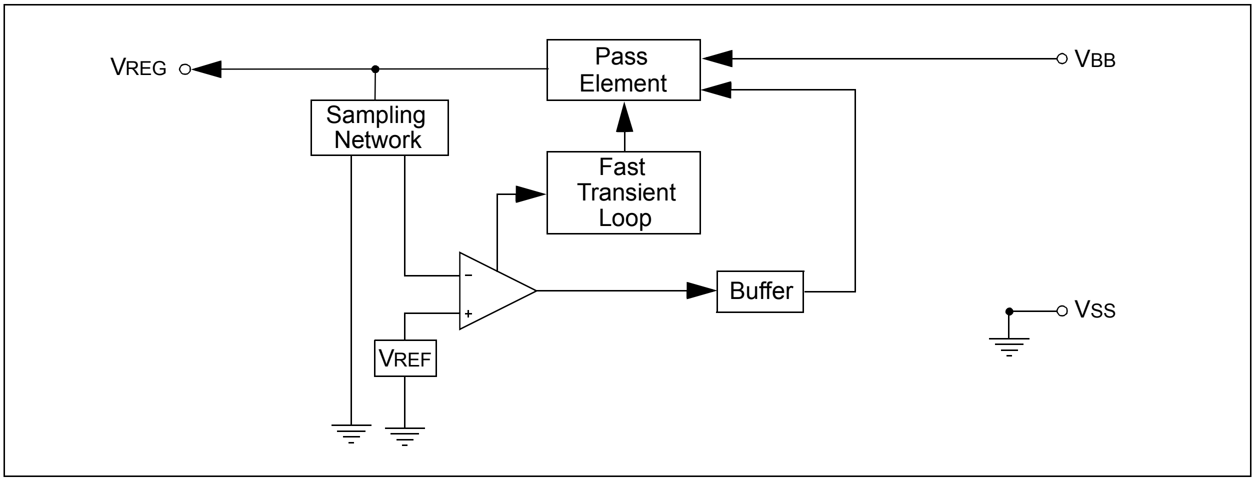

VREG
VBB
Pass Element
Sampling Network
Fast Transient Loop
–
+
Buffer
VREF
VSS

FIGURE 1-4: 5.0V V_{REG} VS. I_{REG} AT VBB = 12V

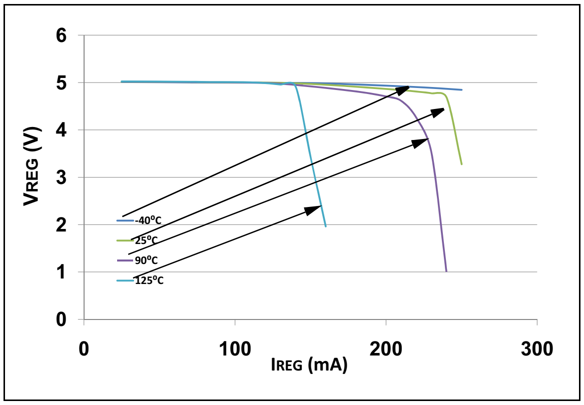


FIGURE 1-5: 3.3V V_{REG} VS. I_{REG} AT VBB = 12V

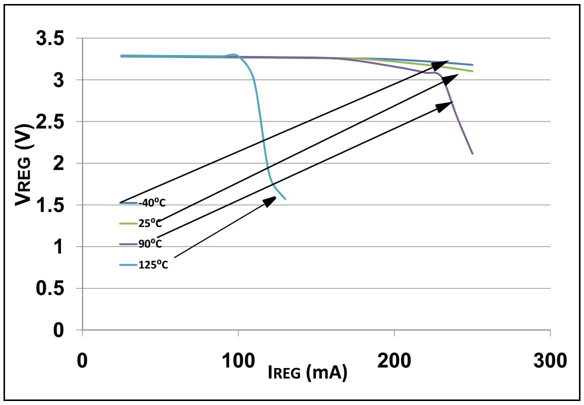
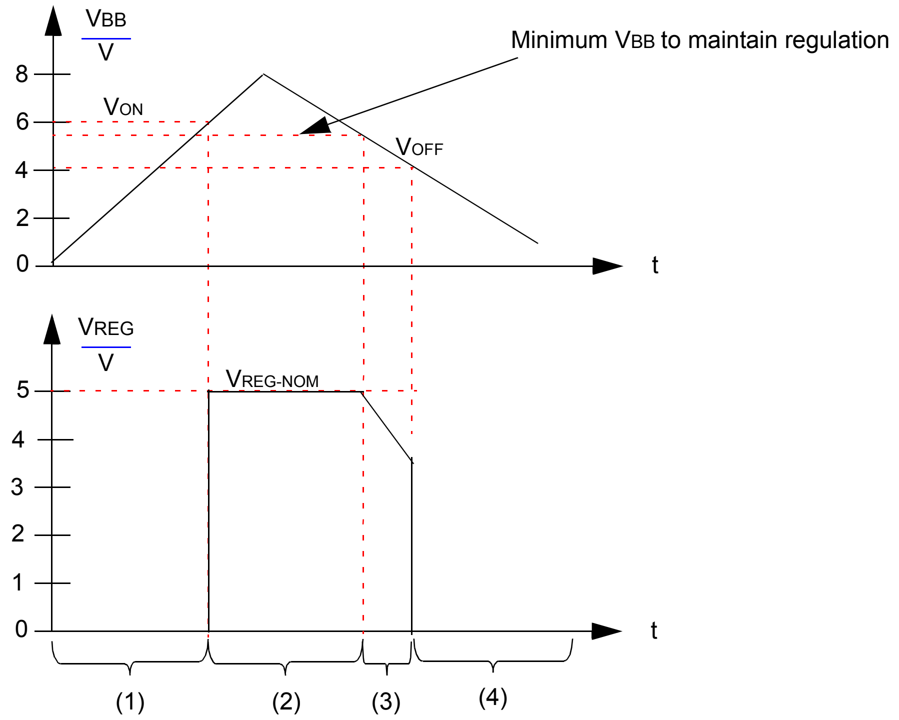


FIGURE 1-6: VOLTAGE REGULATOR OUTPUT ON POWER-ON RESET



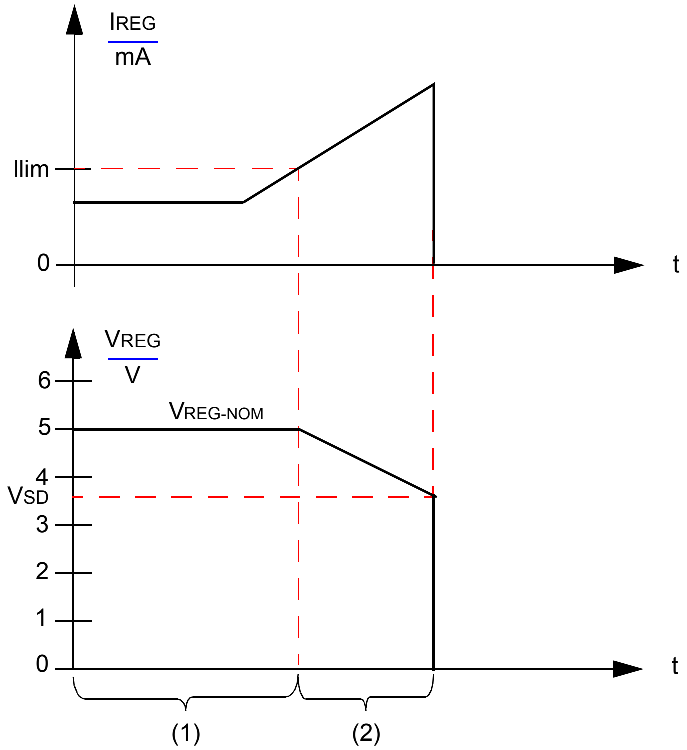
Note 1: Start-up, $V_{BB} < V_{ON}$, regulator off

2: $V_{BB} > V_{ON}$, regulator on

3: $V_{BB} \leq$ Minimum V_{BB} to maintain regulation

4: $V_{BB} < V_{OFF}$, regulator will turn off

FIGURE 1-7: VOLTAGE REGULATOR OUTPUT ON OVER-CURRENT SITUATION



Note 1: IREG less than Ilim, regulator on.

2: After IREG exceeds Ilim, voltage regulator output will be reduced until voltage regulator shutdown voltage V_{SD} is reached.

1.5 Optional External Protection

1.5.1 REVERSE BATTERY PROTECTION

An external reverse-battery-blocking diode should be used to provide polarity protection (see Figure 1-9).

1.5.2 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 43V transient suppressor (TVS) diode, between VBB and ground, with a transient protection resistor (RTP) in series with the battery supply and the VBB pin protects the device from power transients and ESD events greater than 43V (see Figure 1-9). The maximum value for the RTP protection resistor depends upon two parameters: the minimum voltage the part will start at, and the impacts of this RTP resistor on the VBB value, thus on the Bus recessive level and slopes.

This leads to a set of three equations to fulfill.

Equation 1-1 provides a max RTP value according to the minimum battery voltage the user wants.

Equation 1-2 provides a max RTP value according to the maximum error on the recessive level, thus VBB, since the part uses VBB as the reference value for the recessive level.

Equation 1-3 provides a max RTP value according to the maximum relative variation the user can accept on the slope when IREG varies.

Since both Equation 1-1 and Equation 1-2 must be fulfilled, the maximum allowed value for RTP is thus the smaller of the two values found when solving Equation 1-1 and Equation 1-2.

Usually Equation 1-1 gives the higher constraint (smaller value) for RTP as shown in the following example where VBATmin is 8V.

However, the user needs to check that the value found with Equation 1-1 fulfills Equation 1-2 and Equation 1-3 as well.

While this protection is optional, it should be considered as good engineering practice.

EQUATION 1-1:

$$R_{TP} \leq \frac{V_{BATmin} - 5.5V}{250mA}$$

$$5.5V = V_{OFF} + 1.0V$$

250 mA is the peak current at power-on when VBB =5.5V

Assume VBATMIN = 8V. Equation 1-1 shows 10Ω.

EQUATION 1-2:

R_{TP} <= ΔVRECESSIVE / IREGMAX.
ΔVRECESSIVE is the maximum variation tolerated on the recessive level

Assume ΔVRECESSIVE = 1V and IREGMAX = 50 mA Equation 1-2 shows 20Ω.

EQUATION 1-3:

$$R_{TP} \leq \frac{\Delta Slope \times (V_{BATmin} - 1V)}{I_{regmax}}$$

ΔSlope is the maximum variation tolerated on the slope level and IREGMAX is the maximum current the regulator will provide to the load.
VBATmin>VOFF + 1.0V.

Assume ΔSlope = 15%, VBATMIN = 8V and IREGMAX = 50 mA. Equation 1-2 shows 20Ω.

1.5.3 CBAT CAP

Selecting CBAT = 10* CREG is recommended, however, this leads to a high value cap. Lower values for CBAT cap can be used with respect to some rules. In any case, the voltage at the V_{BB} pin should remain above V_{OFF} when the device is turned on.

The current peak at start-up (due to the fast charge of the CREG and CBAT capacitors) may induce a significant drop on the VBB pin. This drop is proportional to the impedance of the VBAT connection (see Figure 1-9).

Assume that the VBAT connection is mainly inductive and resistive, and that the customer knows the resistive and inductive values of the connection.

The following formula gives an indication of the minimum value the customer should use for CBAT:

EQUATION 1-4:

$$\frac{C_{BAT}}{C_{REG}} = \sqrt{\frac{100L^2 + R_{tot}^2}{1 + L^2 + \frac{R_{tot}^2}{100}}}$$

where L is in mH and R_{tot} in Ω.
$R_{tot} = R_{line} + R_{TP}$.

Equation 1-4 allows lower CBAT/CREG values than the 10* ratio we recommend.

Assume that we have a good quality connection with RTOT = 0.1Ω and L = 0.1 mH.

Solving the equation gives CBAT/CREG = 1.

If we increase RTOT up to 1Ω, the result becomes CBAT/CREG = 1.4.

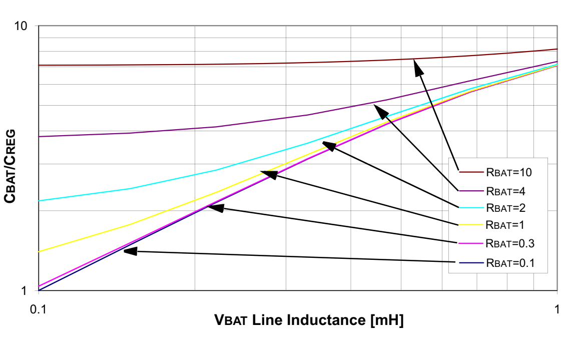
But if the connection is highly resistive or highly inductive (poor connection), the CBAT/CREG ratio greatly increases.

Highly inductive connection: RTOT = 0.1Ω and L = 1 mH: the CBAT/CREG ratio increases to 7!

Highly resistive connection: RTOT = 10Ω and L = 0.1 mH: again the CBAT/CREG ratio increases to 7!

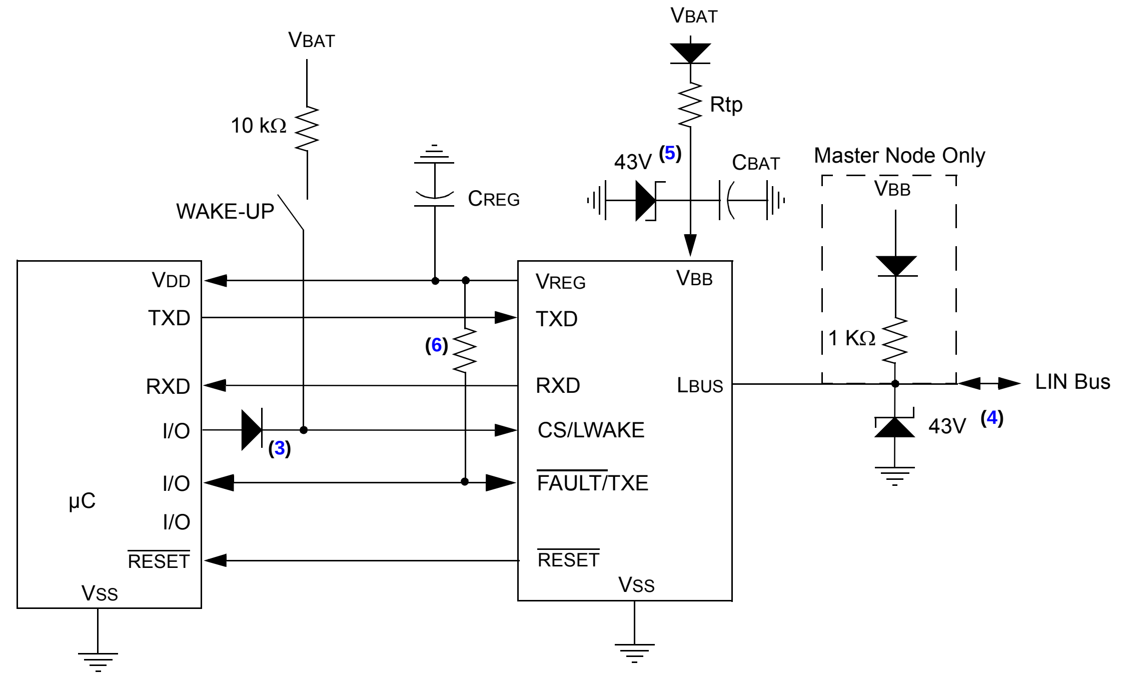
Figure 1-8 shows the minimum recommended CBAT/CREG ratio as a function of the impedance of the VBAT connection.

FIGURE 1-8: Minimum Recommended CBAT/CREG Ratio



1.6 Typical Applications

FIGURE 1-9: TYPICAL APPLICATION CIRCUIT


VBAT
10 kΩ
WAKE-UP
CREG
VBAT
Rtp
43V (5)
CBAT
Master Node Only
VBB
1 KΩ
LIN Bus
43V (4)
VDD
TXD
RXD
I/O
I/O
I/O
μC
RESET
VSS
(6)
(3)
VREG
VBB
TXD
RXD
LBUS
CS/LWAKE
FAULT/TXE
RESET
VSS

Note 1: CREG, the load capacitor, should be ceramic or tantalum rated for extended temperatures, 1.0-22 µF. See Figure 2-1 for selecting the correct ESR.

2: CBAT is the filter capacitor for the external voltage supply. Typically 10 * CREG, with no ESR restriction. See Figure 1-8 to select the minimum recommended value for CBAT. The RTP value is added to the line resistance.

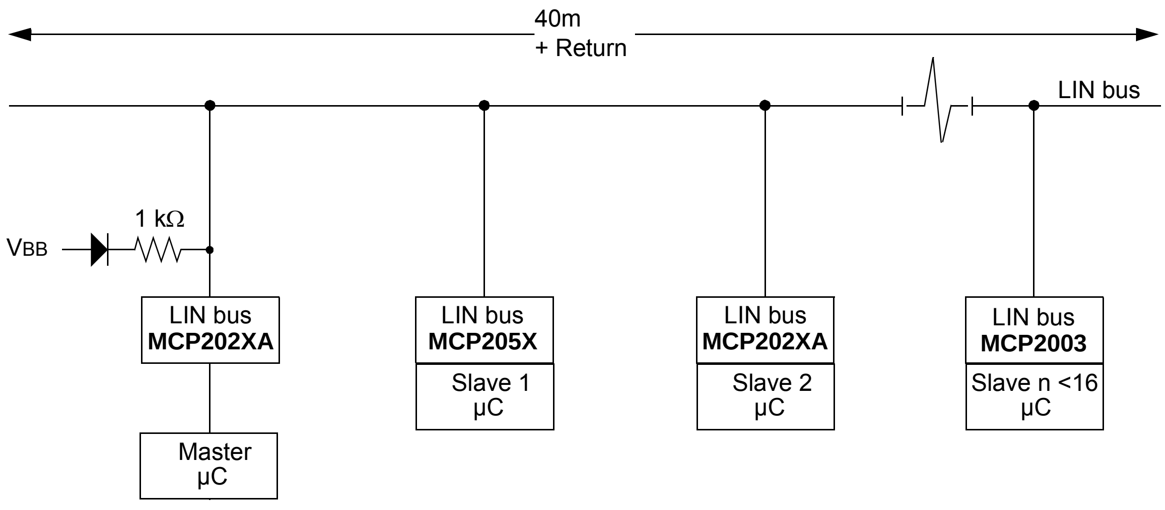
3: This diode is only needed if CS/LWAKE is connected to VBAT supply.

4: Transient suppressor diode. Vclamp L = 43V.

5: This component is for additional load dump protection.

6: An external 10 kΩ resistor is recommended for some applications.

FIGURE 1-10: Typical Lin Network Configuration


40m
+ Return
LIN bus
VBB
1 kΩ
LIN bus
MCP202XA
Master
μC
LIN bus
MCP205X
Slave 1
μC
LIN bus
MCP202XA
Slave 2
μC
LIN bus
MCP2003
Slave n <16
μC

1.7 ICSP™ Considerations

The following should be considered when the MCP2021A/2A is connected to pins supporting in-circuit programming:

- Power used for programming the microcontroller can be supplied from the programmer, or from the MCP2021A/2A.
- The voltage on the pin VREG should not exceed the maximum value of VREG in **Section 2.3 "DC Specifications"**.

NOTES:

2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings†

VIN DC Voltage on RXD, and $\overline{\text{RESET}}$	-0.3V to VREG+0.3
VIN DC Voltage on TXD, CS/LWAKE, $\overline{\text{FAULT}}$/TXE	-0.3 to +40V
VBB Battery Voltage, continuous, non-operating (**Note 1**)	-0.3 to +40V
VBB Battery Voltage, non-operating (LIN bus recessive, no regulator load, t < 60s) (Note 2)	-0.3 to +43V
VBB Battery Voltage, transient ISO 7637 Test 1	-100V
VBB Battery Voltage, transient ISO 7637 Test 2a	+75V
VBB Battery Voltage, transient ISO 7637 Test 3a	-150V
VBB Battery Voltage, transient ISO 7637 Test 3b	+100V
VLBUS Bus Voltage, continuous	-18 to +30V
VLBUS Bus Voltage, transient (**Note 3**)	-27 to +43V
ILBUS Bus Short Circuit Current Limit	200 mA
ESD protection on LIN, VBB (IEC 61000-4-2) (**Note 4**)	±15 KV
ESD protection on LIN, VBB (Human Body Model) (**Note 5**)	±8 KV
ESD protection on all other pins (Human Body Model) (**Note 5**)	±4 KV
ESD protection on all pins (Charge Device Model) (**Note 6**)	±1500V
ESD protection on all pins (Machine Model) (**Note 7**)	±200V
Maximum Junction Temperature	150°C
Storage Temperature	-65 to +150°C

Note 1: LIN 2.x compliant specification.
2: SAE J2602-2 compliant specification.
3: ISO 7637/1 load dump compliant (t < 500 ms).
4: According to IEC 61000-4-2, 330 ohm, 150 pF and Transceiver EMC Test Specifications [2] to [4].
5: According to AEC-Q100-002 / JESD22-A114.
6: According to AEC-Q100-011B.
7: According to AEC-Q100-003 / JESD22-A115.

† **NOTICE**: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.2 Nomenclature Used in This Document

Some terms and names used in this data sheet deviate from those referred to in the LIN specifications. Equivalent values are shown below.

LIN 2.1 Name	Term used in the following tables	
VBAT	*not used*	ECU operating voltage
VSUP	VBB	Supply voltage at device pin
VBUS_LIM	ISC	Current limit of Driver
VBUSREC	VIH(LBUS)	Recessive state
VBUSDOM	VIL(LBUS)	Dominant state

2.3 DC Specifications

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V T_A = -40°C to +125°C					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power						
V_{BB} Quiescent Operating Current	I_{BBQ}	—	—	200	µA	I_{OUT} = 0 mA, L_{BUS} recessive V_{REG} = 5.0V
		—	—	200	µA	I_{OUT} = 0 mA, L_{BUS} recessive V_{REG} = 3.3V
V_{BB} READY Current	I_{BBRD}	—	—	100	µA	I_{OUT} = 0 mA, L_{BUS} recessive V_{REG} = 5.0V
		—	—	100	µA	I_{OUT} = 0 mA, L_{BUS} recessive V_{REG} = 3.3V
V_{BB} Transmitter-off Current	I_{BBTO}	—	—	100	µA	With voltage regulator on, transmitter off, receiver on, $\overline{\text{FAULT}}$/TXE = V_{IL}, CS = V_{IH},V_{REG} = 5.0V
		—	—	100	µA	With voltage regulator on, transmitter off, receiver on, $\overline{\text{FAULT}}$/TXE = V_{IL}, CS = V_{IH},V_{REG} = 3.3V
V_{BB} Power-down Current	I_{BBPD}	—	4.5	8	µA	With voltage regulator powered-off, receiver on and transmitter off, $\overline{\text{FAULT}}$/TXE = V_{IH}, TXD = V_{IH}, CS = V_{IL})
V_{BB} Current with V_{SS} Floating	$I_{BBNOGND}$	-1	—	1	mA	V_{BB} = 12V, GND to V_{BB}, VLIN = 0-18V
Microcontroller Interface						
High-Level Input Voltage (T_{XD}, $\overline{\text{FAULT}}$/TXE)	V_{IH}	2.0	—	V_{REG} +0.3	V	
Low-Level Input Voltage (T_{XD}, $\overline{\text{FAULT}}$/TXE)	V_{IL}	-0.3	—	0.8	V	
High-Level Input Current (T_{XD}, $\overline{\text{FAULT}}$/TXE)	I_{IH}	-2.5	—	0.4	µA	Input voltage = 4.0V. ~800 kΩ internal adaptive pull-up
Low-Level Input Current (T_{XD}, $\overline{\text{FAULT}}$/TXE)	I_{IL}	-10	—	—	µA	Input voltage = 0.5V. ~800 kΩ internal adaptive pull-up
High-Level Input Voltage (CS/LWAKE)	V_{IH}	2.0	—	V_{BB}	V	Through a current-limiting resistor
Low-Level Input Voltage (CS/LWAKE)	V_{IL}	-0.3	—	0.8	V	
High-Level Input Current (CS/LWAKE)	I_{IH}	—	—	8.0	µA	Input voltage = 0.8V_{REG} ~1.3 MΩ internal pull-down to V_{SS}

2.3 DC Specifications (Continued)

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V T_A = -40°C to +125°C					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Low-Level Input Current (CS/LWAKE)	I_{IL}	—	—	5.0	µA	Input voltage = $0.2V_{REG}$ ~1.3 MΩ internal pull-down to V_{SS}
Low-Level Output Voltage (R_{XD})	V_{OLRXD}	—	—	$0.2V_{REG}$	V	I_{OL} = 2 mA
High-Level Output Voltage (R_{XD})	V_{OHRXD}	$0.8V_{REG}$	—	—	V	I_{OH} = 2 mA
Low-Level Output Voltage ($\overline{\text{FAULT}}$/TXE)	V_{OLOD}	—		1.0	V	I_{OL} = 4 mA
Low-Level Output Voltage ($\overline{\text{RESET}}$)	V_{OLRST}	—	—	1.0	V	I_{OL} = 4 mA

2.3 DC Specifications (Continued)

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: VBB = 6.0V to 18.0V TA = -40°C to +125°C					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Bus Interface (DC specifications are for a VBB range of 6.0 to 18.0V)						
High-Level Input Voltage	VIH(LBUS)	0.6 VBB	—	—	V	Recessive state
Low-Level Input Voltage	VIL(LBUS)	-8	—	0.4 VBB	V	Dominant state
Input Hysteresis	VHYS	—	—	0.175 VBB	V	VIH(LBUS) – VIL(LBUS)
Low-Level Output Current	IOL(LBUS)	40	—	200	mA	Output voltage = 0.1 VBB, VBB = 12V
Pull-up Current on Input	IPU(LBUS)	-180	—	-72	µA	~30 kΩ internal pull-up @ VIH (LBUS) = 0.7 VBB, VBB=12V
Short Circuit Current Limit	ISC	50	—	200	mA	**(Note 1)**
High-Level Output Voltage	VOH(LBUS)	0.8 VBB	—	VBB	V	
Driver Dominant Voltage	V_LOSUP	—	—	1.1	V	VBB = 7.3V, RLOAD = 1000Ω
Driver Dominant Voltage	V_HISUP	—	—	1.2	V	VBB = 18V, RLOAD = 1000Ω
Input Leakage Current (at the receiver during dominant bus level)	IBUS_PAS_DOM	-1	—	—	mA	Driver off, VBUS = 0V, VBB = 12V
Input Leakage Current (at the receiver during recessive bus level)	IBUS_PAS_REC	-20	—	20	µA	Driver off, 8V < VBB < 18V 8V < VBUS < 18V VBUS ≥ VBB
Leakage Current (disconnected from ground)	IBUS_NO_GND	-10	—	+10	µA	GNDDEVICE = VBB, 0V < VBUS < 18V, VBB = 12V
Leakage Current (disconnected from VBB)	IBUS_NO_PWR	-10	—	+10	µA	VBB = GND, 0 < VBUS < 18V
Receiver Center Voltage	VBUS_CNT	0.475 VBB	0.5 VBB	0.525 VBB	V	VBUS_CNT = (VIL (LBUS) + VIH (LBUS))/2
Slave Termination	RSLAVE	20	30	47	kΩ	(**Note 2**)
Capacitance of slave node	CSLAVE			50	pF	(**Note 2**)
Wake-Up Voltage Threshold on LIN Bus	$V_{WK(LBUS)}$	—	—	3.4	V	Wake up from POWER-DOWN mode (**Note 3**)

Note 1: Internal current limited. 2.0 ms maximum recovery time (RLBUS = 0Ω, TX = 0, VLBUS = VBB).

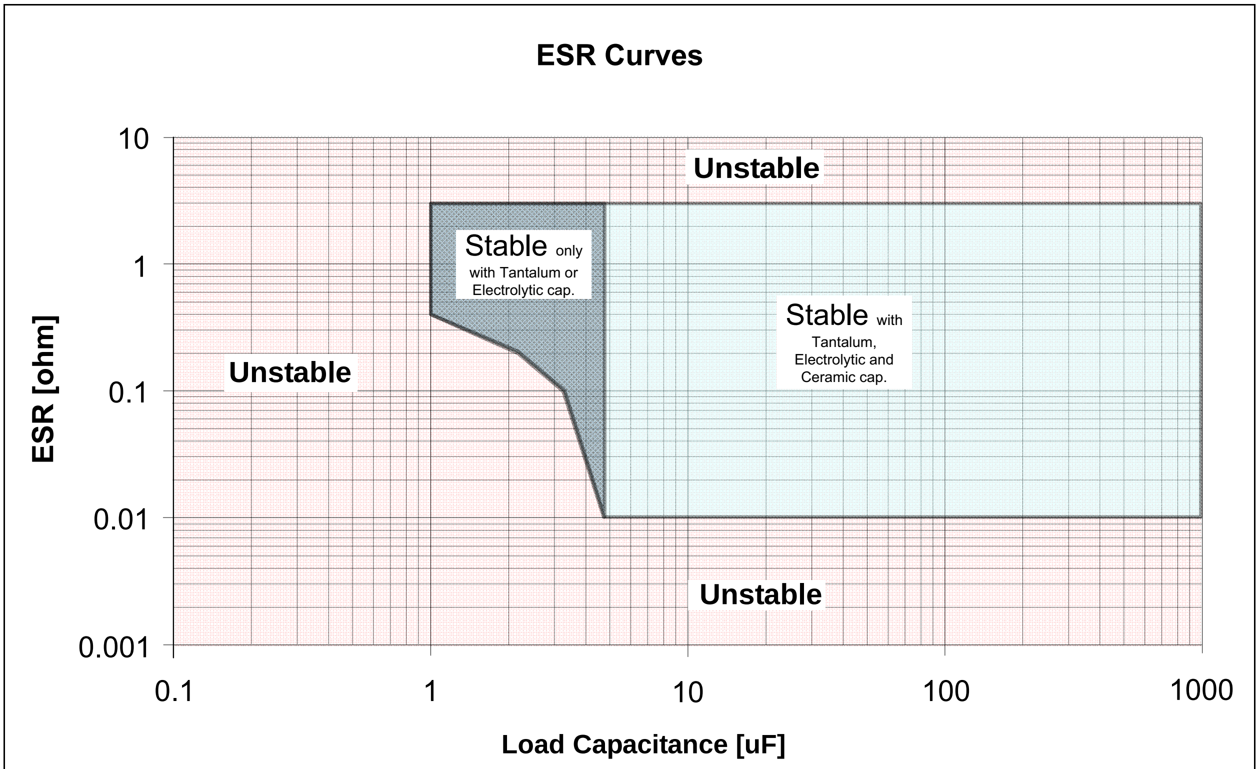
2: For design guidance only, not tested.

3: In POWER DOWN mode, normal LIN recessive/dominant threshold is disabled; $V_{WK(LBUS)}$ is used to detect bus activities.

2.3 DC Specification (Continued)

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V T_A = -40°C to +125°C $C_{LOADREG}$ = 10 µF					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Voltage Regulator - 5.0V						
Output Voltage Range	V_{REG}	4.85	5.00	5.15	V	0 mA < I_{OUT} < 70 mA
Line Regulation	ΔV_{OUT1}	—	10	50	mV	I_{OUT} = 1 mA, 6.0V < V_{BB} < 18V
Load Regulation	ΔV_{OUT2}	—	10	50	mV	5 mA < I_{OUT} <70 mA 6.0V < V_{BB} < 12V
Power Supply Ripple Reject	PSRR	—	—	50	dB	1 V_{PP} @10-20 kHz I_{LOAD} = 20 mA
Output Noise Voltage	eN	—	—	100	μV_{RMS}	10 Hz – 40 MHz C_{FILTER} = 10 µf, C_{BP} = 0.1 µf, I_{LOAD} = 20 mA
Shutdown Voltage Threshold	V_{SD}	3.5	—	4.0	V	See **Figure 1-7** (**Note 1**)
Input Voltage to Turn-Off Output	V_{OFF}	3.9	—	4.5	V	
Input Voltage to Turn-On Output	V_{ON}	5.25	—	6.0	V	
Voltage Regulator - 3.3V						
Output Voltage	V_{REG}	3.20	3.30	3.40	V	0 mA < I_{OUT} < 70 mA
Line Regulation	ΔV_{OUT1}	—	10	50	mV	I_{OUT} = 1 mA, 6.0V < V_{BB} < 18V
Load Regulation	ΔV_{OUT2}	—	10	50	mV	5 mA < I_{OUT} < 70 mA, 6.0V < V_{BB} < 12V
Power Supply Ripple Reject	PSRR	—	—	50	dB	1 V_{PP} @10-20 kHz , I_{LOAD} = 20 mA
Output Noise Voltage	eN	—	—	100	$\mu V_{RMS} / \sqrt{Hz}$	10 Hz – 40 MHz C_{FILTER} = 10 µf, C_{BP} = 0.1 µf, I_{LOAD} = 20 mA
Shutdown Voltage	V_{SD}	2.5	—	2.7	V	See **Figure 1-7** (**Note 1**)
Input Voltage to Turn-Off Output	V_{OFF}	3.9	—	4.5	V	
Input Voltage to Turn-On Output	V_{ON}	5.25	—	6	V	
Note 1: For design guidance only, not tested.						

FIGURE 2-1: ESR CURVES FOR LOAD CAPACITOR SELECTION



Note: The graph shows the minimum required capacitance after derating due to tolerance, temperature and voltage.

2.4 AC Specification

AC CHARACTERISTICS	V_{BB} = 6.0V to 18.0V; T_A = -40°C to +125°C					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Bus Interface - Constant Slope Time Parameters (DC specifications are for a V_{BB} range of 6.0 to 18.0V)						
Slope rising and falling edges	t_{SLOPE}	3.5	—	22.5	µs	7.3V <= V_{BB} <= 18V
Propagation Delay of Transmitter	$t_{TRANSPD}$	—	—	5.0	µs	$t_{TRANSPD}$ = max ($t_{TRANSPDR}$ or $t_{TRANSPDF}$)
Propagation Delay of Receiver	t_{RECPD}	—	—	6.0	µs	t_{RECPD} = max (t_{RECPDR} or t_{RECPDF})
Symmetry of Propagation Delay of Receiver rising edge w.r.t. falling edge	t_{RECSYM}	-2.0	—	2.0	µs	t_{RECSYM} = max (t_{RECPDF} – t_{RECPDR}) R_{RXD} 2.4 kΩ to V_{CC}, C_{RXD} 20 pF
Symmetry of Propagation Delay of Transmitter rising edge w.r.t. falling edge	$t_{TRANSSYM}$	-2.0	—	2.0	µs	$t_{TRANSSYM}$ = max ($t_{TRANSPDF}$ - $t_{TRANSPDR}$)
Bus dominant time-out time	$t_{TO(LIN)}$	—	25	—	mS	
Time to sample FAULT/TXE for bus conflict reporting	t_{FAULT}	—	—	32.5	µs	t_{FAULT} = max ($t_{TRANSPD}$ + t_{SLOPE} + t_{RECPD})
Duty Cycle 1 @20.0 kbit/sec		.396	—	—	%t_{BIT}	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.744 x V_{BB}, $TH_{DOM(MAX)}$ = 0.581 x V_{BB}, V_{BB} =7.0V - 18V; t_{BIT} = 50 µs. D1 = $t_{BUS\_REC(MIN)}$ / 2 x t_{BIT})
Duty Cycle 2 @20.0 kbit/sec		—	—	.581	%t_{BIT}	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.284 x V_{BB}, $TH_{DOM(MAX)}$ = 0.422 x V_{BB}, V_{BB} =7.6V - 18V; t_{BIT} = 50 µs. D2 = $t_{BUS\_REC(MAX)}$ / 2 x t_{BIT})
Duty Cycle 3 @10.4 kbit/sec		.417	—	—	%t_{BIT}	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.778 x V_{BB}, $TH_{DOM(MAX)}$ = 0.616 x V_{BB}, V_{BB} =7.0V - 18V; t_{BIT} = 96 µs. D3 = $t_{BUS\_REC(MIN)}$ / 2 x t_{BIT})
Duty Cycle 4 @10.4 kbit/sec		—	—	.590	%t_{BIT}	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.251 x V_{BB}, $TH_{DOM(MAX)}$ = 0.389 x V_{BB}, V_{BB} =7.6V - 18V; t_{BIT} = 96 µs. D4 = $t_{BUS\_REC(MAX)}$ / 2 x t_{BIT})

2.4 AC Specification (Continued)

AC CHARACTERISTICS	V_{BB} = 6.0V to 18.0V; T_A = -40°C to +125°C					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Voltage Regulator						
Bus Activity Debounce time	t_{BDB}	30	80	250	µs	
Bus Activity to Voltage Regulator Enabled	$t_{BACTIVE}$	35	—	200	µs	
Voltage Regulator Enabled to Ready	t_{VEVR}	300	—	1200	µs	(Note 1)
Chip Select to Ready mode	t_{CSR}	—	—	230	µs	
Chip Select to Power-Down	t_{CSPD}	—	—	330	µs	(Note 2)
Short Circuit to Shut-Down	$t_{SHUTDOWN}$	20	—	100	µs	
$\overline{\text{RESET}}$ Timing						
V_{REG} OK detect to $\overline{\text{RESET}}$ inactive	t_{RPU}	—	—	60	µs	
V_{REG} not OK detect to $\overline{\text{RESET}}$ active	t_{RPD}	—	—	60	µs	

Note 1: Time depends on external capacitance and load. Test condition: C_{REG} = 4.7 µF, no resistor load.

2: For design guidance only, not tested.

2.5 Thermal Specifications

THERMAL CHARACTERISTICS					
Parameter	**Symbol**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Recovery Temperature	$\theta_{RECOVERY}$	+140	—	°C	
Shutdown Temperature	$\theta_{SHUTDOWN}$	+150	—	°C	
Short Circuit Recovery Time	t_{THERM}	1.5	5.0	ms	
Thermal Package Resistances					
Thermal Resistance, 8L-PDIP	θ_{JA}	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	149.5	—	°C/W	
Thermal Resistance, 8L-DFN	θ_{JA}	48	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	100	—	°C/W	

Note 1: The maximum power dissipation is a function of T_{JMAX}, Θ_{JA} and ambient temperature T_A. The maximum allowable power dissipation at an ambient temperature is $P_D = (T_{JMAX} - T_A)\ \Theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the MCP2021A/2A will go into thermal shutdown.

2.6 Timing Diagrams and Specifications

FIGURE 2-2: BUS TIMING DIAGRAM

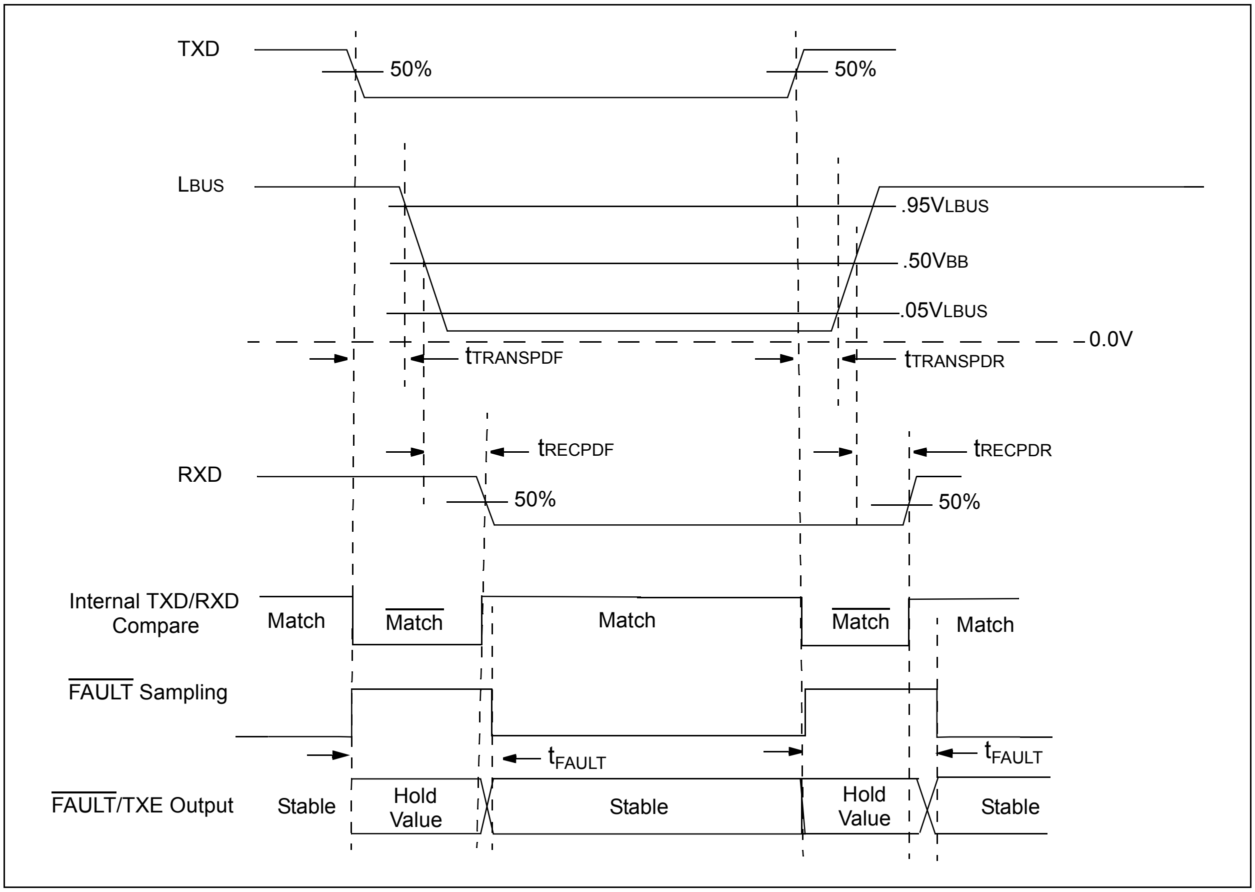

TXD
50%
50%
LBUS
.95VLBUS
.50VBB
.05VLBUS
0.0V
tTRANSPDF
tTRANSPDR
tRECPDF
tRECPDR
RXD
50%
50%
Internal TXD/RXD Compare
Match
$\overline{\text{Match}}$
Match
$\overline{\text{Match}}$
Match
$\overline{\text{FAULT}}$ Sampling
t_{FAULT}
t_{FAULT}
$\overline{\text{FAULT}}$/TXE Output
Stable
Hold Value
Stable
Hold Value
Stable

FIGURE 2-3: REGULATOR BUS WAKE TIMING DIAGRAM

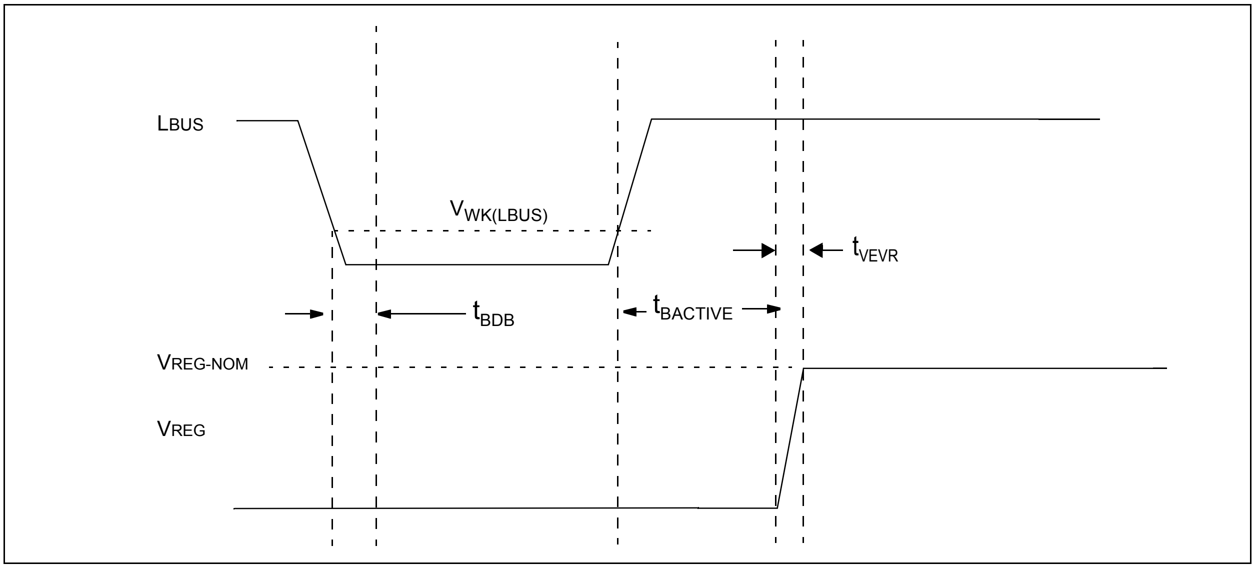

LBUS
$V_{WK(LBUS)}$
t_{VEVR}
t_{BDB}
$t_{BACTIVE}$
VREG-NOM
VREG

FIGURE 2-4: CS/LWAKE, REGULATOR AND $\overline{\text{RESET}}$ TIMING DIAGRAM

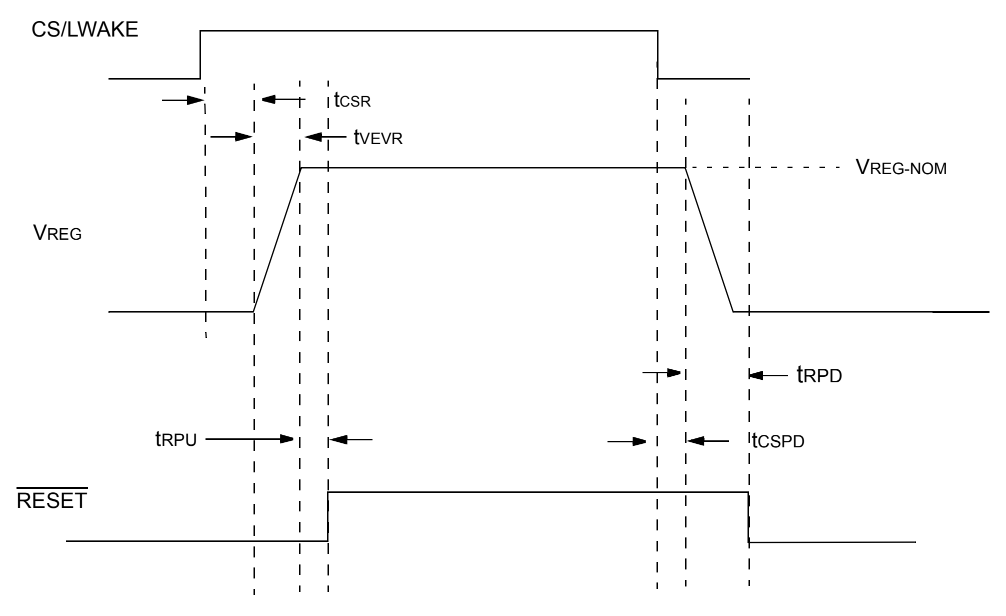

CS/LWAKE
tCSR
tVEVR
VREG-NOM
VREG
tRPD
tRPU
tCSPD
RESET

FIGURE 2-5: TYPICAL IBBQ VS. TEMPERATURE - 5.0V

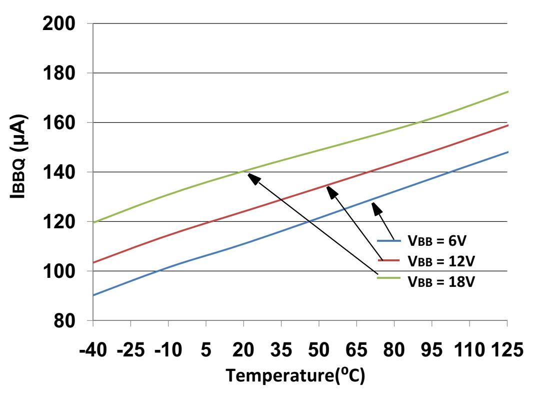


FIGURE 2-6: TYPICAL IBBTO VS. TEMPERATURE - 5.0V

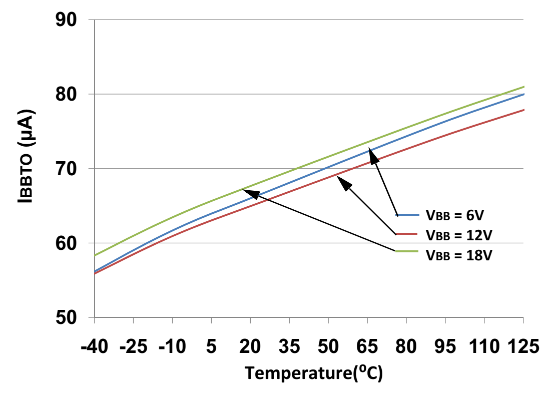


FIGURE 2-7: TYPICAL IPD VS. TEMPERATURE - 5.0V

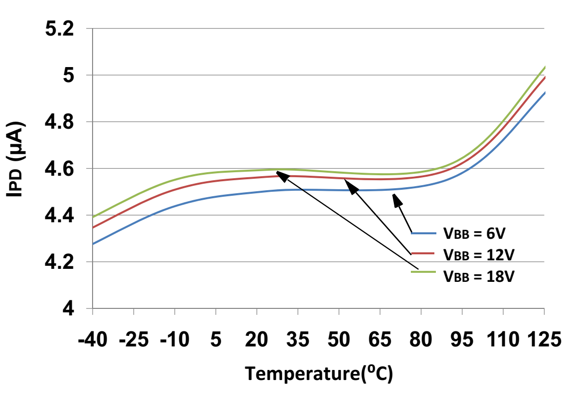


FIGURE 2-8: TYPICAL I_{BBQ}VS. TEMPERATURE - 3.3V

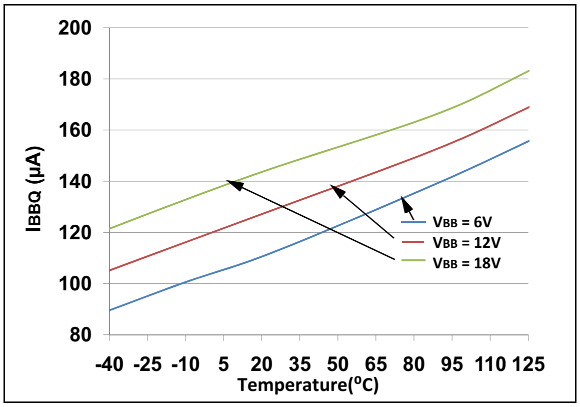


FIGURE 2-9: TYPICAL I_{BBTO} VS. TEMPERATURE - 3.3V

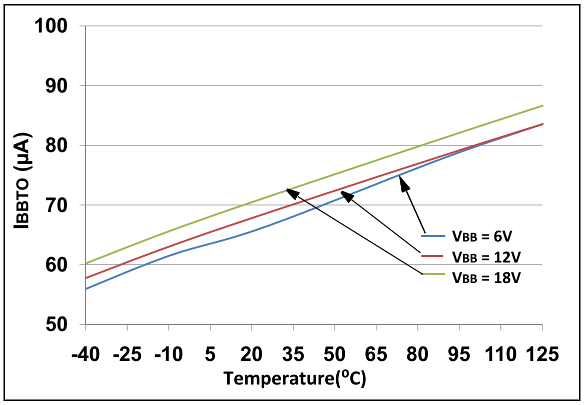
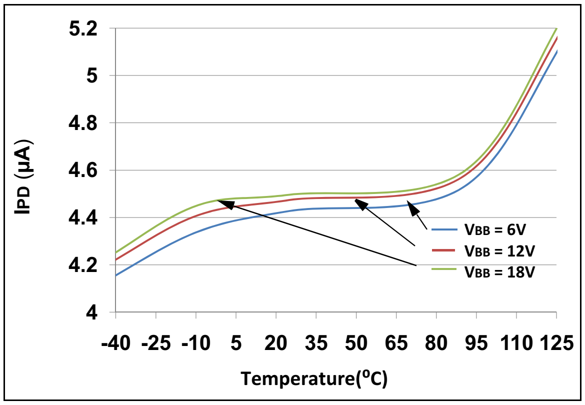


FIGURE 2-10: TYPICAL I_{PD} VS. TEMPERATURE - 3.3V

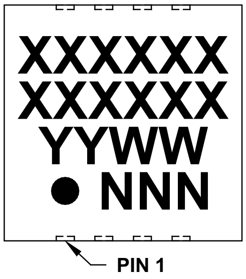


NOTES:

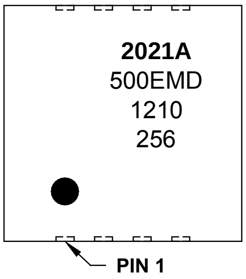
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

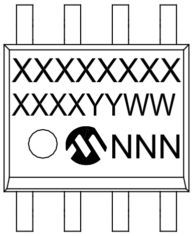
8-Lead DFN (4x4x0.9 mm) **(MCP2021A)**


XXXXXX
XXXXXX
YYWW
NNN
PIN 1

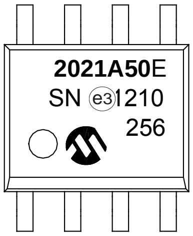
Example


2021A
500EMD
1210
256
PIN 1

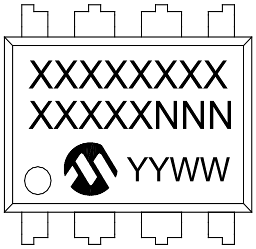
8-Lead SOIC (150 mil) **(MCP2021A)**


XXXXXXXX
XXXXYYWW
NNN

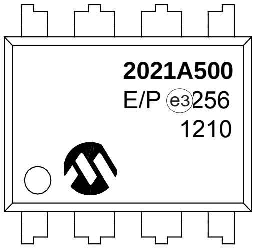
Example:


2021A50E
SN e3 1210
256

8-Lead PDIP (300 mil) **(MCP2021A)**


XXXXXXXX
XXXXXNNN
YYWW

Example

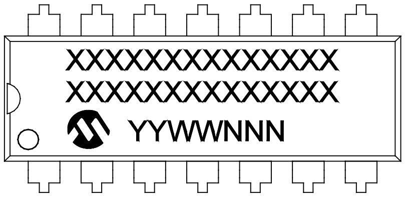

2021A500
E/P e3 256
1210

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

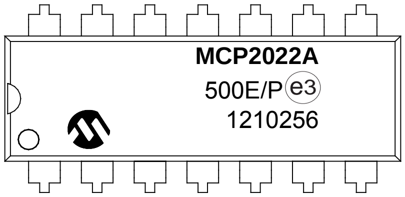
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

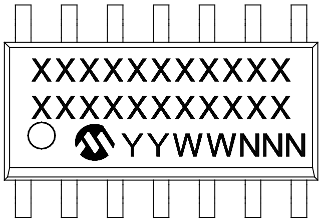
14-Lead PDIP (300 mil) **(MCP2022A)**


XXXXXXXXXXXXXX
XXXXXXXXXXXXXX
YYWWNNN

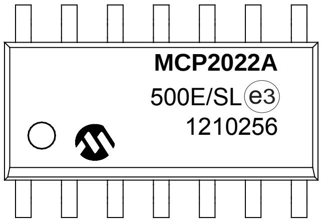
Example


MCP2022A
500E/P e3
1210256

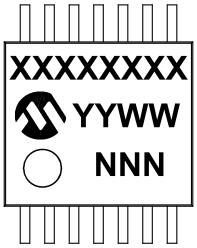
14-Lead SOIC (.150”) **(MC2022A)**


XXXXXXXXXXX
XXXXXXXXXXX
YYWWNNN

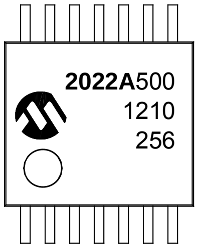
Example


MCP2022A
500E/SL e3
1210256

14-Lead TSSOP **(MCP2022A)**


XXXXXXXX
YYWW
NNN

Example

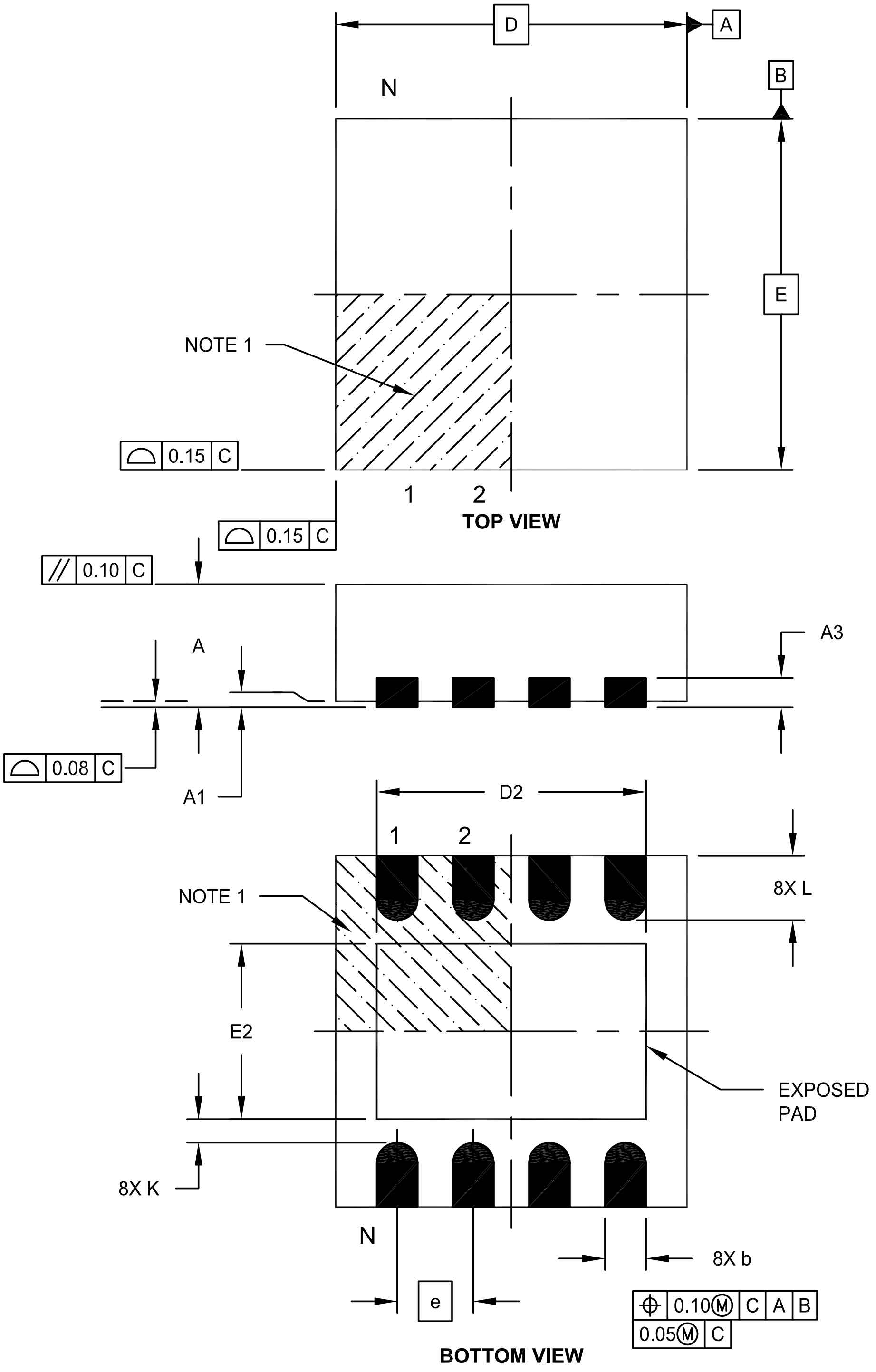

2022A500
1210
256

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

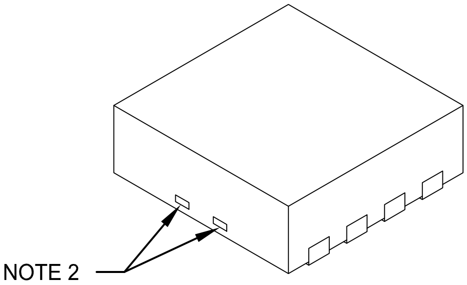
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


D
A
B
N
E
NOTE 1
0.15 C
1
2
TOP VIEW
0.15 C
0.10 C
A
A3
0.08 C
A1
D2
1
2
8X L
NOTE 1
E2
EXPOSED PAD
8X K
N
8X b
e
0.10Ⓜ C A B
0.05Ⓜ C
BOTTOM VIEW

Microchip Technology Drawing C04-131E Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.80 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	4.00 BSC		
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Width	E	4.00 BSC		
Exposed Pad Length	D2	3.40	3.50	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

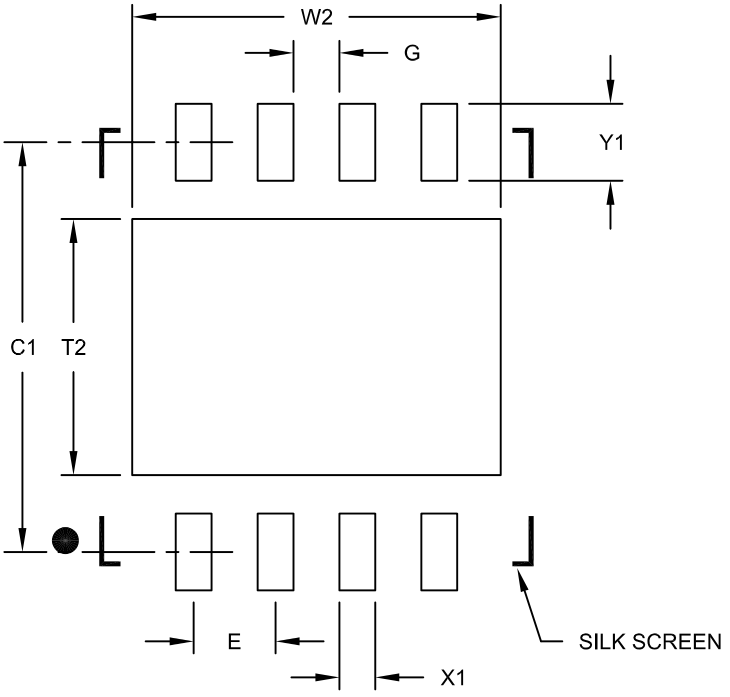
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MD) - 4x4x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Optional Center Pad Width	W2			3.60
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.45		

Notes:

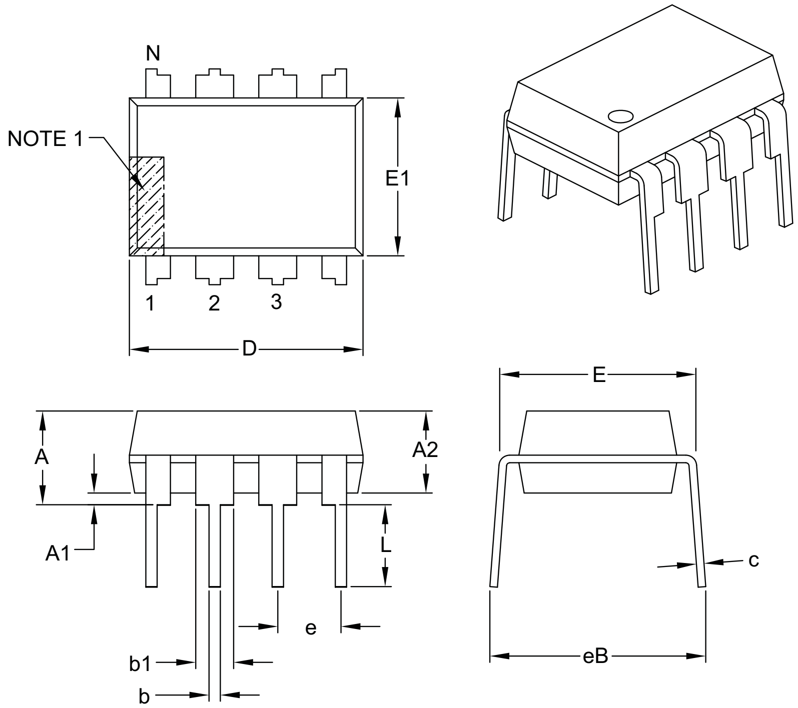
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2131C

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

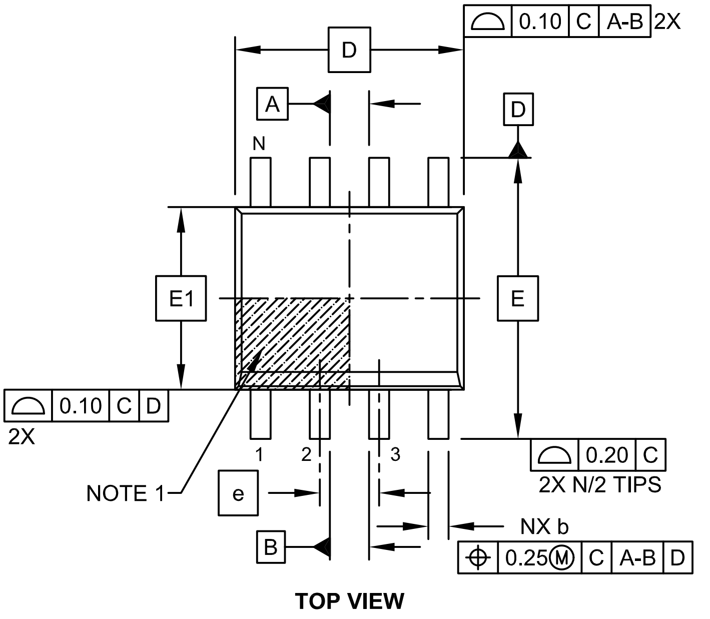
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

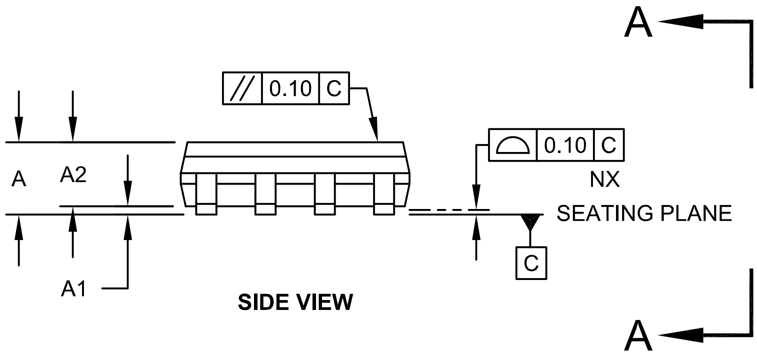
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

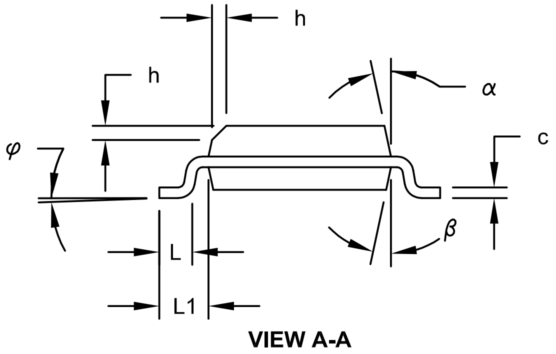
Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


D
0.10 C A-B 2X
A
D
N
E1
E
0.10 C D
2X
1
2
3
0.20 C
2X N/2 TIPS
NOTE 1
e
NX b
B
0.25Ⓜ C A-B D
TOP VIEW

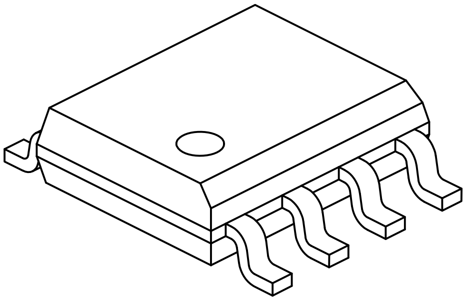

A
0.10 C
0.10 C
NX
A
A2
SEATING PLANE
C
A1
SIDE VIEW
A


h
h
α
φ
c
β
L
L1
VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

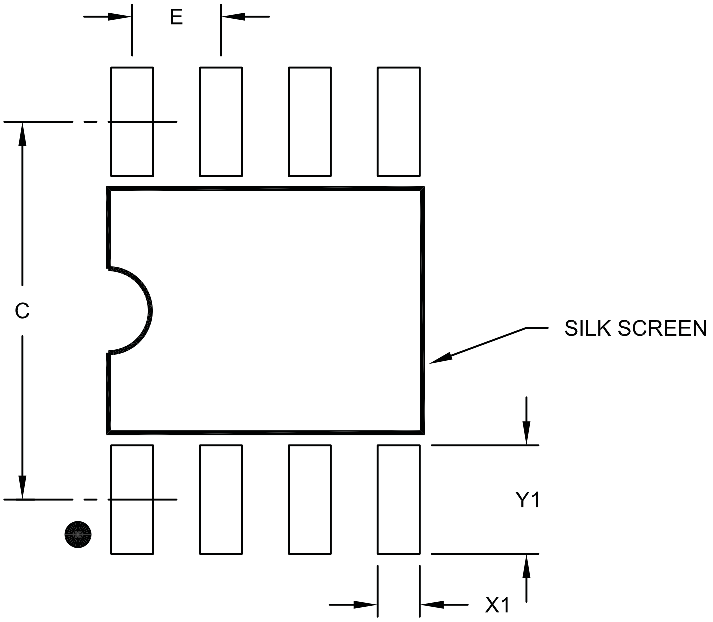
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

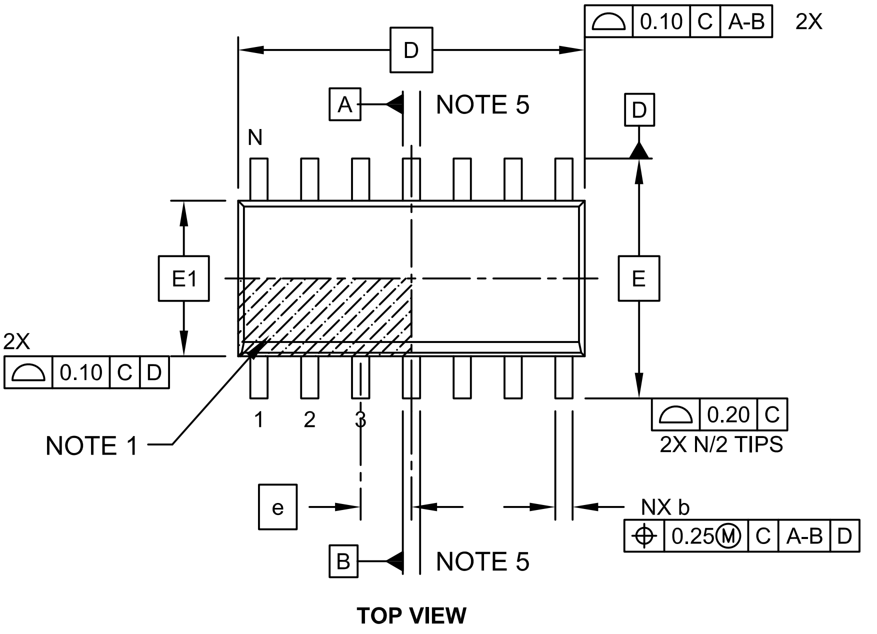
Notes:

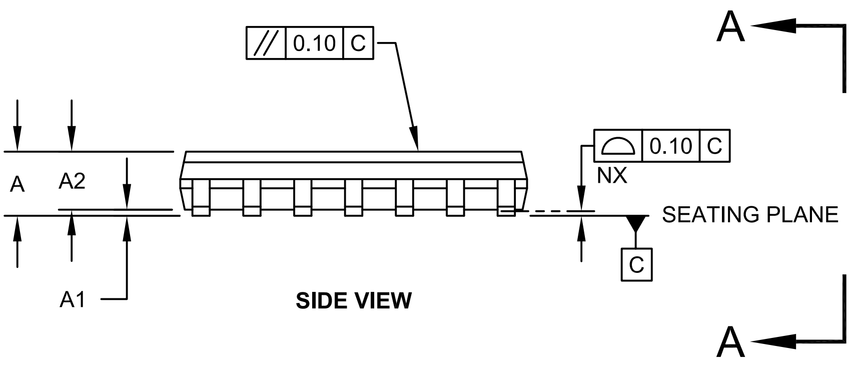
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

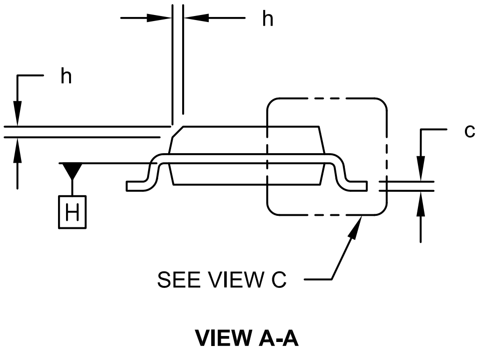
Microchip Technology Drawing No. C04-2057A

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging


0.10 C A-B 2X
D
A NOTE 5
D
N
E1
E
2X
0.10 C D
NOTE 1
1 2 3
0.20 C
2X N/2 TIPS
e
NX b
0.25 M C A-B D
B NOTE 5
TOP VIEW

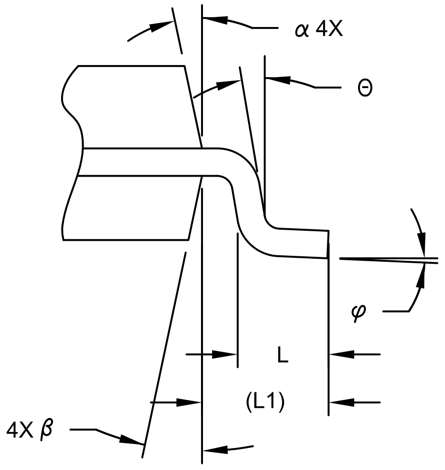

0.10 C
A
0.10 C
NX
A A2
SEATING PLANE
C
A1
SIDE VIEW
A


h
h
c
H
SEE VIEW C
VIEW A-A

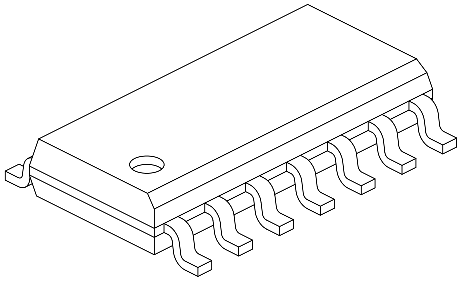
Microchip Technology Drawing No. C04-065C Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

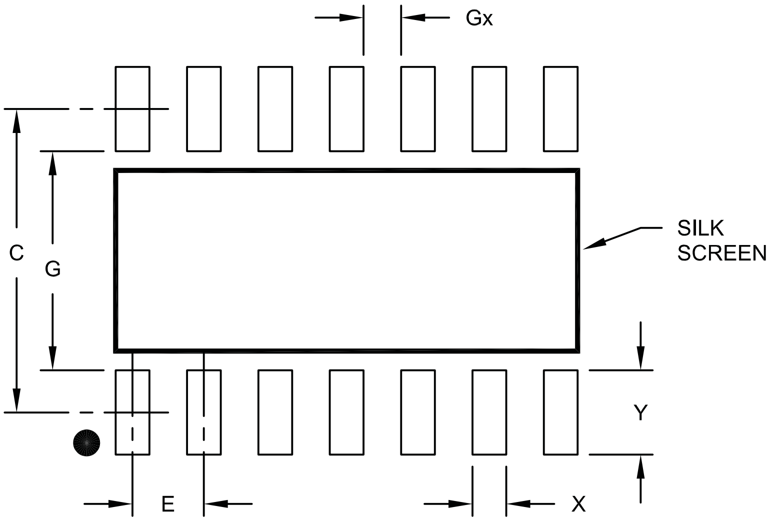
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

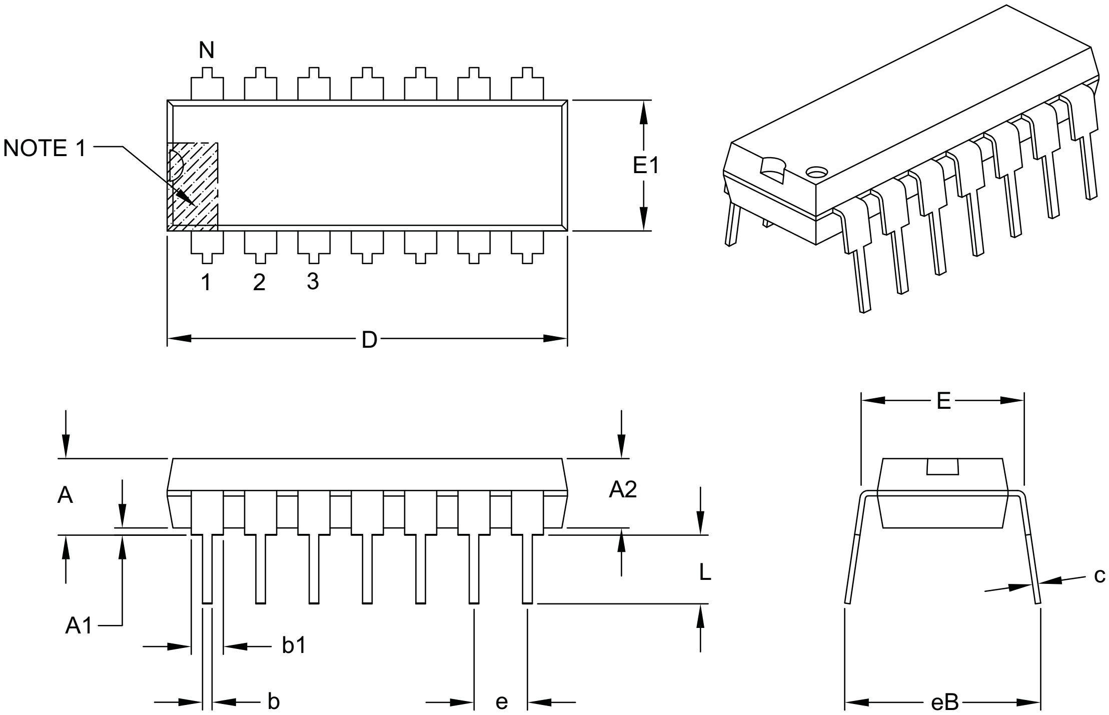
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

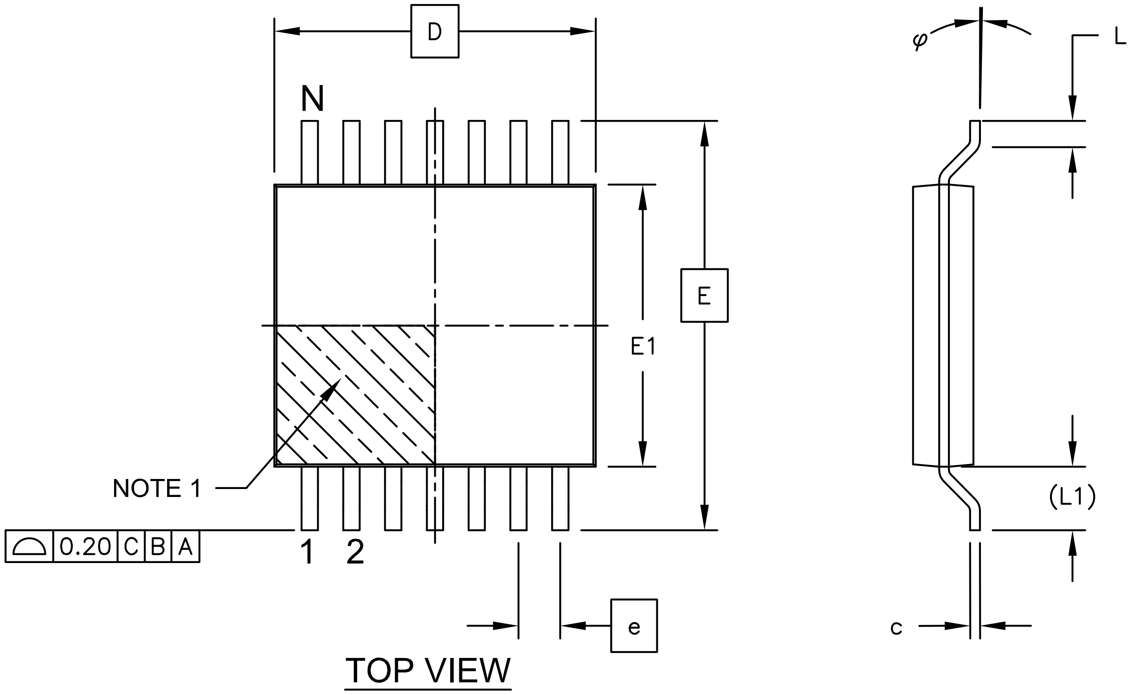
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

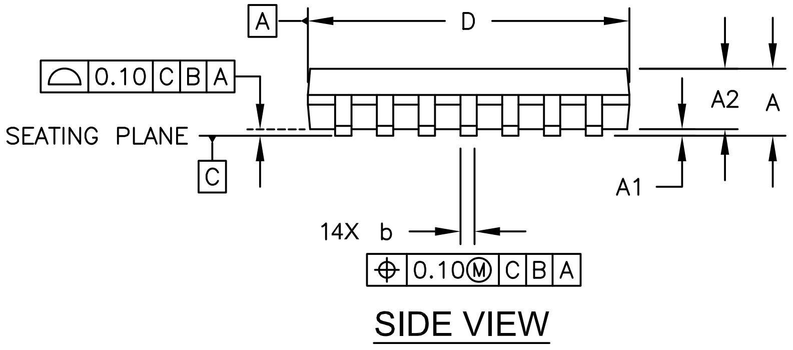
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

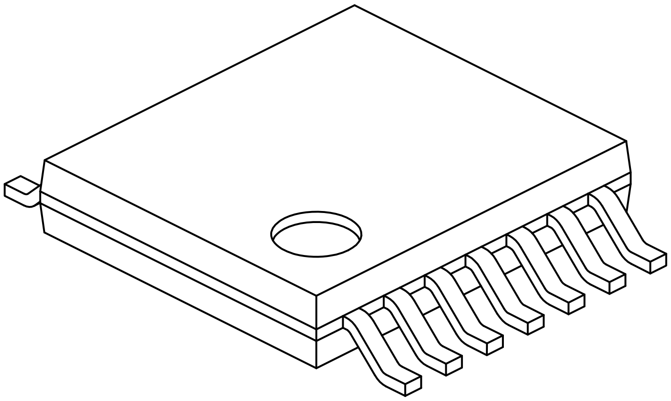

D
N
E
E1
NOTE 1
0.20 C B A
1 2
e
TOP VIEW
φ
L
(L1)
c


A
D
0.10 C B A
SEATING PLANE
C
A2
A
A1
14X b
0.10 Ⓜ C B A
SIDE VIEW

Microchip Technology Drawing C04-087C Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)	1.00 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

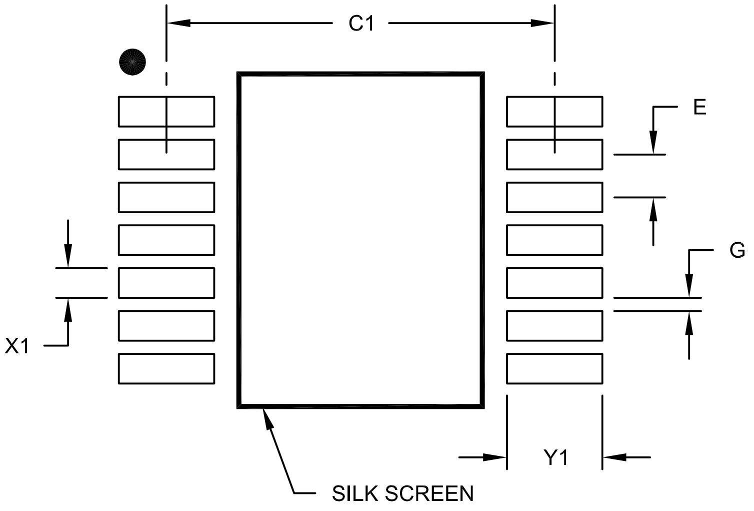
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	**–X**	**/XX**
Device	**Temperature Range**	**Package**

Device:
MCP2021A: LIN Transceiver with Voltage Regulator
MCP2021AT: LIN Transceiver with Voltage Regulator (Tape and Reel) (SOIC only)

Temperature Range:
E = -40°C to +125°C

Package:
MD = Plastic Dual Flat DFN, 8-lead
SN = Plastic Small Outline SOIC, 8-lead
P = Plastic DIP (300 mil Body), 8-lead, 14-lead
SL = Plastic SOIC, (150 mil Body), 14-lead
ST = Plastic TSSOP, 14-lead

Examples:

a) MCP2021A-330E/SN: 3.3V, 8L-SOIC package
b) MCP2021A-330E/P: 3.3V, 8L-PDIP package
c) MCP2021A-500E/SN: 5.0V, 8L-SOIC package
d) MCP2021A-500E/P: 5.0V, 8L-PDIP package
e) MCP2021AT-330E/SN: Tape and Reel, 3.3V, 8L-SOIC package
f) MCP2021AT-500E/SN: Tape and Reel, 5.0V, 8L-SOIC package
g) MCP2022A-330E/SL: 3.3V, 14L-SOIC package
h) MCP2022A-330E/P: 3.3V, 14L-PDIP package
i) MCP2022A-500E/SL: 5.0V, 14L-SOIC package
j) MCP2022A-500E/P: 5.0V, 14L-PDIP package
k) MCP2022AT-330E/SL: Tape and Reel, 3.3V, 14L-SOIC package
l) MCP2022AT-500E/SL: Tape and Reel, 5.0V, 14L-SOIC package
m) MCP2022AT-500E/ST: Tape and Reel, 5.0V, 14L-TSSOP package

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (December 2013)

The following is the list of modifications:

1. Removed two notes in **Section 2.4 “AC Specification”**.
2. Updated Figure 1-4.
3. Added pull-up to $\overline{\text{FAULT}}$/TXE pin in the pin description and typical applications.
4. Revised product identification examples for SOIC package.

Revision A (March 2012)

- Original Release of this Document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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