



MJE13009

NPN SILICON TRANSISTOR

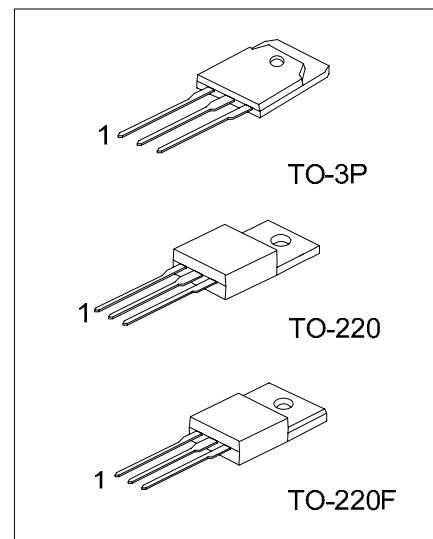
SWITCHMODE SERIES NPN SILICON POWER TRANSISTORS

■ DESCRIPTION

The **MJE13009** is designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

■ FEATURES

- * V_{CEO} 400 V and 300 V
- * Reverse Bias SOA with Inductive Loads @ $T_C = 100$
- * Inductive Switching Matrix 3 ~ 12 Amp, 25 and 100 tc @ 8 A, 100 is 120 ns (Typ).
- * 700 V Blocking Capability
- * SOA and Switching Applications Information.



*Pb-free plating product number:MJE13009L

■ ORDERING INFORMATION

Order Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
MJE13009-TA3-T	MJE13009L-TA3-T	TO-220	B	C	E	Tube
MJE13009-TF3-T	MJE13009L-TF3-T	TO-220F	B	C	E	Tube
MJE13009-T3P-T	MJE13009L-T3P-T	TO-3P	B	C	E	Tube

<p>MJE13009L-TA3-T</p>	<p>(1)Packing Type (2)Package Type (3)Lead Plating</p> <p>(1) T: Tube (2) TA3: TO-220, TF3: TO-220F, T3P: TO-3P (3) L: Lead Free Plating, Blank: Pb/Sn</p>
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■ ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

PARAMETER		SYMBOL	RATINGS		UNIT	
Collector-Emitter Voltage		V _{CEO}	400		V	
Collector-Emitter Voltage (V _{BE} =-1.5V)		V _{CEV}	700		V	
Emitter Base Voltage		V _{EBO}	9		V	
Collector Current	Continuous	I _C	12	24	A	
	Peak*	I _{CM}				
Base Current	Continuous	I _B	6	12	A	
	Peak*	I _{BM}				
Emitter Current	Continuous	I _E	18	36	A	
	Peak*	I _{EM}				
Total Power Dissipation @ Ta = 25		P _D	2	W		
Derate above 25			16	mW/°C		
Total Power Dissipation @ T _C = 25		P _D	100	W		
Derate above 25			800	mW/°C		
Junction Temperature		T _J	+150			
Storage Temperature		T _{STG}	-40 ~ +150			

Note: 1. Pulse Test: Pulse Width = 5ms, Duty Cycle ≤ 10%

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS		UNIT
Thermal Resistance Junction to Ambient		θ _{JA}	54		/W
Thermal Resistance Junction to Case		θ _{JC}	4		/W

■ ELECTRICAL CHARACTERISTICS (T_C = 25 °C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
*OFF CHARACTERISTICS							
Collector-Emitter Sustaining Voltage	V _{CEO}	I _C = 10mA, I _B = 0	400			V	
Collector Cutoff Current	I _{CEV}	V _{BE(OFF)} = 1.5Vdc			1	mA	
V _{CBO} =Rated Value		V _{BE(OFF)} = 1.5Vdc, T _C = 100			5		
Emitter Cutoff Current	I _{EBO}	V _{EB} = 9Vdc, I _C = 0			1	mA	
*ON CHARACTERISTICS							
DC Current Gain	h _{FE1}	I _C = 5A, V _{CE} = 5V			40		
	h _{FE2}	I _C = 8A, V _{CE} = 5V			30		
Current-Emitter Saturation Voltage	V _{CE(SAT)}	I _C = 5A, I _B = 1A			1	V	
		I _C = 8A, I _B = 1.6A			1.5	V	
		I _C = 12A, I _B = 3A			3	V	
		I _C = 8A, I _B = 1.6A, T _C = 100			2	V	
Base-Emitter Saturation Voltage	V _{BE(SAT)}	I _C = 5A, I _B = 1A			1.2	V	
		I _C = 8A, I _B = 1.6A			1.6	V	
		I _C = 8A, I _B = 1.6A, T _C = 100			1.5	V	
DYNAMIC CHARACTERISTICS							
Transition frequency	f _T	I _C = 500mA, V _{CE} = 10V, f = 1MHz	4			MHz	
Output Capacitance	C _{ob}	V _{CB} = 10V, I _E = 0, f = 0.1MHz		180		pF	
SWITCHING CHARACTERISTICS (Resistive Load, Table 1)							
Delay Time	t _{DLY}	V _{CC} = 125Vdc, I _C = 8A I _{B1} = I _{B2} = 1.6A, t _P = 25μs Duty Cycle ≤ 1%			0.06	0.1	μs
Rise Time	t _R				0.45	1	μs
Storage Time	t _S				1.3	3	μs
Fall Time	t _F				0.2	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)							
Voltage Storage Time	t _S	I _C =8A, V _{clamp} =300V, I _{B1} =1.6A			0.92	2.3	μs
Crossover Time	t _C	V _{BE(OFF)} = 5V, T _C = 100			0.12	0.7	μs

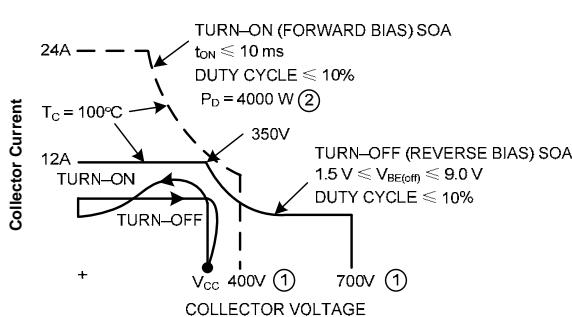
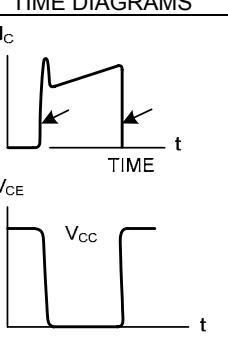
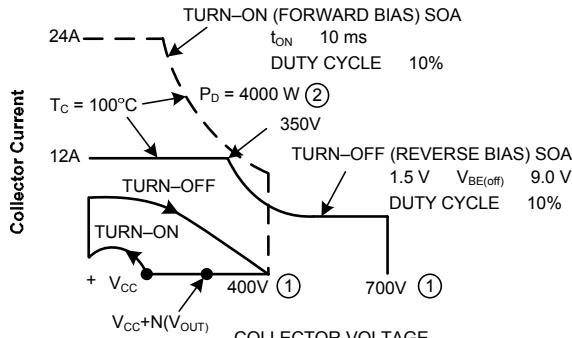
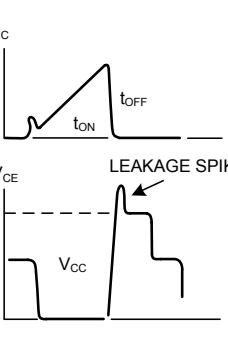
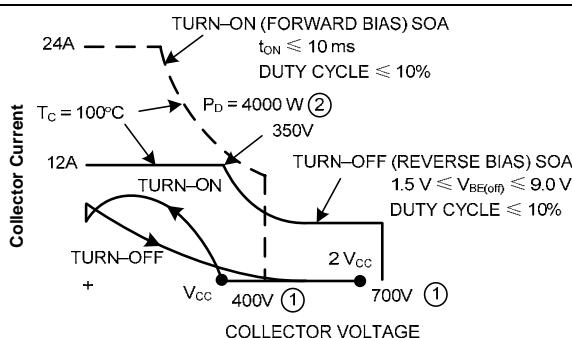
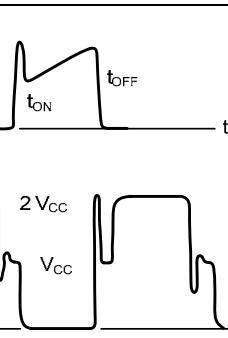
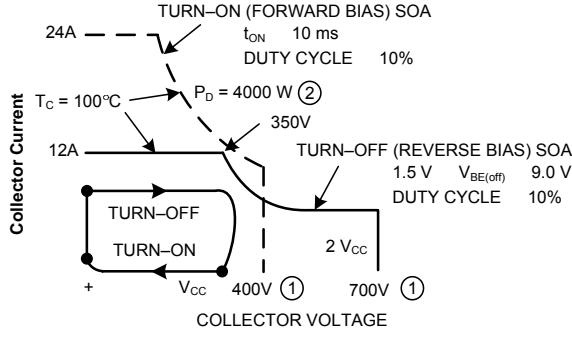
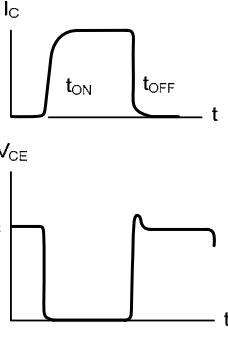
*Pulse Test: Pulse Width = 300μs, Duty Cycle = 2%



■ TABLE 1. TEST CONDITIONS FOR DYNAMIC PERFORMANCE

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING
TEST CIRCUITS		
<p>DUTY CYCLE $t_R, t_F < 10$ ns</p> <p>NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_B</p>	V_{CC} L I_C I_B V_{CE} V_{clamp} $*SELECTED FOR .1 kV$ D.U.T.	$+125V$ R_C TUT $D1$ $-4.0V$ $SCOPE$
CIRCUIT VALUES	<p>Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16</p> <p>GAP for 200 μH/20 A $L_{coil} = 200 \mu$H</p>	$V_{CC} = 20$ V $V_{clamp} = 300$ Vdc $R_C = 15 \Omega$ $D1 = 1N5820 or Equiv.$ $R_B = \Omega$
TEST WAVEFORMS	<p>OUTPUT WAVEFORMS</p> <p>t_1 ADJUSTED TO OBTAIN I_C</p> $t_1 = \frac{L_{coil} (I_{CM})}{V_{CC}}$ $t_2 = \frac{L_{coil} (I_{CM})}{V_{clamp}}$	$+10V$ 0 $-8V$ 25μ s

■ TABLE 2. APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
SERIES SWITCHING REGULATOR		
RINGING CHOKE INVERTER		
PUSH-PULL INVERTER/CONVERTER		
SOLENOID DRIVER		

■ TABLE 3. TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I _c (A)	T _c (ns)	t _{sv} (ns)	t _{rv} (ns)	t _{fi} (ns)	t _{ti} (ns)	t _c (ns)
3	25	770	100	150	200	240
	100	1000	230	160	200	320
5	25	630	72	26	10	100
	100	820	100	55	30	180
8	25	720	55	27	2	77
	100	920	70	50	8	120
12	25	640	20	17	2	41
	100	800	32	24	4	54

■ SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{rv} = Voltage Rise Time, 10–90% V_{CEM}

t_{fi} = Current Fall Time, 90–10% I_{CM}

t_{ti} = Current Tail, 10–2% I_{CM}

t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2 V_{CC} I_C(t_c) f$$

Typical inductive switching waveforms are shown in Figure 14. In general, t_{rv} + t_{fi} = t_c. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25 ns and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100 ns.



■ TYPICAL CHARACTERISTICS

Figure 1. Forward Bias Safe Operating Area

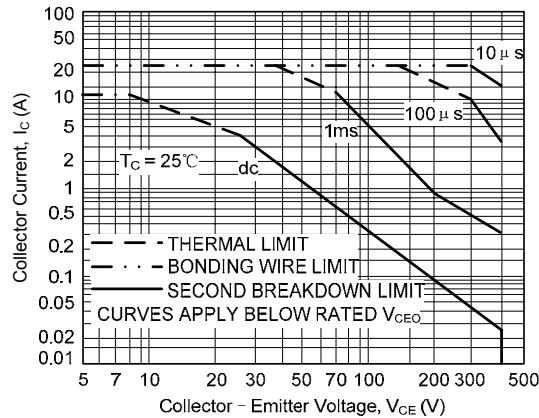


Figure 2. Reverse Bias Switching Safe Operating Area

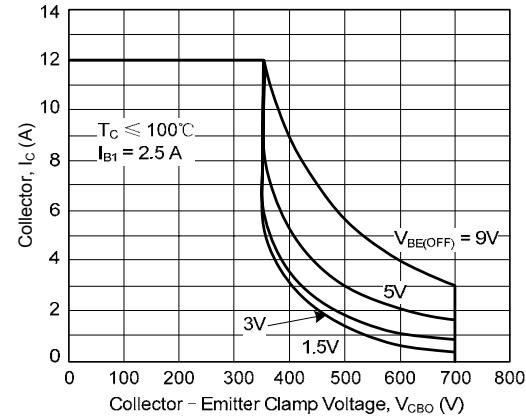
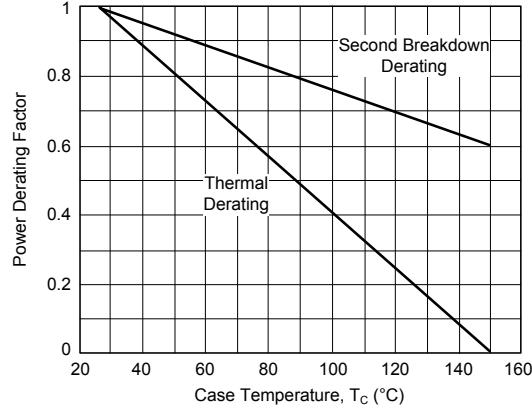


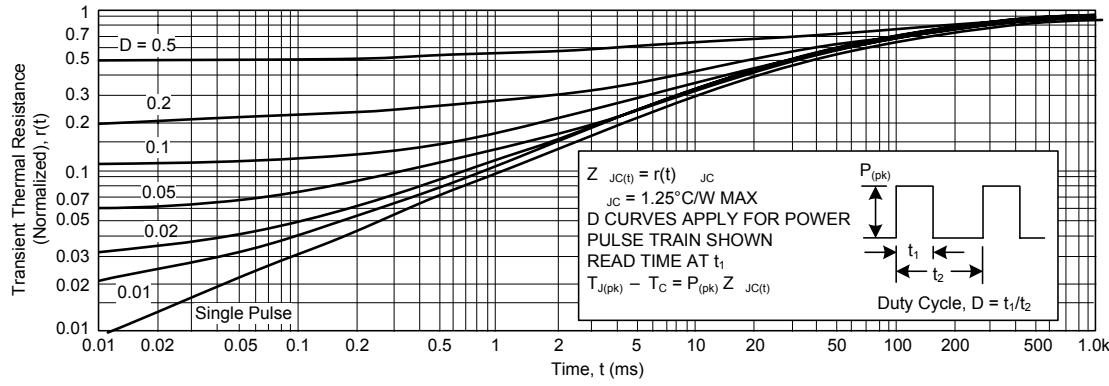
Figure 3. Forward Bias Power Derating



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_c - V_{ce}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_c = 25^\circ\text{C}$; $T_{j(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_c > 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{j(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

Figure 4. Typical Thermal Response [$Z_{jc(t)}$]

■ TYPICAL CHARACTERISTICS (Cont.)

Figure 5. DC Current Gain

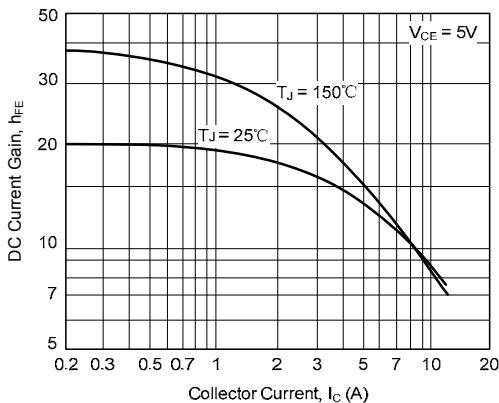


Figure 6. Collector Saturation Region

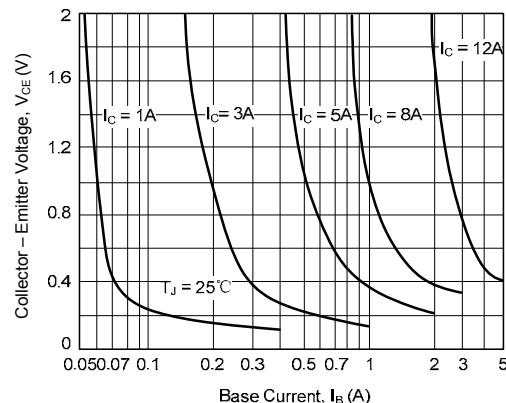


Figure 7. Base – Emitter Saturation Voltage

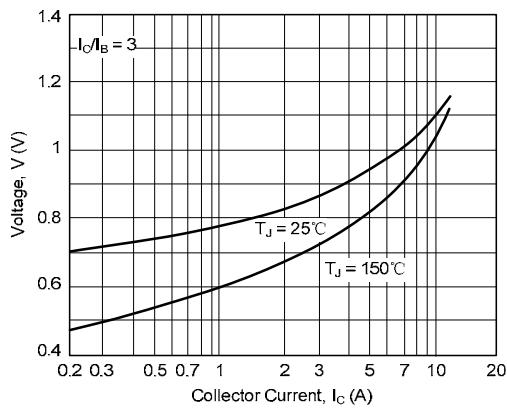


Figure 8. Collector – Emitter Saturation Voltage

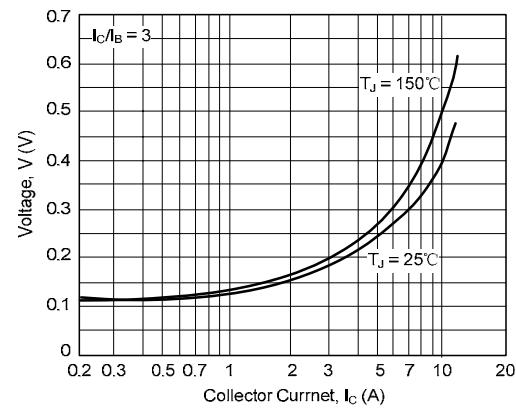


Figure 9. Collector Cutoff Region

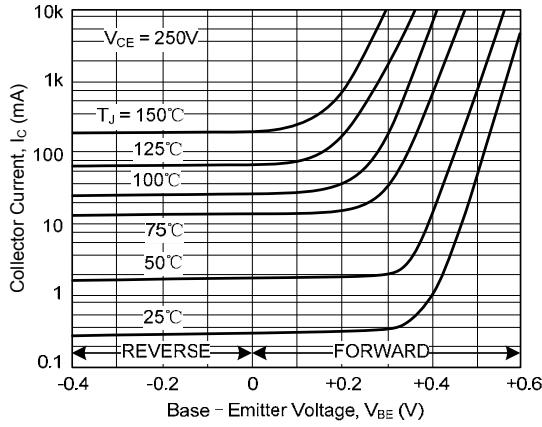
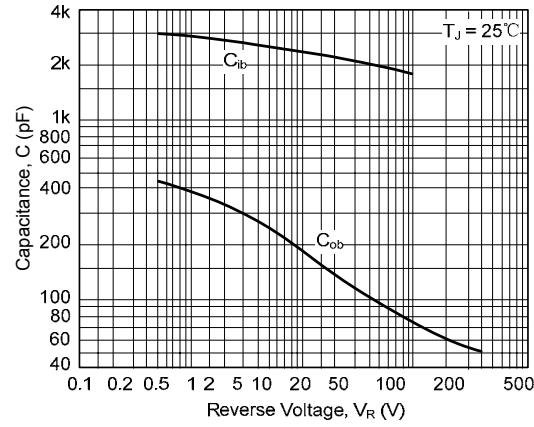


Figure 10. Capacitance



RESISTIVE SWITCHING PERFORMANCE

Figure 11. Turn - On Time

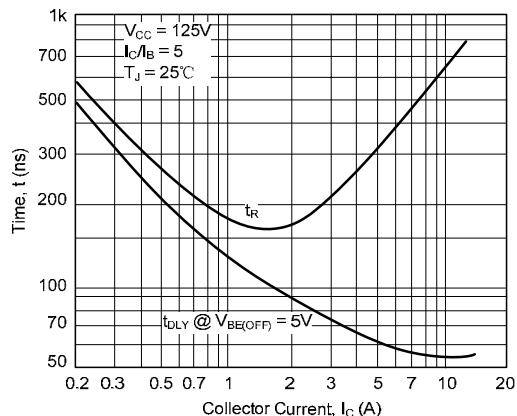
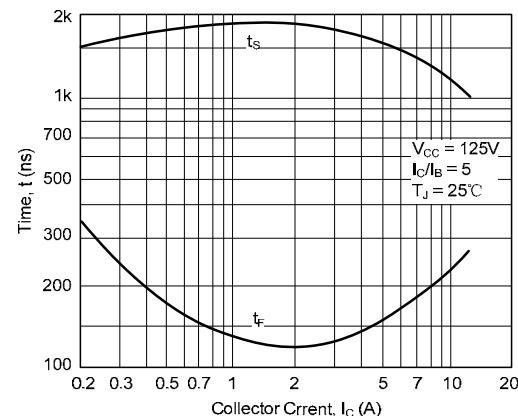
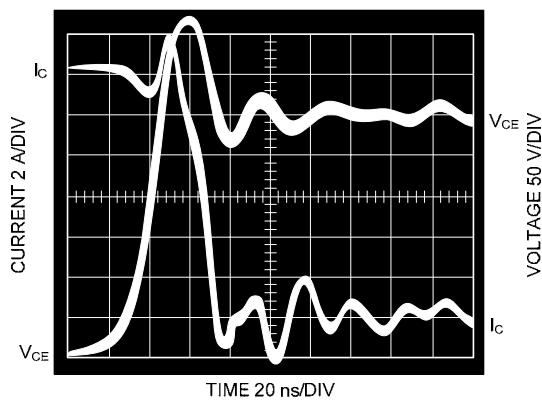


Figure 12. Turn - Off Time

Figure 13. Typical Inductive Switching Waveforms
(at 300V and 12A with $I_{B1} = 2.4A$ and $V_{BE(off)} = 5V$)

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