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ML2724

2.4GHz LOW-IF 1.5Mbps FSK TRANSCEIVER

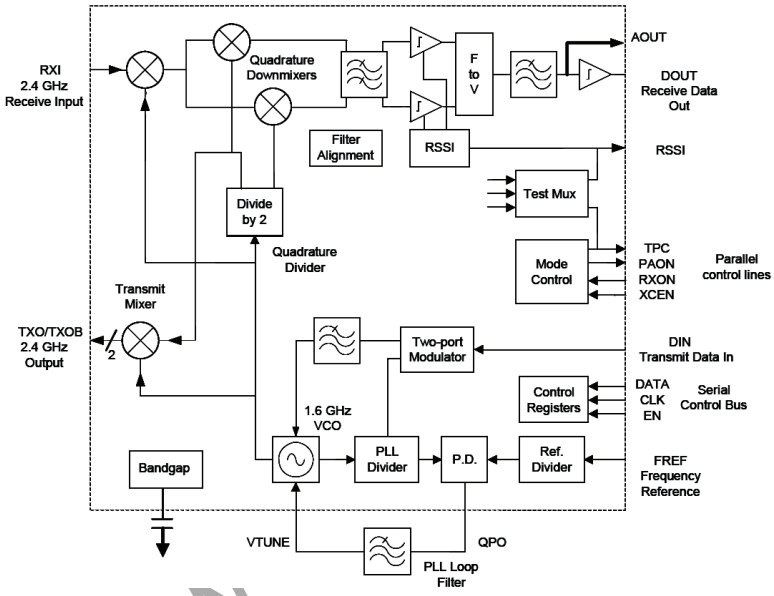
Package: TQFP, 32-Pin, 7mmx7mmx1mm

Features

- Complete 2.4GHz FSK Transceiver
- High data rate (1.5Mbps)
- -81dBm sensitivity @ 0.1% BER (typ)
- 3dBm Output Power (differential, typ)
- Closed Loop TX Modulation
- Low IF Receiver: No external IF filters required.
- Fully Integrated frequency synthesizer:
- No external resonator required.
- Sigma-Delta Fractional-N two-port modulator
- Automatic Filter Alignment
- No manufacturing adjustments required.
- No external data slicer components required
- Control outputs correctly sequence and control PA
- 3-wire control interface
- Analog RSSI output

Applications

- 2.4GHz FSK Data Transceivers
- Digital Cordless Telephones
- Wireless PC Peripherals
- Wireless Game Controllers
- Wireless Streaming Media



Functional Block Diagram

Product Description

The ML2724 is a fully integrated 1.5Mbps frequency shift keyed (FSK) transceiver that operates in the unlicensed 2.4GHz ISM frequency band. The device has been optimized for digital cordless telephone applications and includes all the frequency generation, receive and transmit functions. Automatically adjusted filters eliminate mechanical tuning. Closed loop modulation eliminates frequency drift and permits practically unlimited TX duration. The transmitter generates a 3dBm FSK output signal.

The 1.5Mbps data rate permits data spreading, such as Direct Sequence Spread Spectrum (DSSS) modulation, which improves range. The dual conversion Low-IF receiver has all of the sensitivity and selectivity advantages of a traditional super-heterodyne without requiring costly, bulky external filters, while providing the integration advantages of direct conversion.

The phase locked loop (PLL) synthesizer is completely integrated, including the voltage controlled oscillator (VCO), tuning circuits, and VCO resonator. This allows the ML2724 to be used in frequency hopped spread spectrum (FHSS) applications.The ML2724 contains internal voltage regulation. It also contains PLL and transmitter configuration registers. The device can be placed in a low power standby mode for current sensitive applications. It is packaged in a "Green" Pb-Free 32TQFP.

Ordering Information

ML2724	2.4GHz Low-IF 1.5Mbps FSK Transceiver

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
V_{CCA}, V_{DD}	5.5	V
Junction Temperature	150	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10s)	260	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CCA}=V_{DD}=3.3V, T_A=25°C, f_{REF}=6.144MHz, Data Rate=1.536Mbps, 13kHz Loop Filter.
Operating Conditions					
Normal Temperature Range	-10		60	°C	
V_{CCA} Range	2.7		4.5	V	
V_{DD} Range	2.7		3.3	V	
Thermal Resistance		70		°C/W	
Power Consumption					
V_{CCA}	2.7	3.3	4.5	V	
V_{DD}	2.7		3.3	V	VDD pin (VCCA ≥ VDD always)
V_{BG}		1.23		V	VBG pin 26, IO=0µA
I_{STBY}		10	120	µA	Supply current, standby mode. DC supply connected, XCEN low
I_{RX}		55	76	mA	Supply current, transmit mode. RX chain active, data being received
I_{TX}		50	76	mA	Supply current, transmit mode. P_{OUT}=3dBm
Synthesizer					
f_C	2.4		2.485	GHz	Carrier frequency range
δf		2048			Channel spacing
I_P					Charge pump sink/source current
Φ_N		-95		dBc/Hz	Phase noise at TXO 1.2MHz. Closed loop, loop filter bandwidth 13KHz
Φ_N		-115		dBc/Hz	Phase noise at TXO 3MHz. Closed loop, loop filter bandwidth 13KHz
Φ_N		-125		dBc/Hz	Phase noise at TXO 7MHz. Closed loop, loop filter bandwidth 13KHz
t_{FH}		110	125	µs	From EN asserted to RX valid data(RX), or PAON high (TX) 1 channel
t_{FH}		185	220	µs	From EN asserted to RX valid data(RX), or PAON high (TX) 5 channels
t_{FH}		250	300	µs	From EN asserted to RX valid data(RX), or PAON high (TX) Full range.
t_{TX2RX}		70	120	µs	RXON high to valid RX data

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
t_{RX2TX}		63	75	µs	RXON low to PAON high
t_{WAKE}		240	325	µs	XCEN high to valid RX data, XCEN low period >120 seconds
f_{FREF}		6.144		MHz	
f_{FREF}		12.288		MHz	
V_{FREF}	2.0		VCCA	V_{PP}	6.144MHz or 12.288MHz sine wave, capacitively coupled
Receiver					
Z_{IN}		2.2+j0		Ω	fc=2445MHz
NF		16.5		dB	fc=2445MHz
DR_{RX}		1.536		Mbps	FSK modulation, fdev=+/-512kHz
S	-82	-90		dBm	<12.5% CER at 1.536Mchip/s
S		-81		dBm	<0.1% BER at 1.536Mbps
BW_{RX}		770		kHz	3dB Bandwidth
P_{IMAX}	+5			dBm	<12.5% CER at 1.536Mchip/s
P_{IMAX}	-4			dBm	<0.1% BER at 1.536Mbps
I_{IP3}		-15		dBm	Test tones 2 and 4 channels away
I_{IP3}		-60		dBm	
IRR		35		dB	Measured at 3.5MHz offset
Adjacent channel rejection		6		dB	-80dBm wanted signal <10-3 BER Single 2GFSK modulated interferer with a 1.5MHz – 20dBc bandwidth 1 channel away
Adjacent channel rejection		31		dB	-80dBm wanted signal <10-3 BER Single 2GFSK modulated interferer with a 1.5MHz – 20dBc bandwidth 2 channels away
Adjacent channel rejection		36		dB	-80dBm wanted signal <10-3 BER Single 2GFSK modulated interferer with a 1.5MHz – 20dBc bandwidth 3 or more channels away
IF Filters					
f_{IFC}		1.024		MHz	After automatic filter alignment
BW_{IF}		1.024		kHz	After automatic filter alignment
Limiter, AGC, and FM Demodulator					
t_{OVLD}		5	12	µs	From +15dB at input
Eb/NO		10.5		dB	For 0.1% BER
Co-Channel rejection, 0.1% BER		10.5		dB	-80dBm, modulated with 1.536Mbps GFSK, BT=0.5, PRBS data
V_{ODC}		1.1		V	
V_{OPK}	.55		1.1	V_{PP}	
V_{OL}			0.4	V	IO=100µA, TPC Mode
RSSI Performance					
t_{RRSSI}		4.5		µs	20pF load, 20% to 80%
t_{FRSSI}		3.0		µs	20pF load, 20% to 80%
G_{RSMID}	28	36	42	mV/dB	(V-40dBm – V-60dBm)/20dB

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
V_{RSMX}	1.8	2.3		V	
V_{RSMD}	1.4	1.7	2.0	V	-40dBm into RXI
V_{RSMn}		75		mV	
V_{RSMxc}	1.6	1.95		V	
Transmit RF Mixer					
P_{OSE}	-3	1	5	dBm	TRXO or TRXOB, fC=2.445GHz
P_{ODIF}	-1	3	6	dBm	P(TRXO,TRXOB), fC=2.445GHz
Z_{OUT}		12+j0		Ω	TRXO or TRXOB, fC=2.445GHz
Transmit Modulation					
f_{DEV}	500	512	524	kHz	200µs of consecutive '1's or '0's
f_{OS}	-50		+50	kHz	50µs after RXON low
Transmit Data Filter					
BW_{TX}		1.4		MHz	3dB bandwidth
TX spurious Image		-25		dBc	
TX spurious Image		-20		dBc	
Interface Logic Levels					
Inputs (DIN, XCEN, RXON, Data, Clk, EN)					
V_{IH}	0.75*VDD		VDD	V	never exceed VDD
V_{IL}	0		0.25*VDD	V	
I_B	-5	0	5	µA	
C_{IN}		4		pF	measured at 1MHz
Outputs (DOUT, PAON)					
VOH	VDD-0.4			V	IO=0.1mA
VOL			0.4	V	IO=-0.1mA
I_O	0.1			mA	
VOH	VDD-0.4			V	Sourcing 0.5mA
VOL			0.4	V	Sinking 0.5mA
I_O	0.5			mA	

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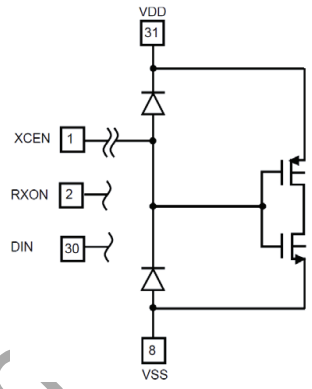
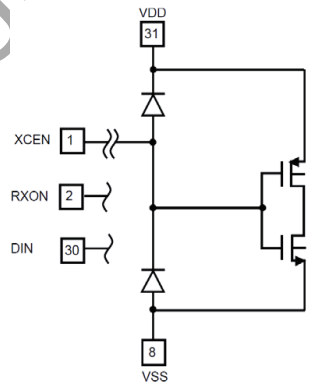
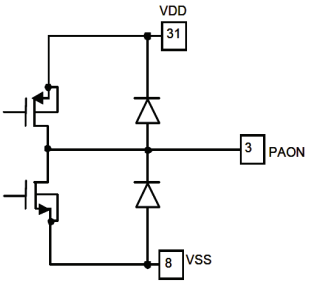
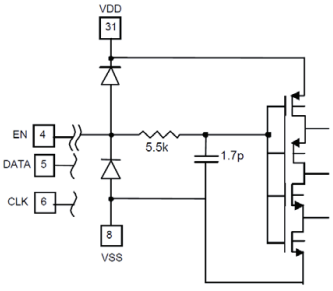
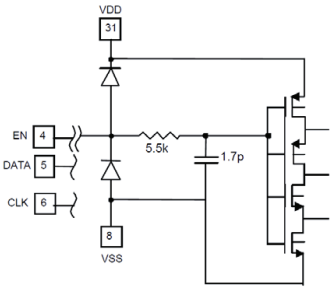
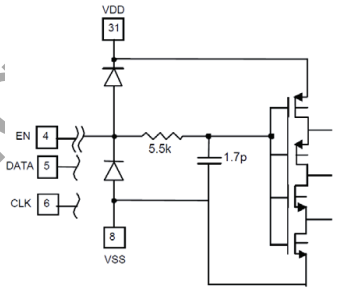
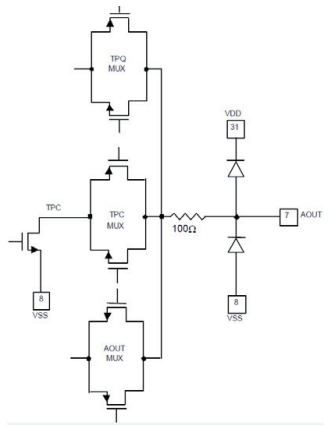
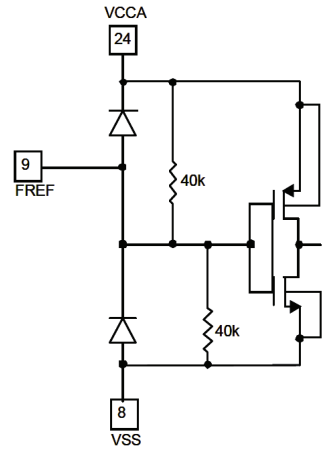
Pin	Function	Description	Interface Schematic
1	XCEN	Enables the bandgap reference and voltage regulators when high. Consumes only leakage current in standby mode when low. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	
2	RXON	TX/RX control input. Switches the transceiver between transmit and receive modes. Circuits are powered up and signal paths reconfigured according to the operating mode. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	
3	PAON	PA control output. Enables the off-chip PA at the correct times in a transmit slot. Goes high when transmit RF is present at TXO; goes low 5µs before transmit RF is removed from TXO. Has interlock logic to shut down the PA if the PLL does not lock.	
4	EN	Control bus enable. Enable pin for the three-wire serial control bus that sets the operating frequency and programmable options. The control registers are loaded on a low-to-high transition of the signal. Serial control bus data is ignored when this signal is high. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	

Pin	Function	Description	Interface Schematic
5	DATA	Serial control bus data. 16-bit words, which include programming data and the two-bit address of a control, register. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	
6	CLK	Serial control bus data is clocked in on the rising edge when EN is low. This is a CMOS input; the thresholds are referenced to VDD and VSS.	
7	AOUT	Multi-function output. In analog output mode this output drives an off-chip data slicer. In transmit power control mode this is an open drain output, which is pulled low when the TPC bit is serial register #1, is clear. Transitions on TPC are synchronized to the falling edge of RXON. In analog test modes this pin and the RSSI output become test access points controlled by the serial control bus.	
8	VSS	Digital ground. Ground for digital I/O circuits and control logic	
9	FREF	Input for the 12.288MHz or 6.144MHz reference frequency. This input is used as the reference frequency for the PLL and as a calibration frequency for the onchip filters. An AC-coupled sine or square wave source drives this self-biased input.	

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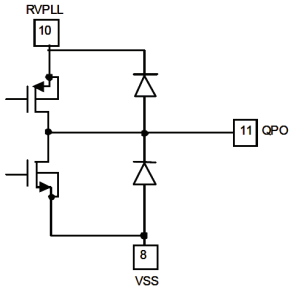
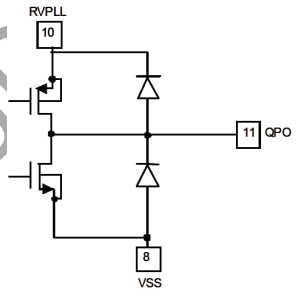
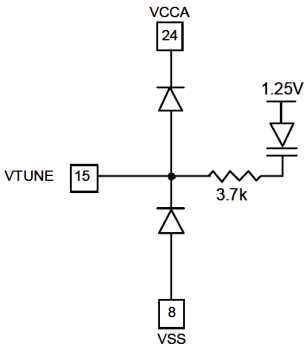
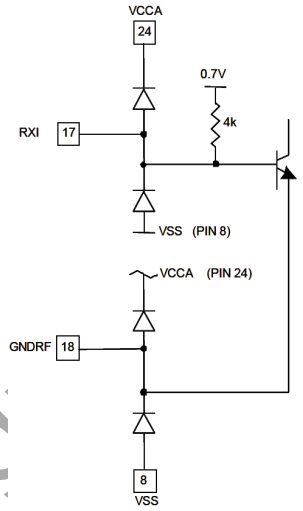
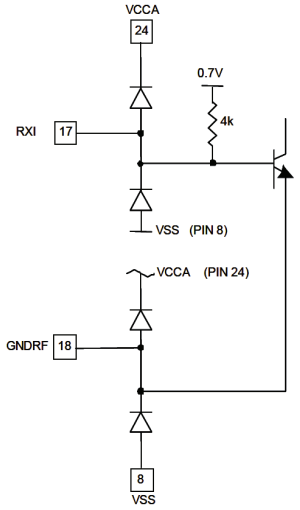
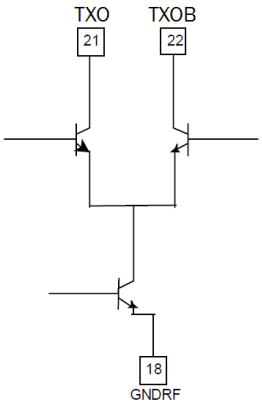
Pin	Function	Description	Interface Schematic
10	RVPLL	PLL supply. DC power supply decoupling point for the PLL dividers, phase detector, and charge pump. This pin is connected to the output of the regulator and to the PLL supplies. There must be a 220nF capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator.	
11	QPO	Charge pump output of the phase detector. This is connected to the external PLL loop filter.	
12	GNDPLL	Ground for the PLL dividers, phase detector, and charge pump.	
13	VVREG	DC power supply input to the VCO voltage regulator. Must be connected to RVQMIF (pin 27) or RVDMD (pin 29) via decoupling network.	
14	RVVCO	DC power supply decoupling point for the VCO. Connected to the output of the VCO regulator. A 220nF capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
15	VTUNE	VCO tuning voltage input from the PLL loop filter. This pin is very sensitive to noise coupling and leakage currents.	
16	GND	DC ground for VCO and LO circuits.	

Pin	Function	Description	Interface Schematic
17	RXI	Receive RF input. Nominal impedance at 2445 MHz is 2.6-j2.6 with a simple matching network required for optimum noise figure. This input connects to the base of an NPN transistor and should be AC-coupled.	
18	GNDRF	Ground return for the receive RF input and transmit RF output.	
19	GNDRXMX	Signal ground for the receive mixers	
20	GNDRXMX2	Signal ground for the receive mixers	
21	TXO	TX RF open-collector output. This output requires a DC path to VCCA.	

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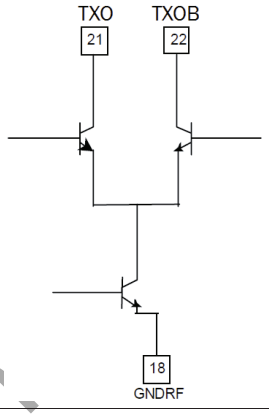
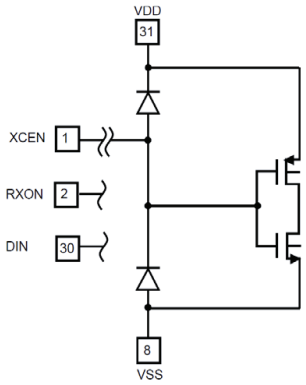
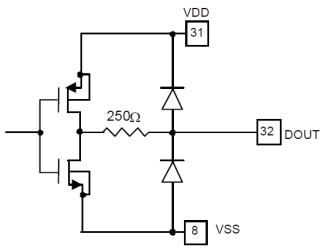
Pin	Function	Description	Interface Schematic
22	TXOB	Complementary TX RF open-collector output. This output requires a DC path to VCCA. For single-ended output applications, this pin should be connected to a dummy load that includes a DC path to VCCA.	
23	RVLO	DC power supply decoupling point for the LO chain. Connected to the output of a regulator. A 220nF capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
24	VCCA	DC power supply input to voltage regulators and unregulated loads: 2.7V to 3.8V. VCCA is the main (or master) analog VCC pin. There must be capacitors to ground from this pin to decouple (bypass) supply noise.	
25	GNDDMD	DC ground to IF, demodulator, and data slicer circuits.	
26	VBG	Bandgap decouple voltage. Decoupled to ground with a 220nF capacitor.	
27	RVQMIF	DC power supply decoupling point for quadrature mixer and IF filter circuits. A 220nF capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
28	RSSI	Buffered analog RSSI output with a nominal sensitivity of 35mV/dB. In analog test modes, this pin and the AOUT output become test access points controlled by the serial control bus.	
29	RVDMD	DC power supply decoupling point for IF, demodulator, and data slicer circuits. A 220nF capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
30	DIN	Transmit data input. Drives the transmit pulse shaping circuits. Serial digital data on this pin becomes FSK modulation on the Transmit RF output. The logic timing on this pin controls data timing. Internal circuits determine the modulation deviation. This is a standard CMOS input referenced to VDD and VSS.	
31	VDD	DC power supply input to the interface logic and control registers. This supply is not connected internally to any other supply pin, but its voltage must be less than, or equal to, the VCCA supply and greater than 2.7V. A capacitor must be tied between this pin and ground to decouple (bypass) noise.	

Pin	Function	Description	Interface Schematic
32	DOUT	Serial digital output after demodulation, chip rate filtering and center data slicing. A CMOS level output (VSS to VDD) with controlled slew rates. A low drive output designed to drive a PCB trace and a CMOS logic input while generating minimal RFI. In digital test modes this pin becomes a test access port controlled by the serial control bus.	

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Theory of Operation

The ML2724 is a fully integrated 1.5Mbps frequency shift keyed (FSK) transceiver that operates in the unlicensed 2.4GHz ISM frequency band. The device has been optimized for digital cordless telephone applications and includes all the frequency generation, receive and transmit functions for a raw data rate of 1.5Mbps. This high data rate allows for data spreading, such as direct ssequence spread spectrum (DSSS) modulation, which improves range. The ML2724 receiver architecture is a dual conversion Low IF, which has all of the sensitivity and selectivity advantages of a traditional super-heterodyne receiver without requiring costly, bulky external filters.

The RF mixer down-converts the 2.4GHz RF input signal to the first intermediate frequency (IF), where it is filtered to remove adjacent channel signals. An active image reject mixer converts this signal down to a low IF frequency, where the data is limited, filtered, and demodulated. This architecture provides all the benefits of direct conversion to baseband while maintaining the stability and robustness of a traditional super-heterodyne.

A single synthesizer is used for both the receiver and the FSK transmitter. The phase locked loop (PLL) is completely integrated, including the voltage controlled oscillator (VCO), tuning circuits, and VCO resonator.

In receive mode, the ML2724 is a dual conversion low IF receiver. No external SAW filters are required. The integrated image reject mixer gives sufficient rejection in this channel. All channel filtering and demodulation is performed using active filters, which are automatically aligned. A matched bit rate filter and a data slicer follow the demodulator. The sliced data is provided at the DOUT pin, and the analog data is available at AOUT.

Filter and modulation compensation circuit results in an adjustment-free transmitter. The VCO is modulated by the transmit data, which is put through a sigma-delta fractional-N PLL ensuring modulation accuracy. This modulation occurs while the phase locked loop is closed, thus allowing practically infinite transmit or receive times with excellent frequency accuracy and stability. A 3dBm FSK-modulated differential signal is output at the TXO/TXOB pins at the 2.4GHz carrier frequency.

The integrated PLL frequency synthesizer includes a fully integrated VCO, prescaler, phase detector and charge pump. The reference frequency is generated from the incoming signal at the FREF pin, which can be either 6.144MHz or 12.288MHz. The loop filter is external to allow customers to optimize their loop bandwidth to their system's lock time and in-band phase noise requirements. This frequency-agile synthesizer allows the ML2724 to be used in frequency-hopped spread spectrum (FHSS) applications with nominal channel spacing of 2.048MHz. Carrier frequency is programmed via the configuration registers and 3-wire serial interface. The VCO tank circuit (inductor and varactor) is fully integrated.

There are three key modes of operation:

- **Standby:** All circuits powered down, except the control interface (Static CMOS)
- **Receive:** Receiver circuits active
- **Transmit:** Modulated RF output from IC

The two operational modes are receive and transmit, controlled by RXON. XCEN is the chip enable/disable control pin, which sets the part in operational or standby modes. The relationship between the parallel control lines and the mode of operation of the IC is given in the table below.

Modes of Operation:

XCEN	RXON	Mode	Function
0	X	Standby	Control interfaces active, all other circuits powered down
1	1	Receive	Receiver time slot
1	0	Transmit	Transmit time slot

Mode Control

The ML2724 is intended for use in TDD and TDMA radios in battery-powered equipment. To minimize power consumption it is designed to switch rapidly from a low power mode (standby) to an active mode. The ML2724 can also make a quick transition from receive to transmit for TDD operation. Prior to transmitting or receiving, time should be allowed for the PLL to lock and for the filters to align. When the ML2724 is operated in single-carrier TDD mode, the LO is automatically shifted by the second (low) IF frequency when the device is switched between receive and transmit modes.

ML2724 carrier frequency can be changed (hopped) at any time, but is usually changed between transmissions. Carrier frequency (channel) is modified in the ML2724 by writing a corresponding new value to the PLL frequency register (Register 1).

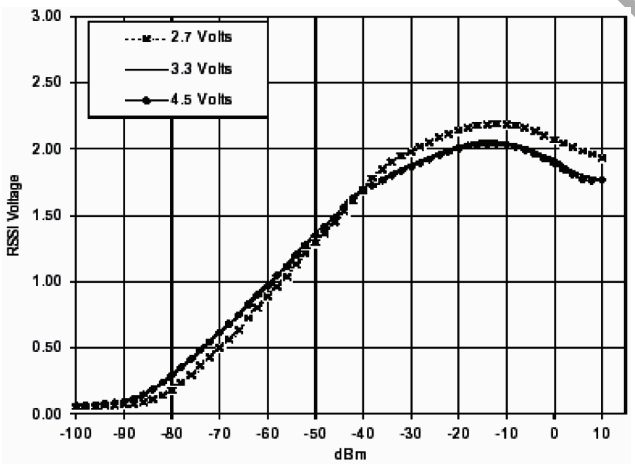
Receive Mode

The ML2724 uses a double-conversion super-heterodyne receiver with a nominal second IF of 1.024MHz. The signal flow in receive mode is from the RF input, through an RF down-conversion mixer and integrated IF filter, image reject quadrature mixer, integrated Low IF filter, hard limiter, frequency to voltage converter, and data filter to the AOUT pin and data slicer where the digital NRZ data is available at the DOUT pin. A 20dB step AGC extends the dynamic range of the receiver. The ML2724 receive chain is a Low IF receiver using advanced integrated radio techniques to eliminate external IF filters and minimize external RF filter requirements. The precision filtering and demodulation circuits give improved performance over conventional radio designs using external filters while providing integration comparable to advanced direct conversion radio designs.

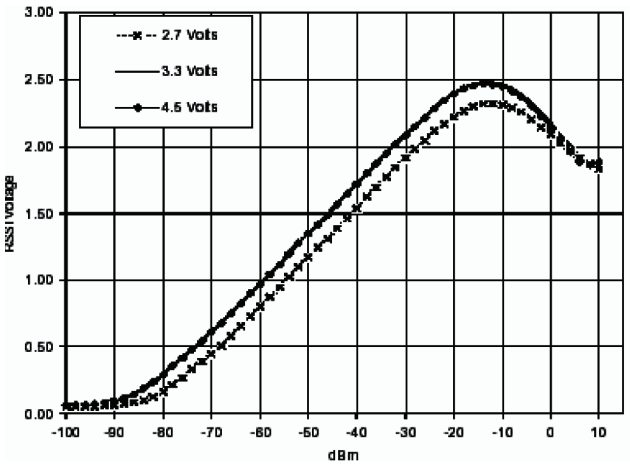
Receive Signal Strength Indication (RSSI)

RSSI is an indication of field strength. It can be used to control transmit power to conserve battery life or it may be used to determine if a given channel is occupied.

RSSI Output Voltage vs. Input Signal Level
(Clipped, 25° C, Various input voltage levels)



RSSI Output Voltage vs. Input Signal Level
(Unclipped, 25° C, Various Input Voltage Levels)



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Automatic Filter Alignment

When ML2724 is placed in receive mode, it automatically tunes all internal filters using the reference frequency from the FREF pin. When the chip is powered up (VDD first applied), tuning information is reset to midrange. This self-calibration sets:

- Discriminator center frequency
- IF filter center frequency and bandwidth
- Receiver data low-pass filter bandwidth
- Transmmit data low-pass filter bandwidth

Transmit Mode

In transmit mode, the PLL is closed to eliminate frequency drift. A two-port modulator modulates both the VCO and the fractional-N PLL. The VCO is directly modulated with filtered FSK transmit data. The PLL is driven by a sigma-delta modulator, which ensures that the PLL follows the mean frequency of the modulated VCO.

The transmit modulation filter is automatically tuned during every receive time, alleviating the need for production alignment. Asserting RXON enables the ML2724. The rising edge of XCEN triggers a complete calibration of all the onchip filters, which takes up to 256µs, which ensures the modulation filters are aligned to prevent unwanted spurious emissions.

PLL Programming and Channel Selection

The ML2724 PLL is programmed via control register 2 to the set RF center frequency of operation of the radio. The PLL does not need to be (though it can be) reprogrammed between receive and transmit modes. Nominal channel separation is 2.048MHz, allowing for over 40 non-overlapping channels in any given location. With careful planning, channels can be programmed in 1024kHz steps as long as care is exercised to insure that two radio links will not share spectrum at any one time. The equation to determine channel center frequency from the ML2724 control register word is:

$$f_C = CHQ<0:11>*1.024MHz$$

Standby Mode

In standby mode, the ML2724 transceiver is powered down. The only circuits active are the control interfaces, which are digital CMOS to minimize power consumption. The serial control interface and control registers remain powered up and will accept and retain programming data as long as the digital supply is present. When exiting standby mode, the device may need to be kept in receive mode for up to 256µs to allow for filter self-calibration.

Test Mode

The RF to digital functionality of the ML2724 requires special test mode circuitry for IC production test and radio debugging. A test register, accessible via the 3-wire serial interface, controls the test multiplexers.

Data Interface

There are two control interfaces: control and serial.

Control Interface

The control interface provides immediate control and monitoring of the ML2724. Input signals include:

- XCEN: Transceiver enable. Places the ML2724 in standby or active (when asserted) modes.
- RXON: Receive on. Places an active ML2724 in receive mode when asserted.
- FREF: Reference frequency input

Output signals include:

- RSSI: Received signal strength indictor: Indicates the power of the received signal.
- PAON: External power amplifier control pin

Serial Interface

A 3-wire serial interface (EN, DATA, CLK) is used for programming the ML2724 configuration registers, which control device mode, pin functions, PLL and reference dividers, internal test modes, and filter alignment. Data words are entered beginning with the MSB ("big-endian"). The word is divided into a leading 14-bit data field followed by a 2-bit address field. When the address field has been decoded, the destination register is loaded on the rising edge of EN. Providing less than 16 bits of data will result in unpredictable behavior when EN goes high.

Data and clock signals are ignored when EN is high. When EN is low, data on the data pin is clocked into a shift register on the rising edge of the CLK pin. This information is loaded into the target control register when EN goes high. This serial interface bus is similar to that commonly found on PLL devices. It can be efficiently programmed by either byte or 16-bit word-oriented serial bus hardware. The data latches are implemented in CMOS and use minimal power when the bus is inactive. Refer to the 3-wire bus timing table and illustration below for timing characteristics, address, and data programming.

3-wire Bus Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Bus Clock (CLK)					
T_r	CLK input rise time			15	ns
T_f	CLK input fall time			15	ns
T_{ck}	CLK period	50			ns
Enable (EN)					
T_{ew}	Minimum pulse width	100			ns
T_L	Delay from last CLK rising ege	15			ns
T_{se}	Set up time to ignore next rising CLK	15			ns
Bus Data (DATA)					
T_s	Data to clock set up time	15			Ns
T_h	Data to clock hold time	15			Ns

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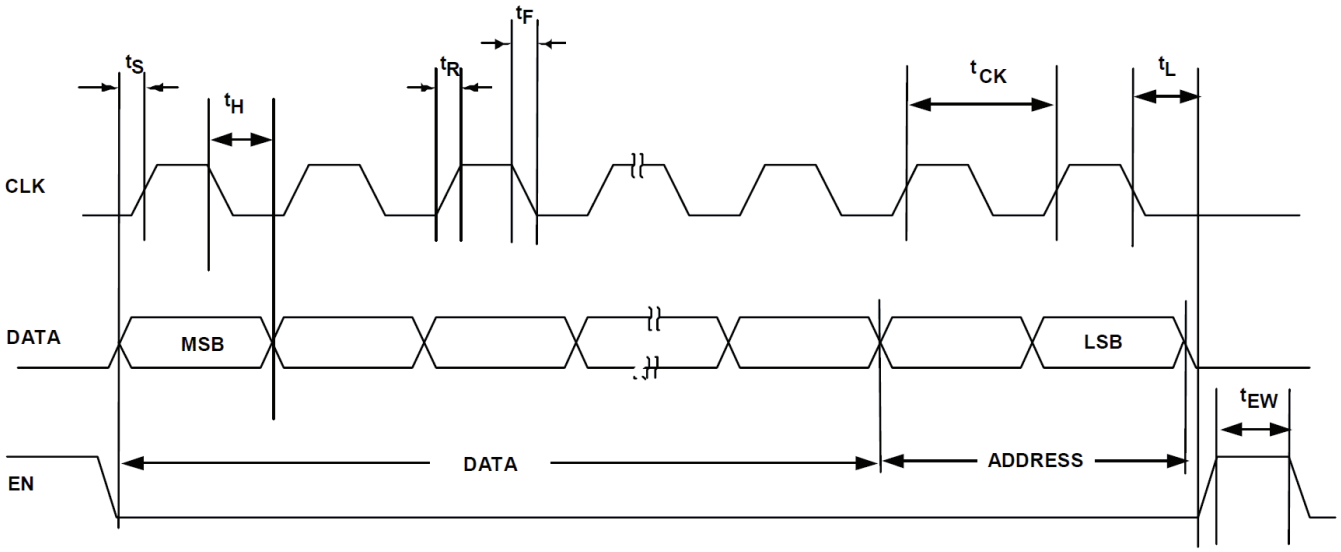
Serial Bus Timing for Address and Data Programming



Control Interfaces and Register Descriptions

Register Information

A 3-wire serial data input bus sets the ML2724's transceiver parameters and programs the PLL circuits. Entering 16-bit words into the ML2724 serial interface performs programming. Three 16-bit registers are partitioned such that 14 bits are dedicated for data to program the operation and two bits identify the register address. The contents of these registers cannot be read back via this bus.

The three registers are:

- **Register 0:** PLL Configuration
- **Register 1:** Channel Frequency Data
- **Register 2:** Internal Test Access

The figure below, shows a register map. The subsequent tables provide detailed diagrams of the register organization. The first two tables outline the PLL configuration and channel frequency registers. The third table displays the filter tuning and test mode register.

Configuration Register Map

MSB															
DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	ADR1	ADR0
Res.	Res.	Res.	Res.	RCLP	LVLO	Res.	TXM	TPC	TXCW	Res.	AOUT	RD0	QPP	0	0
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

MSB															
DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	ADR1	ADR0
Res.	Res.	CHQ11	CHQ10	CHQ9	CHQ8	CHQ7	CHQ6	CHQ5	CHQ4	CHQ3	CHQ2	CHQ1	CHQ0	0	1
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

MSB															
DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	ADR1	ADR0
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DTM2	DTM1	DTM0	ATM2	ATM1	ATM0	1	0
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

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Register 0 – PLL Configuration Register

Name	Description	Definition
Reserved	Reserved	Set to 0 (zero)
Reserved	Reserved	Set to 0
Reserved	Reserved	Set to 0
Reserved	Reserved	Set to 0
RCLP	RSSI Clip Disable	0: RSSI clipped to 1.9V at –15dBm 1: RSSI not clipped
LVLO	Low voltage lockout	0: PAON Undisturbed 1: PAON De-asserted for VCCA<2.65V. Reset on RXON high
Reserved	Reserved	Set to 0
TXM	TX RF Output Mode	0: TX RF Output always on in TX mode 1: TX RF Output follows PAON signal
TPC	Transmit Power Control	0: AOUT pin pulled to ground 1: AOUT pin high impedance
TXCW	Transmit Test Mode	0: FSK modulation in Transmit mode 1: CW (no modulation in Transmit mode)
Reserved	Reserved	Set to 0 (zero)
AOUT	Analog Output	0: AOUT pin is Transmit Power Control 1: AOUT pin is Analog Data Out
RD0	Reference Frequency Select	0: 6.144MHz nominal reference frequency 1: 12.288MHz nominal reference frequency (preferred)
QPP	PLL Charge Pump Polarity	0: For fc < fref, charge pump sources current 1: For fc < fref, charge pump sinks current
ADR1	MSB Address Bit	ADR1=0
ADR0	LSB Address Bit	ADR0=0

Register 1 – Channel Frequency Register

Name	Description	Definition
Reserved	Channel frequency select bits	Set to 0
Reserved	Channel frequency select bits	Set to 0
CHQ11	Channel frequency select bits	Divide ratio=fc/1.024
CHQ10	Channel frequency select bits	Divide ratio=fc/1.024
CHQ9	Channel frequency select bits	Divide ratio=fc/1.024
CHQ8	Channel frequency select bits	Divide ratio=fc/1.024
CHQ7	Channel frequency select bits	Divide ratio=fc/1.024
CHQ6	Channel frequency select bits	Divide ratio=fc/1.024
CHQ5	Channel frequency select bits	Divide ratio=fc/1.024
CHQ4	Channel frequency select bits	Divide ratio=fc/1.024
CHQ3	Channel frequency select bits	Divide ratio=fc/1.024
CHQ2	Channel frequency select bits	Divide ratio=fc/1.024
CHQ1	Channel frequency select bits	Divide ratio=fc/1.024
CHQ0	Channel frequency select bits	Divide ratio=fc/1.024
ADR1	MSB Address Bit	ADR1=0
ADR0	LSB Address Bit	ADR0=0

Register 2 – Test Mode Register

Name	Description	Definition
Reserved	Reserved	Set to 0
Reserved	Reserved	Set to 0
Reserved	Reserved	Set to 0
Reserved	Reserved	Set to 0
Reserved	Reserved	Set to 0
Reserved	Reserved	Set to 0
Reserved	Reserved	Set to 0
Reserved	Reserved	Set to 0
DTM2	Digital test control bits	See table: Digital test control bits
DTM1	Digital test control bits	See table: Digital test control bits
DTM0	Digital test control bits	See table: Digital test control bits
ATM2	Analog test control bits	See table: Analog test control bits
ATM1	Analog test control bits	See table: Analog test control bits
ATM0	Analog test control bits	See table: Analog test control bits
ADR1	MSB address bit	ADR1=0
ADR0	LSB address bit	ADR0=1

Power-On State

On power up, all register bits are cleared to the default value of 0 (zero). Power up is defined as occurring when VDD≥2.0V. The register default values are valid upon power up.

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Control Register Bit Descriptions

ADR<1:0>, All Registers, Bits 0-1

Address Bits: The ADRE <1:0> bits are the least significant bits of each register. Each register is divided into a data field and an address field. The data field is the leading field, while the last two bits clocked into the register are always the address field. When EN goes high, the address field is decoded and the addressed destination register is loaded. The last 16 bits clocked into the serial bus are loaded into the register. Clocking in less than 16 bits results in a potentially incorrect entry into the register.

RES (Reserved), All Registers

Reserved Bits: These bits are reserved. These bits must be cleared to 0s (zeros) for normal operation. When power is reset, all of the registers' data fields are cleared to 0s (zeros).

QPP - Register 0, Bit 2

Charge Pump Polarity: This bit sets the charge pump polarity to sink or source current. For a majority of applications, this bit is cleared (QPP=0). For applications where an external inverting amplifier is used in the loop filter, this bit is set to change the charge pump polarity (see table below).

PLL Charge Pump Polarity

QPP	PLL Charge Pump Polarity
0	$f_c > f_{ref}$ =» Charge pump sinks current.
1	$f_c > f_{ref}$ =» Charge pump sources current.

RDO - Register 0, Bit 3

Reference Divide: This bit sets the reference divider from the FREF pin to the reference input of the PLL phase/frequency detector to either 9 or 18 (see table below).

Reference Frequency Select

RDO	Reference Division	FREF XTAL Freq	PLL Ref Freq
0	9	6.144MHz	682.67kHz
1	18	12.288MHz	682.67kHz

AOUT - Register 0, Bit 4

Analog Output Mode: This bit changes the function of the AOUT pin between an analog data output to transmit power control (see table below).

AOUT Funtion Select

AOUT	AOUT Pin Function
0	Transmit Power Control
1	Data Filter Analog Output

TXCW - Register 0, Bit 6

Transmit Continuous Wave: This bit produces a continuous wave (CW) transmitter output for product test when RXON is low (see table below).

Transmit Modulation Mode

TXCW	Transmit Modulation
0	FSK Modulation
1	CW – No modulation

TPC - Register 0, Bit 7

Transmit Power Control: When the AOUT bit is low, this bit controls the state of the open-drain output pin. Although this bit can be changed at any time, the AOUT pin only changes state at the falling edge of RXON (see table below).

TCP Pin State

TPC	TPC Pin State
0	High impedance
1	Pulled to ground

TXM - Register 0, Bit 8

Transmit Mode: This bit controls the TX RF buffer state timing mode. It must be reset to 0 for normal operation (see table below).

TXMode

TXM	TXRF Buffer Behavior
0	RF output always on in TX mode
1	RF output follows PAON

LVLO - Register 0, Bit 10

Low Voltage Lock Out: The LVLO bit enables a transmit low voltage lockout latch, which shuts off the transmitter by de-asserting the PAON output. This latch is set if the supply voltage drops below 2.65V and is reset when the RXON control input goes high (see table below).

LVLO Operation

LVLO	PAON Behavior
0	PA_{ON} Undisturbed
1	PA_{ON} de-asserted when VCCA<2.65V, Reset by RXON high

RCLP - Register 0, Bit 11

RSSI Clip Enable: The RCLP bit disables the RSSI clipping circuitry. With RCLP low, the RSSI output voltage is clipped to a maximum of about 2.0V at –10dBm. With RCLP high, the RSSI is not clipped (see table below).

RCLP Operation

RCLP	RSSI BEHAVIOR
0	RSSI output clipped to a maximum of ~1.9V at –15dBm
1	RSSI output not clipped

CHQ <11:0> - Register 1, Bits 2-13

Channel Frequency Selection: These bits set the RF carrier frequency for the transceiver (see table below). With a 6.144MHz or 12.288MHz clock at the FREF pin, the channel frequency value is calculated by multiplying the CHQ value by 1.024. The recommended operating range value of the CHQ is from 2,346 to 2,424. These bits must be programmed to a valid channel frequency before XCEN is asserted.

Main Divider

B15	B14	B13 to B2	B1	B0
0	0	CHQ – PLL Divide Ration	0	1

The divide ratio is calculated as $f_C/1.024$ where f_C is the channel frequency in MHz.

$$f_C = 1.024 * CHQ$$

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ATM<2:0> - Register 2, Bits 2-4

Analog Test Mode: The test mode selected is described in the table below. The performance of the ML2724 is not specified in these test modes. Although primarily intended for IC test and debug, they also can help in debugging the radio system. The default (power-up) state of these bits is ATM<2:0>=<0,0,0>. When a non-zero value is written to the field, the RSSI and AOUT pins become analog test access ports, giving access to the outputs of key signal processing stages in the transceiver. During normal operation, ATM<2:0> must be set to all zeros.

Analog Test Control Bits

ATM2	ATM1	ATM0	RSSI	AOUT
0	0	0	RSSI	Set by AOUT bit
0	0	1	No connect	No Connect
0	1	0	I IF Filter Output	Q IF Filter Output
0	1	1	Q IF Filter Output -ve Output	Q IF Filter + ve Output
1	0	0	I IF Filter Output -ve Output	I IF Filter + ve Output
1	0	1	Data Filter +ve Output	Data Filter – ve Output
1	1	0	I IF Filter Ouput +ve Output	Q IF Limiter Outputs
1	1	1	1.67V voltge reference	VCO Modulation Port Input

DTM <2:0> - Register 2, Bits 5-7

Digital Test Mode: The DTM<2:0> bit functions are described in the table below. The performance of the ML2724 is not specified in these test modes. Although primarily intended for IC test and debug, they also can help in debugging the radio system. The default (power up) state of these bits is DTM<2:0>=<0,0,0>. When a non-zero value is written to these fields, the DOUT and PAON pins become a digital test access port for key digital signals in the transceiver. During normal operation, DTM<2:0> must be set to all zeros.

Digital Test Control Bits

DTM2	DTM1	DTM0	PAON	DOUT
0	0	0	PA Control	Data out
0	0	1	PA Control	AGC switch state
0	1	0	PA Control	PLL main divider output
0	1	1	PA Control	PLL reference divider output
1	0	0	S - D Modulation LSB	Sigma - Delta modulation MSB

Data Interfaces

Baseband Interface: DIN & DOUT

The DIN and DOUT pins are digital CMOS signals that correspond to FSK modulation of the carrier frequency. The ML2724 is designed to operate as an FSK transceiver in the 2.4GHz ISM band. Frequency deviation and transmit filtering is determined in the transceiver.

Data on the DIN pin is filtered and presented to the transmit two-port modulator. There is no re-timing of the bits, so the transmitted FSK data takes its timing from the input data. In the receive chain, FSK demodulation, data filtering, and data slicing take place in the ML2724, and the digital data is output on the DOUT pin. Bit and word rate timing recovery are performed off chip. The data filter output is available on the AOUT pin for use with an optional external data slicer.

RSSI & FREF

FREF (pin 9) is the master reference frequency for the transceiver. It supplies the frequency reference for the RF channel frequency and the filter tuning. The FREF pin is a CMOS input with internal biasing resistors. It can be AC coupled to sine or square wave source. The FREF input can also be driven by a CMOS logic output. The frequency of the FREF input is limited to one of: 6.144MHz or 12.288MHz.

The Received Signal Strength Indicator (RSSI) pin supplies a voltage proportional to the logarithm of the received power level. It is normally connected to the input of a low speed ADC and is used during channel scanning to detect clear channels on which the radio may transmit. It can also be used to set transmit power to optimize power consumption while maintaining an acceptable bit error rate (BER).

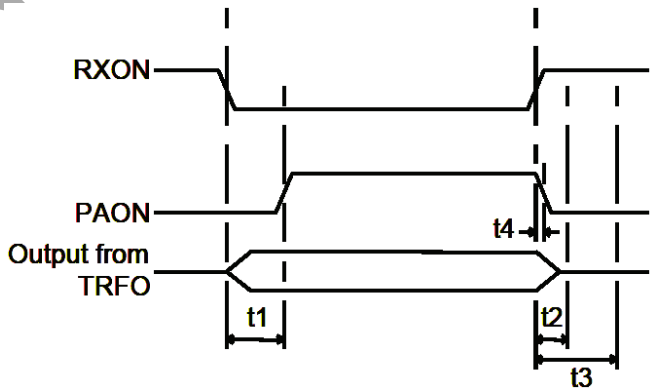
PA Control Outputs (PAON & AOUT)

The PAON (PA control) is a CMOS output that controls an optional off-chip RF PA. It outputs a logic high when the PA should be enabled and a logic low at all other times. This output is inhibited when the PLL fails to lock.

AOUT (pin 7) normally supplies the analog (not data-sliced) data output, but it can also be configured as an open-drain output for transmit power control. This mode is controlled by the TPC bit in Register 0. This bit can be changed at any time, but the AOUT pin will not change mode until the beginning of the next transmit slot, triggered by a falling edge on RXON (see figure and table below).

In analog test modes the RSSI and AOUT pins become analog test access ports that allow the user to observe internal signals in the ML2724.

Power Amplifier Interface



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Power Amplifier Timing

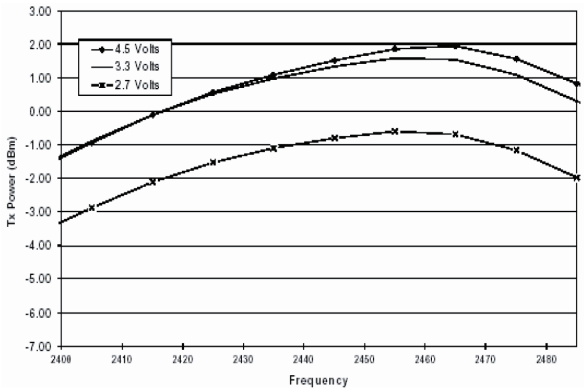
Symbol	Parameter	Time/ μ S
T1	RXON falling edge to PAON rising edge	62.5
T2	RXON rising edge to PLL frequency shift	6.5
T3	RXON rising edge to RECEIVE mode	70
0	RXON rising edge to PAON falling edge	<0.1

RF Interface: RXI & TXO/TXOB

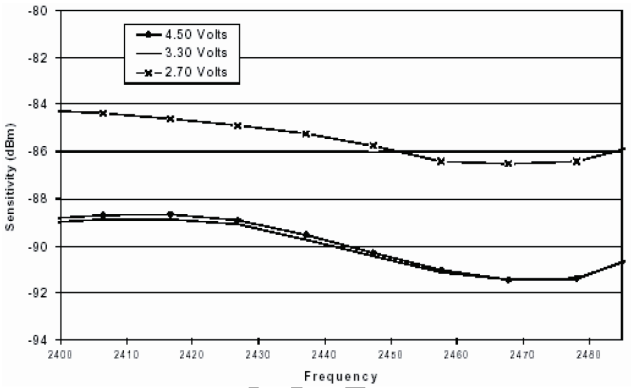
The RXI receive input (pin 17) and the TXO/TXOB differential transmit outputs (pins 21 and 22) are the only RF I/O pins. The RXI pin requires a simple impedance matching network for optimum input noise figure. The TXO/TXOB pins require a matching network for maximum power output into the RF power amp. If a single-ended output is preferred, the signal from the TXO pin can be matched to the power amp and the TXOB output can be shunted to a power supply through a dummy load. The RF input and output ground (pin 18) must have a direct connection to the RF ground plane, and the RF power supply pins must be decoupled to the same ground plane as close to the device as possible.

Performance Graphs

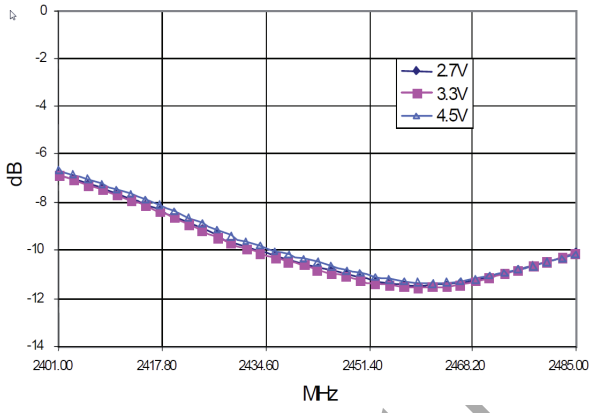
Output Power (Single Ended) vs. Frequency



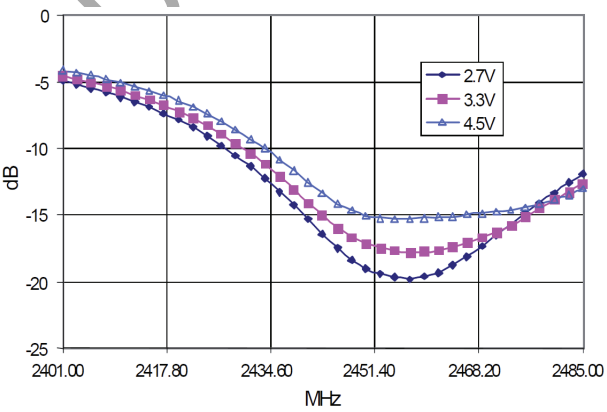
RX Sensitivity (12.5% BER) vs. Frequency



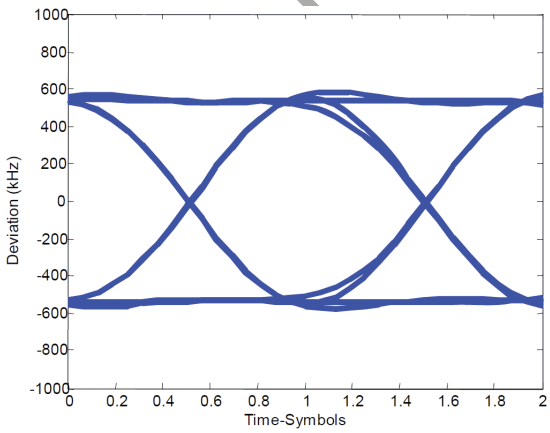
Input Return Loss vs. Frequency and Voltage



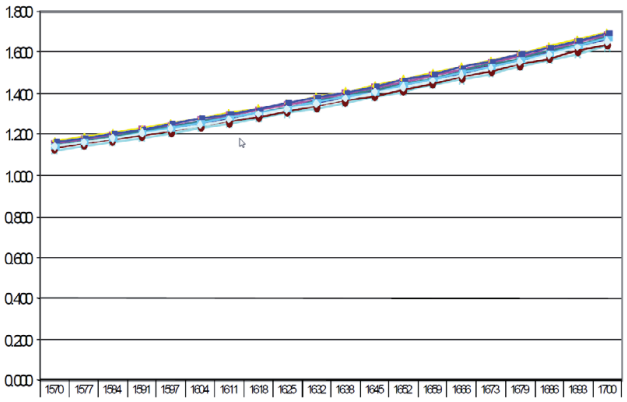
Output Match (SE) vs. Frequency and Voltage



TX Eye Diagram



VCO Tuning Voltage vs. Frequency



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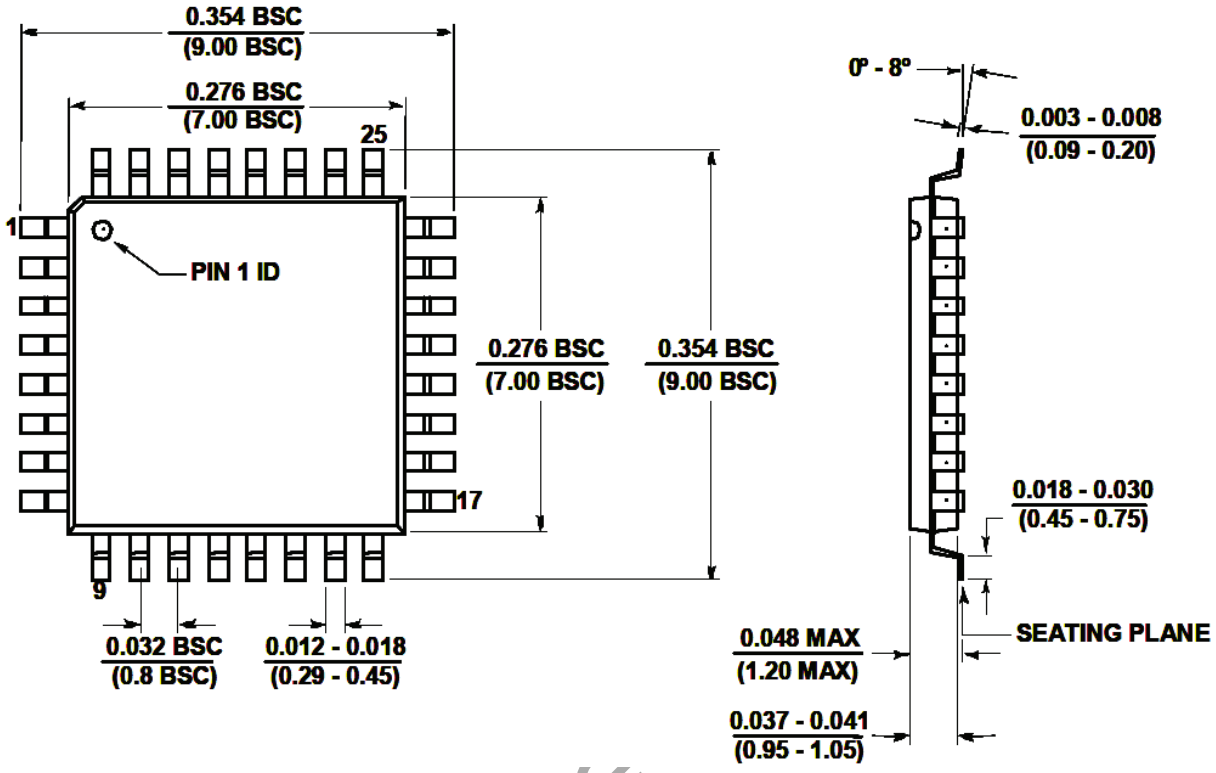
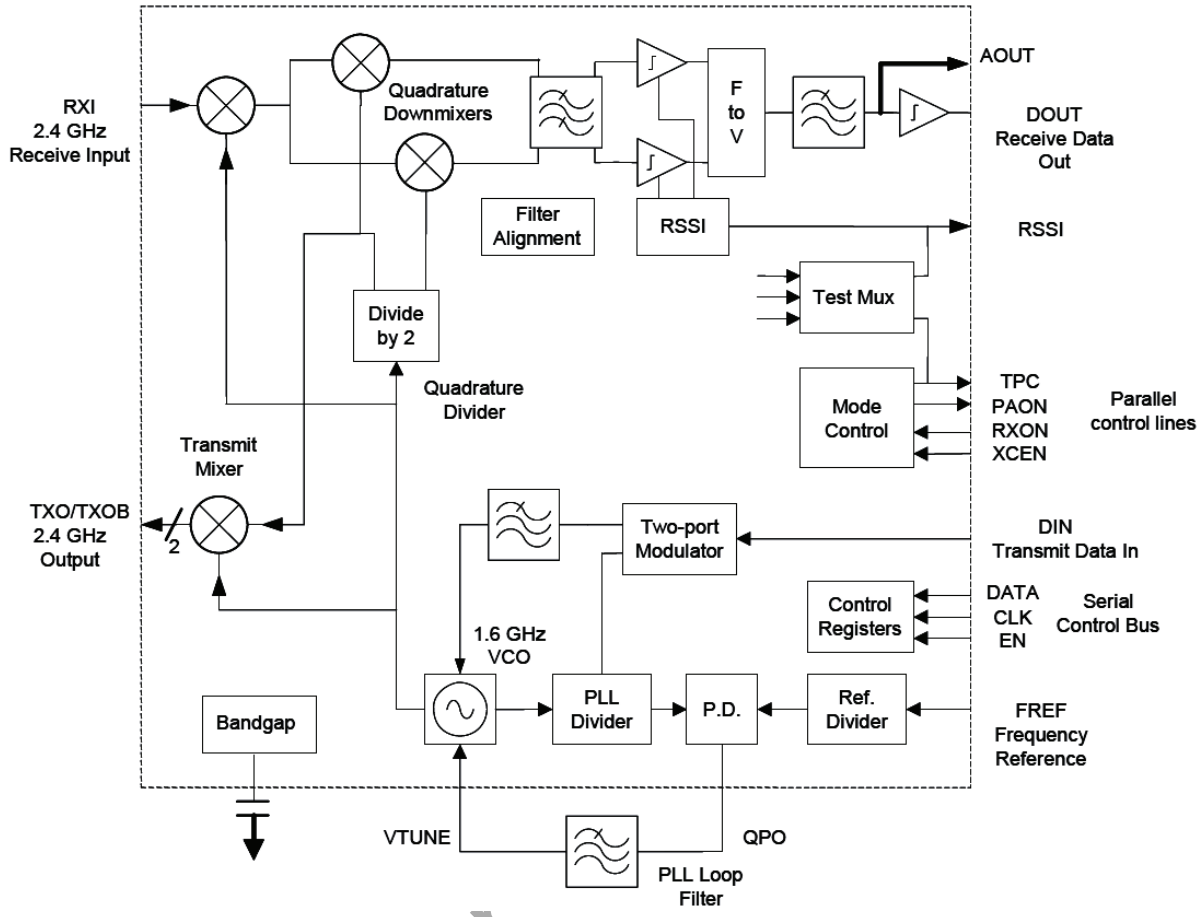
Physical Dimensions (inches/millimeters)



Note: This package meets "Green" Pb-Free requirements and is compliant with the European Union directives WEEE (Waste Electrical and Electronic Equipment) and RoHS (Restriction of the use of certain Hazardous Substances in electrical and electronic equipment). The package pins are finished with 100% matte tin.

Detailed Functional Block Diagram



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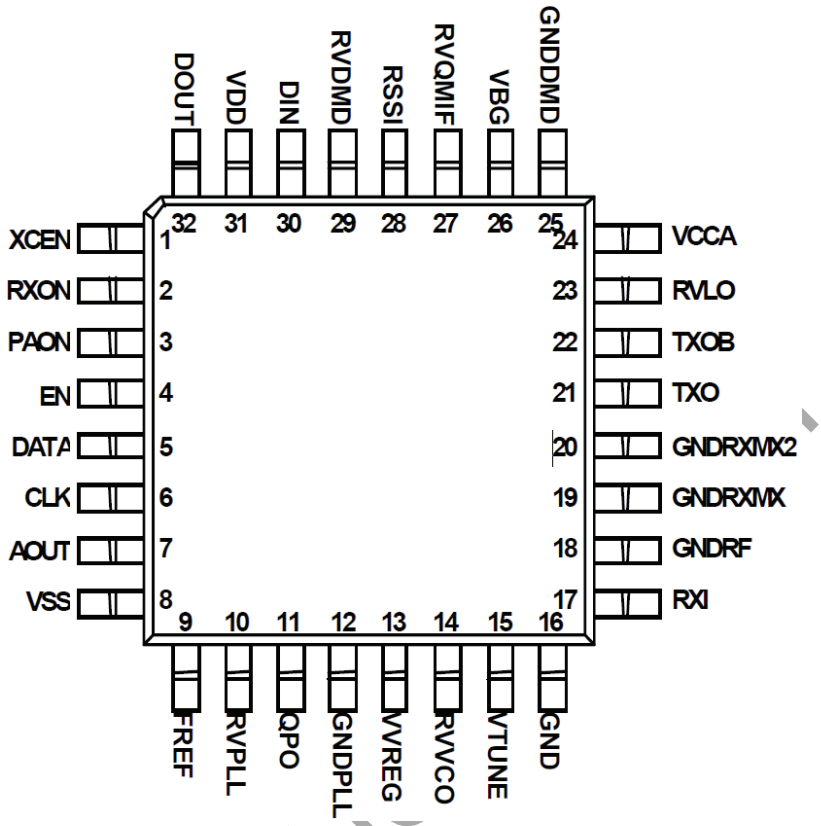
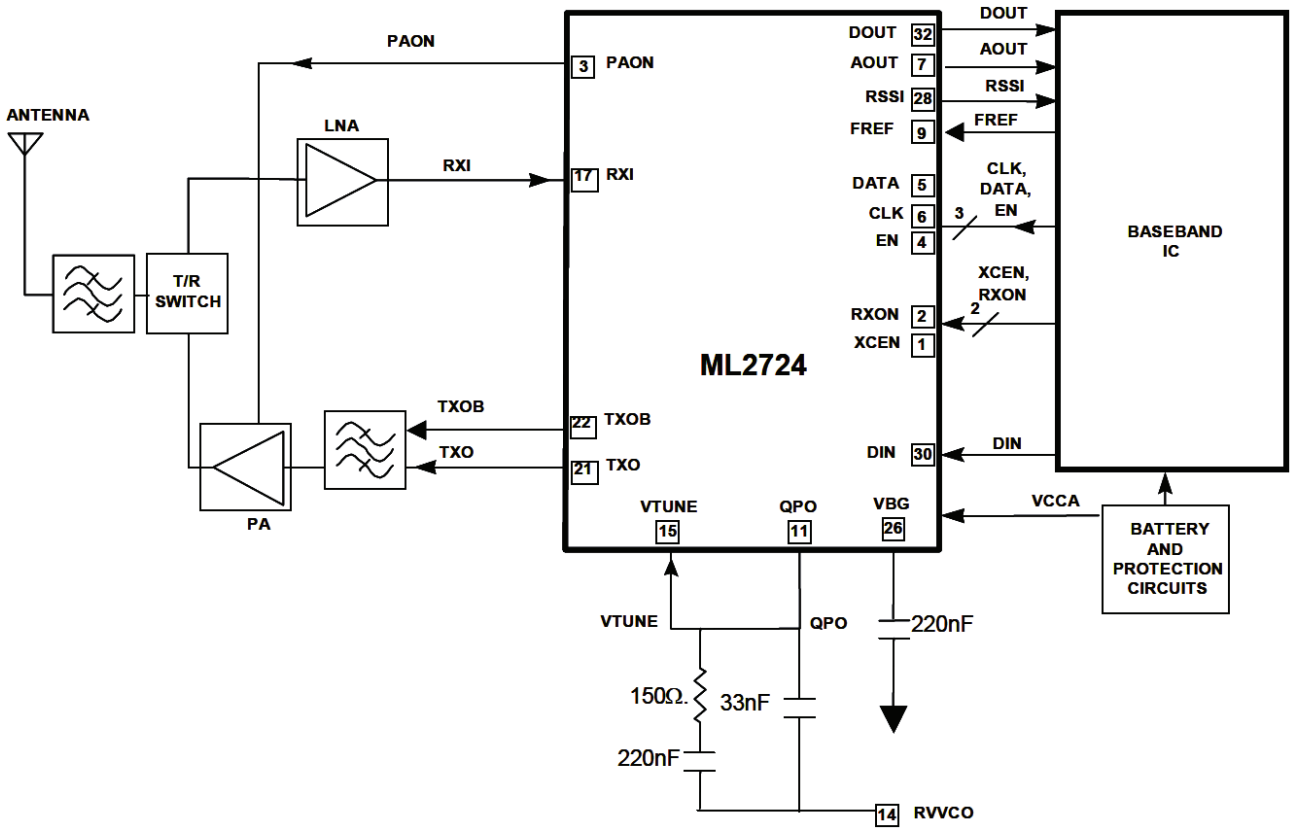
Pin Out



Application Schematic



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Ordering Information

Part Number	Description	Devices/Container
ML2724DH	32TQFP 7mmx7mmx1mm -10°C to 60°C	Antistatic Tray (250)
ML2724DH-T		Tape and Reel (2500)