

October 1987 Revised May 2002

# MM74C89

# 64-Bit 3-STATE Random Access Read/Write Memory

### **General Description**

The MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The four 3-STATE data output lines working in conjunction with the memory enable input provide for easy memory expansion.

**Address Operation:** Address inputs must be stable  $t_{SA}$   $\underline{prior}$   $t_{O}$  the positive to negative transition of  $\overline{memory}$  enable. It is thus not necessary to hold address information stable for more than  $t_{HA}$  after the memory is enabled (positive to negative transition of  $\overline{memory}$  enable).

**Write Operation:** Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable LOW.

**Read Operation:** The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable LOW and write enable HIGH.

When the device is writing or disabled the output assumes a 3-STATE (Hi-z) condition.

### **Features**

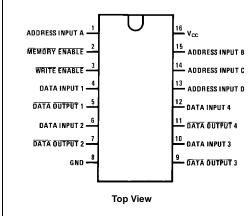
- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45 V<sub>CC</sub> (typ.)
- Low power TTL compatibility: fan out of 2 driving 74L
- Low power consumption: 100 nW/package (typ.)
- Fast access time: 130 ns (typ.) at V<sub>CC</sub> = 10V
- 3-STATE output

**Note:** The timing is different than the DM7489 in that a positive to negative transition of the  $\overline{\text{memory}}$  enable must occur for the memory to be selected.

### **Ordering Code:**

Order Number	Package Number	Package Description	
MM74C89N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide	

### **Connection Diagram**



### **Truth Table**

ME WE Operation		Operation	Condition of Outputs				
٦	L	Write	3-STATE				
L			Complement of Selected Word				
Н	L	Inhibit, Storage Inhibit, Storage	3-STATE				
Н	Н	Inhibit, Storage	3-STATE				

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DS005888

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# MM74C89 **Logic Diagram** READ/WRITE CIRCUITRY INPUT B → ADDRESS DECODER

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# **Absolute Maximum Ratings**(Note 1)

Voltage at any Pin -0.3V to  $V_{CC}$  +0.3V -55°C to +125°C Operating Temperature Range -65°C to +150°C Storage Temperature Range (T<sub>S</sub>)

Power Dissipation (P<sub>D</sub>)

Dual-In-Line 700 mW

Small Outline 500 mW

Operating V<sub>CC</sub> Range 3.0V to 15V Absolute Maximum  $V_{\rm CC}$ 18V

Lead Temperature (T<sub>L</sub>)

(Soldering, 10 seconds) 260°C Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual

device operation.

### **DC Electrical Characteristics**

Symbol	Parameter	Conc
Min/Max lin	nits apply across temperature range, unle	ess otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
CMOS TO	смоѕ	•					
V <sub>IN(1)</sub>	Logical "1" Input Voltage	V <sub>CC</sub> = 5.0V	3.5			V	
		V <sub>CC</sub> = 10V	8.0			V	
V <sub>IN(0)</sub>	Logical "0" Input Voltage	V <sub>CC</sub> = 5.0V			1.5	V	
		V <sub>CC</sub> = 10V			2.0	V	
V <sub>OUT(1)</sub>	Logical "1" Output Voltage	$V_{CC} = 5.0V, I_{O} = -10 \mu A$	4.5			V	
		$V_{CC} = 10V$ , $I_O = -10 \mu A$	9.0			V V	
V <sub>OUT(0)</sub>	Logical "0" Output Voltage	$V_{CC} = 5.0V, I_{O} = +10 \mu A$			0.5	V	
		$V_{CC} = 10V, I_{O} = +10 \mu A$			1.0	v	
I <sub>IN(1)</sub>	Logical "1" Input Current	V <sub>CC</sub> = 15V, V <sub>IN</sub> = 15V		-0.005	1.0	μΑ	
I <sub>IN(0)</sub>	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μΑ	
l <sub>oz</sub>	Output Current in	V <sub>CC</sub> = 15V, V = 15V		0.005	1.0	μА	
	High Impedance State	$V_{CC} = 15V, V_{O} = 0V$	-1.0	-0.005		μΛ	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = 15V		0.05	300	μΑ	
CMOS/LP1	TL INTERFACE	•				•	
V <sub>IN(1)</sub>	Logical "1" Input Voltage	V <sub>CC</sub> = 4.75V	V <sub>CC</sub> – 1.5			V	
V <sub>IN(0)</sub>	Logical "0" Input Voltage	V <sub>CC</sub> = 4.75V			0.8	V	
V <sub>OUT(1)</sub>	Logical "1" Output Voltage	$V_{CC} = 4.75V, I_{O} = -360 \mu A$	2.4			V	
V <sub>OUT(0)</sub>	Logical "0" Output Voltage	$V_{CC} = 4.75V$ , $I_{O} = +360 \mu A$			0.4	V	
OUTPUT D	RIVE (See 54C/74C Family Chara	cteristics Data Sheet) (Short Circuit Cu	irrent)				
I <sub>SOURCE</sub>	Output Source Current	$V_{CC} = 5.0V$ , $V_{OUT} = 0V$	-1.75 -:	-3.3		mA	
	(P-Channel)	$T_A = 25^{\circ}C$	10	3.3			
I <sub>SOURCE</sub>	Output Source Current	$V_{CC} = 10V, V_{OUT} = 0V$	-8.0	-15		mA	
	(P-Channel)	$T_A = 25^{\circ}C$	-0.0				
I <sub>SINK</sub>	Output Sink Current	$V_{CC} = 5.0V$ , $V_{OUT} = V_{CC}$	1.75	3.6		mA	
	(N-Channel)	$T_A = 25^{\circ}C$	1.75				
I <sub>SINK</sub>	Output Sink Current	V <sub>CC</sub> = 10V, V <sub>OUT</sub> = V <sub>CC</sub>	8.0	16		mA	
	(N-Channel)	$T_A = 25^{\circ}C$	0.0				

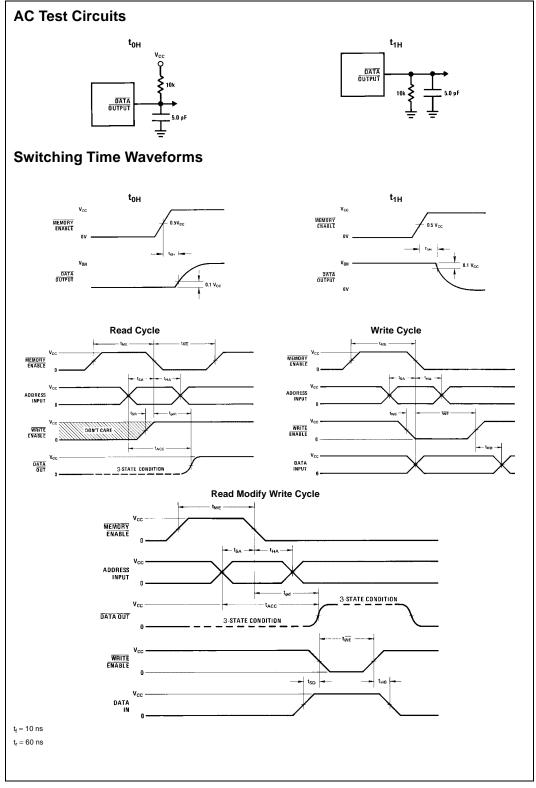
# AC Electrical Characteristics (Note 2)

 $T_A = 25$ °C,  $C_L = 50$  pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
t <sub>pd</sub>	Propagation Delay from	V <sub>CC</sub> = 5V		270	500	ns	
	Memory Enable	V <sub>CC</sub> = 10V		100	220		
t <sub>ACC</sub>	Access Time from	V <sub>CC</sub> = 5V		350	650	ns	
	Address Input	V <sub>CC</sub> = 10V		130	280		
t <sub>SA</sub>	Address Setup Time	V <sub>CC</sub> = 5V	150			ne	
		V <sub>CC</sub> = 10V	60			ns	
t <sub>HA</sub>	Address Hold Time	V <sub>CC</sub> = 5V	60			no	
		V <sub>CC</sub> = 10V	40			ns	
t <sub>ME</sub>	Memory Enable Pulse Width	V <sub>CC</sub> = 5V	400	250		ns	
		V <sub>CC</sub> = 10V	150	90			
t <sub>SR</sub>	Write Enable Setup	V <sub>CC</sub> = 5V	0			ns	
	Time for a Read	V <sub>CC</sub> = 10V	0				
t <sub>WS</sub>	Write Enable Setup	V <sub>CC</sub> = 5V			t <sub>ME</sub>	ns	
	Time for a Write	V <sub>CC</sub> = 10V			t <sub>ME</sub>		
t <sub>WE</sub>	Write Enable Pulse Width	$V_{CC} = 5V$ , $t_{WS} = 0$	300	160		ns	
		$V_{CC} = 10V, t_{WS} = 0$	100	60			
t <sub>HD</sub>	Data Input Hold Time	V <sub>CC</sub> = 5V	50			no	
		V <sub>CC</sub> = 10V	25			ns	
t <sub>SD</sub>	Data Input Setup	V <sub>CC</sub> = 5V	50			ns	
		V <sub>CC</sub> = 10V	25				
t <sub>1H</sub> , t <sub>0H</sub>	Propagation Delay from a Logical	$V_{CC} = 5V, C_L = 5 pF, R_L = 10k$		180	300	ns	
	"1" or Logical "0" to the High	$V_{CC} = 10V, C_L = 5 pF, R_L = 10k$		-85	120		
	Impedance State from Memory Enable						
t <sub>1H</sub> , t <sub>0H</sub>	Propagation Delay from a Logical	$V_{CC} = 50V, C_L = 5 pF, R_L = 10k$		180	300	ns	
	"1" or Logical "0" to the High	$V_{CC} = 10V, C_L = 5 pF, R_L = 10k$		85	120		
	Impedance State from Write Enable						
C <sub>IN</sub>	Input Capacity	Any Input (Note 3)		5		pF	
C <sub>OUT</sub>	Output Capacity	Any Output (Note 3)		6.5		pF	
C <sub>PD</sub>	Power Dissipation Capacity	(Note 4)		230		pF	

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C<sub>PD</sub> determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics application note, AN-90.



#### Physical Dimensions inches (millimeters) unless otherwise noted 0.740 - 0.780 0.090 (18.80 - 19.81)(2.286)<u>16 15 14 13 12 11 10 9</u> [6] [15] [ INDEX AREA 0.250 ± 0.010 $(6.350 \pm 0.254)$ PIN NO. 1 PIN NO. 1 2 3 4 5 6 7 8 1 2 IDENT IDENT OPTION 02 0.065 0.130 ± 0.005 $\frac{0.060}{(1.524)}$ 4º TYP 0.300 - 0.320 (1.651)(3.302 ± 0.127) OPTIONAL (7.620 - 8.128) 0.145 - 0.200 (3.683 - 5.080) 95°±5° $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 900 + 40 TYP 0.020 MIN 0.280 (0.508) $\frac{0.125 - 0.150}{(3.175 - 3.810)}$ (7.112) MIN $(0.762 \pm 0.381)$ 0.014 - 0.023 0.100 ± 0.010 (0.325 +0.040 -0.015 (0.356 - 0.584) $(2.540 \pm 0.254)$ 0.050 ± 0.010 (1.270 ± 0.254) N16E (REV F) TYP

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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