

MM70C95/MM80C95, MM70C97/MM80C97 TRI-STATE® Hex Buffers MM70C96/MM80C96, MM70C98/MM80C98 TRI-STATE Hex Inverters

General Description

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The MM70C95/MM80C95 and the MM70C97/MM80C97 convert CMOS or TTL outputs to TRI-STATE outputs with no logic inversion, the MM70C96/MM80C96 and the MM70C98/MM80C98 provide the logical opposite of the input signal. The MM70C95/MM80C95 and the MM70C96/MM80C96 have common TRI-STATE controls for all six devices. The MM70C97/MM80C97 and the MM70C98/MM80C98 have two TRI-STATE controls; one for two devices and one for the other four devices. Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

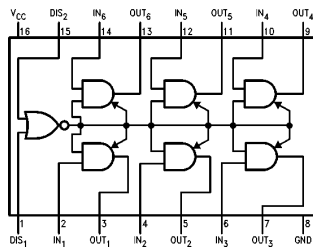
- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} (typ.)
- TTL compatible Drive 1 TTL Load

Applications

- Bus drivers Typical propagation delay into 150 pF load is 40 ns

Connection Diagrams (Dual-In-Line Packages)

MM70C95/MM80C95

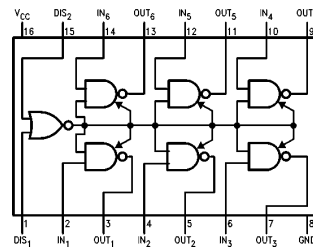


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Top View

Order Number MM70C95 or MM80C95

MM70C96/MM80C96

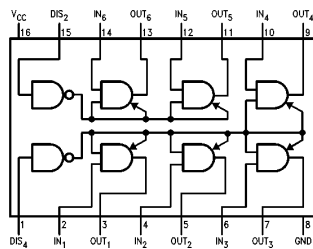


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Top View

Order Number MM70C96 or MM80C96

MM70C97/MM80C97

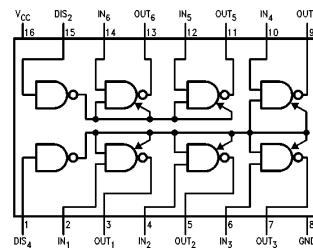


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Top View

Order Number MM70C97 or MM80C97

MM70C98/MM80C98



TL/F/5907-4

Top View

Order Number MM70C98 or MM80C98

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	−0.3V to $V_{CC} + 0.3V$
Operating Temperature Range	−55°C to +125°C
MM70CXX	−40°C to +85°C
MM80CXX	

Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Power Supply Voltage (V_{CC})	18V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical “1” Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical “0” Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical “1” Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical “0” Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			0.5 1.0	V V
$I_{IN(1)}$	Logical “1” Input Current	$V_{CC} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical “0” Input Current		−1.0	−0.005		μA
I_{OZ}	Output Current in High Impedance State	$V_{CC} = 15V, V_O = 15V$ $V_{CC} = 15V, V_O = 0V$	−1.0	0.005 −0.005	1.0	μA μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.01	15	μA

TTL INTERFACE

$V_{IN(1)}$	Logical “1” Input Voltage	70C $V_{CC} = 4.5V$ 80C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical “0” Input Voltage	70C $V_{CC} = 4.5V$ 80C $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical “1” Output Voltage	70C $V_{CC} = 4.5V, I_O = -1.6 mA$ 80C $V_{CC} = 4.75V, I_O = -1.6 mA$	2.4 2.4			V V
$V_{OUT(0)}$	Logical “0” Output Voltage	70C $V_{CC} = 4.5V, I_O = 1.6 mA$ 80C $V_{CC} = 4.75V, I_O = 1.6 mA$			0.4 0.4	V V

OUTPUT DRIVE (Short Circuit Current)

I_{SOURCE}	Output Source Current	$V_{CC} = 5V, V_{IN(1)} = 5V$ $T_A = 25^\circ C, V_{OUT} = 0V$	−4.35			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V, V_{IN(1)} = 10V$ $T_A = 25^\circ C, V_{OUT} = 0V$	−20			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V, V_{IN(0)} = 0V$ $T_A = 25^\circ C, V_{OUT} = V_{CC}$	4.35			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V, V_{IN(0)} = 0V$ $T_A = 25^\circ C, V_{OUT} = V_{CC}$	20			mA

Note 1: “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the device should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

AC Electrical Characteristics* $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0} , t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output MM70C95/MM80C95, MM70C97/MM80C97 MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		60 25 70 35	100 40 150 75	ns ns ns ns
t_{pd0} , t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output MM70C95/MM80C95, MM70C97/MM80C97 MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5\text{V}$, $C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}$, $C_L = 150\text{ pF}$ $V_{CC} = 5\text{V}$, $C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}$, $C_L = 150\text{ pF}$		85 40 95 45	160 80 210 110	ns ns ns ns
t_{1H} , t_{0H}	Delay from Disable Input to High Impedance State, (from Logical "1" or Logical "0") MM70C95/MM80C95 MM70C96/MM80C96 MM70C97/MM80C97 MM70C98/MM80C98	$R_L = 10\text{k}$, $C_L = 5\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		80 50 100 70 70 50 90 70	135 90 180 125 125 90 170 125	ns ns ns ns ns ns ns ns
t_{H1} , t_{H0}	Delay from Disable Input to Logical "1" Level (from High Impedance State) MM70C95/MM80C95 MM70C96/MM80C96 MM70C97/MM80C97 MM70C98/MM80C98	$R_L = 10\text{k}$, $C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		120 50 130 60 95 40 120 50	200 90 225 110 175 80 200 90	ns ns ns ns ns ns ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacitance TRI-STATE	Any Output (Note 2)		11		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		60		pF

*AC Parameters are guaranteed by DC correlated testing.

Truth Tables

MM70C95/MM80C95

Disable DIS ₁	Input DIS ₂	Input	Output
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C96/MM80C96

Disable DIS ₁	Input DIS ₂	Input	Output
0	0	0	1
0	0	1	0
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C97/MM80C97

Disable DIS ₄	Input DIS ₂	Input	Output
0	0	0	0
0	0	1	1
X	1	X	H-z*
1	X	X	H-z**

MM70C98/MM80C98

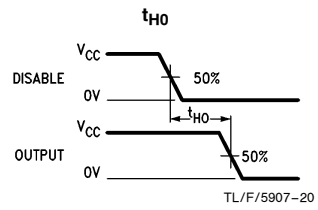
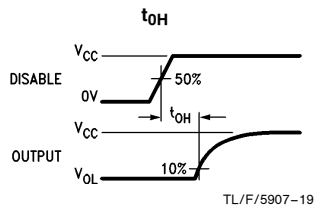
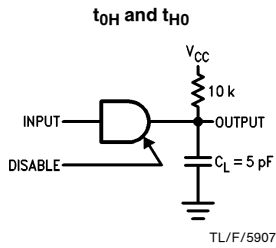
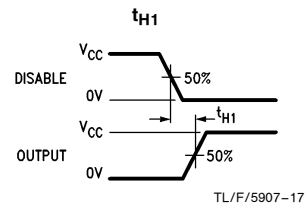
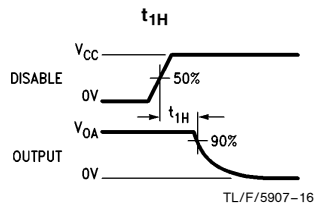
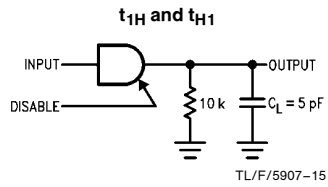
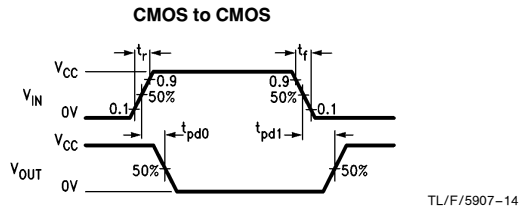
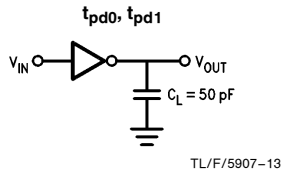
Disable DIS ₄	Input DIS ₂	Input	Output
0	0	0	1
0	0	1	0
X	1	X	H-z*
1	X	X	H-z**

*Output 5–6 only

**Output 1–4 only

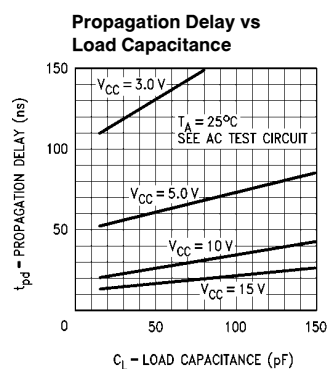
X = Irrelevant

AC Test Circuits and Switching Time Waveforms

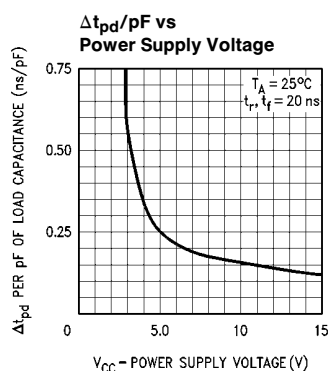


Note: Delays measured with input t_r , $t_f \leq 20$ ns.

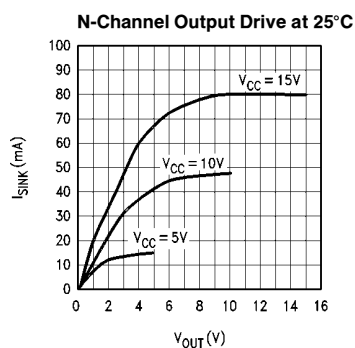
Typical Performance Characteristics



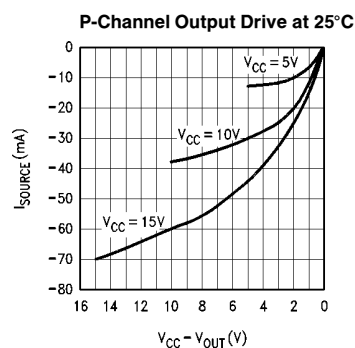
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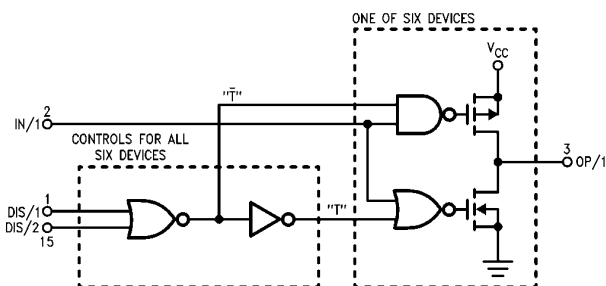
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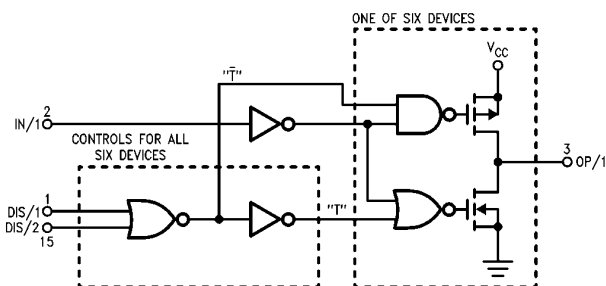
Schematic Diagrams

MM70C95/MM80C95 TRI-STATE



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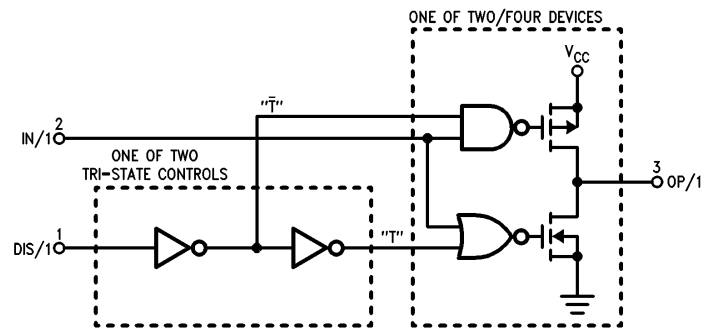
MM70C96/MM80C96 TRI-STATE



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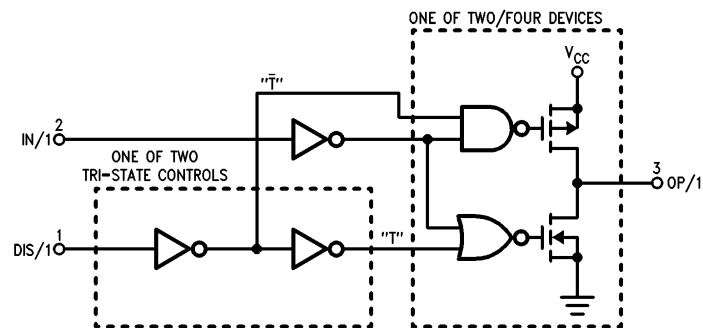
Schematic Diagrams (Continued)

MM70C97/MM80C97 TRI-STATE



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MM70C98/MM80C98 TRI-STATE



TL/F/5907-12

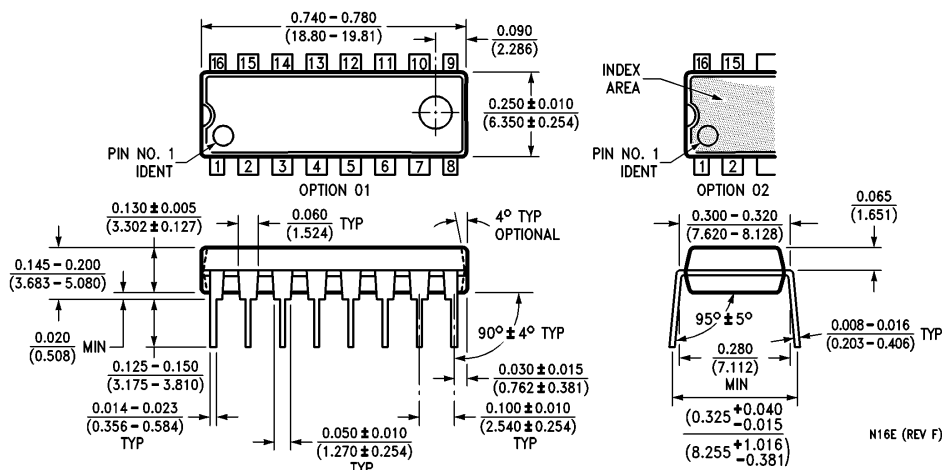
The image contains three mechanical drawings of the J16A (REV L) package:

- Top View:** Shows a rectangular package with 16 pins (8 on each long side). Dimensions include a total width of $0.785 [19.94] \text{ MAX}$, a pin pitch of $0.037 \pm 0.005 [0.94 \pm 0.13] \text{ TYP}$, and a pin diameter of $0.025 [0.64]$. The package body has a width of $0.220-0.310 [5.59-7.87]$ and a thickness of $0.005-0.020 \text{ TYP} [0.13-0.51]$. A corner radius of $R 0.025 [0.64]$ is specified.
- Side View:** Shows the package height and pin details. The maximum height is $0.200 [5.08] \text{ MAX TYP}$. The pin height is $0.125-0.200 [3.18-5.08] \text{ TYP}$. The pin diameter is $0.080 [2.03] \text{ MAX}$ at both ends. The pin angle is $90^\circ \pm 4^\circ \text{ TYP}$. The pin spacing is $0.018 \pm 0.003 [0.46 \pm 0.08] \text{ TYP}$. The package body thickness is $0.020-0.060 [0.51-1.52] \text{ TYP}$.
- Cross-sectional View:** Shows the package mounted on a substrate with glass sealant. The package height is $0.290-0.320 [7.37-8.13]$. The sealant thickness is $0.180 \text{ MAX} [4.57]$. The package body thickness is $0.010 \pm 0.002 [0.25 \pm 0.05] \text{ TYP}$. The pin angle is $95^\circ \pm 5^\circ \text{ TYP}$. The substrate thickness is $0.310-0.410 [7.87-10.41]$.

J16A (REV L)

J16A (REV L)

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number MM70C95N, MM70C96N, MM70C97N, MM70C98N,
MM80C95N, MM80C96N, MM80C97N or MM80C98N
NS Package Number N16E

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