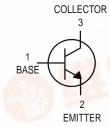
Amplifier Transistors NPN Silicon



MMBT6428LT1 MMBT6429LT1



CASE 318-08, STYLE 6 SOT-23 (TO-236AB)

WWW.DZSC

MAXIMUM RATINGS

Rating	Symbol	6428LT1	6429LT1	Unit
Collector-Emitter Voltage	VCEO	50	45	Vdc
Collector - Base Voltage	V _{CBO}	60	55	Vdc
Emitter-Base Voltage	VEBO	6.0		Vdc
Collector Current — Continuous	IC	200		mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board ⁽¹⁾ T _A = 25°C	PD	225	mW
Derate above 25°C	750.0V	1.8	mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate,(2) T _A = 25°C	PD	300	mW
Derate above 25°C		2.4	mW/°C
Thermal Resistance, Junction to Ambient	$R_{ heta JA}$	417	°C/W
Junction and Storage Temperature	TJ, T _{Stg}	-55 to +150	°C

DEVICE MARKING

MMBT6428LT1 = 1KM; MMBT6429LT1 = 1L

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS		•		•	
Collector-Emitter Breakdown Voltage (IC = 1.0 mAdc, IB = 0) (IC = 1.0 mAdc, IB = 0)	MMBT6428 MMBT6429	V _{(BR)CEO}	50 45	南南	Vdc
Collector-Base Breakdown Voltage (I _C = 0.1 mAdc, I _E = 0) (I _C = 0.1 mAdc, I _E = 0)	MMBT6428 MMBT6429	V(BR)CBO	60 55	ZSC.C.	Vdc
Collector Cutoff Current (V _{CE} = 30 Vdc)	Chin and	ICES	_	0.1	μAdc
Collector Cutoff Current (V _{CB} = 30 Vdc, I _E = 0)		ICBO	_	0.01	μAdc
Emitter Cutoff Current (VEB = 5.0 Vdc, IC = 0)		IEBO	_	0.01	μAdc

- 1. FR-5 = $1.0 \times 0.75 \times 0.062$ in.
- 2. Alumina = $0.4 \times 0.3 \times 0.024$ in. 99.5% alumina.



ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$ unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS		•		•	
DC Current Gain (I _C = 0.01 mAdc, V _{CE} = 5.0 Vdc)	MMBT6428 MMBT6429	h _{FE}	250 500	_ _	_
$(I_C = 0.1 \text{ mAdc}, V_{CE} = 5.0 \text{ Vdc})$	MMBT6428 MMBT6429		250 500	650 1250	
$(I_C = 1.0 \text{ mAdc}, V_{CE} = 5.0 \text{ Vdc})$	MMBT6428 MMBT6429		250 500	_ _	
$(I_C = 10 \text{ mAdc}, V_{CE} = 5.0 \text{ Vdc})$	MMBT6428 MMBT6429		250 500	_ _	
Collector-Emitter Saturation Voltage ($I_C = 10 \text{ mAdc}$, $I_B = 0.5 \text{ mAdc}$) ($I_C = 100 \text{ mAdc}$, $I_B = 5.0 \text{ mAdc}$)		VCE(sat)	_	0.2 0.6	Vdc
Base-Emitter On Voltage (I _C = 1.0 mAdc, V _{CE} = 5.0 mAdc)		V _{BE} (on)	0.56	0.66	Vdc
SMALL-SIGNAL CHARACTERISTICS		-		-	
Current-Gain — Bandwidth Product (I _C = 1.0 mAdc, V _{CE} = 5.0 Vdc, f = 100 MHz)		fΤ	100	700	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 MHz)		C _{obo}	_	3.0	pF
Input Capacitance (VEB = 0.5 Vdc, I _C = 0, f = 1.0 MHz)		C _{ibo}	_	8.0	pF

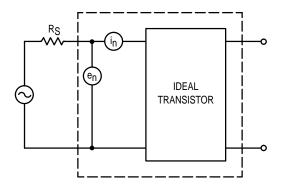
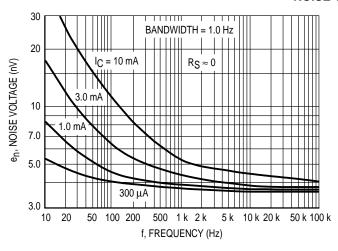


Figure 1. Transistor Noise Model

NOISE CHARACTERISTICS

 $(VCE = 5.0 Vdc, TA = 25^{\circ}C)$

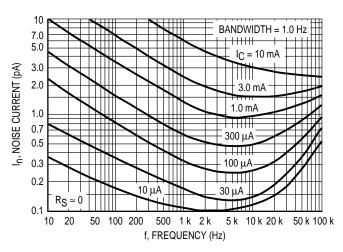
NOISE VOLTAGE



BANDWIDTH = 1.0 Hz 20 $R_S \approx 0$ en, NOISE VOLTAGE (nV) f = 10 Hz 10 7.0 1.0 kHz 5.0 100 kHz 3.0 0.01 0.02 0.5 1.0 5.0 10 IC, COLLECTOR CURRENT (mA)

Figure 2. Effects of Frequency

Figure 3. Effects of Collector Current



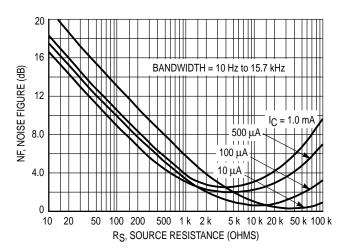
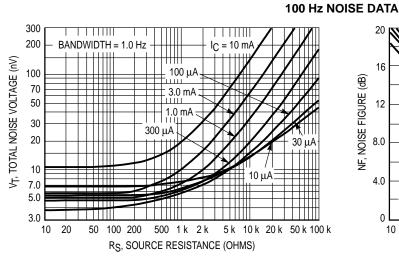


Figure 4. Noise Current

Figure 5. Wideband Noise Figure



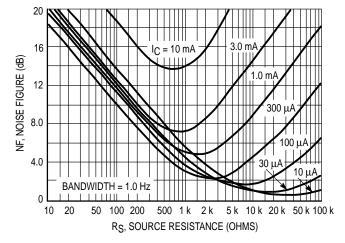


Figure 6. Total Noise Voltage

Figure 7. Noise Figure

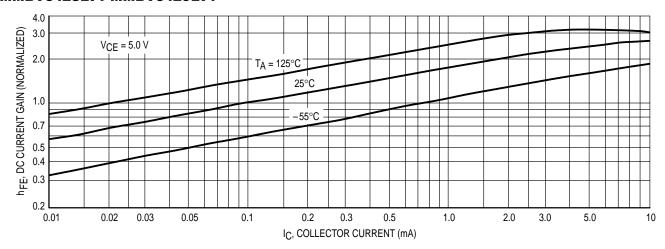


Figure 8. DC Current Gain

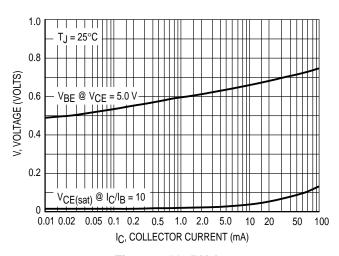


Figure 9. "On" Voltages

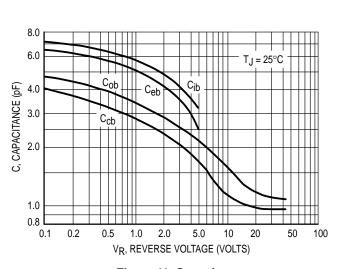


Figure 11. Capacitance

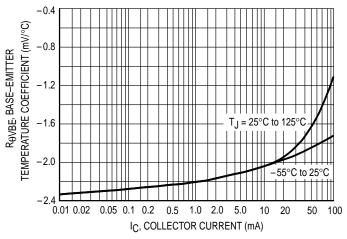


Figure 10. Temperature Coefficients

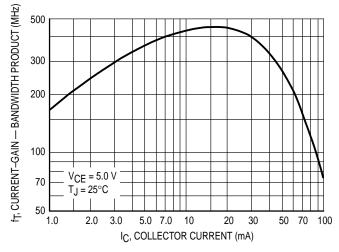
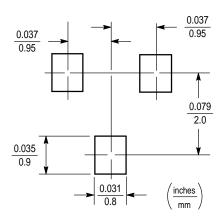


Figure 12. Current-Gain — Bandwidth Product

INFORMATION FOR USING THE SOT-23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-23

SOT-23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $\mathsf{TJ}_{(\text{max})}$, the maximum rated junction temperature of the die, $\mathsf{R}_{\theta}\mathsf{JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_{A} . Using the values provided on the data sheet for the SOT–23 package, P_{D} can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150^{\circ}C - 25^{\circ}C}{556^{\circ}C/W} = 225 \text{ milliwatts}$$

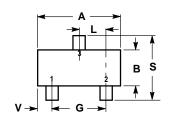
The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

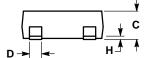
SOLDERING PRECAUTIONS

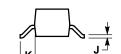
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes.
 Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.
- * Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS







CASE 318-08 SOT-23 (TO-236AB) ISSUE AE

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.1102	0.1197	2.80	3.04
В	0.0472	0.0551	1.20	1.40
С	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
Н	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
٧	0.0177	0.0236	0.45	0.60

STYLE 6:

PIN 1. BASE

EMITTER

COLLECTOR

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How to reach us:

USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE (602) 244-6609 INTERNET: http://Design-NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

