

# MMBTA20LT1

## General Purpose Amplifier

### NPN Silicon

#### Features

- Pb-Free Package is Available



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#### MAXIMUM RATINGS

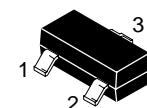
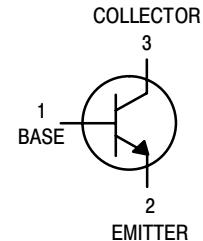
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	40	Vdc
Emitter-Base Voltage	$V_{EBO}$	4.0	Vdc
Collector Current – Continuous	$I_C$	100	mAdc

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board, (Note 1) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate, (Note 2) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

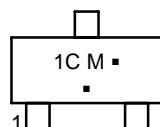
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR-5 =  $1.0 \times 0.75 \times 0.062$  in.
2. Alumina =  $0.4 \times 0.3 \times 0.024$  in. 99.5% alumina.



**SOT-23 (TO-236)  
CASE 318  
STYLE 6**

#### MARKING DIAGRAM



1C = Specific Device Code

M = Date Code\*

■ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or overbar may vary depending upon manufacturing location.

#### ORDERING INFORMATION

Device	Package	Shipping†
MMBTA20LT1	SOT-23	3,000 / Tape & Reel
MMBTA20LT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel

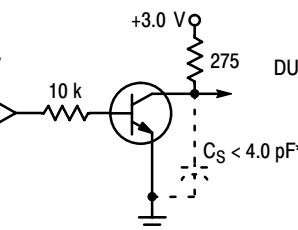
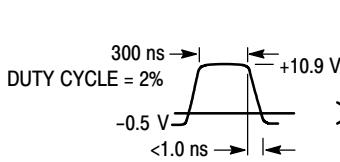
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MMBTA20LT1

ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Breakdown Voltage ( $I_C = 1.0 \text{ mA}$ , $I_B = 0$ )	$V_{(\text{BR})\text{CEO}}$	40	—	Vdc
Emitter-Base Breakdown Voltage ( $I_E = 100 \mu\text{A}$ , $I_C = 0$ )	$V_{(\text{BR})\text{EBO}}$	4.0	—	Vdc
Collector Cutoff Current ( $V_{CB} = 30 \text{ Vdc}$ , $I_E = 0$ )	$I_{\text{CBO}}$	—	100	nAdc
<b>ON CHARACTERISTICS</b>				
DC Current Gain ( $I_C = 5.0 \text{ mA}$ , $V_{CE} = 10 \text{ Vdc}$ )	$h_{\text{FE}}$	40	400	—
Collector-Emitter Saturation Voltage ( $I_C = 10 \text{ mA}$ , $I_B = 1.0 \text{ mA}$ )	$V_{CE(\text{sat})}$	—	0.25	Vdc
<b>SMALL-SIGNAL CHARACTERISTICS</b>				
Current-Gain – Bandwidth Product ( $I_C = 5.0 \text{ mA}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 100 \text{ MHz}$ )	$f_T$	125	—	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 1.0 \text{ MHz}$ )	$C_{\text{obo}}$	—	4.0	pF

## EQUIVALENT SWITCHING TIME TEST CIRCUITS



\*Total shunt capacitance of test jig and connectors

Figure 1. Turn-On Time

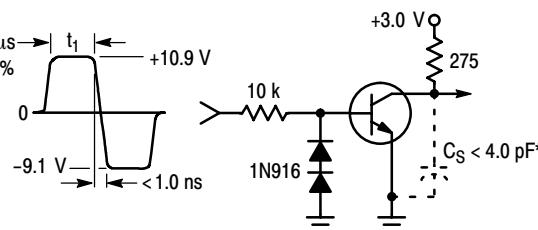


Figure 2. Turn-Off Time

## TYPICAL NOISE CHARACTERISTICS

( $V_{CE} = 5.0$  Vdc,  $T_A = 25^\circ\text{C}$ )

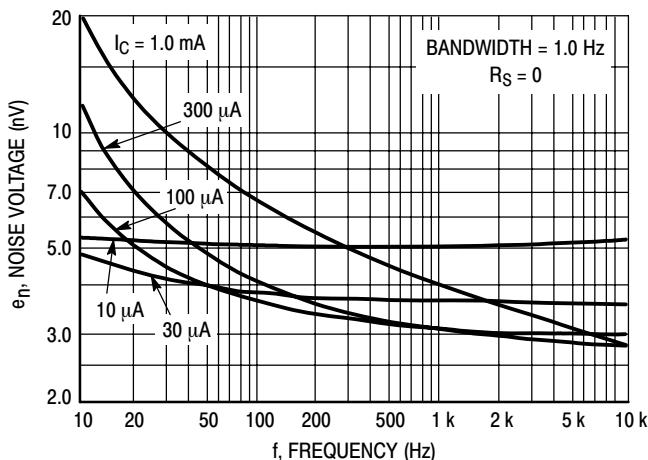


Figure 3. Noise Voltage

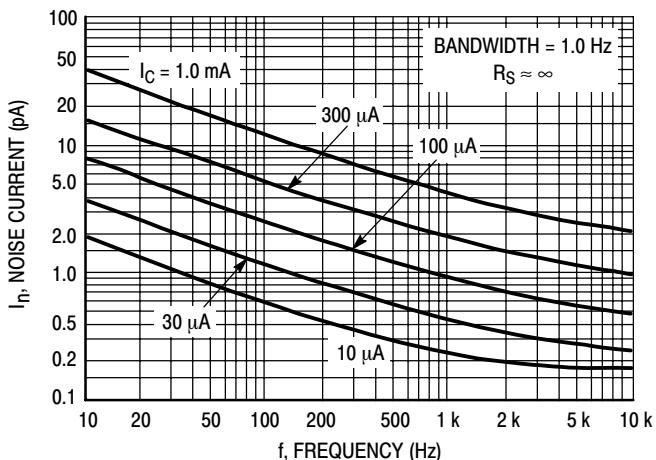


Figure 4. Noise Current

## NOISE FIGURE CONTOURS

( $V_{CE} = 5.0$  Vdc,  $T_A = 25^\circ\text{C}$ )

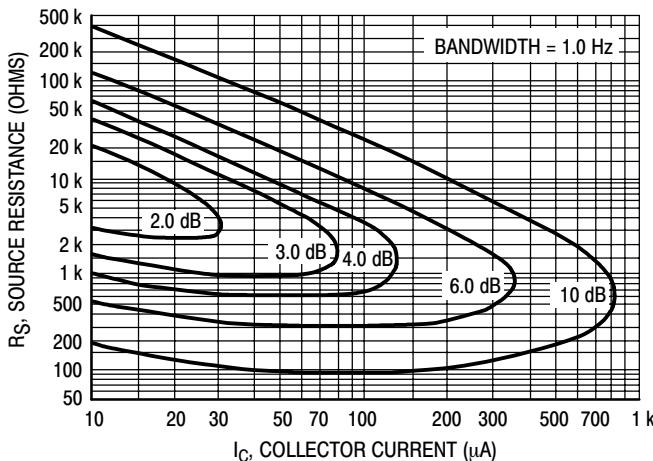


Figure 5. Narrow Band, 100 Hz

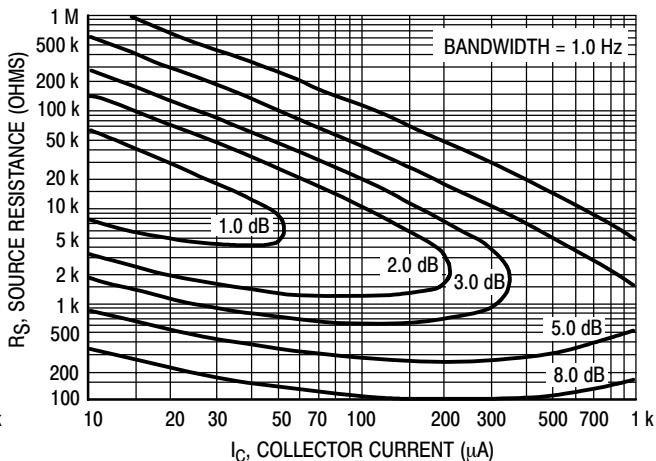


Figure 6. Narrow Band, 1.0 kHz

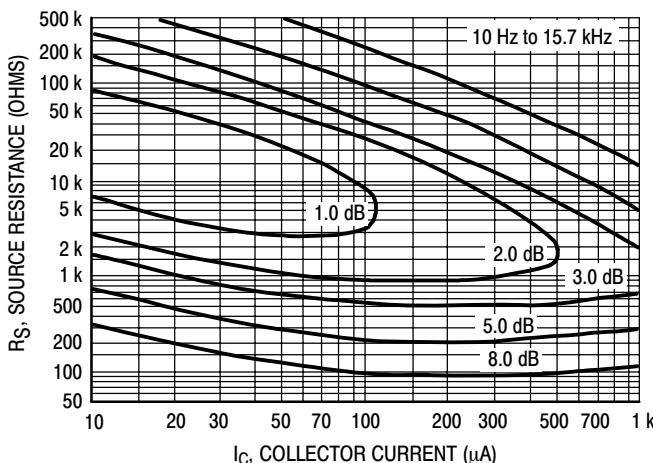


Figure 7. Wideband

Noise Figure is defined as:

$$NF = 20 \log_{10} \left( \frac{(e_n^2 + 4KTR_S + I_n^2 R_S^2)^{1/2}}{4KTR_S} \right)$$

$e_n$  = Noise Voltage of the Transistor referred to the input. (Figure 3)

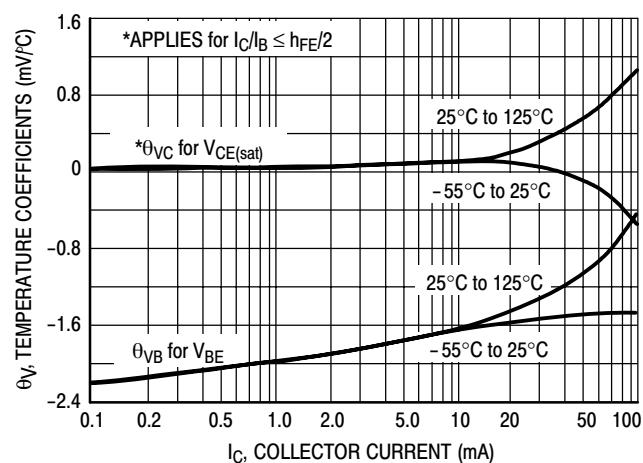
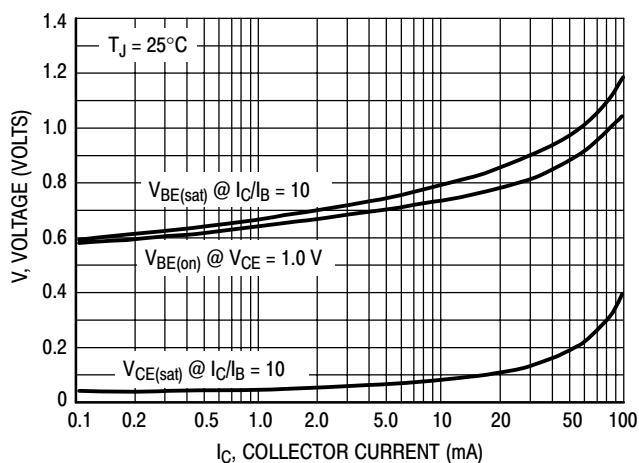
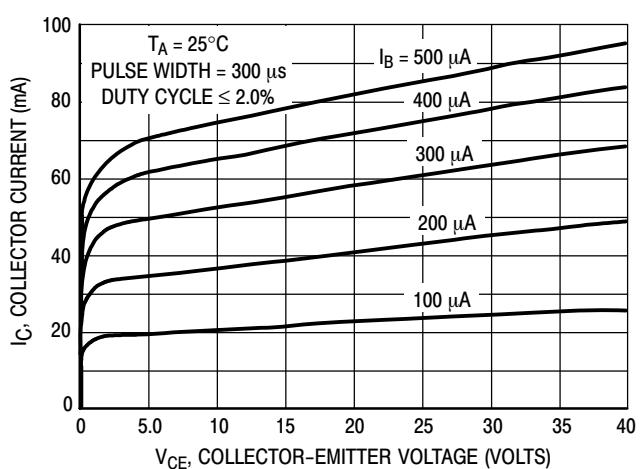
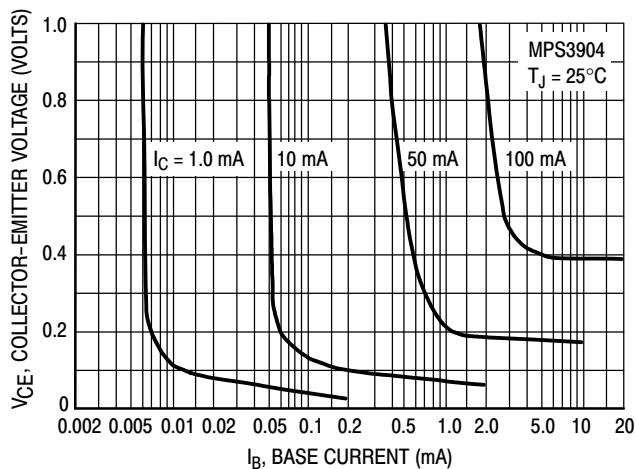
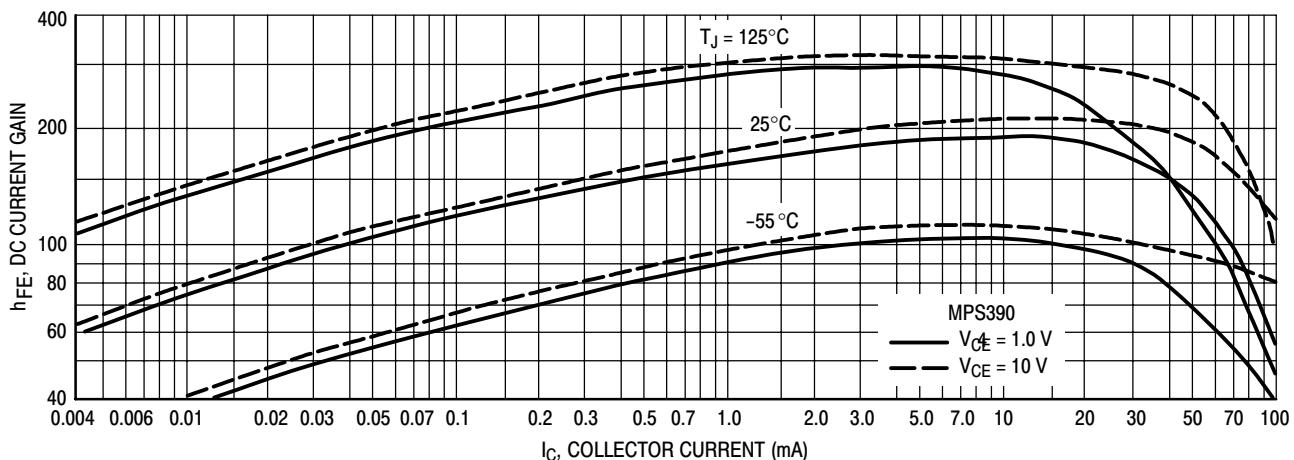
$I_n$  = Noise Current of the Transistor referred to the input. (Figure 4)

K = Boltzman's Constant ( $1.38 \times 10^{-23} \text{ J/K}$ )

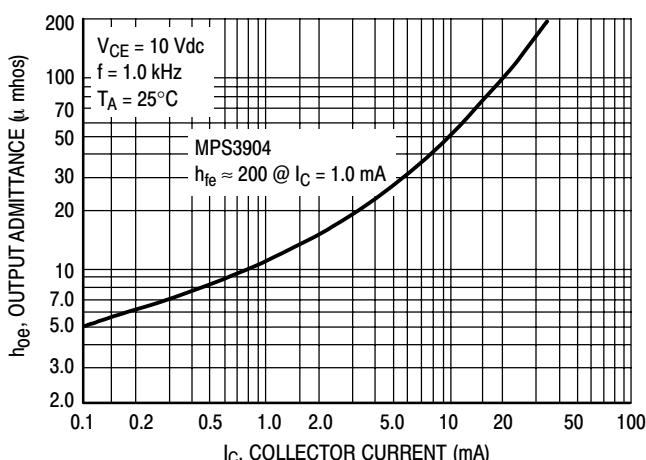
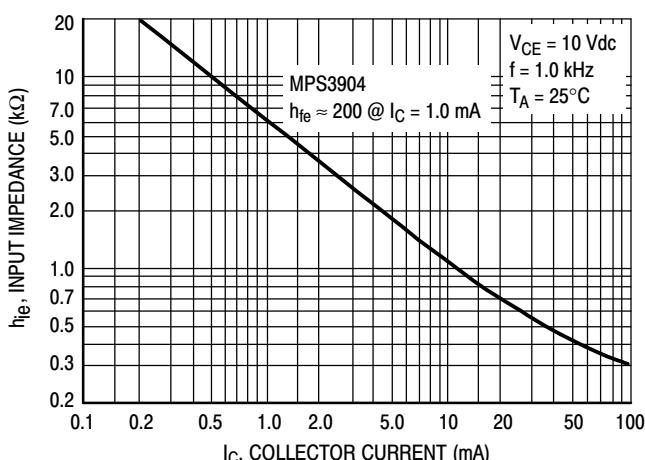
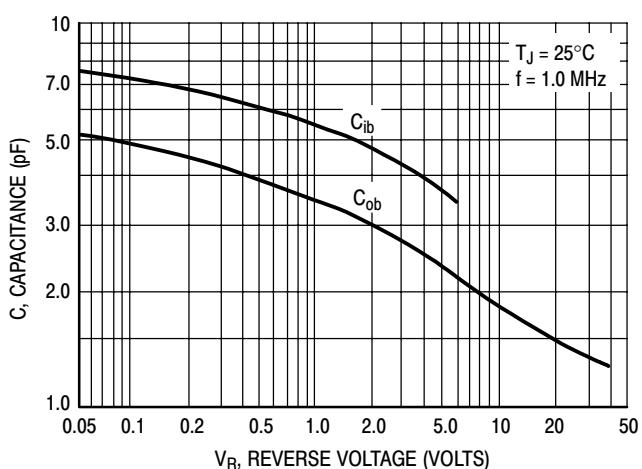
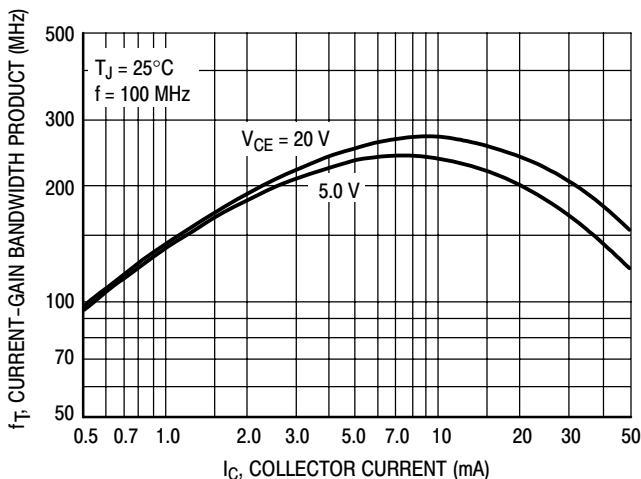
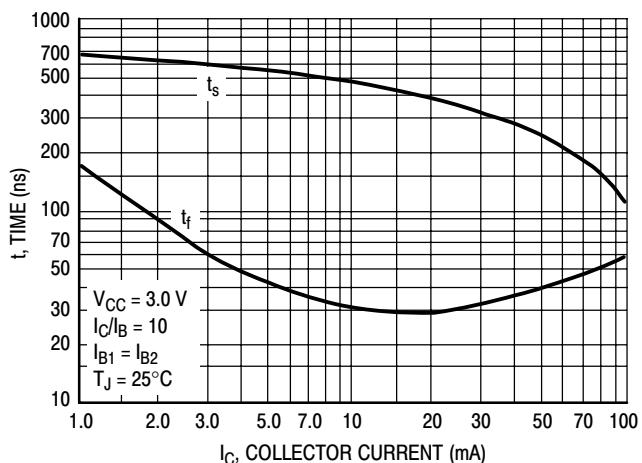
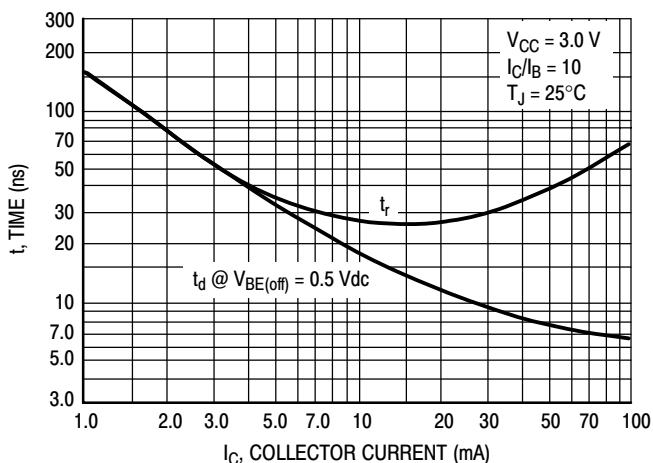
T = Temperature of the Source Resistance ( $^\circ\text{K}$ )

$R_S$  = Source Resistance (Ohms)

## TYPICAL STATIC CHARACTERISTICS



## TYPICAL DYNAMIC CHARACTERISTICS



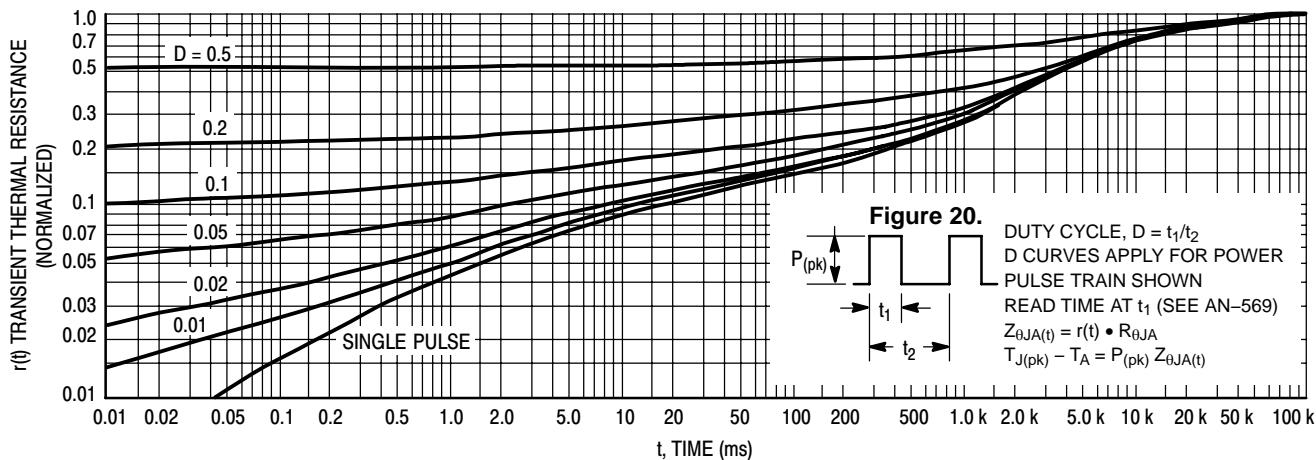


Figure 19. Thermal Response

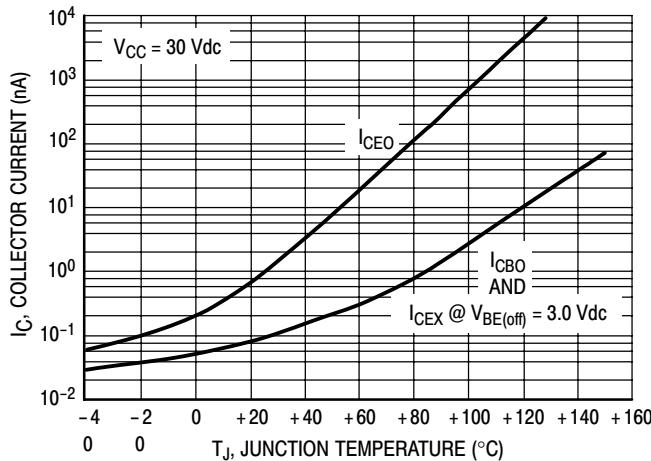


Figure 21.

## DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 20. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 19 was calculated for various duty cycles.

To find  $Z_{\theta JA(t)}$ , multiply the value obtained from Figure 19 by the steady state value  $R_{\theta JA}$ .

Example:

The MPS3904 is dissipating 2.0 watts peak under the following conditions:

$$t_1 = 1.0 \text{ ms}, t_2 = 5.0 \text{ ms. (D = 0.2)}$$

Using Figure 19 at a pulse width of 1.0 ms and D = 0.2, the reading of  $r(t)$  is 0.22.

The peak rise in junction temperature is therefore

$$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88^{\circ}\text{C}.$$

For more information, see AN-569.

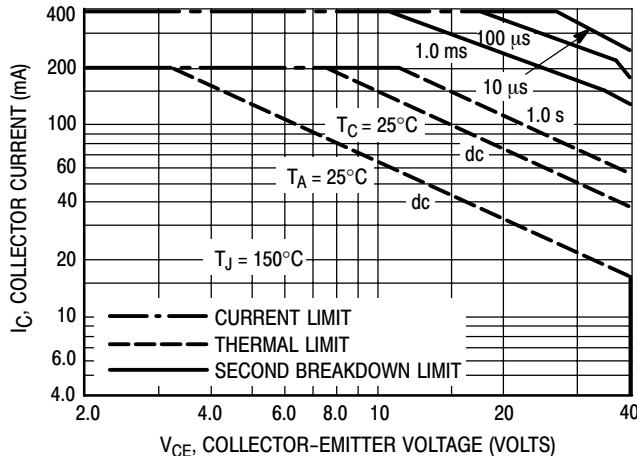


Figure 22.

The safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 22 is based upon  $T_{j(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  or  $T_A$  is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided  $T_{j(pk)} \leq 150^{\circ}\text{C}$ .  $T_{j(pk)}$  may be calculated from the data in Figure 19. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

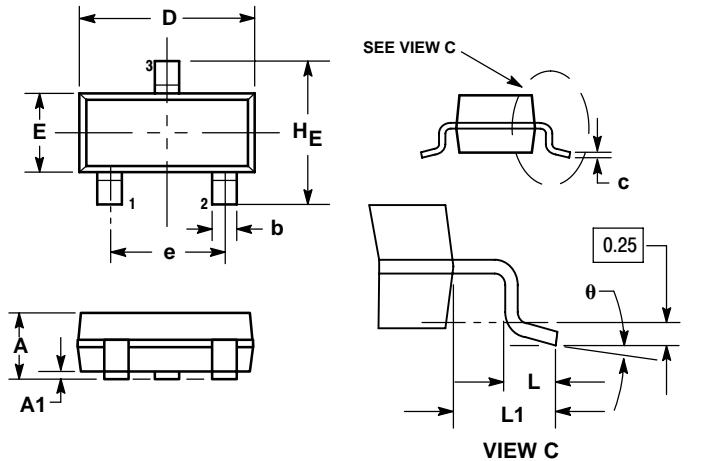
# MMBTA20LT1

## PACKAGE DIMENSIONS

### SOT-23 (TO-236)

CASE 318-08

ISSUE AN

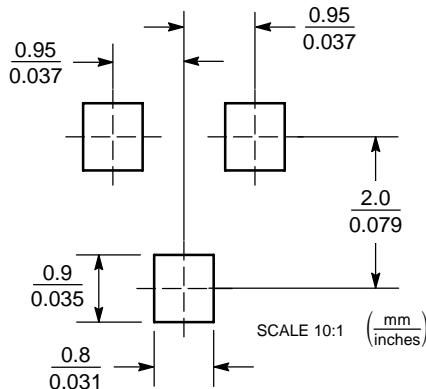


NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.  
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.  
 4. 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6:  
 PIN 1. BASE  
 2. Emitter  
 3. Collector

## SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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