MMDF2N02E

Power MOSFET
2 Amps, 25 Volts
N−Channel SO−8, Dual

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain−to−source diode has a low reverse recovery time. These devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc−dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

Features

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive − Can Be Driven by Logic ICs
- Miniature SO−8 Surface Mount Package − Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- I_{DSS} Specified at Elevated Temperatures
- Avalanche Energy Specified
- Mounting Information for SO−8 Package Provided
- This is a Pb−Free Device

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	25	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	± 20	Vdc
Drain Current – Continuous @ T_A = 25°C – Continuous @ T_A = 100°C – Single Pulse ($t_p \leq$ 10 μs)	I_D I_D I_{DM}	3.6 2.5 18	Adc Apk
Total Power Dissipation @ T_A = 25°C (Note 1)	P_D	2.0	W
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 20 Vdc, V_{GS} = 10 Vdc, Peak I_L = 9.0 Apk, L = 6.0 mH, R_G = 25 Ω)	E_{AS}	245	mJ
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 0.0625″ from case for 10 seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided) with one die operating, 10 sec. max.
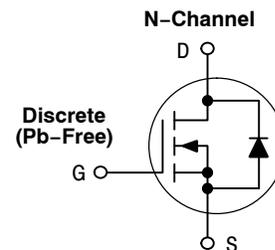
ON Semiconductor®

http://onsemi.com

2 AMPERES, 25 VOLTS
$R_{DS(on)}$ = 100 mΩ

N−Channel

Discrete (Pb−Free)
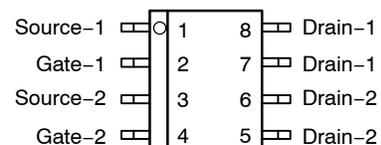

MARKING DIAGRAM

SO−8
CASE 751
STYLE 11

F2N02
AYWW■

F2N02 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb−Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT

Source−1	1	8	Drain−1
Gate−1	2	7	Drain−1
Source−2	3	6	Drain−2
Gate−2	4	5	Drain−2

ORDERING INFORMATION

Device	Package	Shipping†
MMDF2N02ER2G	SO−8 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 µAdc)	$V_{(BR)DSS}$	25	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)	I_{DSS}	 – –	 – –	 1.0 10	µAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)	I_{GSS}	–	–	100	nAdc
ON CHARACTERISTICS (Note 2)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 µAdc	$V_{GS(th)}$	1.0	2.0	3.0	Vdc
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.2 Adc) (V_{GS} = 4.5 Vdc, I_D = 1.0 Adc)	$R_{DS(on)}$	 – –	 0.083 0.110	 0.100 0.200	Ω
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.0 Adc)	g_{FS}	1.0	2.6	–	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	–	380	532	pF
Output Capacitance	C_{oss}	–	235	329	
Transfer Capacitance	C_{rss}	–	55	110	
SWITCHING CHARACTERISTICS (Note 3)					
Turn–On Delay Time	$t_{d(on)}$	–	7.0	21	ns
Rise Time	t_r	–	17	30	
Turn–Off Delay Time	$t_{d(off)}$	–	27	48	
Fall Time	t_f	–	18	30	
Turn–On Delay Time	$t_{d(on)}$	–	10	30	
Rise Time	t_r	–	35	70	
Turn–Off Delay Time	$t_{d(off)}$	–	19	38	
Fall Time	t_f	–	25	50	
Gate Charge	Q_T	–	10.6	30	nC
	Q_1	–	1.3	–	
	Q_2	–	2.9	–	
	Q_3	–	2.7	–	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage (Note 2) (I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	–	1.0	1.4	Vdc
Reverse Recovery Time See Figure 11	t_{rr}	–	34	66	ns
	t_a	–	17	–	
	t_b	–	17	–	
Reverse Recovery Storage Charge	Q_{RR}	–	0.03	–	µC

Note: The dynamic characteristics conditions (V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz) apply to C_{iss}, C_{oss}, C_{rss}.
Switching conditions (V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω) apply to first switching group.
Switching conditions (V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc, R_G = 9.1 Ω) apply to second switching group.
Gate Charge conditions (V_{DS} = 16 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc).
Reverse Recovery conditions (I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/µs).

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
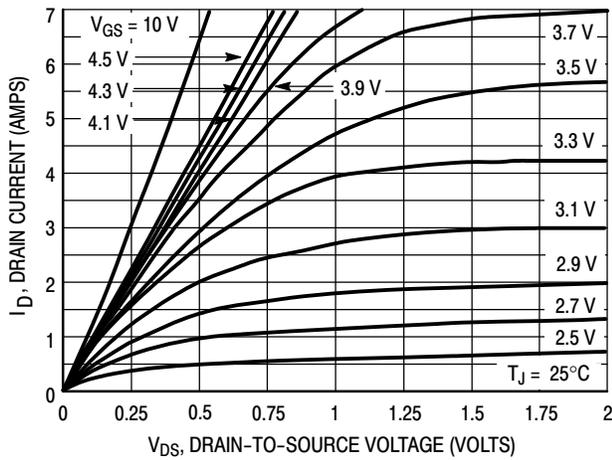
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TYPICAL ELECTRICAL CHARACTERISTICS
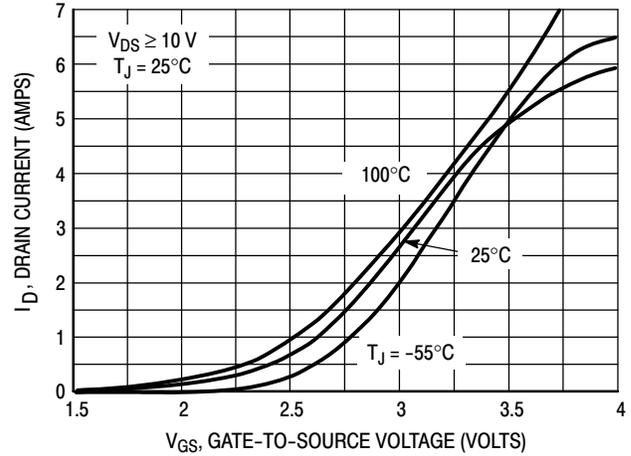

Figure 1. On−Region Characteristics
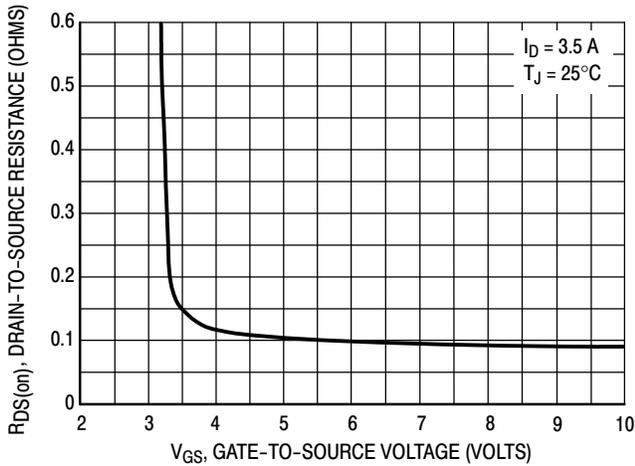

Figure 2. Transfer Characteristics

**Figure 3. On−Resistance versus
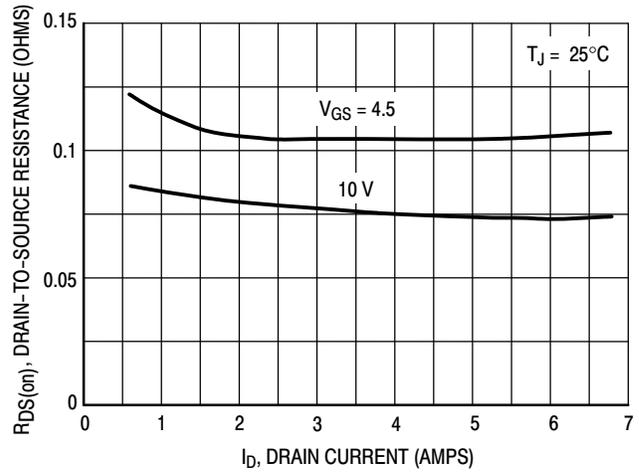Gate−to−Source Voltage**

**Figure 4. On−Resistance versus Drain Current
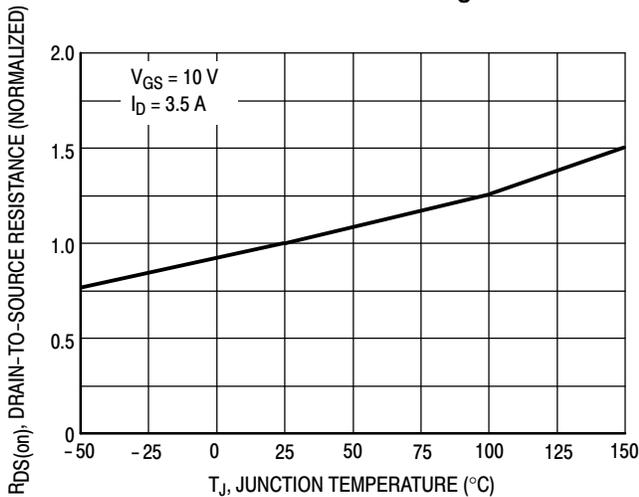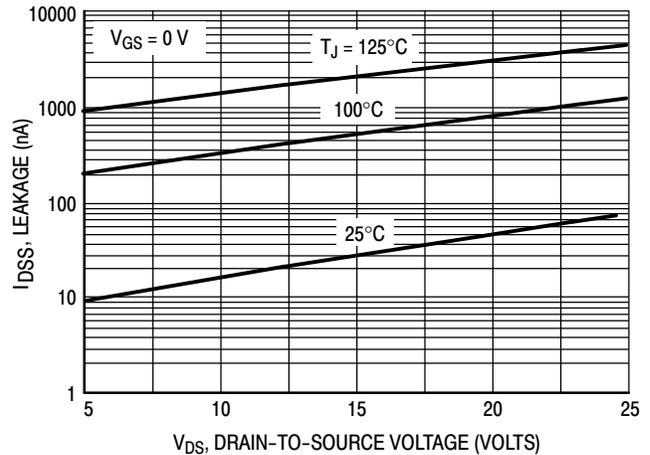and Gate Voltage**

**Figure 5. On−Resistance Variation with
Temperature**

**Figure 6. Drain−to−Source Leakage Current
versus Voltage**

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that:

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$$

$$t_f = Q_2 \times R_G/V_{GSP}$$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G \, C_{iss} \, \text{In} \, [V_{GG}/(V_{GG} - V_{GSP})]$$

$$t_{d(off)} = R_G \, C_{iss} \, \text{In} \, (V_{GG}/V_{GSP})$$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.
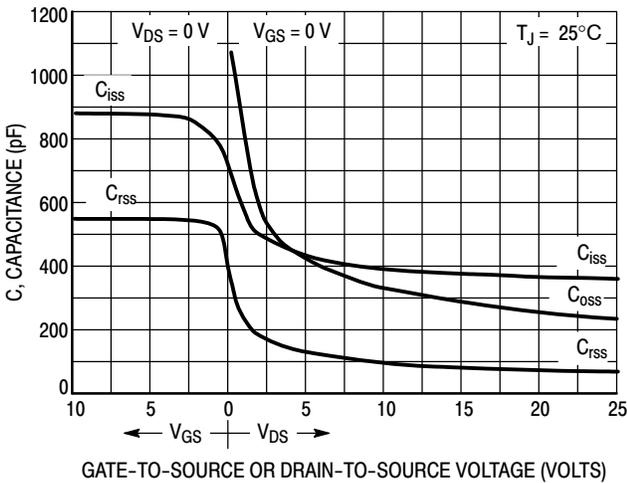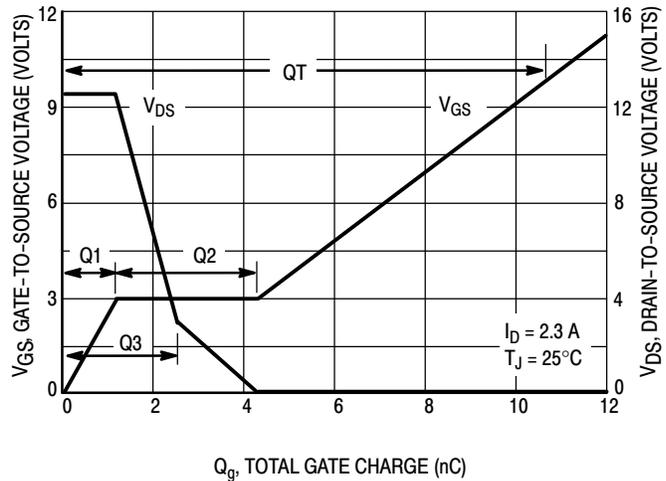

Figure 7. Capacitance Variation

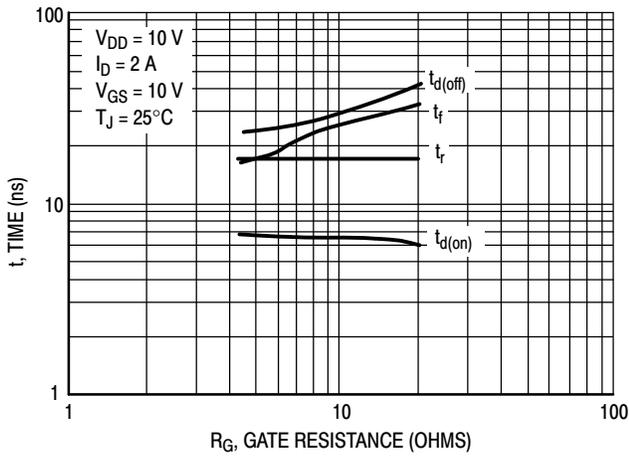**Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge**

Figure 9. Resistive Switching Time Variation versus Gate Resistance
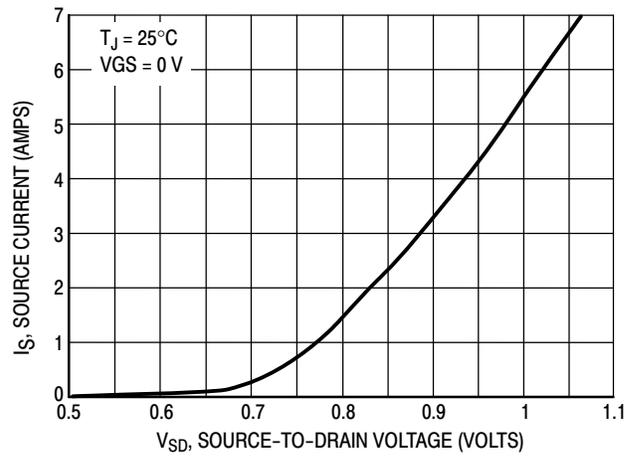

Figure 10. Diode Forward Voltage versus Current
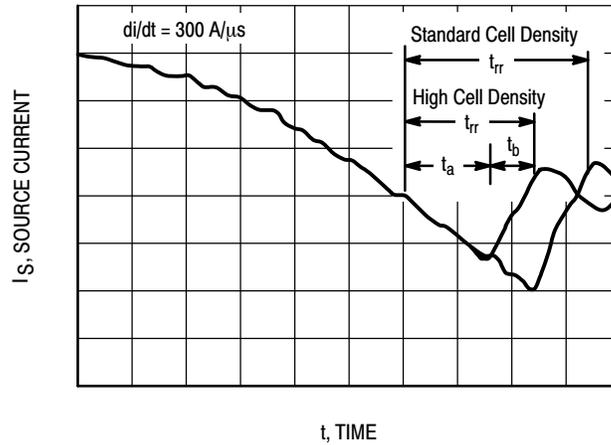

Figure 11. Reverse Recovery Time (t$_{rr}$)

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain−to−source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T$_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance − General Data and Its Use."

Switching between the off−state and the on−state may traverse any load line provided neither rated peak current (I$_{DM}$) nor rated voltage (V$_{DSS}$) is exceeded, and that the transition time (t$_r$, t$_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed (T$_{J(MAX)}$ − T$_C$)/(R$_{\theta JC}$).

A power MOSFET designated E−FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non−linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E−FETs can withstand the stress of drain−to−source avalanche at currents up to rated pulsed current (I$_{DM}$), the energy rating is specified at rated continuous current (I$_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I$_D$ can safely be assumed to equal the values indicated.
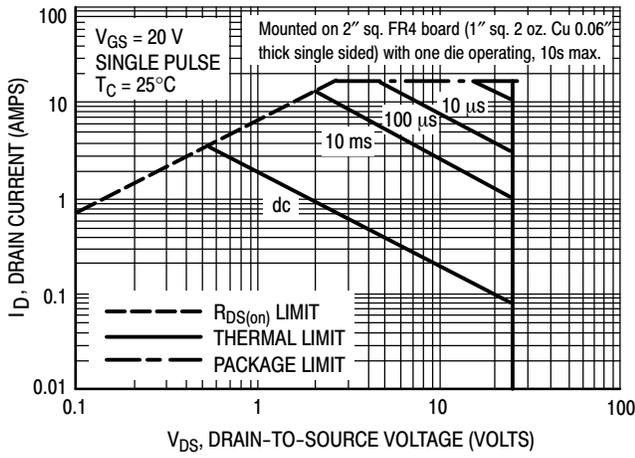
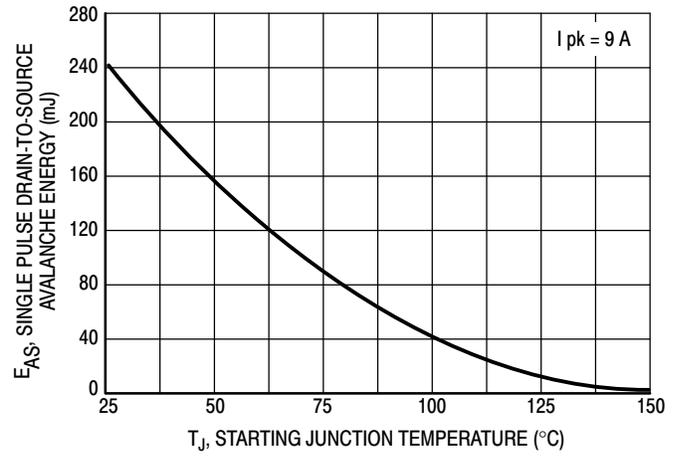Figure 12. Maximum Rated Forward Biased
Safe Operating Area

Figure 13. Maximum Avalanche Energy versus
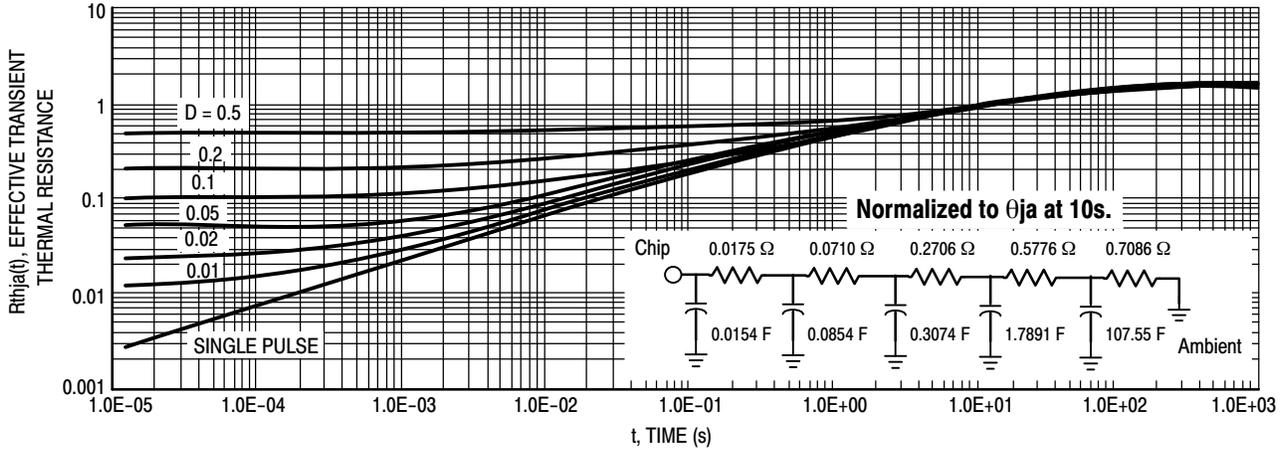Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

Normalized to θja at 10s.
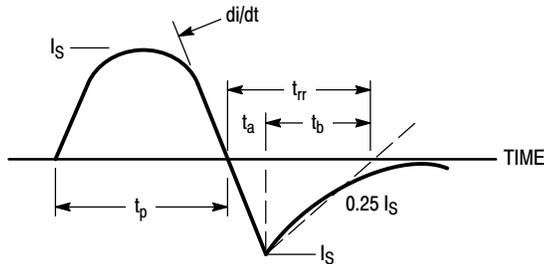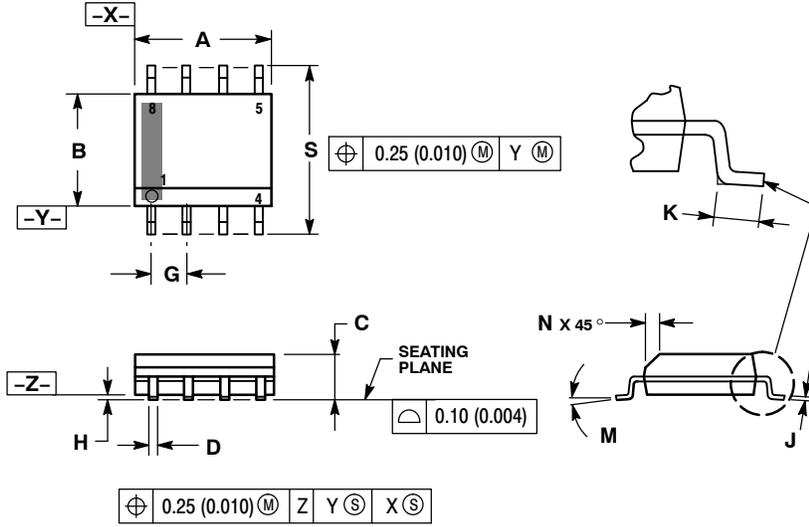
Figure 14. Thermal Response

Figure 15. Diode Reverse Recovery Waveform

MMDF2N02E

## PACKAGE DIMENSIONS

SOIC−8
CASE 751−07
ISSUE AG

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

SOLDERING FOOTPRINT*

SCALE 6:1 $\left(\dfrac{mm}{inches}\right)$
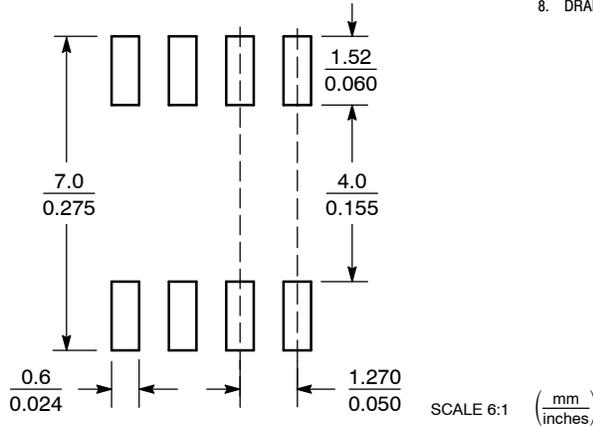
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MMDF2N02E/D

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