

DESCRIPTION

The MP20043 is a dual-channel, low noise, low dropout and high PSRR linear regulator with programmable output voltage. The output voltage of MP20043 ranges from 1.2V to 3.3V in 100mV increments and 2.5% accuracy by operating from a +2.5V to +5.5V input. The different output voltage options can be programmed by setting the voltage of P1 and P2 to VDD, GND or floating. There are 9 different voltage settings in one chip. Each output channel can supply up to 300mA of load current.

The MP20043 uses two internal PMOSs as the pass devices, which consumes 150 μ A supply current when both channels are enabled at no load condition. The EN1 and EN2 pins control each output respectively. When both channels shutdown simultaneously, the chip turns off and consumes nearly zero operation current which is suitable for battery-power devices. The MP20043 also features current limiting and over temperature protection.

It is available in a TQFN8 (2mm $\times$ 2mm) package

FEATURES

- Programmable Output Voltage
- Up to 300mA Output Current (Each LDO)
- 60mV Dropout at 100mA Load
- Dual Shutdown Pins Control Each Output
- 75dB PSRR at 1kHz
- 7 μ V_{RMS} Low Noise Output
- Current Limiting and Thermal Protection
- Short Circuit Protection
- Two LDOs in TQFN8 (2mm $\times$ 2mm) Package
- Output Load Discharge when Disabled

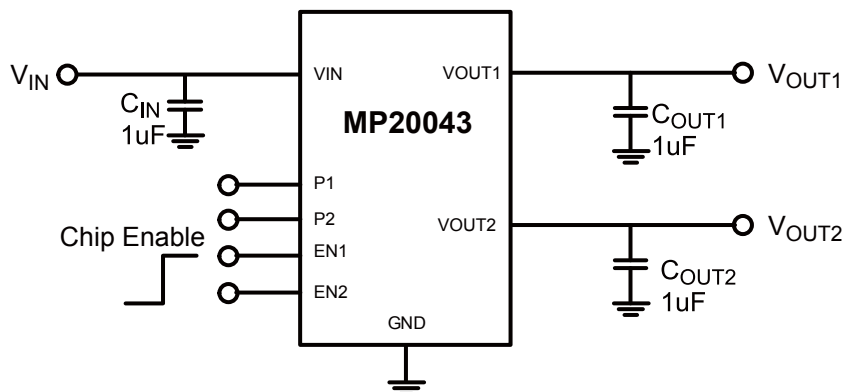
APPLICATIONS

- Cellular Phones
- Battery-powered Equipment
- Laptop, Notebook, and Palmtop Computers
- Hand-held Equipment
- Wireless LAN

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION

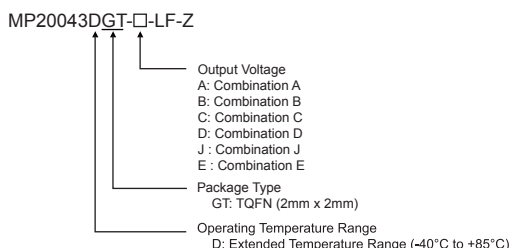


ORDERING INFORMATION*

Part Number*	Package	Top Marking	Free Air Temperature (T _A)
MP20043DGT-A-LF-Z	TQFN8 (2mm×2mm)	4N	-40°C to +85°C
MP20043DGT-B-LF-Z		6X	
MP20043DGT-C-LF-Z		3Z	
MP20043DGT-D-LF-Z		4Z	
MP20043DGT-J-LF-Z			
MP20043DGT-E-LF-Z		AH	

* Available options are identified by those with top marking. For other options, please contact factory to check availability.

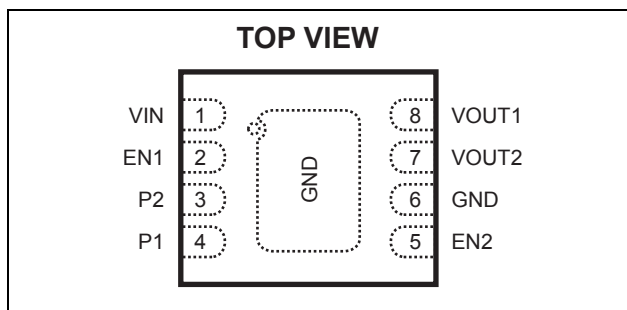
ORDERING GUIDE**



** For RoHS Compliant Packaging, add suffix - LF (e.g. MP20043DGT-□-LF);

For Tape and Reel, add suffix -Z (e.g. MP20043DGT-□-LF-Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply Input Voltage 6V
All Other Pins 5.5V

Power Dissipation, PD @ T_A =25°C, ⁽²⁾

TQFN-8L 1.5W

Storage Temperature Range -65°C to 150°C

Lead Temperature (Soldering, 10sec)260°C

ESD Susceptibility

HBM (Human Body Mode) 2kV

MM (Machine Mode) 200V

Recommended Operating Conditions ⁽³⁾

Supply Input Voltage.....2.5V to 5.5 V

Operating Junct. Temp (T_J)..... -40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
TQFN 8L.....	80	16 °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7 4-layer board.

PROGRAMMABLE OUTPUT VOLTAGE SETTING

Combination A:

P1 State	P2 State	VOUT1	VOUT2
L	L	1.5V	2.8V
L	H	1.8V	2.9V
L	Open	1.8V	2.8V
H	L	1.8V	2.7V
H	H	1.8V	2.6V
H	Open	2.7V	2.8V
Open	L	2.8V	2.8V
Open	H	2.9V	2.9V
Open	Open	2.8V	3.3V

Combination C:

P1 State	P2 State	VOUT1	VOUT2
L	L	1.8V	2.8V
L	H	1.8V	2.85V
L	Open	1.8V	3V
H	L	1.85V	2.85V
H	H	2.6V	2.7V
H	Open	2.6V	3.3V
Open	L	2.85V	3.3V
Open	H	3V	3.3V
Open	Open	3.3V	3.3V

Combination B:

P1 State	P2 State	VOUT1	VOUT2
L	L	1.2V	2.8V
L	H	1.5V	1.8V
L	Open	1.5V	2.8V
H	L	1.8V	2.6V
H	H	1.8V	2.8V
H	Open	2.8V	2.8V
Open	L	2.8V	3.3V
Open	H	3V	3.3V
Open	Open	3.3V	3.3V

Combination D:

P1 State	P2 State	VOUT1	VOUT2
L	L	1.8V	2.9V
L	H	2.6V	2.8V
L	Open	1.8V	2.8V
H	L	2.9V	2.9V
H	H	2.8V	3.3V
H	Open	2.8V	2.8V
Open	L	1.8V	2.6V
Open	H	1.8V	2.7V
Open	Open	1.5V	2.8V

Combination J:

P1 State	P2 State	VOUT1	VOUT2
L	L	3.3V	3.3V
L	H	1.1V	3.3V
L	Open	1.2V	2.5V
H	L	1.8V	3.3V
H	H	1.1V	1.8V
H	Open	1.1V	2.5V
Open	L	1.2V	1.8V
Open	H	1.2V	3.3V
Open	Open	1.8V	2.5V

Combination E:

P1 State	P2 State	VOUT1	VOUT2
L	L	1.2V	3.3V
L	H	1.2V	1.8V
L	Open	1.2V	1.5V
H	L	1.5V	2.5V
H	H	1.8V	2.5V
H	Open	1.8V	3.3V
Open	L	2.5V	3.3V
Open	H	1.8V	1.8V
Open	Open	1.5V	3.3V

ELECTRICAL CHARACTERISTICS

$V_{IN} = (V_{OUT} + 0.4V)$ or $+2.5V$, whichever is greater. $C_{IN} = C_{OUT1} = C_{OUT2} = 1\mu F$, $EN1 = EN2 = V_{IN}$, Typical Value at $T_A = 25^\circ C$ for each LDO unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Voltage Accuracy	ΔV_{OUT}	$I_{LOAD} = 1mA$	-2.5		2.5	%
Maximum Output Current	I_{MAX}	Continuous	300			mA
Current Limit	I_{LIM}	Short circuit current limit		660		mA
Quiescent Current	I_G	No Load (Single Channel)		90		μA
		No Load (Dual Channel)		150		μA
Shutdown Supply Current	I_{GSD}	$EN1 = EN2 = GND$		0.01	1	μA
Dropout Voltage ⁽⁵⁾	V_{DROP}	$I_{OUT} = 100mA$		60	120	mV
		$I_{OUT} = 300mA$		180	280	mV
Line Regulation ⁽⁶⁾	ΔV_{LINE}	$V_{IN} = (V_{OUT} + 0.4V \text{ or } 2.5V \text{ to } 5.5V, I_{OUT} = 1mA)$	-		0.1	%/V
Load Regulation ⁽⁷⁾	ΔV_{LOAD}	$V_{OUT} > 1.5V$			1.2	%
		$V_{OUT} \leq 1.5V$			1.8	%
EN Logic High	V_{IH}	$V_{IN} = 2.5V \text{ to } 5.5V$	1.6			V
EN Logic Low	V_{IL}	$V_{IN} = 2.5V \text{ to } 5.5V$			0.4	V
EN Input Bias Current	I_{SD}	$EN = GND \text{ or } V_{IN}$			100	nA
Thermal Shutdown Temperature	T_{SD}			140		$^\circ C$
Thermal Shutdown Hysteresis	ΔT_{SD}			10		$^\circ C$
Output Voltage Noise	V_{NOISE}	10Hz to 30kHz, $C_{OUT} = 1\mu F, I_{LOAD} = 1mA$		7		μV_{RMS}
Output Voltage AC PSRR		100Hz, $C_{OUT} = 1\mu F, I_{LOAD} = 300mA$ (Single Channel loaded)		75		dB
		1kHz, $C_{OUT} = 1\mu F, I_{LOAD} = 300mA$ (Single Channel loaded)		75		dB
Output Voltage Discharge Resistance in Shutdown		$V_{IN} = 5V, EN1 = EN2 = GND$	20		100	Ω
P1/P2 Termination bias for setting High, Low, Open States		$V_{IN} = 2.5V \text{ to } 5.5V$	High state bias current		5	μA
			Low state bias current	-8		
			Open state		0.7	V

Notes:

5) Dropout Voltage is defined as the input to output differential when the output voltage drops 100mV below its nominal value.

$$6) \text{ Line Regulation} = \frac{V_{OUT[V_{IN(MAX)}]} - V_{OUT[V_{IN(MIN)}]}}{[V_{IN(MAX)} - V_{IN(MIN)}] \times V_{OUT(NOM)}} \times 100(\% / V)$$

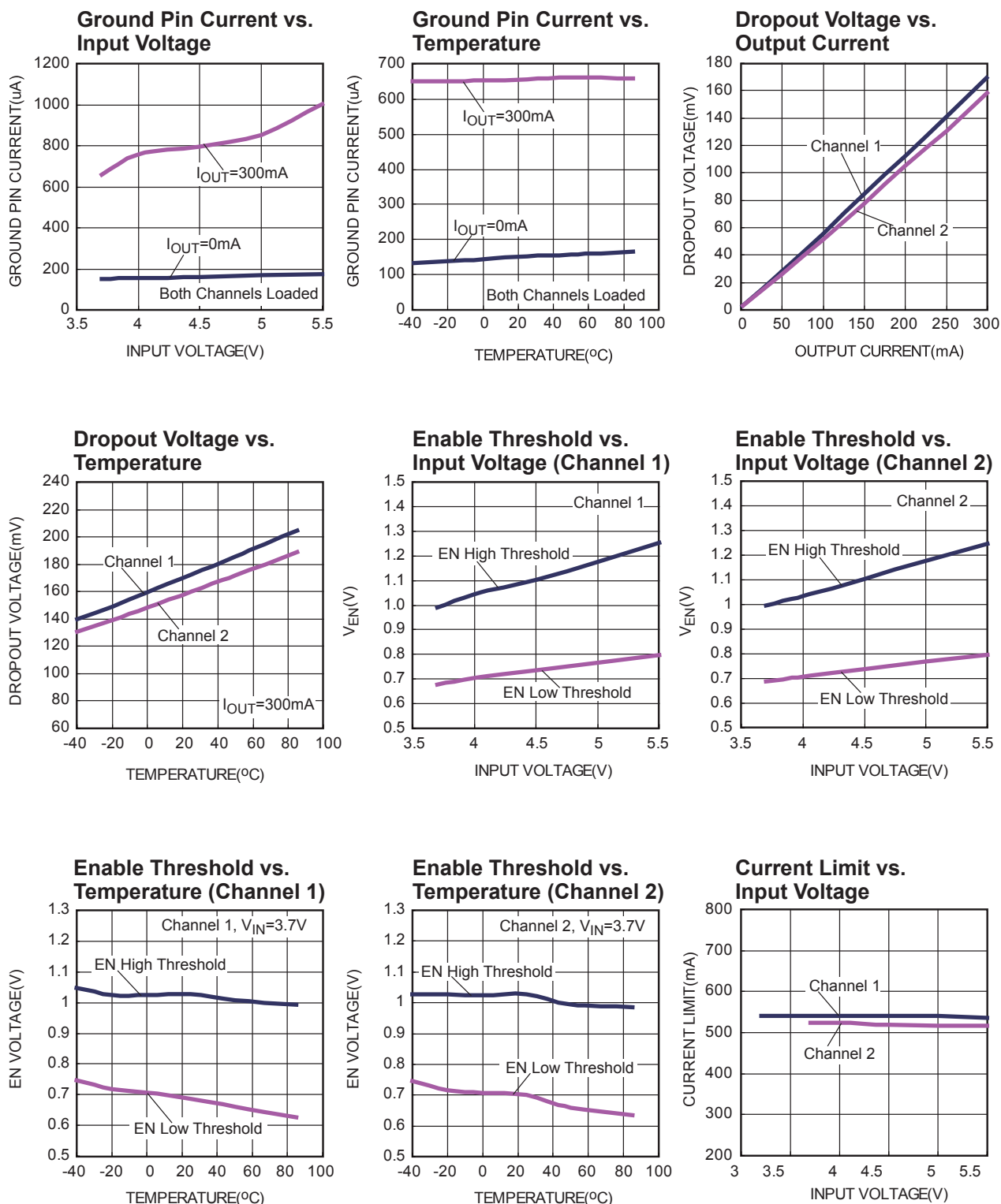
$$7) \text{ Load Regulation} = \frac{V_{OUT[I_{OUT(MAX)}]} - V_{OUT[I_{OUT(MIN)}]}}{V_{OUT(NOM)}} \times 100(\%)$$

PIN FUNCTIONS

Pin #	Name	Description
1	VIN	Supply Input Pin
2	EN1	Channel 1 Enable (Active High). Do Not Float This Pin.
3	P2	Programming input 2. The state of P2 selects one of nine output voltage options.
4	P1	Programming input 1. The state of P1 selects one of nine output voltage options.
5	EN2	Channel 2 Enable (Active High). Do Not Float This Pin.
6	GND	Common Ground
7	VOUT2	Channel 2 Output Voltage
8	VOUT1	Channel 1 Output Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

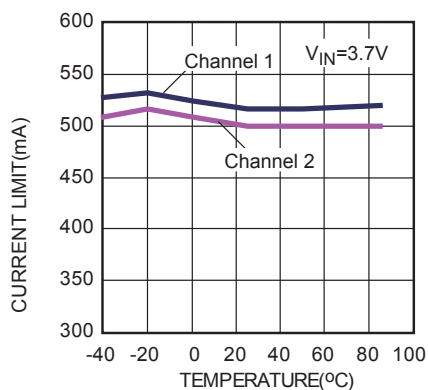
Test Combination A, $V_{IN} = 3.7V$, P1 Open, P2 Open ($V_{OUT1}=2.8V$, $V_{OUT2}=3.3V$), $C_{IN} = C_{OUT1}=C_{OUT2}=1\mu F$, $EN1=EN2=V_{IN}$, $T_A = +25^{\circ}C$, unless otherwise noted.



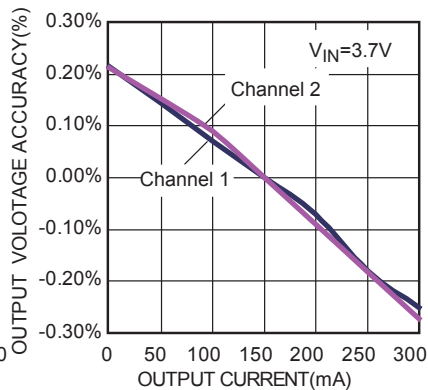
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Test Combination A, $V_{IN} = 3.7V$, P1 Open, P2 Open ($V_{OUT1}=2.8V$, $V_{OUT2}=3.3V$), $C_{IN} = C_{OUT1} = C_{OUT2} = 1\mu F$, $EN1=EN2= V_{IN}$, $T_A = +25^{\circ}C$, unless otherwise noted.

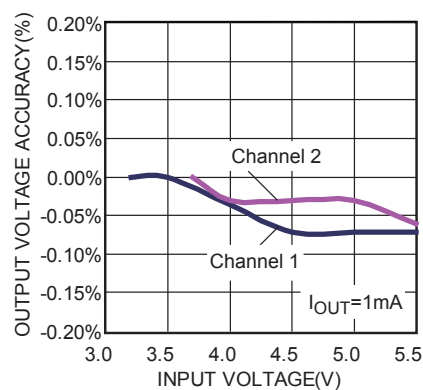
Current Limit vs. Temperature



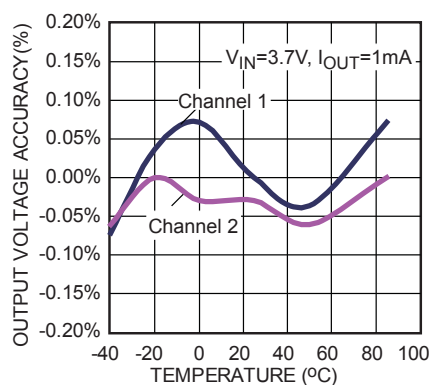
Load Regulation



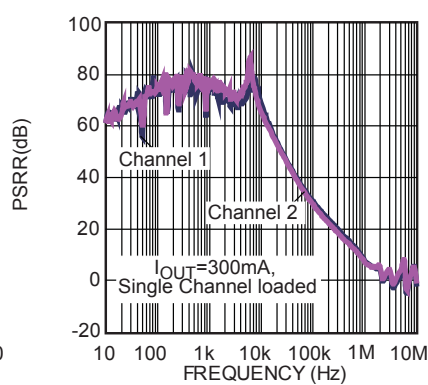
Line Regulation



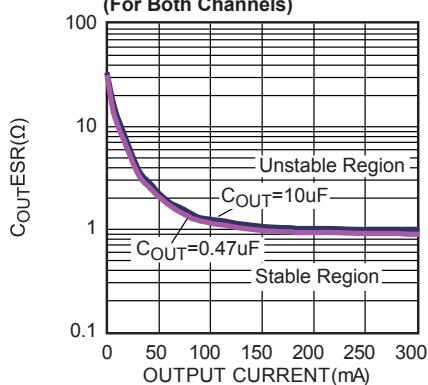
Output Voltage Accuracy



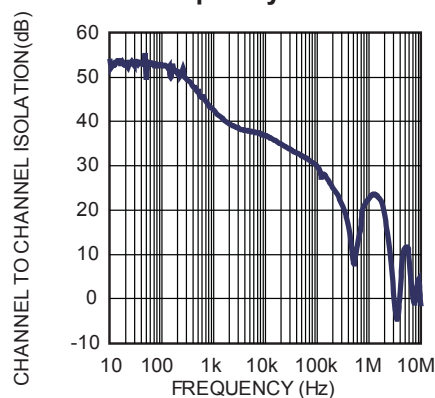
PSRR



**C_{OUT} ESR Stability vs. Output Current
(For Both Channels)**



Channel to Channel Isolation vs. Frequency

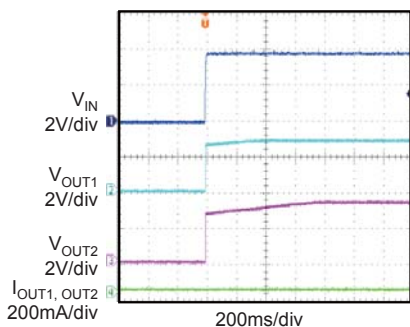


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Test Combination A, $V_{IN} = 3.7V$, P1 Open, P2 Open ($V_{OUT1}=2.8V$, $V_{OUT2}=3.3V$), $C_{IN} = C_{OUT1} = C_{OUT2} = 1\mu F$, $EN1=EN2= V_{IN}$, $T_A = +25^{\circ}C$, unless otherwise noted.

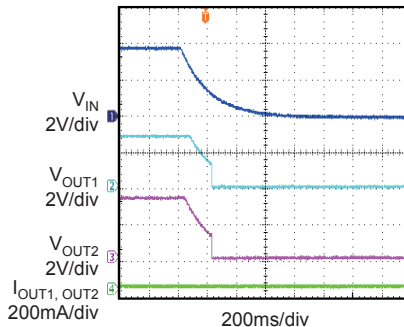
Input Power Up

$V_{IN}=3.7V$, No Load



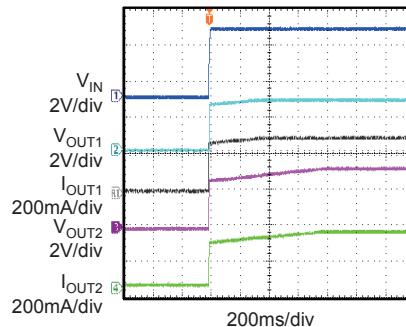
Input Power Down

$V_{IN}=3.7V$, No Load



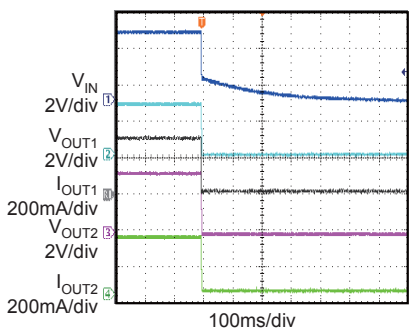
Input Power Up

$V_{IN}=3.7V$, $I_{OUT1}=I_{OUT2}=300mA$, with Resistive Load



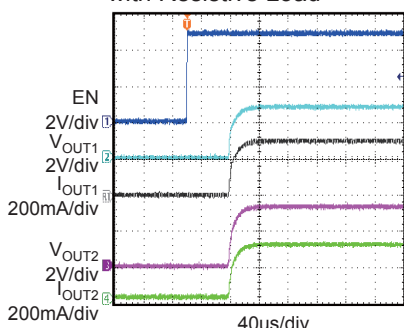
Input Power Down

$V_{IN}=3.7V$, $I_{OUT1}=I_{OUT2}=300mA$, with Resistive Load



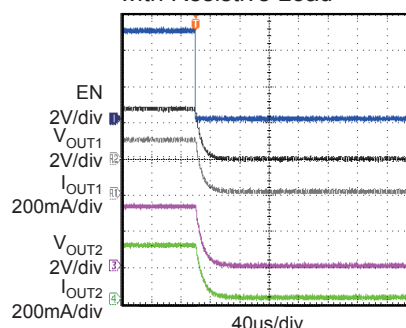
EN Start Up

$V_{IN}=3.7V$, $I_{OUT1}=I_{OUT2}=300mA$, with Resistive Load



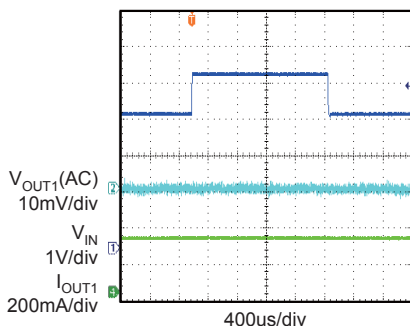
EN Shut Down

$V_{IN}=3.7V$, $I_{OUT1}=I_{OUT2}=300mA$, with Resistive Load



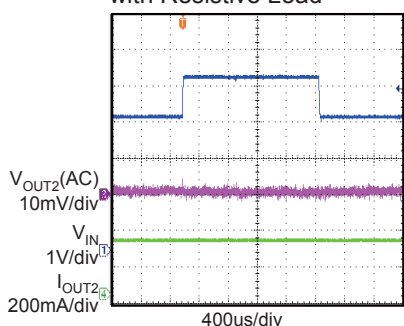
Line Transient (Channel 1)

$V_{IN}=3.7V$ to $4.7V$, $I_{OUT1}=300mA$, with Resistive Load



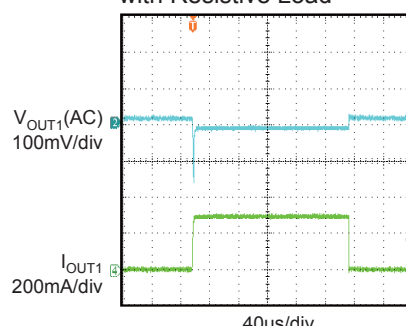
Line Transient (Channel 2)

$V_{IN}=3.7V$ to $4.7V$, $I_{OUT2}=300mA$, with Resistive Load



Load Transient (Channel 1)

$V_{IN}=3.7V$, $I_{OUT1}=1mA$ to $300mA$, with Resistive Load

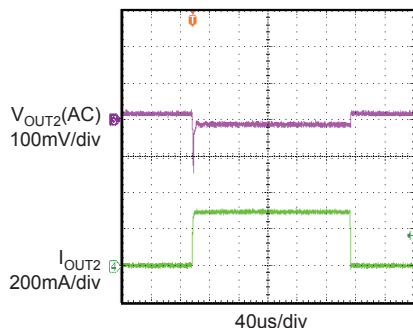


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Test Combination A, $V_{IN} = 3.7V$, P1 Open, P2 Open ($V_{OUT1}=2.8V$, $V_{OUT2}=3.3V$), $C_{IN} = C_{OUT1} = C_{OUT2} = 1\mu F$, $EN1=EN2= V_{IN}$, $T_A = +25^{\circ}C$, unless otherwise noted.

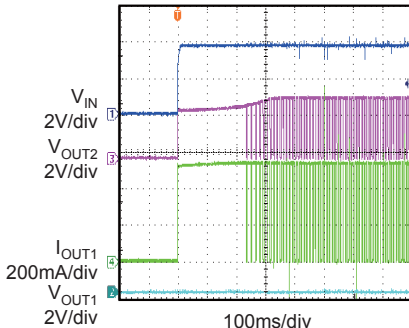
Load Transient (Channel 2)

$V_{IN}=3.7$, $I_{OUT2}=1mA$ to 300mA, with Resistive Load



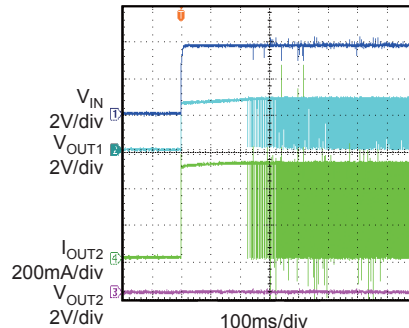
OCP Start Up

$V_{IN}=3.7V$, Short VOUT1 to END before Start Up



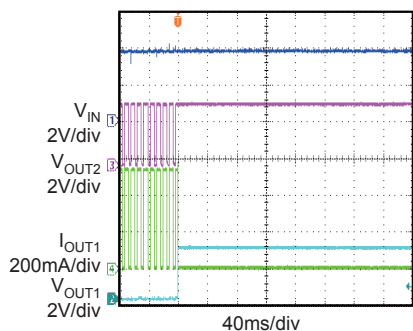
OCP Start Up

$V_{IN}=3.7V$, Short VOUT2 to END before Start Up



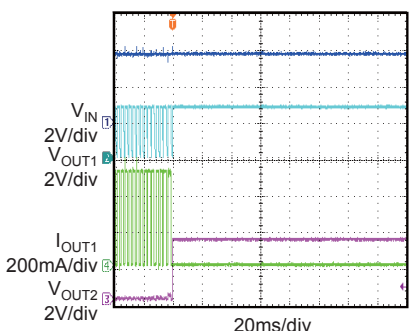
OCP Recovery

$V_{IN}=3.7V$, Remove the Over Current Condition of Channel 1



OCP Recovery

$V_{IN}=3.7V$, Remove the Over Current Condition of Channel 2



FUNCTION BLOCK DIAGRAM

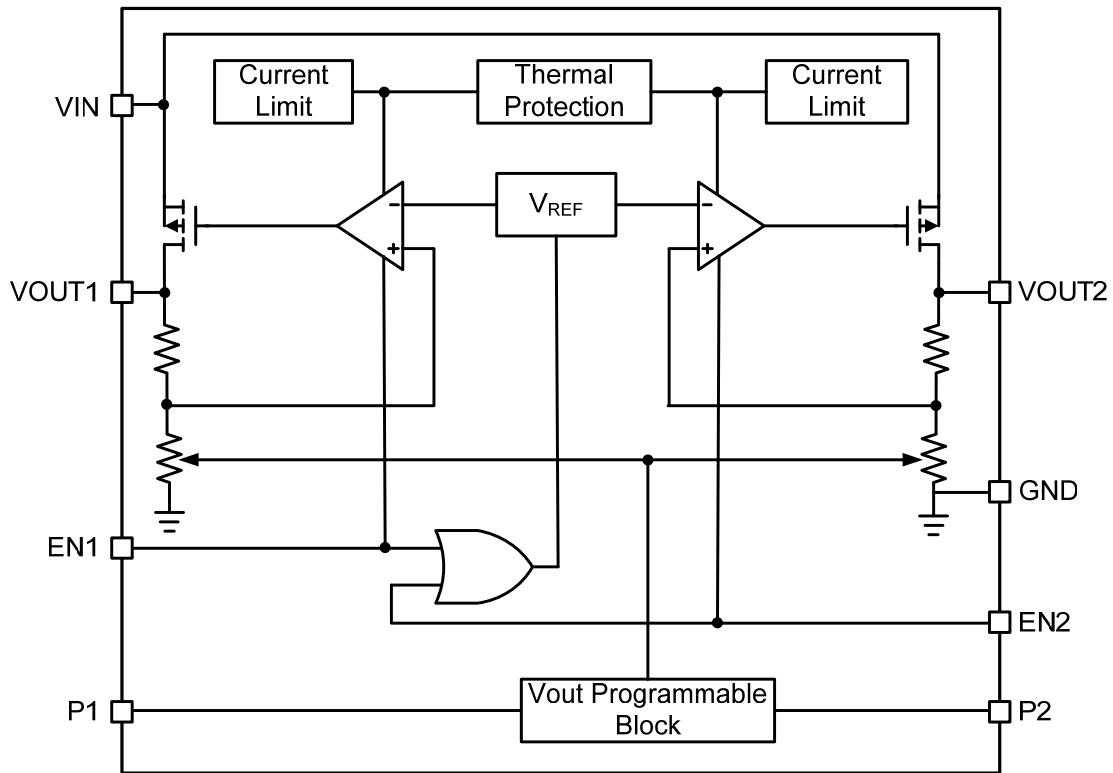


Figure1—Function Block Diagram

OPERATION

The MP20043 integrates two low noise, low dropout, low quiescent current and high PSRR linear regulators. It is intended for use in devices that require very low voltage, low quiescent current power such as wireless LAN, battery-powered equipment and hand-held equipment. Output voltages are optional ranging from 1.2V to 3.3V, and each channel can supply current up to 300mA. The part uses internal PMOSs as the pass elements and features internal thermal shutdown and internal current limit circuits.

Dropout Voltage

Dropout voltage is the minimum input to output differential voltage required for the regulator to maintain an output voltage within 100mV of its nominal value. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage of MP20043 is very low.

Shutdown

The MP20043 has two EN pins to control each channel respectively. And each channel can be switched ON or OFF by a logic input at the EN pin. A high voltage at this pin will turn the device on. When the EN pin is low, the regulator output is off. The EN pin should be

tied to VIN to keep the regulator output always on if the application does not require the shutdown feature. Do not float the EN pins.

Current Limit

The MP20043 includes two independent current limit structures which monitor and control each PMOS's gate voltage limiting the guaranteed maximum output current to 490mA.

Thermal Protection

Thermal protection turns off the PMOS when the junction temperature exceeds +140°C, allowing the IC to cool. When the IC's junction temperature drops by 10°C, the PMOS will be turned on again. Thermal protection limits total power dissipation in the MP20043. For reliable operation, the junction temperature should be limited to 125 °C maximum.

Internal P-Channel Pass Device

The MP20043 features dual typical 0.6Ω P-channel MOSFET pass devices. It provides several advantages over similar designs using PNP pass transistors, including longer battery life.

APPLICATION INFORMATION

Output Voltage

The output voltage of MP20043 is programmable with setting different states of P1 PIN and P2 PIN. For combination A, the setting rule is as the following table:

Table 1 Programmable Output Voltage Setting (Combination A)

P1 State	P2 State	V _{OUT1}	V _{OUT2}
L	L	1.5V	2.8V
L	H	1.8V	2.9V
L	Open	1.8V	2.8V
H	L	1.8V	2.7V
H	H	1.8V	2.6V
H	Open	2.7V	2.8V
Open	L	2.8V	2.8V
Open	H	2.9V	2.9V
Open	Open	2.8V	3.3V

For example, when P1 and P2 are both open, output voltage of channel 1 is 2.8V, and the output voltage of channel 2 is 3.3V.

Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature difference between the junction and ambient air, and the rate of airflow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_{(MAX)} = (T_{Junction} - T_{Ambient}) / \theta_{JA}$$

Where $(T_{Junction} - T_{Ambient})$ is the temperature difference between the junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the ambient environment. Connect the GND pin of MP20043 to ground using a large pad or ground plane helps to channel heat away.

Input Capacitor Selection

Using a capacitor whose value is $>0.47\mu F$ on the MP20043 input and the amount of capacitance can be increased without limit.

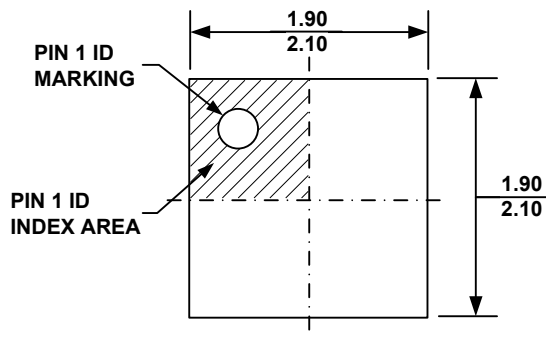
Input capacitor of larger value will help improve line transient response with the drawback of increased size. Ceramic capacitors are preferred, but tantalum capacitors may also sufficient.

Output Capacitor Selection

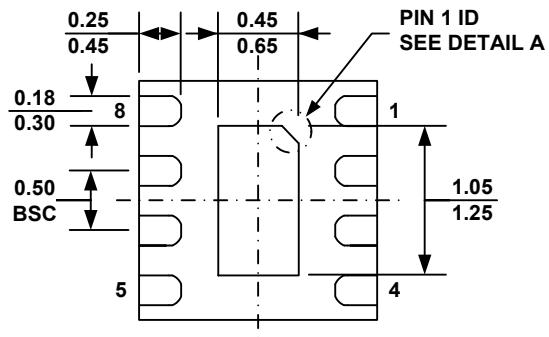
The MP20043 is designed specifically to work with very low ESR ceramic output capacitor in space-saving and performance consideration. A ceramic capacitor in the range of $0.47\mu F$ and $10\mu F$, and with ESR lower than 1Ω is suitable for the MP20043 application circuit. Output capacitor of larger values will help to improve load transient response and reduce noise with the drawback of increased size.

PACKAGE INFORMATION

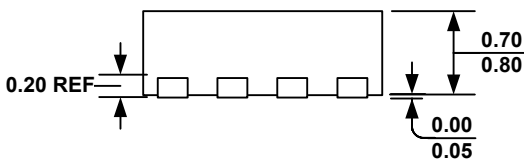
TQFN8 (2mm×2mm)



TOP VIEW

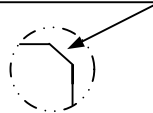


BOTTOM VIEW

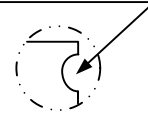


SIDE VIEW

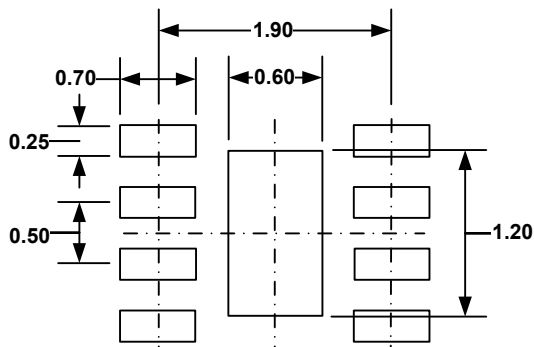
PIN 1 ID OPTION A
0.30x45° TYP.



PIN 1 ID OPTION B
R0.20 TYP.



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION WCCD-3.
- 5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.