PCB Layout Design Guidelines for MPQ8632 and MPQ8636 Families

Application Note

Prepared by Christine Cheng

Jan, 2013

ABSTRACT

This application note gives the detailed layout guidelines for a reliable operation and better performance of MPQ8632 family and MPQ8636 family.

LAYOUT FOR HIGH CURRENT INTEGRRATED DC-DC CONVERTERS

Other than the traditional converter that combines the controller with external power-FETs, the MPQ8632 and MPQ8636 families provide high power density, fully integrated solutions for DC-DC converters, with output current from 4A-20A in a small QFN3x4mm or QFN5x4mm packages, this kind of integrated structure makes the converter much smaller and can also reduce the parasitic parameters, contributing to higher switching frequency with better efficiency performance. However, the PCB layout should be paid more attention for the fully integration making the logic circuit very close to the power-FETs. The high dv/dt noise will easily be coupled into logic circuit and leads to system instability. Hence, a carefully designed PCB layout is required to ensure a proper operation.

INDEX

INTRODUCTION

HOW IMPORTANT A LAYOUT IS TO THE HIGH CURRENT DC-DC CONVERTERS

The MPQ8632 and MPQ8636 are families of fully integrated high frequency synchronous rectified step-down switch mode converters. These parts offer a very compact solution to achieve 4A-20A output current in a small QFN3x4mm or QFN5x4mm package. For these highly integrated DC-DC converters with high current and high switching frequency, a poor layout will degrade the performance of the converter, causing ground bounce, EMI problems, resistive power loss, high voltage stress on power-FETs, poor line and load regulation and even system instability.

GENERAL DESIGN GUIDELINES

There are some general design guidelines for a proper layout. Generally, the MPQ8632 and MPQ8636 are the power devices so that they require more careful design layout.

1) The power trace (VIN, PGND, SW) should be placed short and wide with minimized loop area. That means, the input and output capacitors should be placed as close as possible to the IC. The input capacitor should be placed next to VIN and PGND pins. And the output capacitor should be placed in a way that its GND is close to the IC's PGND. Also, the inductor should be placed close to the SW pins and connect directly to the output capacitor.

2) The VCC decoupling capacitor should be placed close to VCC and AGND pins, and located in the same layer with the IC. Also the VCC decoupling capacitor should be connected to AGND (analog ground of the IC), not PGND. The AGND should be well separated from PGND and finally single point connected to PGND.

3) The feedback resistors, which means output dividers, should be placed close to the IC and directly connect to FB and AGND, avoiding vias on FB trace. It is important that the signals path do not conduct power, such as feedback resistors.

4) Keep the switching node (SW) plane small. Keep the BST voltage path (path from BST to SW) as short as possible.

5) The sensitive notes like FB, VCC, AGND and output sense path should be placed far from the high dv/dt signals, e.g. SW.

6) To get better thermal performance, at least two layers are required to form VIN and PGND trace. Add several VIAs with 8mil_dril/18mil_copper width close to the IN and PGND pads and 16 mil_dril/28mil_copper width close to the input capacitors to help on thermal dissipation. Four-layer layout is strongly recommended to achieve better thermal performance.

CRITICAL DESIGN NOTES FOR THE PCB LAYOUT

The above section describes some general layout recommendations that should be considered for an integrated converter. This section will focus on some specific layout suggestions that are critical for MPQ8632 and MPQ8636 families. When designing, one should strictly follow these design notes for a better and reliable performance. Since most of the parts in these two families have similar pin-out and package structure, these parts are separated into three series in this section by package type as listed below:

Package 13-Pin-QFN3x4mm, including MPQ8632GL-4/6/8/10/12, MPQ8632HGL-10, MPQ8636GL-10, MPQ8636HGL-10, these parts are pin-to-pin.

Package 16-Pin-QFN3x4mm, including MPQ8632GLE-4/6/8/10/12, MPQ8632HGLE-10, MPQ8636GLE-10, MPQ8636HGLE-10, these parts are pin-to-pin. They are enhanced package version for Package 13-Pin-QFN3x4mm parts.

Package 25-Pin-QFN5x4mm, including MPQ8632GV-15/20, MPQ8636GV-20, also they are pin-to-pin.

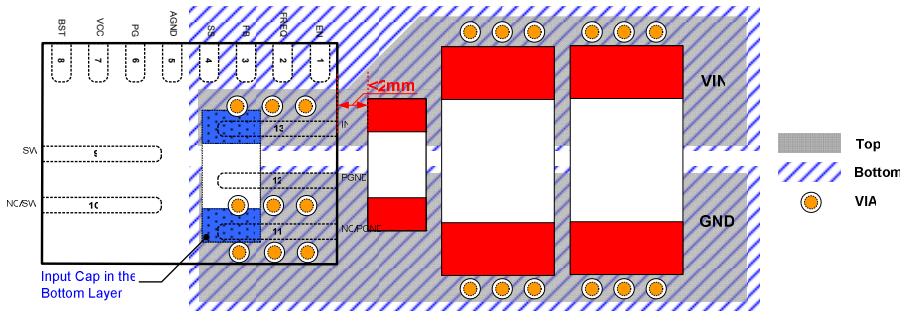
Package 29-Pin-QFN5x4mm, including MPQ8632GVE-15/20, MPQ8636GVE-20, they are pin-to-pin too. And they are enhanced package version for Package 25-Pin-QFN5x4mm parts.

INPUT CAPACITOR

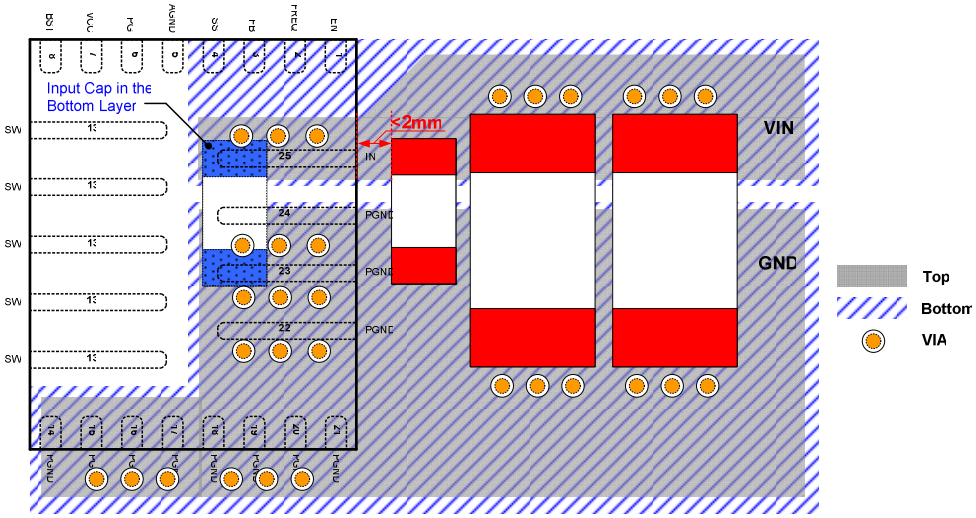
1) INPUT CAPACITOR WITHOUT FORBIDDEN AREA

For both Package 13-Pin-QFN3x4mm and Package 25-Pin-QFN5x4mm series, input capacitors should be placed both on top and bottom layers. On the top layer, the decoupling capacitor, usually the 0.1μF-1uF 0402/0603 package ceramic capacitor, should be placed most close to the IN and PGND pins within **2mm** of the IC edge. These connections should be done with short, direct and wide traces. On the bottom layer, at least one 0603 or 0402 size input capacitor, like 0.1μF-1μF, should be placed directly below the IC to decouple VIN and PGND, connecting to these pins through vias, so as to make the best decoupling effect. **Keep in mind that the input capacitor on the bottom layer is the absolutely necessary. Without them the converter might be failed to operate normally.**

Figure 1 shows the optimized input capacitor arrangement based on Package 13-Pin-QFN3x4mm and Package 25-Pin-QFN5x4mm series.



a) Recommend input capacitor placement for Package 13-Pin-QFN3x4mm



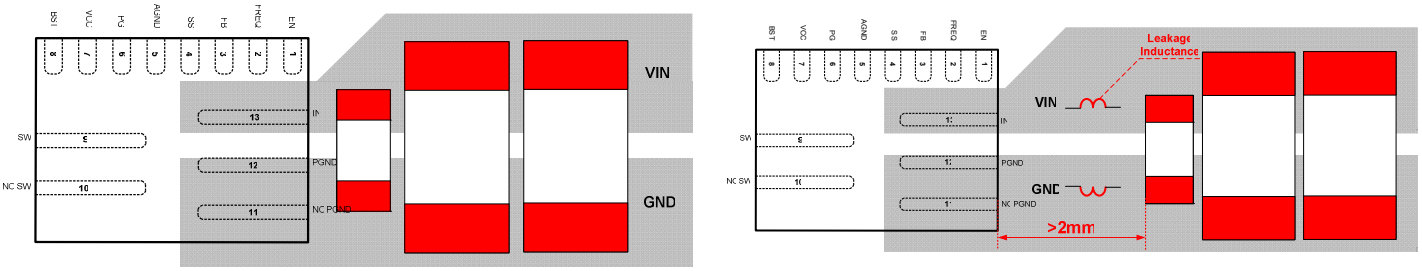
b) recommend input capacitor placement for Package 25-Pin-QFN5x4mm

Figure 1—Optimized and recommended input capacitor placement for Package 13-Pin-QFN3x4mm and Package 25-Pin-QFN5x4mm series

The input capacitor should be carefully placed to reduce the leakage inductance, or else, the high voltage spike caused by fast di/dt would cause extra voltage stress to the HS-MOS. Taking 13-Pin-QFN3x4mm series as an example, layout shown in Figure 2 are some common unqualified VIN capacitor layouts which will degrade the performance and stability.

For Figure 2-a), the input capacitor in the bottom layer is removed. Remember that the input capacitor in the bottom layer is a necessary.

Another bad example is given as Figure 2-b); it's even worse than the one shown in Figure 2-a. The input capacitors on the top layer are >2mm away from the IC edge, this will increase the leakage from Vin Capacitor to HS-MOS, leading to higher voltage stress during switching periods.



a) NG, Remove the Bottom Input Capacitor

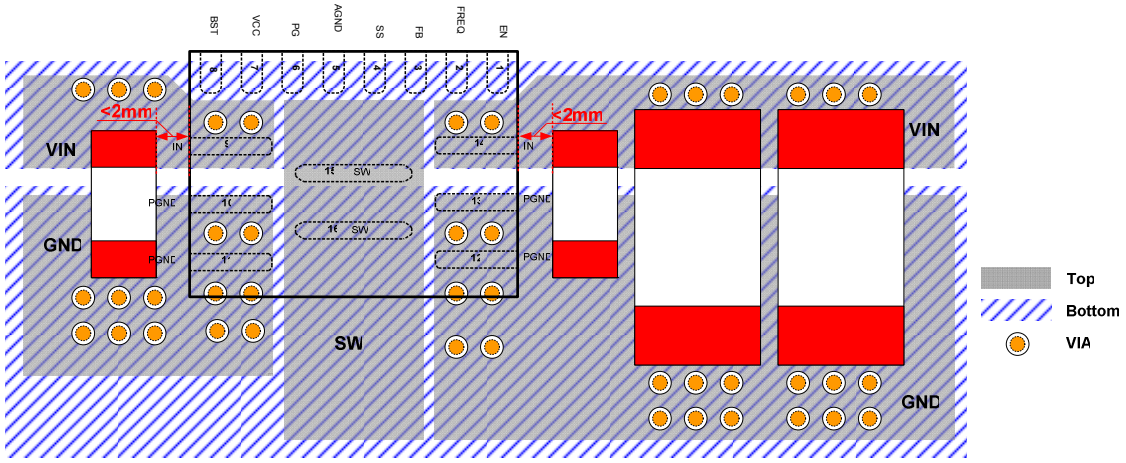
b) NG, Capacitor placed far from Vin and GND

Figure 2— Unqualified input capacitor placement for Package 13-Pin-QFN3x4mm and package 25-Pin-QFN5x4mm series

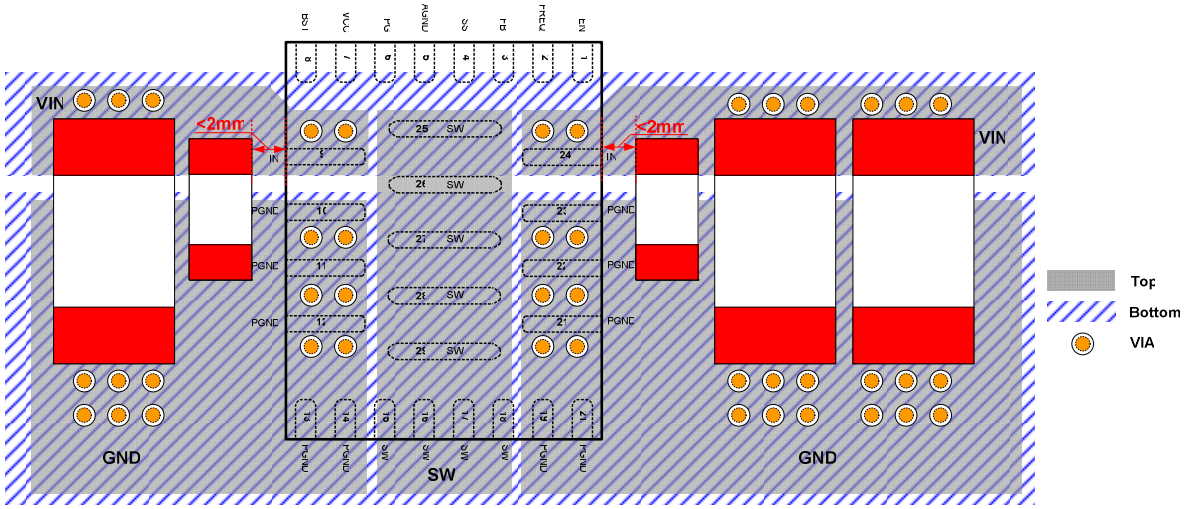
For Package 16-Pin-QFN3x4mm series and Package 29-Pin-QFN5x4mm series, the IN and PGND pins distribute at two opposite sides of the IC. Input capacitor should be placed at both sides, especially the 0.1uF-1uF 0402/0603 size decoupling capacitor. Put it within 2mm from the IC edge. Connect the

input capacitors to IN and PGND with short, direct and wide traces, joint these two VIN planes with vias through the bottom layer.

Recommended input capacitor placements for Package 16-Pin-QFN3x4mm series and Package 29-Pin-QFN5x4mm series are given as Figure 3.



a) Recommend input capacitor placement for Package 16-Pin-QFN3x4mm series



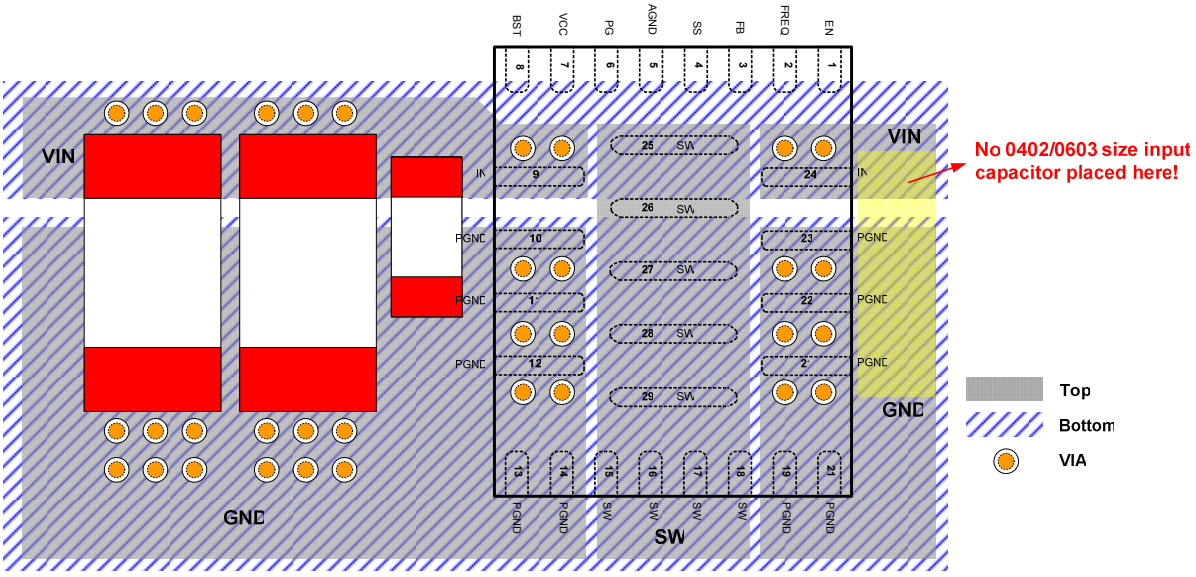
b) Recommend input capacitor placement for Package 29-Pin-QFN5x4mm

Figure 3—Optimized input capacitor placement for Package 16-Pin-QFN3x4mm Series and Package 29-Pin-QFN5x4mm Series

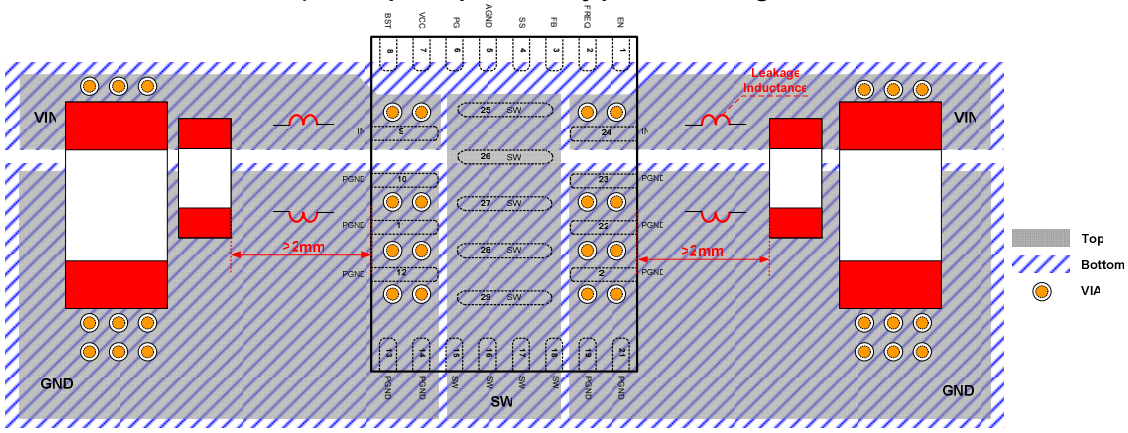
Figure 4 is some common unqualified VIN capacitor layouts which will degrade the performance for Package 29-Pin-QFN5x4mm series.

For Figure 4-a), the input capacitor only placed on one side or no 0402/0603 size decoupling capacitor on the other side. The VIN and PGND pins on the other side are far away from the input capacitor and badly decoupled. It will result in high voltage stress on the internal DMOS unit cells on this side.

For Figure 4-b), input capacitors placed on both sides in this case, however, they are >2mm away from the IC edge and far away VIN and PGND pins. This will increase the leakage from Vin Capacitor to HS-MOS, leading to higher voltage stress during switching periods.



a) NG, Input capacitor only placed on single side

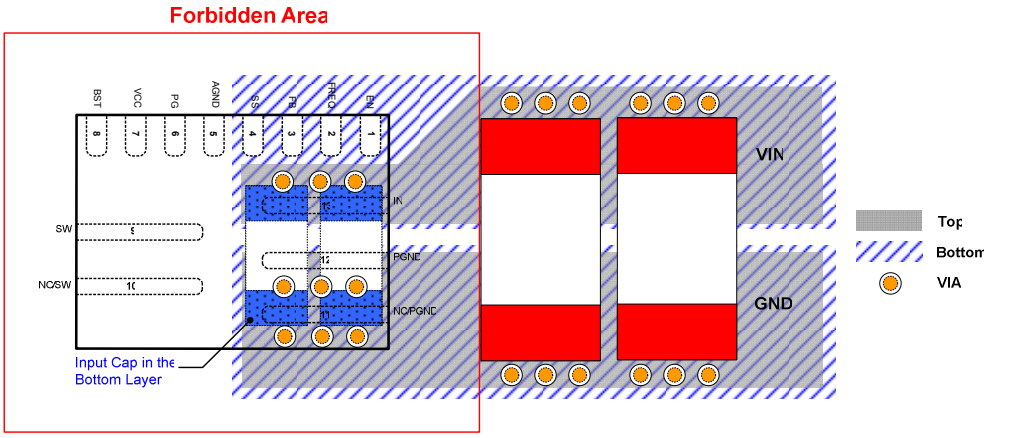


b) NG, Input capacitor placed far from VIN and PGND pins

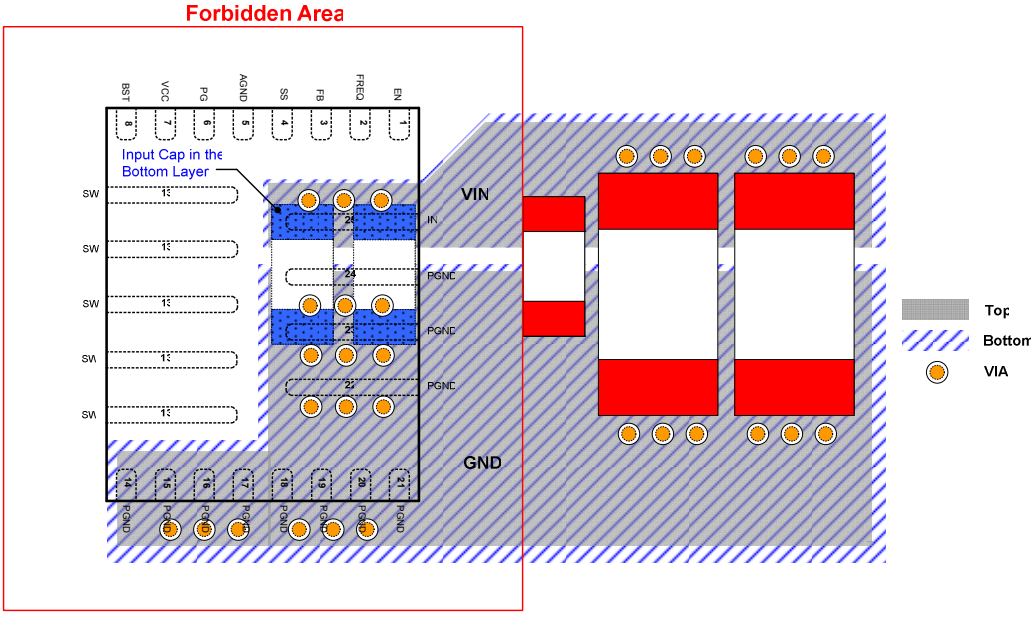
Figure 4—Unqualified input capacitor placement for Package 29-Pin-QFN5x4mm series

2) INPUT CAPACITOR WITH FORBIDDEN AREA

Some SMT house may suggest reserving a so called “forbidden area” around the IC, and it is not allowed to put the decoupling capacitor close to the IC inside the forbidden area. Actually, it’s not recommended to have forbidden area for the high current fully integrated converters. If it has to be, then it is strongly recommended to place ceramic capacitors in the bottom layer of the part. For Package 13-Pin-QFN3x4mm and Package 25-Pin-QFN5x4mm series, **at least two 0.1µF-1µF 0603 or 0402 size input capacitors should be placed directly below the IC to decouple VIN and PGND**, connecting to these pins through vias. Figure 5 shows the recommended input capacitor layout for applications with forbidden area.



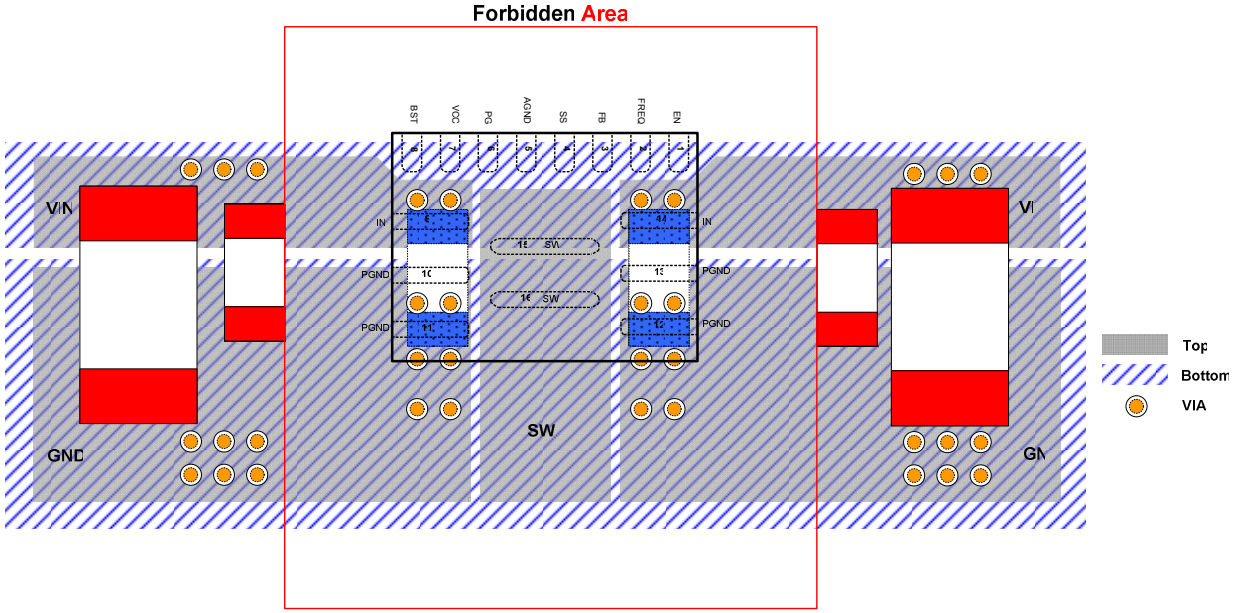
a) Package 13-Pin-QFN3x4mm series



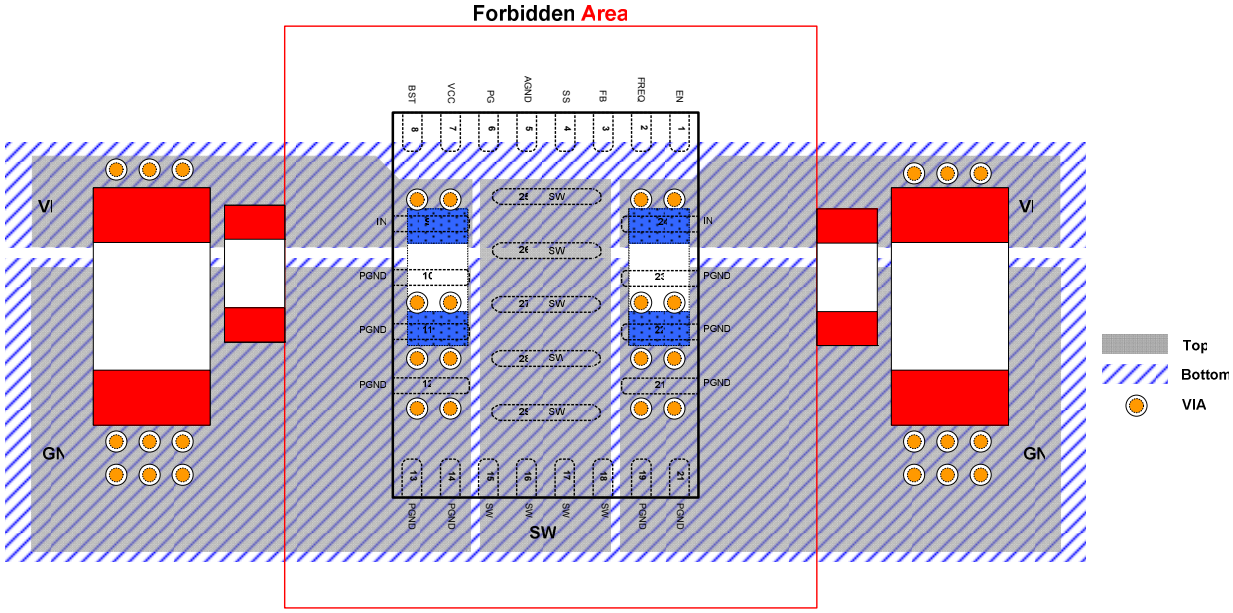
b) Package 25-Pin-QFN5x4mm series

Figure 5—Recommend input capacitor placement for applications with forbidden area Package 13-Pin-QFN3x4mm and package 25-Pin-QFN5x4mm series

For Package 16-Pin-QFN3x4mm series and Package 29-Pin-QFN5x4mm series, **at least one 0.1μF-1μF 0603 or 0402 size input capacitors should be placed directly below the IC on each side to decouple VIN and PGND**, connecting to these pins through vias. Figure 6 shows the recommended input capacitor layout for applications with forbidden area.



a) Package 16-Pin-QFN3x4mm series



b) Package 29-Pin-QFN5x4mm series

Figure 6—Recommend input capacitor placement for applications with forbidden area

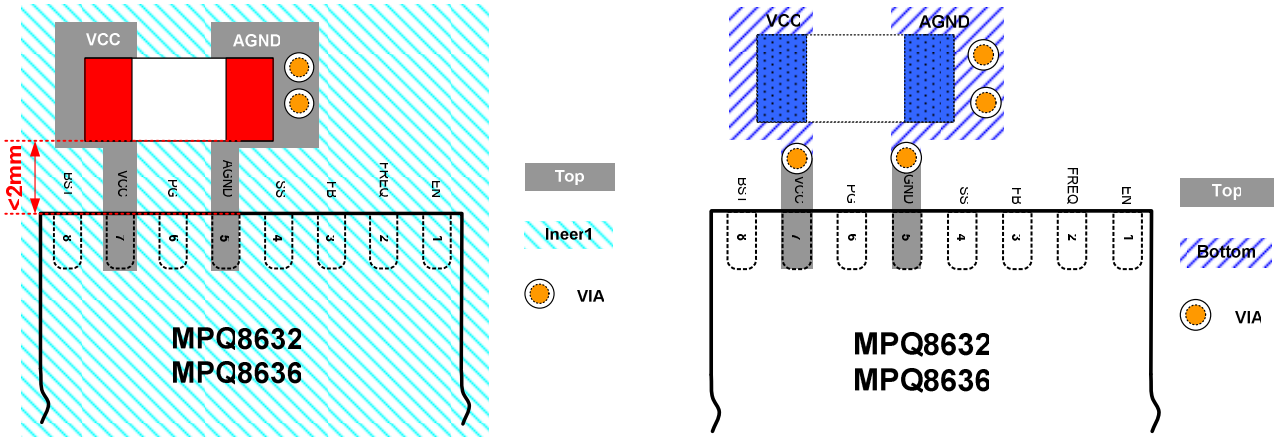
Package 16-Pin-QFN3x4mm series and Package 29-Pin-QFN5x4mm series

VCC DECOUPLING CAPACITOR AND AGND TO PGND CONNECTIONS

For MPQ8632 and MPQ8636 families, the VCC is an internal 4.8V LDO output that powers control circuits and drivers. VCC decoupling capacitor plays an important role in the DC-DC converters to make the logic circuits not noise coupled and then get a stable operation. Hence,

1) The VCC capacitor is required to be placed within 2mm from IC edge so as close to VCC and AGND pins. It is highly recommended to put the VCC capacitor in the same layers with the IC so that less or no via is required since vias will induce additional leakage inductance.
2) Besides the VCC capacitor placement, the connection from AGND to PGND is recommended to set close to the capacitor by at least two vias, and this connection is the only bridge from AGND to PGND, which means, the AGND of the system is Kelvin connect at VCC capacitor only to PGND plane in the inner1 layer.

The pin-out of control pins for both MPQ8632 and MPQ8636 families are same, even though their packages are different. VCC and AGND are located at the same side of the IC. The VCC capacitor can be easily placed next to VCC and AGND. Remember to put the VCC capacitor in the same layer with the IC and <2mm of the IC edge so as to minimize the leakage inductance from the capacitor to the VCC pin. Figure 7-a) shows the recommended VCC capacitor placement. Figure 7-b) has a VCC capacitor placed next to VCC and AGND pins; however, it is put in a different layer with the IC and connected to VCC and PGND pins through vias with leakage inductance. This is not as good as the recommended way.



a) Recommend

a) Not Recommend

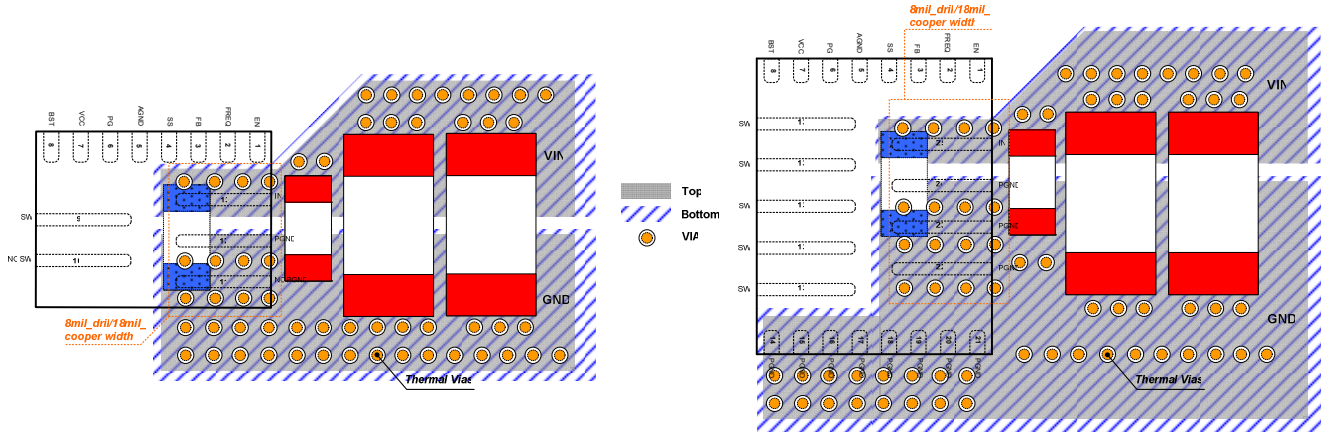
Figure 7—VCC capacitor placement for MPQ8632 and MPQ8636 families

ENHANCE INPUT POWER TRACE

The MPQ8632 and MPQ8636 families provides high power density solutions for DC-DC converters with output current around 4-20A in a small QFN3x4mm or QFN5x4mm package, hence, a better thermal performance is expected to prevent the converter from a high temperature rise. It is recommended that:

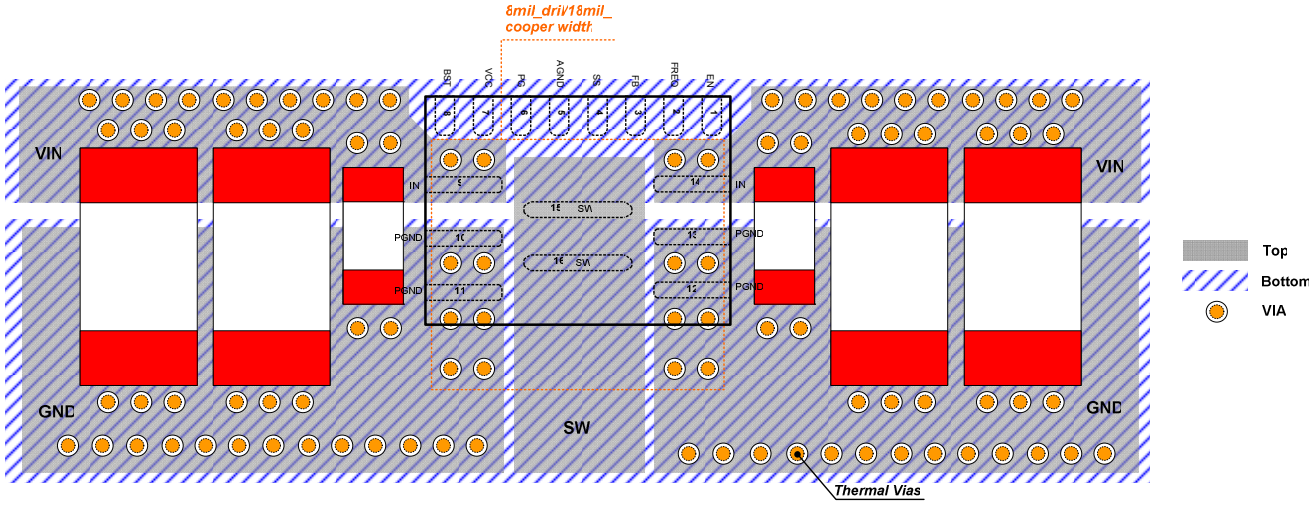
1) At least two layers are needed for the VIN and PGND power trace. Keep it short, direct and wide, and connect the two layers with vias. These vias are recommended to have 8mil_drill/18mil_copper width near the VIN and PGND pads and 16mil_drill/28mil_copper width near the input capacitors.
2) The vias placed under the part is quite important for thermal dissipation. It also helps to reduce the leakage inductance to the power MOSFET. **It is strongly recommended to place 8mil_drill/18mil_copper width vias between VIN and PGND pads directly under the part. For Package 13-Pin-QFN3x4mm series and Package 25-Pin-QFN5x4mm series, place at least 3 vias each under VIN and PGND. For Package 29-Pin-QFN5x4mm series, 2 vias each is recommended**.
3) Also, for a better thermal dissipation, place 16mil_drill/28mil_copper width vias as many as possible (>20) between the two input trace layers next to the VIN and PGND pins around the input capacitors.

Figure 8 describes the recommended layout for the enhanced VIN and PGND traces.

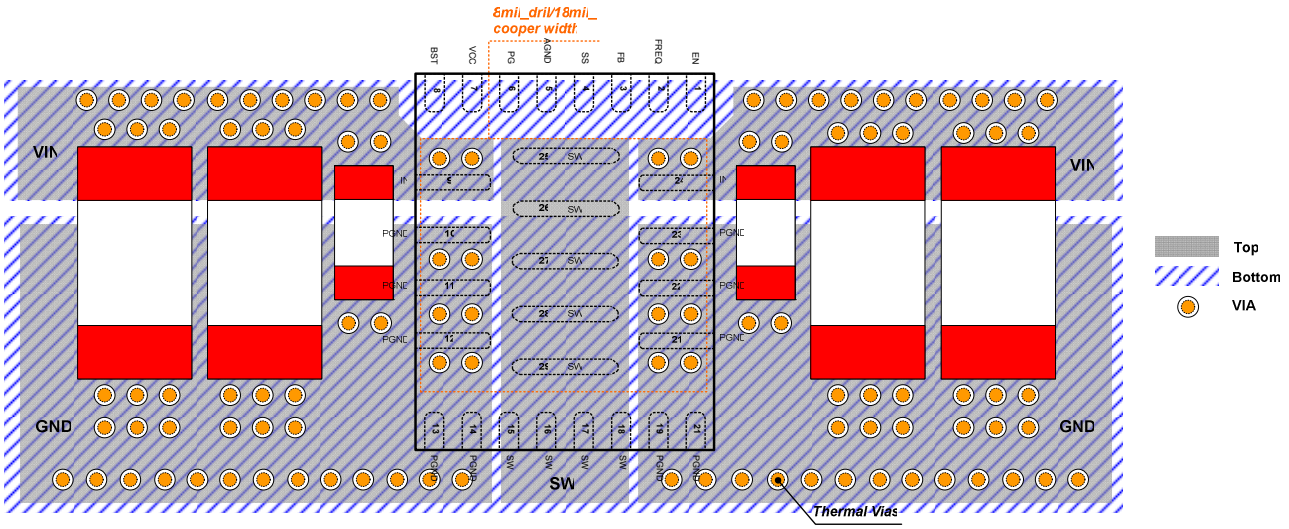


a) Package 13-Pin-QFN5x4mm Series

b) Package 25-Pin-QFN5x4mm Series



c) Package 16-Pin-QFN3x4mm Series



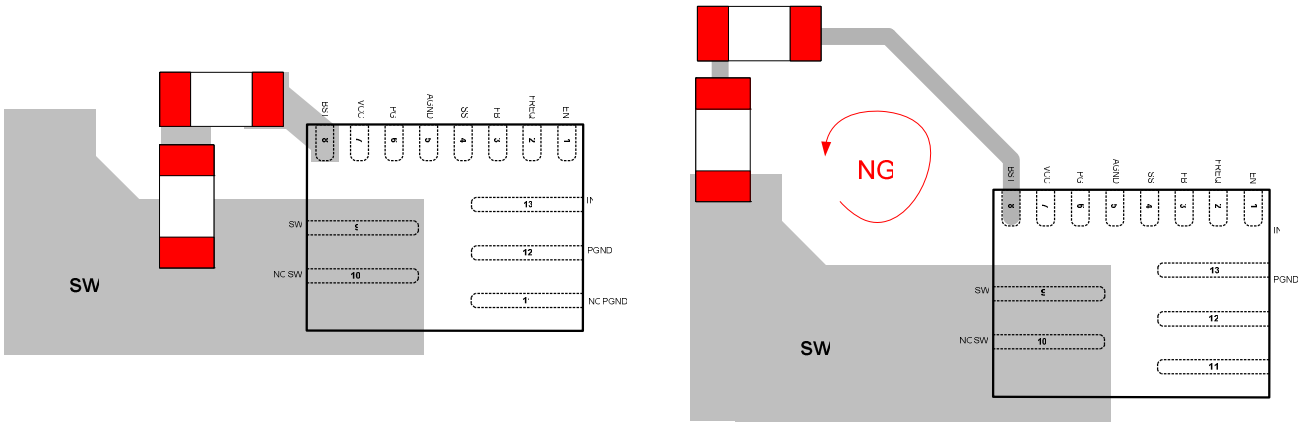
d) Package 29-Pin-QFN5x4mm Series

Figure 8—Recommend enhanced VIN and PGND Trace

BST RC PLACE AND TRACE

The BST capacitor provides a power source for the HS-MOS driver, the BST node changes as SW switches, so it is recommended to shrink the loop from the BST to SW and also make the leakage inductance smaller by **25-50mil traces**.

For Package 13-Pin-QFN3x4mm series and Package 25-Pin-QFN5x4mm series, they share similar pin-out and BST is located near SW pins. Take Package 13-Pin-QFN3x4mm series as an example, Figure 9-a) shows the recommended BST RC traces, and Figure 9-b) presents an example of poor BST loop layout.



a) Recommend BST trace, small loop and wider traces **b)Not Good BST trace**

Figure 9—Recommend and Not Good BST Loop Placement for Package 13-Pin-QFN3x4mm and Package 25-Pin-QFN5x4mm Series

For Package 29-Pin-QFN5x4mm series, BST is located away from SW pins. BST loop can only connect to SW node through vias. Remember to shrink the BST loop by connecting to SW with short traces. Figure 10 shows the recommend BST RC traces for Package 29-Pin-QFN5x4mm series.

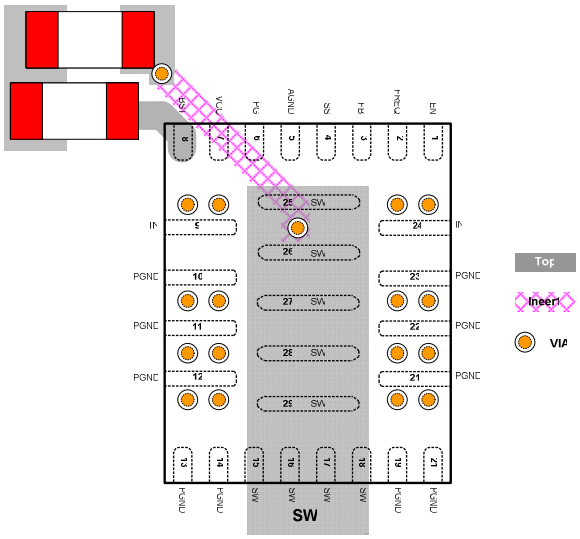


Figure 10—Recommend and Not Good BST Loop Placement for Package 29-Pin-QFN5x4mm Series

FEEDBACK RESISTORS, COMPENSATION NETWORK AND OUTPUT SENSE

A poor feedback and external compensation network layout will degrade system stability and also leads to poor line and load regulation. Several recommendations are listed as below:

1) The feedback resistors should be placed next to the FB pin to reduce the leakage inductance between tap of the resistors and FB pin. Do not connect FB to these resistors through vias.
2) The down side resistor, usually named as R2, need to be connected to AGND, not PGND.
3) The up resistor R1 should be connect to the output capacitor where you want the output voltage to be at your setting
4) MPQ8632 and MPQ8636 are COT parts and need external compensation to make the system stable. When the output capacitors are ceramic ones, a RC compensation network, usually named as R4/C4 is needed. Then, place them near the FB resistors to make the FB trace short. Especially the compensation resistor, the node connect to net FB is more important. Remember to put this node near FB resistors to get better line and load regulation. Then connect the other node to SW with short path to reduce its noise.
5) When the external RC compensation network is applied, the compensation capacitor C4 should be connected to output too. It should share the same path with FB resistors output sense. Also C4 should be placed near R1 to make sure that no noise is coupled into the output sense loop.

Figure 11 describes the optimized FB resistors, compensation R4/C4 network and output sense layout for MPQ8632 and MPQ8636 families. We can see that the output dividers R1 and R2 are close to the

IC. The external compensation network R4/C4 is near the output dividers. R1 and C4 connect to output through the same path.

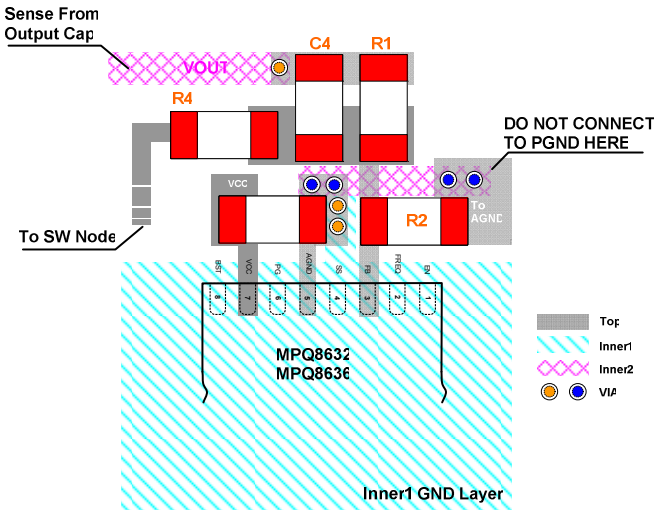


Figure 11—Recommend feedback resistors placement

GENERAL RECOMMEND PCB LAYOUT FOR MPQ8632 AND MPQ8636 FAMILIES

Based on the above sections, the map of PCB layout with all the design note included is shown below. We recommend use at least 4 layers PCB for these high current POL solution to achieve better thermal performance and get stable operation. The layer structure can be as follow.

RECOMMEND LAYOUT FOR 13-PIN-QFN3X4MM SERIES: MPQ8632GL-4/6/8/10/12, MPQ8632HGL-10, MPQ8636GL-10, MPQ8636HGL-10

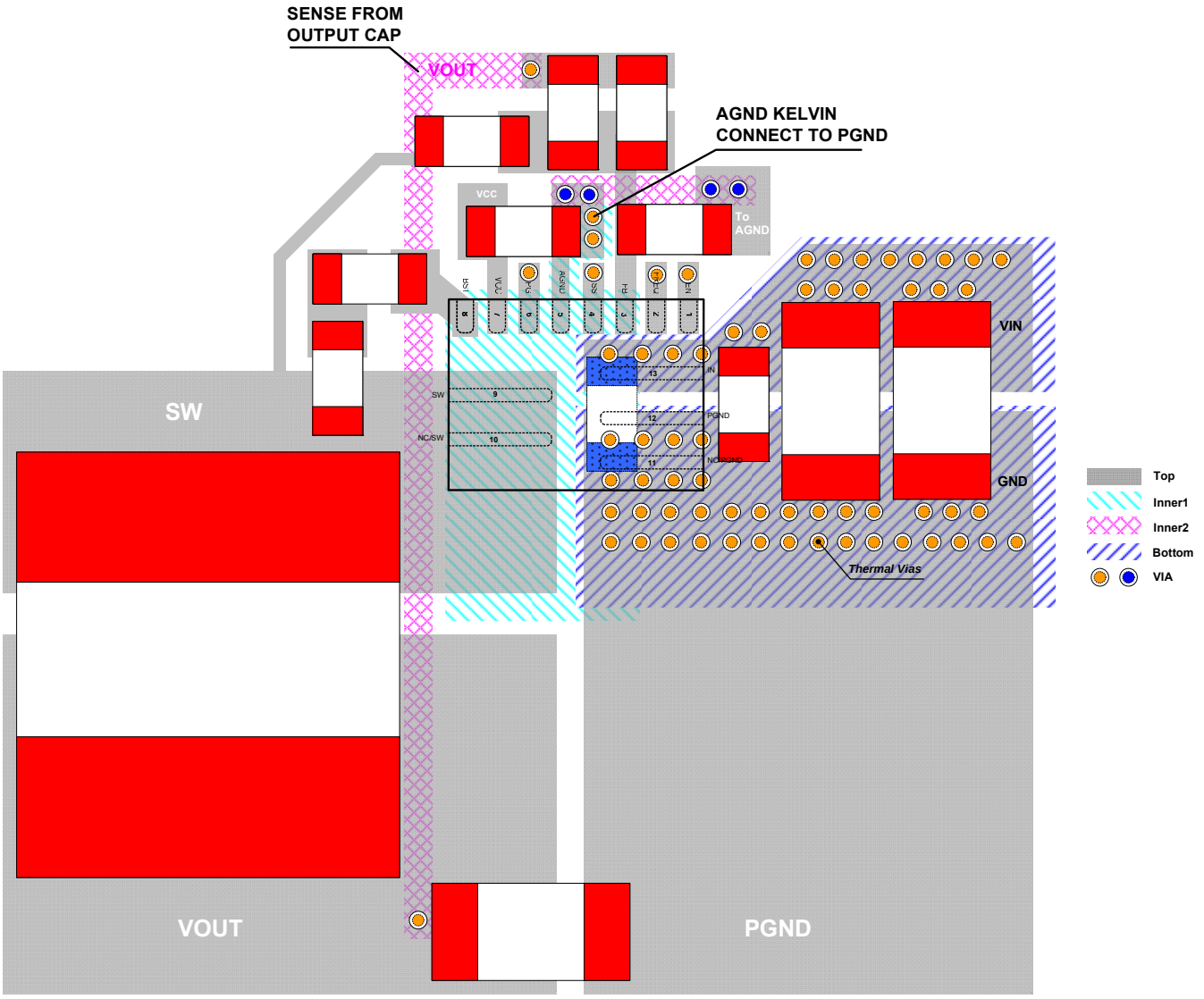


Figure 12—Recommend Layout for 13-Pin-QFN3x4mm Series MPQ8632GL-4/6/8/10/12, MPQ8632HGL-10, MPQ8636GL-10, MPQ8636HGL-10

RECOMMEND LAYOUT FOR 16-PIN-QFN3X4MM SERIES: MPQ8632GLE-4/6/8/10/12, MPQ8632HGLE-10, MPQ8636GLE-10, MPQ8636HGLE-10

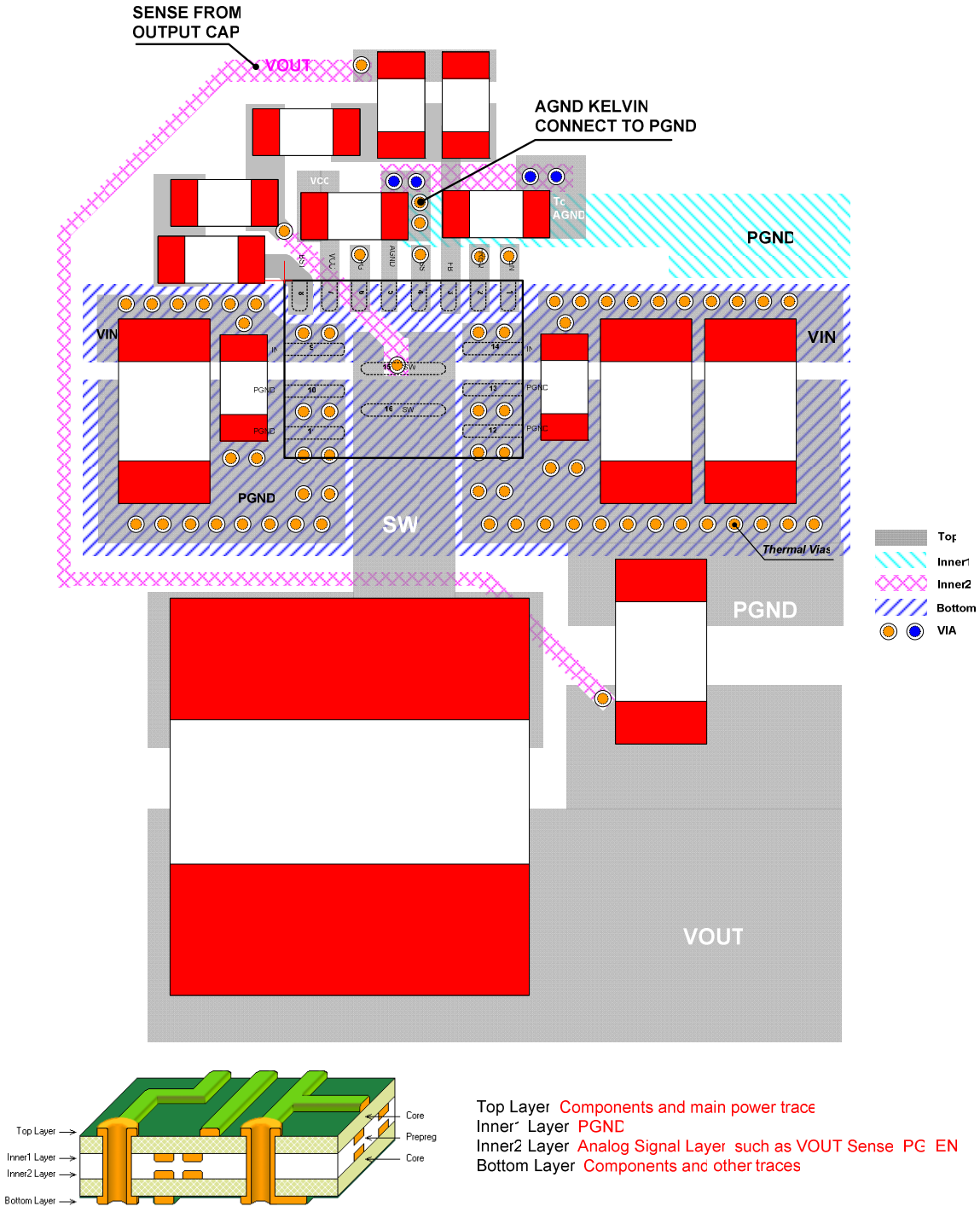


Figure 13—Recommend Layout for 16-Pin-QFN3x4mm Series MPQ8632GLE-4/6/8/10/12, MPQ8632HGLE-10, MPQ8636GLE-10, MPQ8636HGLE-10

RECOMMEND LAYOUT FOR 25-PIN-QFN5X4MM SERIES: MPQ8632GV-15/20, MPQ8636GV-20

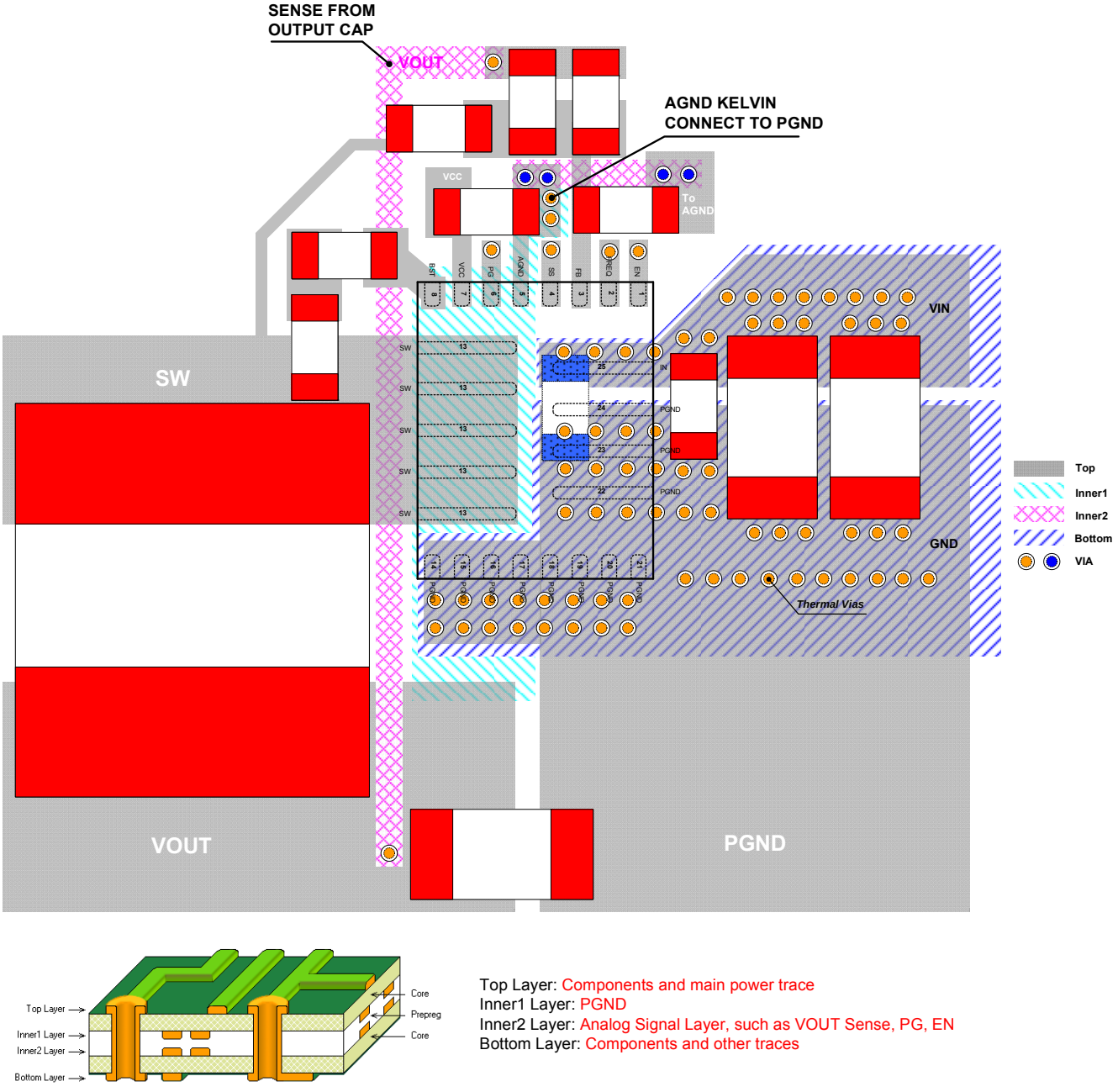


Figure 14—Recommend Layout for 25-Pin-QFN5x4mm Series MPQ8632GV-15/20, MPQ8636GV-20

RECOMMEND LAYOUT FOR 29-PIN-QFN5X4MM SERIES: MPQ8632GVE-15/20, MPQ8636GVE-20

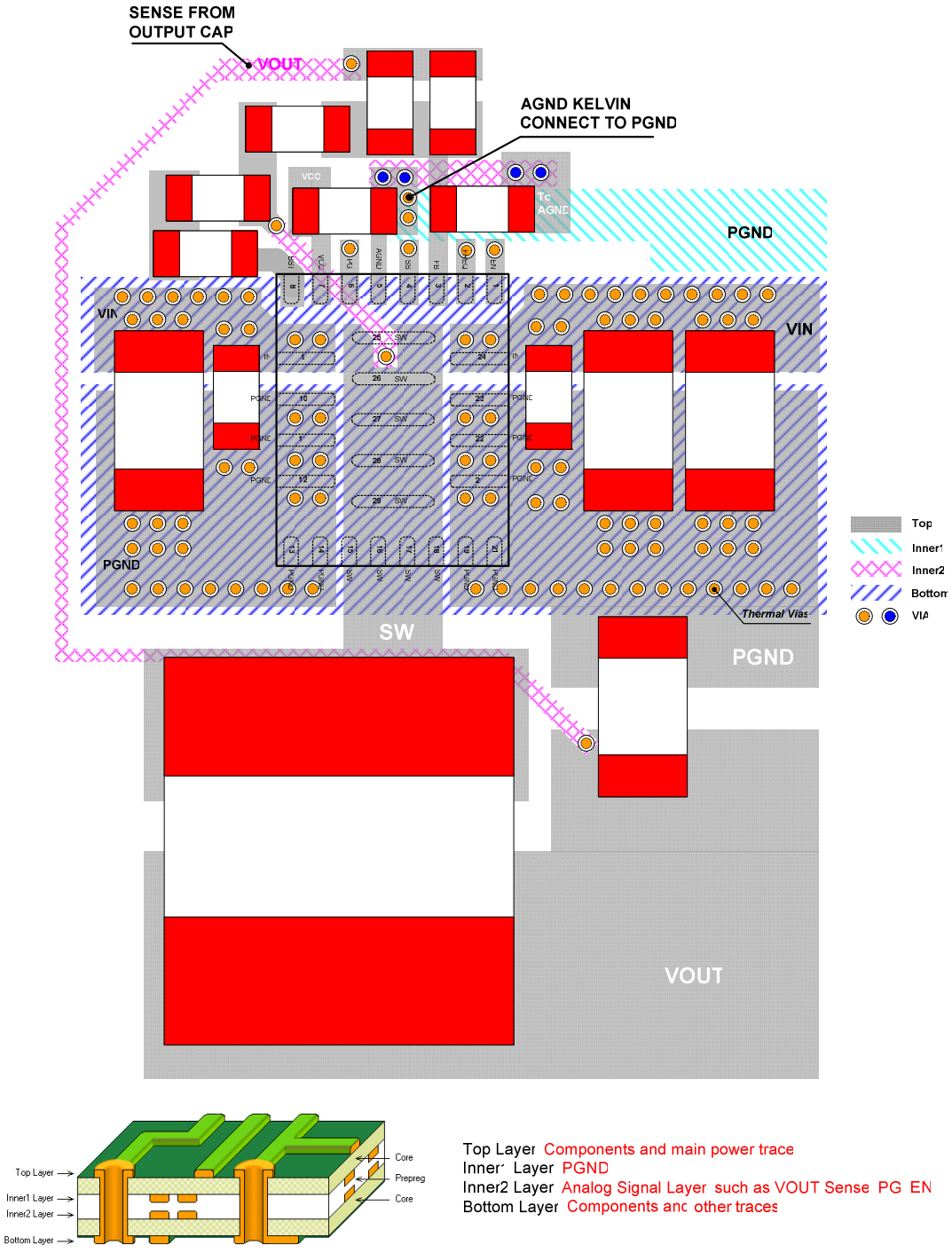


Figure 15—Recommend Layout for 29-Pin-QFN5x4mm Series MPQ8632GVE-15/20, MPQ8636GVE-20