DDR3 SDRAM SODIMM

MT16JSF25664HZ – 2GB

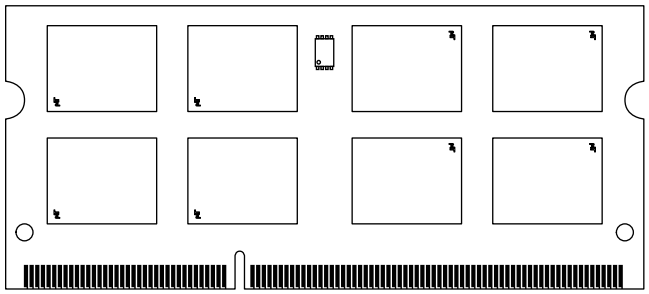
MT16JSF51264HZ – 4GB

Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 204-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC3- 12800, PC3-10600, PC3-8500, or PC3-6400
- 2GB (256 Meg x 64), 4GB (512 Meg x 64)
- V_{DD} = 1.5V ±0.075V
- V_{DDSPD}= +3.0V to +3.6V
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Dual rank
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 8 internal device banks
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 204-Pin SODIMM (MO-268 R/C F)

Module height: 30mm (1.18in)



Options — Marking

- Operating temperature[1]
  - Commercial (0°C ≤ T_A ≤ +70°C) — None
  - Industrial (–40°C ≤ T_A ≤ +85°C) — I
- Package
  - Halogen-free DIMM — Z
- Frequency/CAS latency
  - 1.25ns @ CL = 11 (DDR3-1600) — -1G6
  - 1.5ns @ CL = 9 (DDR3-1333) — -1G4
  - 1.87ns @ CL = 7 (DDR3-1066) — -1G1
  - 1.87ns @ CL = 8 (DDR3-1066)[2] — -1G0
  - 2.5ns @ CL = 5 (DDR3-800)[2] — -80C
  - 2.5ns @ CL = 6 (DDR3-800)[2] — -80B

Notes: 1. Contact Micron for industrial temperature module offerings.
2. Not recommended for new designs.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)							^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G6	PC3-12800	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	1066	–	800	667	15	15	52.5
-80C	PC3-6400	–	–	–	–	–	800	800	12.5	12.5	50
-80B	PC3-6400	–	–	–	–	–	800	667	15	15	52.5

Table 2: Addressing

Parameter	2GB	4GB
Refresh count	8K	8K
Row address	16K A[13:0]	32K A[14:0]
Device bank address	8 BA[2:0]	8 BA[2:0]
Device configuration	1Gb (128 Meg x 8)	2Gb (256 Meg x 8)
Column address	1K A[9:0]	1K A[9:0]
Module rank address	2 S#[1:0]	2 S#[1:0]

Table 3: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT41J128M8,[1] 1Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT16JSF25664H(I)Z-1G6__	2GB	256 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT16JSF25664H(I)Z-1G4__	2GB	256 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT16JSF25664H(I)Z-1G1__	2GB	256 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT16JSF25664HZ-1G4D1.

Table 4: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT41J256M8,[1] 2Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT16JSF51264H(I)Z-1G6__	4GB	512 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT16JSF51264H(I)Z-1G4__	4GB	512 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT16JSF51264H(I)Z-1G1__	4GB	512 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT16JSF51264HZ-1G4D1.

Pin Assignments and Descriptions

Table 5: Pin Assignments

204-Pin DDR3 SODIMM Front								204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	53	DQ19	105	V_{DD}	157	DQ42	2	V_{SS}	54	V_{SS}	106	V_{DD}	158	DQ46
3	V_{SS}	55	V_{SS}	107	A10	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47
5	DQ0	57	DQ24	109	BA0	161	V_{SS}	6	DQ5	58	DQ29	110	RAS#	162	V_{SS}
7	DQ1	59	DQ25	111	V_{DD}	163	DQ48	8	V_{SS}	60	V_{SS}	112	V_{DD}	164	DQ52
9	V_{SS}	61	V_{SS}	113	WE#	165	DQ49	10	DQS0#	62	DQS3#	114	S0#	166	DQ53
11	DM0	63	DM3	115	CAS#	167	V_{SS}	12	DQS0	64	DQS3	116	ODT0	168	V_{SS}
13	V_{SS}	65	V_{SS}	117	V_{DD}	169	DQS6#	14	V_{SS}	66	V_{SS}	118	V_{DD}	170	DM6
15	DQ2	67	DQ26	119	A13	171	DQS6	16	DQ6	68	DQ30	120	ODT1	172	V_{SS}
17	DQ3	69	DQ27	121	S1#	173	V_{SS}	18	DQ7	70	DQ31	122	NC	174	DQ54
19	V_{SS}	71	V_{SS}	123	V_{DD}	175	DQ50	20	V_{SS}	72	V_{SS}	124	V_{DD}	176	DQ55
21	DQ8	73	CKE0	125	NC	177	DQ51	22	DQ12	74	CKE1	126	V_{REFCA}	178	V_{SS}
23	DQ9	75	V_{DD}	127	V_{SS}	179	V_{SS}	24	DQ13	76	V_{DD}	128	V_{SS}	180	DQ60
25	V_{SS}	77	NC	129	DQ32	181	DQ56	26	V_{SS}	78	NC	130	DQ36	182	DQ61
27	DQS1#	79	BA2	131	DQ33	183	DQ57	28	DM1	80	NC/A14	132	DQ37	184	V_{SS}
29	DQS1	81	V_{DD}	133	V_{SS}	185	V_{SS}	30	RESET#	82	V_{DD}	134	V_{SS}	186	DQS7#
31	V_{SS}	83	A12	135	DQS4#	187	DM7	32	V_{SS}	84	A11	136	DM4	188	DQS7
33	DQ10	85	A9	137	DQS4	189	V_{SS}	34	DQ14	86	A7	138	V_{SS}	190	V_{SS}
35	DQ11	87	V_{DD}	139	V_{SS}	191	DQ58	36	DQ15	88	V_{DD}	140	DQ38	192	DQ62
37	V_{SS}	89	A8	141	DQ34	193	DQ59	38	V_{SS}	90	A6	142	DQ39	194	DQ63
39	DQ16	91	A5	143	DQ35	195	V_{SS}	40	DQ20	92	A4	144	V_{SS}	196	V_{SS}
41	DQ17	93	V_{DD}	145	V_{SS}	197	SA0	42	DQ21	94	V_{DD}	146	DQ44	198	EVENT#
43	V_{SS}	95	A3	147	DQ40	199	V_{DDSPD}	44	V_{SS}	96	A2	148	DQ45	200	SDA
45	DQS2#	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	V_{SS}	202	SCL
47	DQS2	99	V_{DD}	151	V_{SS}	203	V_{TT}	48	V_{SS}	100	V_{DD}	152	DQS5#	204	V_{TT}
49	V_{SS}	101	CK0	153	DM5	–	–	50	DQ22	102	CK1	154	DQS5	–	–
51	DQ18	103	CK0#	155	V_{SS}	–	–	52	DQ23	104	CK1#	156	V_{SS}	–	–

Table 6: Pin Descriptions

Symbol	Type	Description
A[14:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC4/BL8 identification as "BL on-the-fly" during CAS commands. The address inputs also provide the op-code during the mode register command set. A[12:0] address the 1Gb DDR3 devices. A[13:0] address the 1Gb DDR3 devices. A[14:0] address the 2Gb DDR3 devices.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command.
CK[1:0], CK#[1:0]	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE[1:0]	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DM[7:0]	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of the DQS. Although the DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
ODT[1:0]	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DD}. RESET# assertion and deassertion are asynchronous.
S#[1:0]	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[1:0]	Input	**Presence-detect address inputs:** These pins are used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize communication to and from the temperature sensor/SPD EEPROM.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[7:0], DQS#[7:0]	I/O	**Data strobe:** DQS and DQS# are differential data strobes. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the module on the I^2C bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.

Table 6: Pin Descriptions (Continued)

Symbol	Type	Description
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** +3.0V to +3.6V. The component V_{DD} and V_{DDQ} are connected to the module Vdd.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address (V_{DD}/2).
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM (V_{DD}/2).
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address (V_{DD}/2).
NC	–	**No connect:** These pins are not connected on the module.

DQ Map

Table 7: Component-to-Module DQ Map (Front)

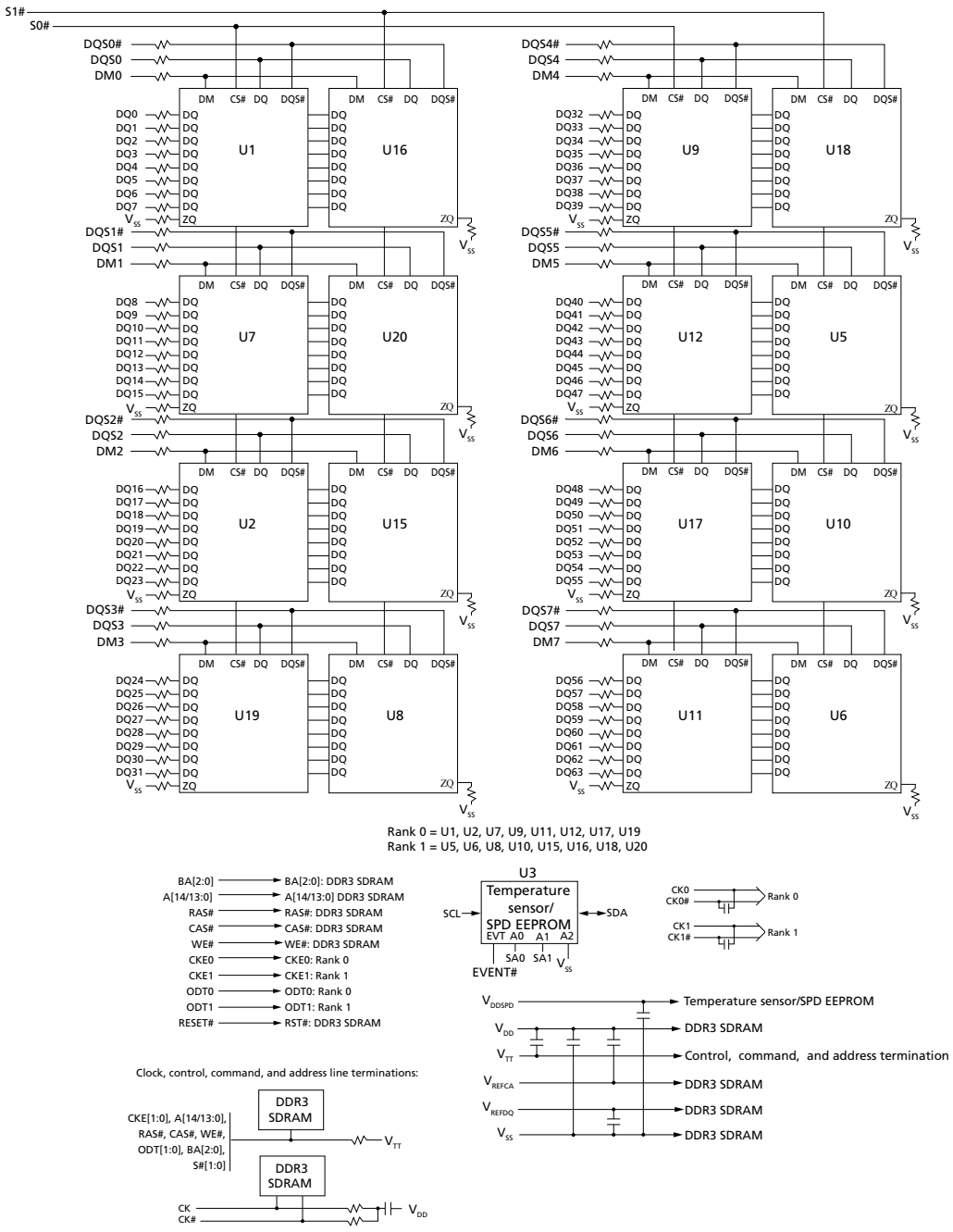
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	2	15	U2	0	18	51
	1	5	6		1	21	42
	2	3	17		2	19	53
	3	0	5		3	16	39
	4	6	16		4	22	50
	5	4	4		5	20	40
	6	7	18		6	23	52
	7	1	7		7	17	41
U5	0	42	157	U6	0	58	191
	1	45	148		1	61	182
	2	43	159		2	59	193
	3	40	147		3	56	181
	4	46	158		4	62	192
	5	44	146		5	60	180
	6	47	160		6	63	194
	7	41	149		7	57	183
U7	0	13	24	U8	0	26	67
	1	10	33		1	29	58
	2	8	21		2	27	69
	3	11	35		3	24	57
	4	9	23		4	30	68
	5	15	36		5	28	56
	6	12	22		6	31	70
	7	14	34		7	25	59
U9	0	34	141	U10	0	53	166
	1	37	132		1	50	175
	2	35	143		2	48	163
	3	32	129		3	51	177
	4	38	140		4	49	165
	5	36	130		5	55	176
	6	39	142		6	52	164
	7	33	131		7	54	174

Table 8: Component-to-Module DQ Map (Back)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	61	182	U12	0	45	148
	1	58	191		1	42	157
	2	56	181		2	40	147
	3	59	193		3	43	159
	4	57	183		4	41	149
	5	63	194		5	47	160
	6	60	180		6	44	146
	7	62	192		7	46	158
U15	0	21	42	U16	0	5	6
	1	18	51		1	2	15
	2	16	39		2	0	5
	3	19	53		3	3	17
	4	17	41		4	1	7
	5	23	52		5	7	18
	6	20	40		6	4	4
	7	22	50		7	6	16
U17	0	50	175	U18	0	37	132
	1	53	166		1	34	141
	2	51	177		2	32	129
	3	48	163		3	35	143
	4	54	174		4	33	131
	5	52	164		5	39	142
	6	55	176		6	36	130
	7	49	165		7	38	140
U19	0	29	58	U20	0	10	33
	1	26	67		1	13	24
	2	24	57		2	11	35
	3	27	69		3	8	21
	4	25	59		4	14	34
	5	31	70		5	12	22
	6	28	56		6	15	36
	7	30	68		7	9	23

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	+1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	+1.975	V

Table 10: Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage	1.425	1.5	1.575	V	
I_{VTT}	Termination reference current from V_{TT}	–600	–	+600	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	1

Table 10: Operating Conditions (Continued)

Symbol	Parameter		Min	Nom	Max	Units	Notes
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA	–32	0	+32	µA	
		S#, CKE, ODT, CK, CK#	–16	0	+16		
		DM	–4	0	+4		
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DD}; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	–10	0	+10	µA	
I_{VREF}	V_{REF} supply leakage current; V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V)		–16	0	+16	µA	
T_A	Module ambient operating temperature	Commercial	0	–	+70	°C	2, 3
		Industrial	–40	–	+85	°C	
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	+95	°C	2, 3, 4
		Industrial	–40	–	+95	°C	

Notes:
1. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. T_A and T_C are simultaneous requirements.
3. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
4. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown below.

Table 11: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

Table 12: DDR3 I_{DD} Specifications and Conditions – 2GB

Values are for the MT41J128M8 DDR3 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	800	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}[1]	1056	976	896	816	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}[1]	1216	1136	1056	976	mA
Precharge power-down current: Slow exit	I_{DD2P}[2]	192	192	192	192	mA
Precharge power-down current: Fast exit	I_{DD2P}[2]	720	640	560	480	mA
Precharge quiet standby current	I_{DD2Q}[2]	1072	960	848	736	mA
Precharge standby current	I_{DD2N}[2]	1120	1040	880	800	mA
Precharge standby ODT current	I_{DD2NT}[2]	856	776	696	616	mA
Active power-down current	I_{DD3P}[2]	720	640	560	480	mA
Active standby current	I_{DD3N}[2]	1072	992	912	832	mA
Burst read operating current	I_{DD4R}[1]	2096	1696	1376	1136	mA
Burst write operating current	I_{DD4W}[1]	2096	1856	1616	1376	mA
Refresh current	I_{DD5B}[2]	4160	3840	3520	3200	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}[2]	96	96	96	96	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}[2]	144	144	144	144	mA
All banks interleaved read current	I_{DD7}[1]	4896	4016	3216	2896	mA
Reset current	I_{DD8}[2]	224	224	224	224	mA

Notes:
1. One module rank in the active I_{DD}; the other rank in I_{DD2P} (slow exit).
2. All ranks in this I_{DD} condition.

Table 13: DDR3 I_{DD} Specifications and Conditions – 4GB

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	800	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}[1]	TBD	816	736	656	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}[1]	TBD	1016	896	776	mA
Precharge power-down current: Slow exit	I_{DD2P}[2]	TBD	192	192	192	mA
Precharge power-down current: Fast exit	I_{DD2P}[2]	TBD	560	480	480	mA
Precharge quiet standby current	I_{DD2Q}[2]	TBD	1040	880	720	mA
Precharge standby current	I_{DD2N}[2]	TBD	1040	880	720	mA

Table 13: DDR3 I_{DD} Specifications and Conditions – 4GB (Continued)

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1600	1333	1066	800	Units
Precharge standby ODT current	I_{DD2NT}[2]	TBD	776	696	576	mA
Active power-down current	I_{DD3P}[2]	TBD	720	640	560	mA
Active standby current	I_{DD3N}[2]	TBD	1200	960	800	mA
Burst read operating current	I_{DD4R}[1]	TBD	1696	1376	1096	mA
Burst write operating current	I_{DD4W}[1]	TBD	2016	1696	1336	mA
Refresh current	I_{DD5B}[2]	TBD	4080	3920	3600	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}[2]	TBD	144	144	144	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}[2]	TBD	192	192	192	mA
All banks interleaved read current	I_{DD7}[1]	TBD	3016	2656	2416	mA
Reset current	I_{DD8}[2]	TBD	224	224	224	mA

Notes:
1. One module rank in the active I_{DD}; the other rank in I_{DD2P} (slow exit).
2. All ranks in this I_{DD} condition.

Temperature Sensor with Serial Presence-Detect EEPROM

The temperature from the integrated thermal sensor is monitored and converts into a digital word via the I^2C bus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. User-specific information can be written into the remaining 128 bytes of storage. READ/WRITE operations between the system (master) and the EEPROM (slave) device occur via an I^2C bus. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protect. For further information please refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

Table 14: Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	+3.0	+3.6	V
Supply current: V_{DD} = 3.3V	I_{DD}	–	+2.0	mA
Input high voltage: Logic 1; SCL, SDA	V_{IH}	+1.45	V_{DDSPD} + 1	V
Input low voltage: Logic 0; SCL, SDA	V_{IL}	–	+0.55	V
Output low voltage: I_{OUT} = 2.1mA	V_{OL}	–	+0.4	V
Input current	I_{IN}	–5.0	+5.0	µA
Temperature sensing range	–	–40	+125	°C
Temperature sensor accuracy (initial release)	–	–2.0	+2.0	°C
Temperature sensor accuracy (class B)	–	–1.0	+1.0	°C

Table 15: Sensor and EEPROM Serial Interface Timing

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	^tBUF	4.7	–	µs
SDA fall time	^tF	20	300	ns
SDA rise time	^tR	–	1,000	ns
Data hold time	$^tHD:DAT$	200	900	ns
Start condition hold time	$^tH:STA$	4.0	–	µs
Clock HIGH period	^tHIGH	4.0	50	µs
Clock LOW period	^tLOW	4.7	–	µs
SCL clock frequency	^tSCL	10	100	kHz
Data setup time	$^tSU:DAT$	250	–	ns

Table 15: Sensor and EEPROM Serial Interface Timing (Continued)

Parameter/Condition	Symbol	Min	Max	Units
Start condition setup time	^{t}SU:STA	4.7	–	µs
Stop condition setup time	^{t}SU:STO	4.0	–	µs

EVENT# Pin

The temperature sensor also adds the EVENT# pin (open drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. The open-drain output of EVENT# under the three separate operating modes is illustrated below. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and only returns to the logic HIGH state when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.

SMBus Slave Subaddress Decoding

The temperature sensor's physical address differs from the SPD EEPROM's physical address: binary 0011 for A0, A1, and RW#, where A1 and A0 are the two slave subaddress pins, and the RW# bit is the READ/WRITE flag.

If the slave base address is fixed for the temperature sensor/SPD EEPROM, then the pins set the subaddress bits of the slave address, enabling the devices to be located anywhere within the eight slave address locations. For example, they could be set from 30h to 3Eh.

Figure 3: EVENT# Pin Functionality

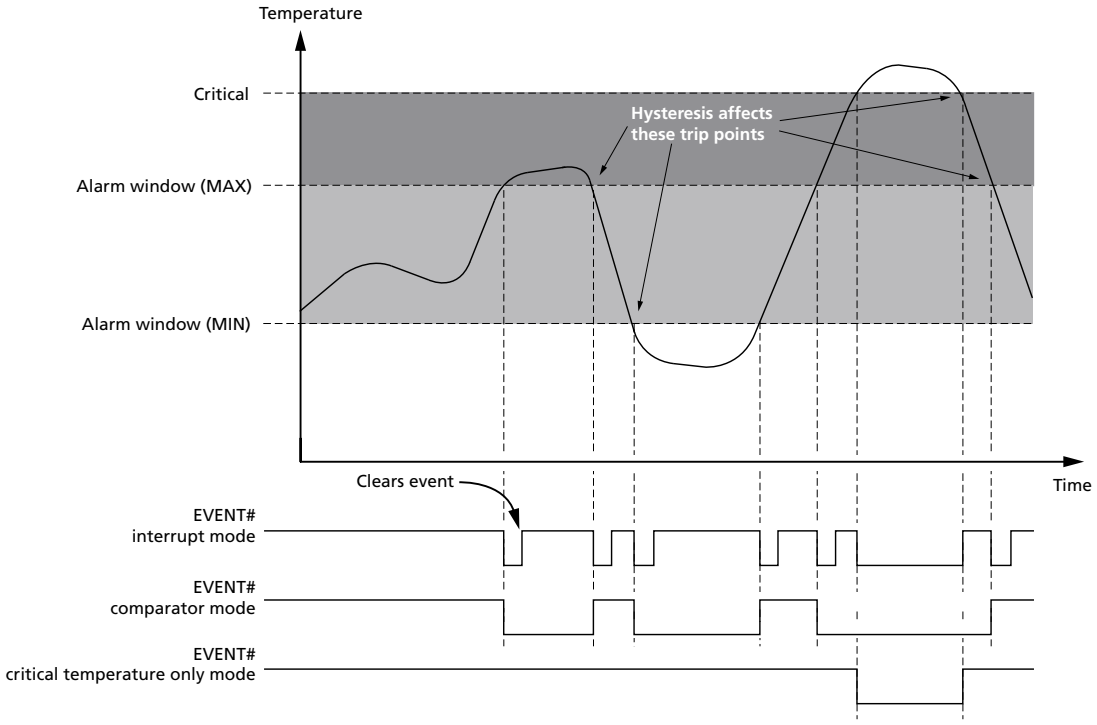


Table 16: Temperature Sensor Registers

Name	Address	Power-on Default
Pointer register	Not applicable	Undefined
Capability register	0x00	0x0001
Configuration register	0x01	0x0000
Alarm temperature upper boundary register	0x02	0x0000
Alarm temperature lower boundary register	0x03	0x0000
Critical temperature register	0x04	0x0000
Temperature register	0x05	Undefined

Pointer Register

The pointer register selects which of the 16-bit registers is being accessed in subsequent READ and WRITE operations. This register is a write-only register.

Table 17: Pointer Register Bits 0–7

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	Register select	Register select	Register select	Register select

Table 18: Pointer Register Bits 0–2 Descriptions

Bit			Register
2	1	0	
0	0	0	Capability register
0	0	1	Configuration register
0	1	0	Alarm temperature upper boundary register
0	1	1	Alarm temperature lower boundary register
1	0	0	Critical temperature register
1	0	1	Temperature register

Capability Register

The capability register indicates the features and functionality supported by the temperature sensor. This register is a read-only register.

Table 19: Capability Register (Address: 0x00)

Bit							
15	14	13	12	11	10	9	8
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Bit							
7	6	5	4	3	2	1	0
RFU	RFU	RFU	Temperature resolution		Wider range	Precision	Has alarm and critical temperature

Table 20: Capability Register Bit Description

Bit	Description
0	Basic capability 1: Has alarm and critical trip point capabilities
1	Accuracy 0: ±2°C over the active range and ±3°C over the monitor range 1: ±1°C over the active range and ±2°C over the monitor range
2	Wider range 0: Temperatures lower than 0°C are clamped to a binary value of 0 1: Temperatures below 0°C can be read

Table 20: Capability Register Bit Description (Continued)

Bit	Description
4:3	Temperature resolution 00: 0.5°C LSB 01: 0.25°C LSB 10: 0.125°C LSB 11: 0.0625°C LSB
15:5	0: Must be set to zero

Configuration Register

Table 21: Configuration Register (Address: 0x01)

Bit							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RFU	RFU	RFU	RFU	RFU	Hysteresis		Shutdown mode
Bit							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Critical lock bit	Alarm lock bit	Clear event	Event output status	Event output control	Critical event only	Event polarity	Event mode

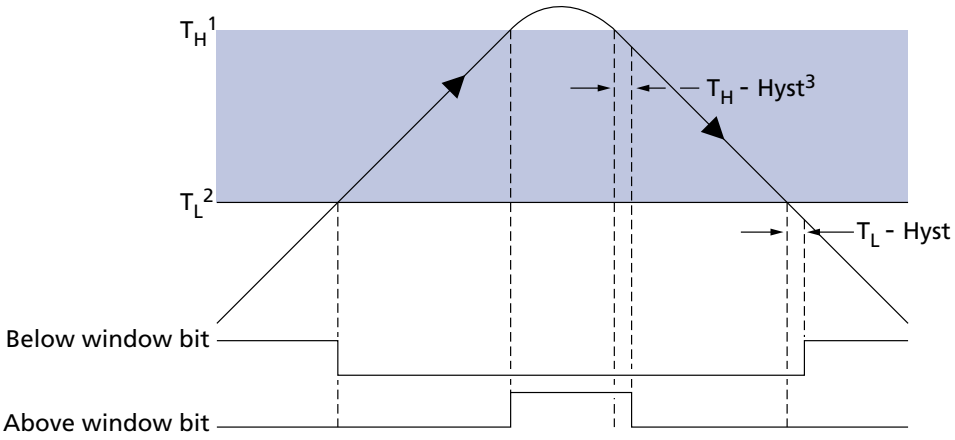
Table 22: Configuration Register Bit Descriptions

Bit	Description	Notes
0	Event mode 0: Comparator mode 1: Interrupt mode	Event mode cannot be changed if either of the lock bits is set.
1	EVENT# polarity 0: Active LOW 1: Active HIGH	EVENT# polarity cannot be changed if either of the lock bits is set.
2	Critical event only 0: EVENT# trips on alarm or critical temperature event 1: EVENT# trips only if critical temperature is reached	
3	Event output control 0: Event output disabled 1: Event output enabled	
4	Event status 0: EVENT# has not been asserted by this device 1: EVENT# is being asserted due to an alarm window or critical temperature condition	This is a read-only field in the register. The event causing the event can be determined from the read temperature register.
5	Clear event 0: No effect 1: Clears the event when the temperature sensor is in the interrupt mode	

Table 22: Configuration Register Bit Descriptions (Continued)

Bit	Description	Notes
6	Alarm window lock bit 0: Alarm trips are not locked and can be changed 1: Alarm trips are locked and cannot be changed	
7	Critical trip lock bit 0: Critical trip is not locked and can be changed 1: Critical trip is locked and cannot be changed	
8	Shutdown mode 0: Enabled 1: Shutdown	The shutdown mode is a power-saving mode that disables the temperature sensor.
10:9	Hysteresis enable 00: Disable 01: Enable at 1.5°C 10: Enable at 3°C 11: Enable at 6°C	When enabled, a hysteresis is applied to temperature movement around the trip points (see Figure 4 (page 20)). As an example, if the hysteresis register is enabled to a delta of 6°C, the preset trip points will toggle when the temperature reaches the programmed value. These values will reset when the temperature drops below the trip points minus the set hysteresis level. In this case, this would be critical temperature minus 6°C. The hysteresis is applied to both the above alarm window and the below alarm window bits found in the read-only temperature register (see Table 23 (page 20)). EVENT# is also affected by this register.

Figure 4: Hysteresis Applied to Temperature Around Trip Points



Notes:
1. T_H is the value set in the alarm temperature upper boundary trip register.
2. T_L is the value set in the alarm temperature lower boundary trip register.
3. Hyst is the value set in the hysteresis bits of the configuration register.

Table 23: Hysteresis Applied to Alarm Window Bits in the Temperature Register

Condition	Below Alarm Window Bit		Above Alarm Window Bit	
	Temperature Gradient	Critical Temperature	Temperature Gradient	Critical Temperature
Sets	Falling	T_L - Hyst	Rising	T_H
Clears	Rising	T_L	Falling	T_H - Hyst

Temperature Format

The temperature trip point registers and temperature readout register use a 2's complement format to enable negative numbers. The least significant bit (LSB) is equal to 0.0625°C or 0.25°C, depending on which register is referenced. For example, assuming an LSB of 0.0625°C:

- A value of 0x018C would equal 24.75°C
- A value of 0x06C0 would equal 108°C
- A value of 0x1E74 would equal –24.75°C

Temperature Trip Point Registers

The upper and lower temperature boundary registers are used to set the maximum and minimum values of the alarm window. LSB for these registers is 0.25°C. All RFU bits in the register will always report zero.

Table 24: Alarm Temperature Lower Boundary Register (Address: 0x02)

Bit														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Alarm window upper boundary temperature												

Table 25: Alarm Temperature Lower Boundary Register (Address: 0x03)

Bit														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Alarm window lower boundary temperature												

Critical Temperature Register

The critical temperature register is used to set the maximum temperature above the alarm window. The LSB for this register is 0.25°C. All RFU bits in the register will always report zero.

Table 26: Critical Temperature Register (Address: 0x04)

Bit														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	MSB										LSB	RFU	RFU
			Critical temperature trip point												

Temperature Register

The temperature register is a read-only register that provides the current temperature detected by the temperature sensor. The LSB for this register is 0.0625°C with a resolution of 0.0625°C. The most significant bit (MSB) is 128°C in the readout section of this register.

The upper three bits of the register are used to monitor the trip points that are set in the previous three registers.

Table 27: Temperature Register (Address: 0x05)

Bit															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Above critical trip	Above alarm window	Below alarm window	MSB												LSB
			Temperature												

Table 28: Temperature Register Bit Descriptions

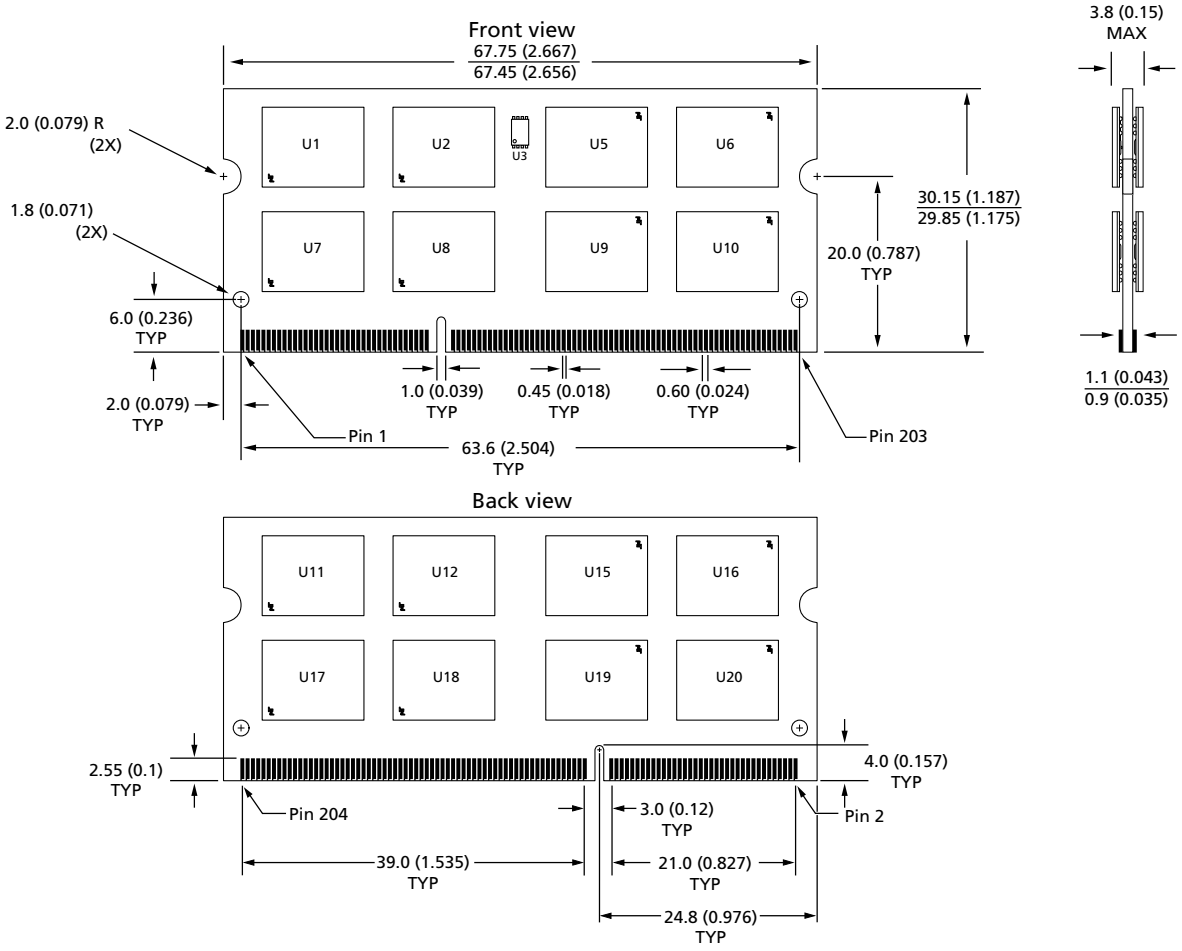
Bit	Description
13	Below alarm window 0: Temperature is equal to or above the lower boundary 1: Temperature is below alarm window
14	Above alarm window 0: Temperature is equal to or below the upper boundary 1: Temperature is above alarm window
15	Above critical trip point 0: Temperature is below critical trip point 1: Temperature is above critical trip point

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

Module Dimensions

Figure 5: 204-Pin DDR3 SODIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.