## **INTEGRATED CIRCUITS**

## DATA SHEET

# **74F367**Hex buffer/driver

Product data 2004 Jan 30 Replaces Product specification 74F365/74F367 of 2000 Jun 30





Hex buffer/driver 74F367

## **FEATURES**

- High-impedance NPN base inputs for reduced loading (20  $\mu$ A in HIGH and LOW states)
- High-speed
- Bus oriented
- 3-State buffer outputs sink 64 mA

TYPE TYPICAL PROPAGATION DELAY		TYPICAL SUPPLY CURRENT (TOTAL)
74F367	5.0 ns	36 mA

## **ORDERING INFORMATION**

COMMERCIAL RANGE:  $V_{CC}$  = 5 V  $\pm$  10%;  $T_{amb}$  = 0 °C to +70 °C

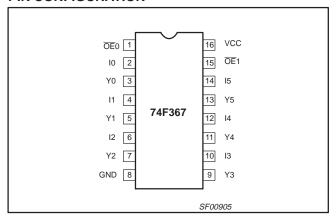
Type number	Package	Package								
	Name	Description	Version							
N74F367N	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4							
N74F367D	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1							

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH / LOW	LOAD VALUE HIGH / LOW
10 - 15	Inputs	1.0 / 0.033	20 μΑ / 20 μΑ
OE0, OE1	Output enable inputs (active-LOW)	1.0 / 0.033	20 μΑ / 20 μΑ
Y0 - Y5	Data Outputs	750 / 106.7	15 mA / 64 mA

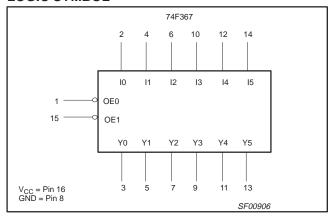
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 μA in the HIGH state and 0.6 mA in the LOW state.

## **PIN CONFIGURATION**

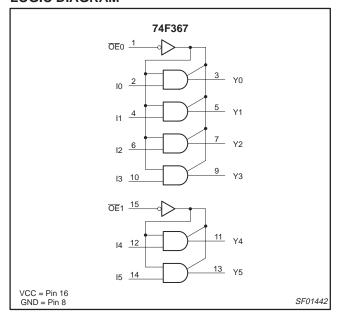


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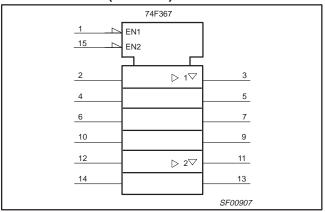
## **LOGIC SYMBOL**



## **LOGIC DIAGRAM**



## LOGIC SYMBOL (IEEE/IEC)



## **FUNCTION TABLE**

INP	OUTPUTS	
<del>OE</del> n	In	Yn
L	L	L
L	Н	Н
Н	Х	Z

H = HIGH voltage level L = LOW voltage level

X = Don't care Z = High impedance "off" state

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## **ABSOLUTE MAXIMUM RATINGS**

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage range	-0.5 to +7.0	V
I <sub>IN</sub>	Input current range	−30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in HIGH output state range	-0.5 to 5.5	V
I <sub>OUT</sub>	Current applied to output in LOW output state	128	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		UNIT		
STWIBUL	PARAMETER	MIN	TYP	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	HIGH-level input voltage	2.0	_	-	V
V <sub>IL</sub>	LOW-level input voltage	_	_	0.8	V
I <sub>IK</sub>	Input clamp current	_	_	-18	mA
I <sub>OH</sub>	HIGH-level output current	_	_	-15	mA
I <sub>OL</sub>	LOW-level output current	_	_	64	mA
T <sub>amb</sub>	Operating free-air temperature range	0	_	70	°C

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## DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

CVMDOL	DADAMETED	TEST COMPITION	vic1		UNIT		
SYMBOL	PARAMETER	TEST CONDITION	TEST CONDITIONS			MAX	
		V <sub>CC</sub> = MIN; V <sub>IL</sub> = MAX;	± 10% Vcc	2.4	_	_	V
V	HIGH-level output voltage	$V_{IH} = MIN; I_{OH} = -3 \text{ mA}$	± 5% Vcc	2.7	3.3	_	V
V <sub>OH</sub>	nigh-level output voltage	V <sub>CC</sub> = MIN; V <sub>IL</sub> = MAX;	± 10% Vcc	2.0	_	_	V
		$V_{IH} = MIN; I_{OH} = -15 \text{ mA}$	± 5% Vcc	2.0	_	-	V
V	Low lovel output voltage	V <sub>CC</sub> = MIN; V <sub>IL</sub> = MAX;	± 10% Vcc	_	_	0.55	V
V <sub>OL</sub>	Low-level output voltage	V <sub>IH</sub> = MIN; I <sub>OL</sub> = MAX	± 5% Vcc	_	0.42	0.55	V
$V_{IK}$	Input clamp voltage	$V_{CC} = MIN; I_I = I$	_	-0.73	-1.2	V	
l <sub>l</sub>	Input current at maximum input voltage	$V_{CC} = 0 \text{ V}; V_{I} = 7.0 \text{ V}$		_	_	100	μΑ
I <sub>IH</sub>	HIGH-level input current	$V_{CC} = MAX; V_I = 2$	_	_	20	μΑ	
I <sub>IL</sub>	LOW-level input current	$V_{CC} = MAX; V_I = 0.5 V$		_	_	-20	μΑ
I <sub>OZH</sub>	Off-state output current, HIGH-level voltage applied	$V_{CC} = MAX; V_O = 2.7 V$		_	-	50	μΑ
I <sub>OZL</sub>	Off-state output current, LOW-level voltage applied	$V_{CC} = MAX; V_O = 0.5 V$		_	-	-50	μΑ
los	Short-circuit output current <sup>3</sup>	$V_{CC} = MAX$		-100	_	-225	mA
	I <sub>CCH</sub>	V <sub>CC</sub> = MAX		_	25	35	mA
I <sub>CC</sub>	Supply current (total) I <sub>CCL</sub>			_	47	62	mA
	I <sub>CCZ</sub>			_	35	48	mA

## NOTES:

- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- For conditions shown as wind of what, use the appropriate value specified under recommended operating conditions for the applicable.
   All typical values are at V<sub>CC</sub> = 5 V, T<sub>amb</sub> = 25 °C.
   Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## **AC ELECTRICAL CHARACTERISTICS**

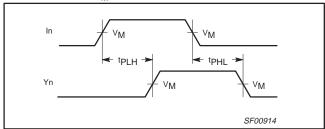
SYMBOL	PARAMETER	TEST CONDITIONS	V	<sub>mb</sub> = +25 ° <sub>CC</sub> = +5.0 0 pF; R <sub>L</sub> =	V	$V_{CC} = +5.$	C to +125 °C 0 V ± 10% R <sub>L</sub> = 500 Ω	UNIT
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>n</sub> to Y <sub>n</sub>	Waveform 1	2.5 2.5	4.5 5.5	6.5 7.0	2.0 2.0	7.0 7.5	ns ns
t <sub>PZH</sub>	Output Enable time to HIGH or LOW level	Waveform 2 Waveform 3	3.0 3.0	5.5 6.5	7.5 8.5	3.0 3.0	8.5 9.0	ns ns
t <sub>PHZ</sub>	Output Disable time from HIGH to LOW level	Waveform 2 Waveform 3	2.0 2.0	4.5 4.0	6.5 6.5	2.0 2.0	7.0 7.0	ns ns

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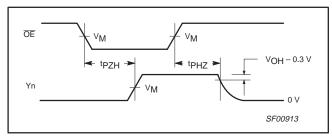
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## **AC WAVEFORMS**

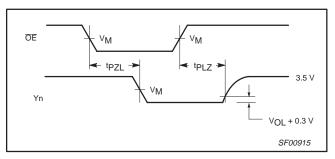
For all waveforms,  $V_M = 1.5 \text{ V}$ 



Waveform 1. For non-inverting outputs

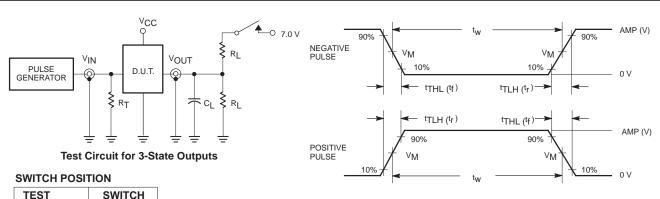


Waveform 2. 3-State Output Enable time to HIGH level and Output Disable time from HIGH level



Waveform 3. 3-State Output Enable time to LOW level and Output Disable time from LOW level

## **TEST CIRCUIT AND WAVEFORM**



TEST	SWITCH
t <sub>PLZ</sub>	closed
t <sub>PZL</sub>	closed
All other	open

## **DEFINITIONS:**

 $R_L$  = Load resistor;

see AC electrical characteristics for value.

C<sub>L</sub> = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

INPUT PULSE REQUIREMENTS										
тапппу	amplitude	V <sub>M</sub>	V <sub>M</sub> rep. rate		t <sub>TLH</sub>	t <sub>THL</sub>				
74F	3.0 V	1.5 V	1 MHz	500 ns	2.5 ns	2.5 ns				

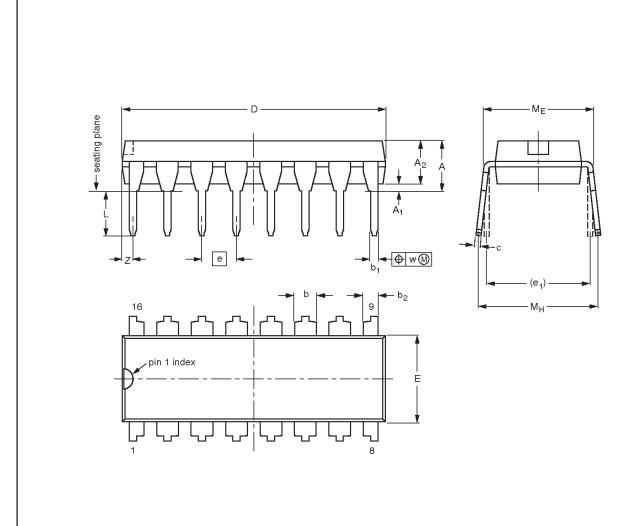
**Input Pulse Definition** 

SF00777

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## DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



0 5 10 mm scale

## DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	е	e <sub>1</sub>	L	ME	Мн	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

#### Note

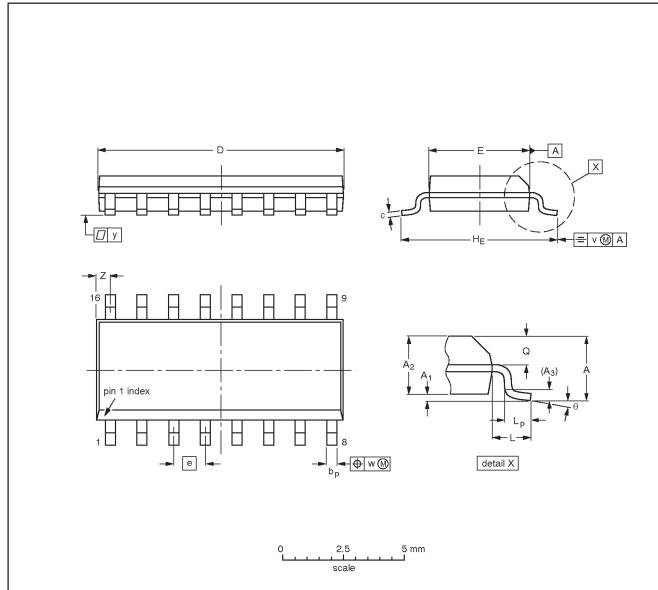
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT38-4					<del>-95-01-14-</del> 03-02-13

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## SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



## DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	У	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075		0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUEDATE	
SOT109-1	076E07	MS-012				<del>99-12-27</del> 03-02-19	

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#### **REVISION HISTORY**

Rev	Date	Description				
_4	20040130	Product data (9397 750 12742). 853-0042 ECN 01-A15335 of 21 January 2004. Replaces 74F365_74F367_3 dated 2000 Jun 30 (9397 750 07283).				
		Modifications:				
		● Delete all references to 74F365 (product discontinued).				
_3	20000630	Product specification (9397 750 07283). ECN 853-0042 24024 of 30 June 2000. Supersedes data of 1999 Jan 08.				

#### **Data sheet status**

Level	Data sheet status [1]	Product status <sup>[2] [3]</sup>	Definitions
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