

# NBSG11

## 2.5V/3.3V SiGe 1:2 Differential Clock Driver with RSECL\* Outputs

### \*Reduced Swing ECL

#### Description

The NBSG11 is a 1-to-2 differential fanout buffer, optimized for low skew and Ultra-Low JITTER.

Inputs incorporate internal 50  $\Omega$  termination resistors and accept Negative ECL (NECL), Positive ECL (PECL), CML, LVCMOS, LVTTL, or LVDS. Outputs are Reduced Swing ECL (RSECL), 400 mV. All outputs loaded with 50  $\Omega$  to  $V_{CC} - 1.5$  V for BGA package and  $V_{CC} - 2$  V for QFN package.

#### Features

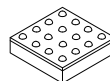
- Maximum Input Clock Frequency up to 12 GHz Typical
- Maximum Input Data Rate up to 12 Gb/s Typical
- 30 ps Typical Rise and Fall Times
- 125 ps Typical Propagation Delay
- RSPECL Output with Operating Range:  $V_{CC} = 2.375$  V to 3.465 V with  $V_{EE} = 0$  V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -2.375$  V to  $-3.465$  V
- RSECL Output Level (400 mV Peak-to-Peak Output), Differential Output Only
- 50  $\Omega$  Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices
- Pb-Free Packages are Available



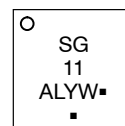
ON Semiconductor®

<http://onsemi.com>

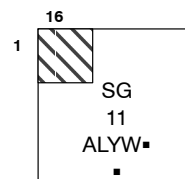
#### MARKING DIAGRAMS\*



FCBGA-16  
BA SUFFIX  
CASE 489



QFN-16  
MN SUFFIX  
CASE 485G



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb-Free Package

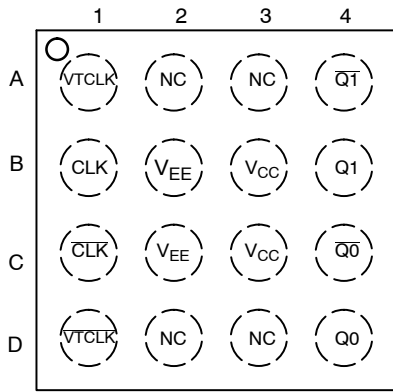
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

# NBSG11



# NBSG11

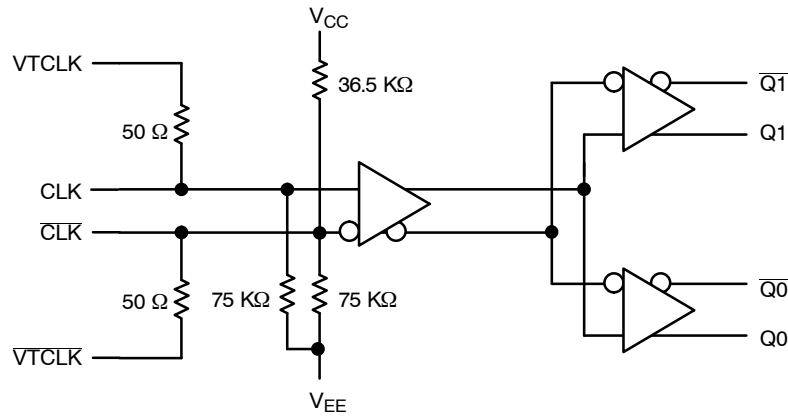


Figure 3. Logic Diagram

Table 2. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK and VTCLK to VCC
LVDS	Connect VTCLK and VTCLK together
AC-COUPLED	Bias VTCLK and VTCLK Inputs within (VIHCMR) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	An external voltage should be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTL and VCC/2 for LVCMOS inputs.

Table 3. ATTRIBUTES

Characteristics		Value	
Internal Input Pulldown Resistor (CLK, $\overline{\text{CLK}}$ )		75 k $\Omega$	
Internal Input Pullup Resistor ( $\overline{\text{CLK}}$ )		36.5 k $\Omega$	
ESD Protection	Human Body Model Machine Model	> 2 kV > 100 V	
Moisture Sensitivity (Note 4)		Pb Pkg	Pb-Free Pkg
FCBGA-16 QFN-16		Level 3 Level 1	Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
Transistor Count		125	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

4. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	Positive Power Supply	$V_{EE} = 0\text{ V}$		3.6	V
$V_{EE}$	Negative Power Supply	$V_{CC} = 0\text{ V}$		-3.6	V
$V_I$	Positive Input Negative Input	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	3.6 -3.6	V V
$V_{INPP}$	Differential Input Voltage $ D - \bar{D} $	$V_{CC} - V_{EE} \geq 2.8\text{ V}$ $V_{CC} - V_{EE} < 2.8\text{ V}$		2.8 $ V_{CC} - V_{EE} $	V V
$I_{out}$	Output Current	Continuous Surge		25 50	mA mA
$T_A$	Operating Temperature Range	FCBGA-16 QFN-16		-40 to +70 -40 to +85	°C
$T_{stg}$	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) (Note 5)	0 lfpm 500 lfpm 0 lfpm 500 lfpm	FCBGA-16 FCBGA-16 QFN-16 QFN-16	108 86 41.6 35.2	°C/W °C/W °C/W °C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	1S2P (Note 5) 2S2P (Note 6)	FCBGA-16 QFN-16	5.0 4.0	°C/W °C/W
$T_{sol}$	Wave Solder Pb Pb-Free			225 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

5. JEDEC standard multilayer board – 1S2P (1 signal, 2 power).

6. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

# NBSG11

**Table 5. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT**  $V_{CC} = 2.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 7)

Symbol	Characteristic	-40°C			25°C			70°C(BGA)/85°C(QFN)**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
$V_{OH}$	Output HIGH Voltage (Note 8)	1450	1530	1575	1525	1565	1600	1550	1590	1625	mV
$V_{OUTPP}$	Output Amplitude Voltage	350	410	525	350	410	525	350	410	525	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended) (Note 10)	$V_{CC} - 1435\text{ mV}$	$V_{CC} - 1000\text{ mV}^*$	$V_{CC}$	$V_{CC} - 1435\text{ mV}$	$V_{CC} - 1000\text{ mV}^*$	$V_{CC}$	$V_{CC} - 1435\text{ mV}$	$V_{CC} - 1000\text{ mV}^*$	$V_{CC}$	V
$V_{IL}$	Input LOW Voltage (Single-Ended) (Note 11)	$V_{IH} - 2.5\text{ V}$	$V_{CC} - 1400\text{ mV}^*$	$V_{IH} - 150\text{ mV}$	$V_{IH} - 2.5\text{ V}$	$V_{CC} - 1400\text{ mV}^*$	$V_{IH} - 150\text{ mV}$	$V_{IH} - 2.5\text{ V}$	$V_{CC} - 1400\text{ mV}^*$	$V_{IH} - 150\text{ mV}$	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9)	1.2		2.5	1.2		2.5	1.2		2.5	V
$R_{TIN}$	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	$\Omega$
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ , $V_{IHMAX}$ )		80	150		80	150		80	150	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ , $V_{ILMIN}$ )		25	100		25	100		25	100	$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

\*Typicals used for testing purposes.

\*\*The device packaged in FCBGA-16 have maximum temperature specification of 70°C and devices packaged in QFN-16 have maximum temperature specification of 85°C.

7. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.125 V to -0.965 V.

8. All loading with 50  $\Omega$  to  $V_{CC} - 1.5\text{ V}$  for BGA package and  $V_{CC} - 2.0\text{ V}$  for QFN package.  $V_{OH}/V_{OL}$  measured at  $V_{IH}/V_{IL}$ .

9.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

10.  $V_{IH}$  cannot exceed  $V_{CC}$ .

11.  $V_{IL}$  always  $\geq V_{EE}$ .

**Table 6. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 12)

Symbol	Characteristic	-40°C			25°C			70°C(BGA)/85°C(QFN)**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
$V_{OH}$	Output HIGH Voltage (Note 13)	2250	2330	2375	2325	2365	2400	2350	2390	2425	mV
$V_{OUTPP}$	Output Amplitude Voltage	350	410	525	350	410	525	350	410	525	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended) (Note 15)	$V_{CC} - 1435\text{ mV}$	$V_{CC} - 1000\text{ mV}^*$	$V_{CC}$	$V_{CC} - 1435\text{ mV}$	$V_{CC} - 1000\text{ mV}^*$	$V_{CC}$	$V_{CC} - 1435\text{ mV}$	$V_{CC} - 1000\text{ mV}^*$	$V_{CC}$	V
$V_{IL}$	Input LOW Voltage (Single-Ended) (Note 16)	$V_{IH} - 2.5\text{ V}$	$V_{CC} - 1400\text{ mV}^*$	$V_{IH} - 150\text{ mV}$	$V_{IH} - 2.5\text{ V}$	$V_{CC} - 1400\text{ mV}^*$	$V_{IH} - 150\text{ mV}$	$V_{IH} - 2.5\text{ V}$	$V_{CC} - 1400\text{ mV}^*$	$V_{IH} - 150\text{ mV}$	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Note 14) (Differential Configuration)	1.2		3.3	1.2		3.3	1.2		3.3	V
$R_{TIN}$	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	$\Omega$
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ , $V_{IHMAX}$ )		80	150		80	150		80	150	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ , $V_{ILMIN}$ )		25	100		25	100		25	100	$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

12. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925 V to -0.165 V.

13. All loading with 50  $\Omega$  to  $V_{CC} - 1.5\text{ V}$  for BGA package and  $V_{CC} - 2.0\text{ V}$  for QFN package.  $V_{OH}/V_{OL}$  measured at  $V_{IH}/V_{IL}$ .

14.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

15.  $V_{IH}$  cannot exceed  $V_{CC}$ .

16.  $V_{IL}$  always  $\geq V_{EE}$ .

\*Typicals used for testing purposes.

\*\*The device packaged in FCBGA-16 have maximum temperature specification of 70°C and devices packaged in QFN-16 have maximum temperature specification of 85°C.

**Table 7. DC CHARACTERISTICS, NECL OR RSNECL INPUT WITH NECL OUTPUT** $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$  (Note 17)

Symbol	Characteristic	-40°C			25°C			70°C(BGA)/85°C(QFN)**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
$V_{OH}$	Output HIGH Voltage (Note 18)	-1050	-970	-925	-975	-935	-900	-950	-910	-875	mV
$V_{OUTPP}$	Output Amplitude Voltage	350	410	525	350	410	525	350	410	525	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended) (Note 20)	$V_{CC}-1435\text{ mV}$	$V_{CC}-1000\text{ mV}^*$	$V_{CC}$	$V_{CC}-1435\text{ mV}$	$V_{CC}-1000\text{ mV}^*$	$V_{CC}$	$V_{CC}-1435\text{ mV}$	$V_{CC}-1000\text{ mV}^*$	$V_{CC}$	V
$V_{IL}$	Input LOW Voltage (Single-Ended) (Note 21)	$V_{IH}-2.5\text{ V}$	$V_{CC}-1400\text{ mV}^*$	$V_{IH}-150\text{ mV}$	$V_{IH}-2.5\text{ V}$	$V_{CC}-1400\text{ mV}^*$	$V_{IH}-150\text{ mV}$	$V_{IH}-2.5\text{ V}$	$V_{CC}-1400\text{ mV}^*$	$V_{IH}-150\text{ mV}$	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 19)	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	V
$R_{TIN}$	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	$\Omega$
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ , $V_{IHMAX}$ )		80	150		80	150		80	150	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ , $V_{ILMIN}$ )		25	100		25	100		25	100	$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

17. Input and output parameters vary 1:1 with  $V_{CC}$ .

18. All loading with  $50\ \Omega$  to  $V_{CC} - 1.5\text{ V}$  for BGA package and  $V_{CC} - 2.0\text{ V}$  for QFN package.  $V_{OH}/V_{OL}$  measured at  $V_{IH}/V_{IL}$ .

19.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

20.  $V_{IH}$  cannot exceed  $V_{CC}$ .

21.  $V_{IL}$  always  $\geq V_{EE}$ .

\*Typicals used for testing purposes.

\*\*The device packaged in FCBGA-16 have maximum temperature specification of 70°C and devices packaged in QFN-16 have maximum temperature specification of 85°C.

**Table 8. AC CHARACTERISTICS for FCBGA-16**
 $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$  or  $V_{CC} = 2.375\text{ V}$  to  $3.465\text{ V}$ ;  $V_{EE} = 0\text{ V}$ 

Symbol	Characteristic	-40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Frequency (See Figure 4. $F_{\max}/\text{JITTER}$ ) (Note 22)	10.709	12		10.709	12		10.709	12		GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential	90	125	160	90	125	160	90	125	160	ps
$t_{SKEW}$	Duty Cycle Skew (Note 23) Within-Device Skew (Note 24) Device-to-Device Skew (Note 25)		3 6 25	15 15 50		3 6 25	15 15 50		3 6 25	15 15 50	ps
$t_{JITTER}$	RMS Random Clock Jitter $f_{in} < 10\text{ GHz}$ Peak-to-Peak Data Dependent Jitter $f_{in} < 10\text{ Gb/s}$		0.2 10	1		0.2 10	1		0.2 10	1	ps
$V_{INPP}$	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 26)	75		2600	75		2600	75		2600	mV
$t_r$ $t_f$	Output Rise/Fall Times (20% – 80%) @ 1 GHz	20	30	55	20	30	55	20	30	55	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

22. Measured using a 500 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 1.5\text{ V}$  for BGA package. For minimum  $f_{\max}$  value of 10.709 GHz, output amplitude is approximately 200 mV (as shown in Figure 4, where output P-P spec is shown as a minimum/guarantee of around 150 mV). Input edge rates 40 ps (20% – 80%).

23. See Figure 5.  $t_{SKEW} = |t_{PLH} - t_{PHL}|$  for a nominal 50% Differential Clock Input Waveform.

24. Within-Device skew is defined as identical transitions on similar paths through a device.

25. Device-to-device skew for identical transitions at identical  $V_{CC}$  levels.

26.  $V_{INPP}$  (MAX) cannot exceed  $V_{CC} - V_{EE}$ .



**Table 9. AC CHARACTERISTICS for QFN-16**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$  or  $V_{CC} = 2.375\text{ V}$  to  $3.465\text{ V}$ ;  $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Frequency (See Figure 4. $F_{\max}/\text{JITTER}$ ) (Note 27)	10.5	12		10.5	12		10.5	12		GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential	90	125	160	90	125	160	90	125	160	ps
$t_{SKEW}$	Duty Cycle Skew (Note 28) Within-Device Skew (Note 29) Device-to-Device Skew (Note 30)		3 6 25	15 15 50		3 6 25	15 15 50		3 6 25	15 15 50	ps
$t_{JITTER}$	RMS Random Clock Jitter $f_{in} < 10\text{ GHz}$ Peak-to-Peak Data Dependent Jitter $f_{in} < 10\text{ Gb/s}$		0.2 10.7	1		0.2 10.7	1		0.2 10.7	1	ps
$V_{INPP}$	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 31)	75		2600	75		2600	75		2600	mV
$t_r$ $t_f$	Output Rise/Fall Times (20% – 80%) @ 1 GHz	15	30	55	20	30	55	20	30	55	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

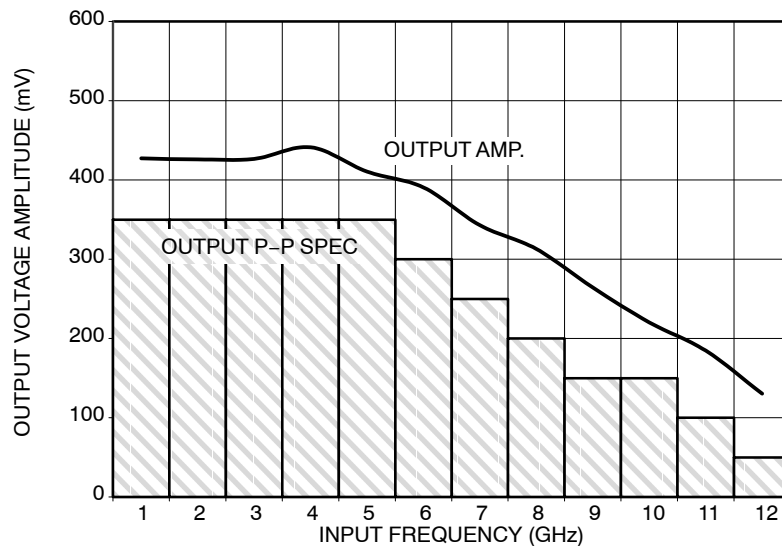
27. Measured using a 500 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$  for QFN package. For minimum  $f_{\max}$  value of 10.5 GHz, output amplitude is approximately 200 mV (as shown in Figure 4, where output P-P spec is shown as a minimum/guarantee of around 150 mV). Input edge rates 40 ps (20% – 80%).

28. See Figure 5.  $t_{SKEW} = |t_{PLH} - t_{PHL}|$  for a nominal 50% Differential Clock Input Waveform.

29. Within-Device skew is defined as identical transitions on similar paths through a device.

30. Device-to-device skew for identical transitions at identical  $V_{CC}$  levels.

31.  $V_{INPP}$  (MAX) cannot exceed  $V_{CC} - V_{EE}$ .



**Figure 4. Output Amplitude ( $V_{OUTPP}$ ) vs. Input Frequency ( $F_{IN}$ ) at Ambient Temperature (Typical)**

## NBSG11

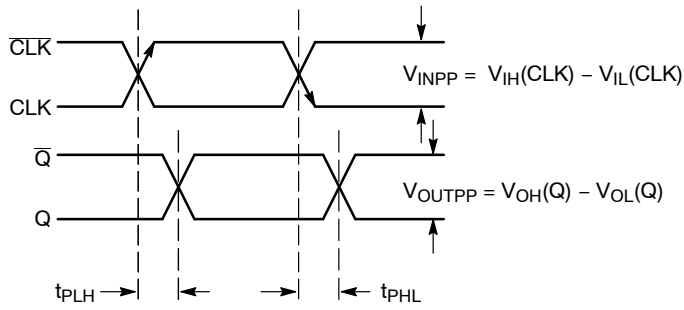


Figure 5. AC Reference Measurement

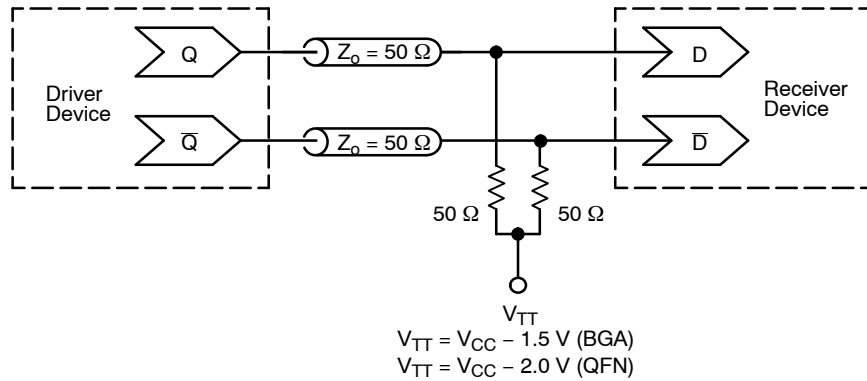


Figure 6. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NBSG11BAHTBG	FCBGA-16 (Pb-Free)	100 / Tape & Reel
NBSG11BAR2	FCBGA-16	100 / Tape & Reel (Contact Sales Representative)
NBSG11MN	QFN-16	123 Units / Rail
NBSG11MNG	QFN-16 (Pb-Free)	123 Units / Rail
NBSG11MNR2	QFN-16	3000 / Tape & Reel
NBSG11MNR2G	QFN-16 (Pb-Free)	3000 / Tape & Reel
NBSG11MNHTBG	QFN-16 (Pb-Free)	100 / Tape & Reel

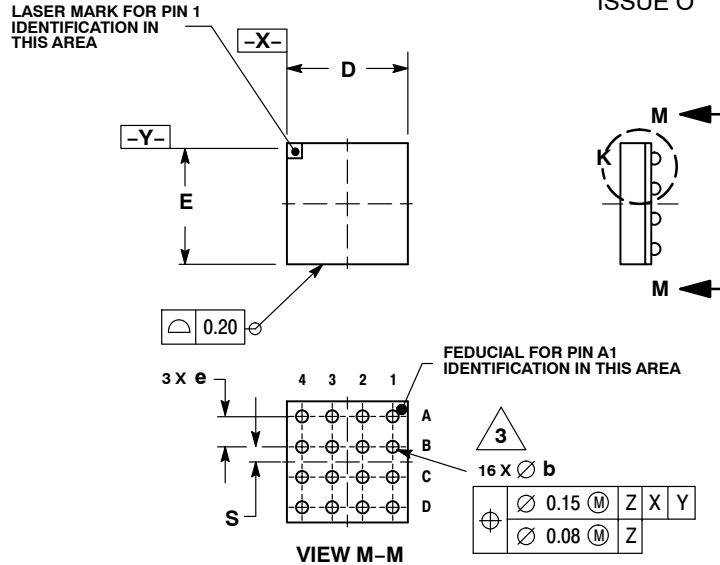
Board	Description
NBSG11BAEVB	NBSG11BA Evaluation Board

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NBSG11

## PACKAGE DIMENSIONS

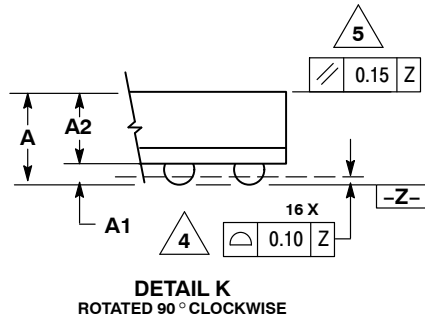
**FCBGA-16**  
**BA SUFFIX**  
 PLASTIC 4X4 (mm) BGA FLIP CHIP PACKAGE  
 CASE 489-01  
 ISSUE O



### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

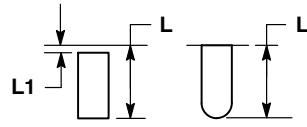
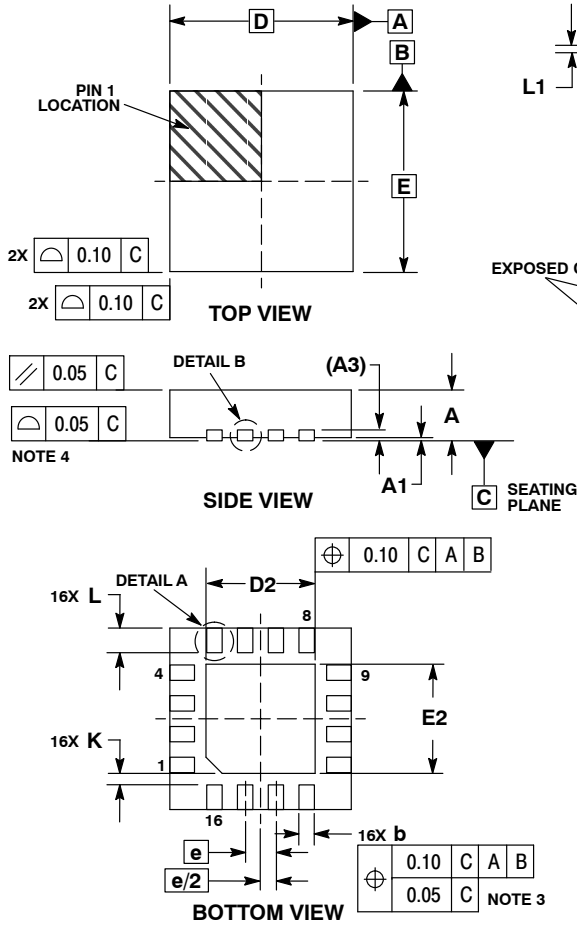
DIM	MILLIMETERS	
	MIN	MAX
A	1.40	MAX
A1	0.25	0.35
A2	1.20	REF
b	0.30	0.50
D	4.00	BSC
E	4.00	BSC
e	1.00	BSC
S	0.50	BSC



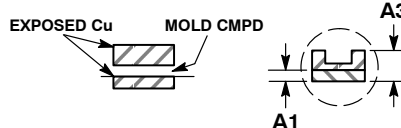
# NBSG11

## PACKAGE DIMENSIONS

QFN16 3x3, 0.5P  
CASE 485G-01  
ISSUE E



DETAIL A  
ALTERNATE TERMINAL  
CONSTRUCTIONS

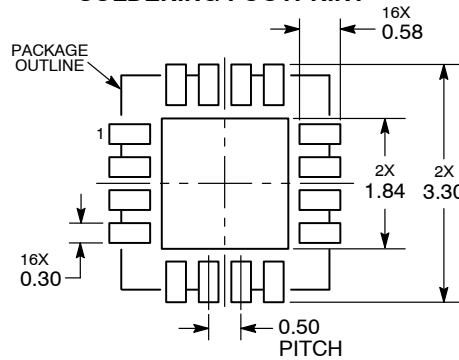


DETAIL B  
ALTERNATE  
CONSTRUCTIONS

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
  4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.


MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.18	0.30
D	3.00	BSC
D2	1.65	1.85
E	3.00	BSC
E2	1.65	1.85
e	0.50	BSC
K	0.18	TYP
L	0.30	0.50
L1	0.00	0.15

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[NBSG11BA](#) [NBSG11BAR2](#) [NBSG11MN](#) [NBSG11MNG](#) [NBSG11MNR2](#)