



# NX3008PBKMB

30 V, single P-channel Trench MOSFET

Rev. 1 — 11 May 2012

Product data sheet

## 1. Product profile

### 1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Very fast switching
- Low threshold voltage
- Trench MOSFET technology
- ESD protection up to 2 kV
- Ultra thin package profile with 0.37 mm height

### 1.3 Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

### 1.4 Quick reference data

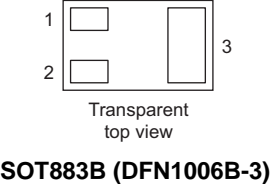
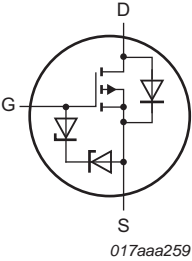
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-30	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	<a href="#">[1]</a> -	-	-300	mA
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -200\text{ mA}; T_j = 25\text{ °C}$	-	2.8	4.1	$\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	D	drain		

3. Ordering information

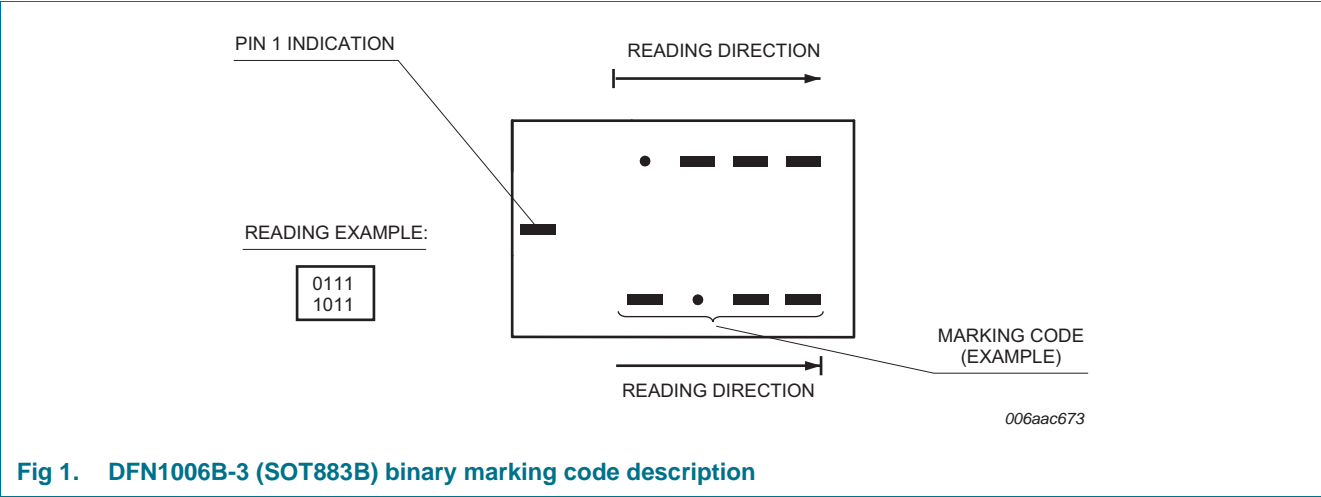
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX3008PBKMB	DFN1006B-3	Leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.37 mm	SOT883B

4. Marking

Table 4. Marking codes

Type number	Marking code
NX3008PBKMB	0000 0100



## 5. Limiting values

**Table 5. Limiting values**

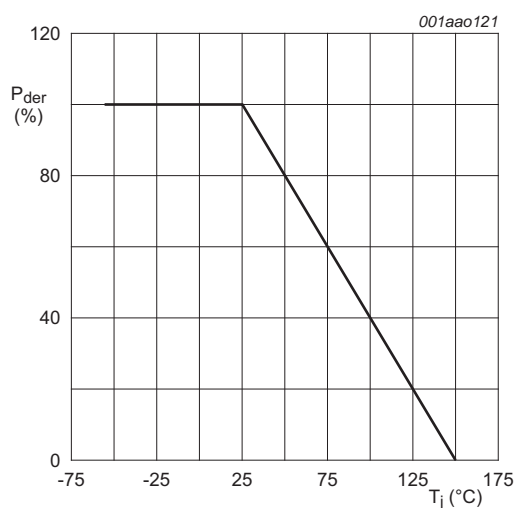
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$	-	-30	V
$V_{GS}$	gate-source voltage		-8	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-300	mA
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-185	mA
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	-1.2	A
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	360	mW
			[1]	715	mW
		$T_{sp} = 25\text{ }^{\circ}\text{C}$	-	2700	mW
$T_j$	junction temperature		-55	150	$^{\circ}\text{C}$
$T_{amb}$	ambient temperature		-55	150	$^{\circ}\text{C}$
$T_{stg}$	storage temperature		-65	150	$^{\circ}\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-300	mA
<b>ESD maximum rating</b>					
$V_{ESD}$	electrostatic discharge voltage	HBM	[3]	2000	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

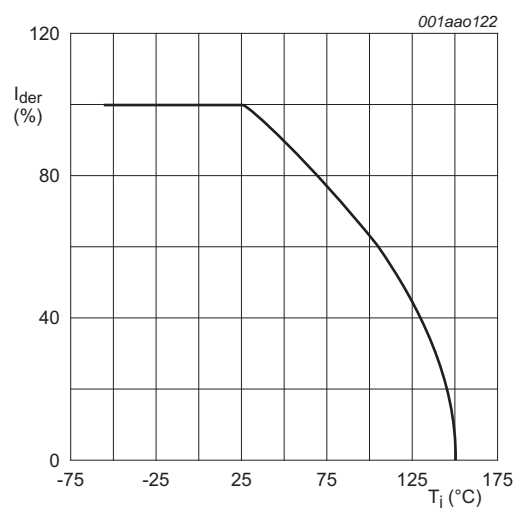
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



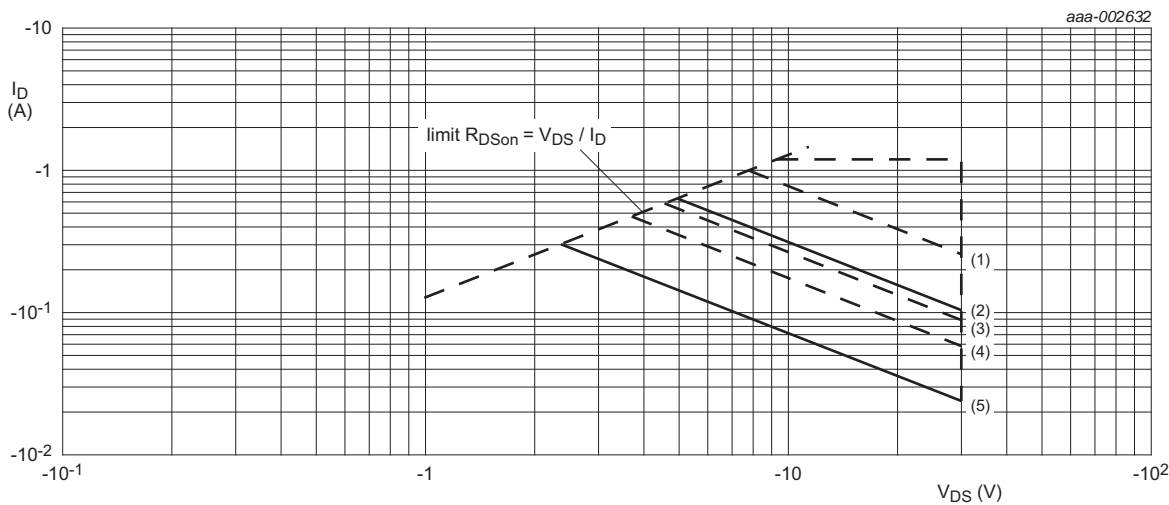
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of junction temperature**



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

**Fig 3. Normalized continuous drain current as a function of junction temperature**



$I_{DM}$  is single pulse

(1)  $t_p = 1$  ms

(2) DC;  $T_{sp} = 25$  °C

(3)  $t_p = 10$  ms

(4)  $t_p = 100$  ms

(5) DC;  $T_{amb} = 25$  °C; drain mounting pad  $1\text{ cm}^2$

Fig 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	305	360 K/W
			[2]	-	150	175 K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	40	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $1\text{ cm}^2$ .

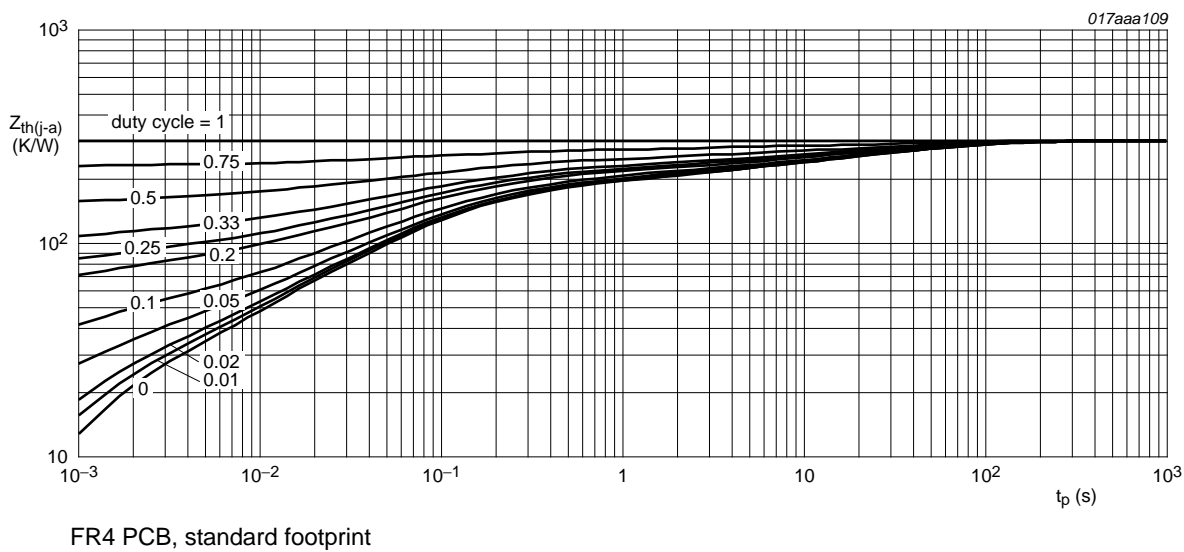


Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

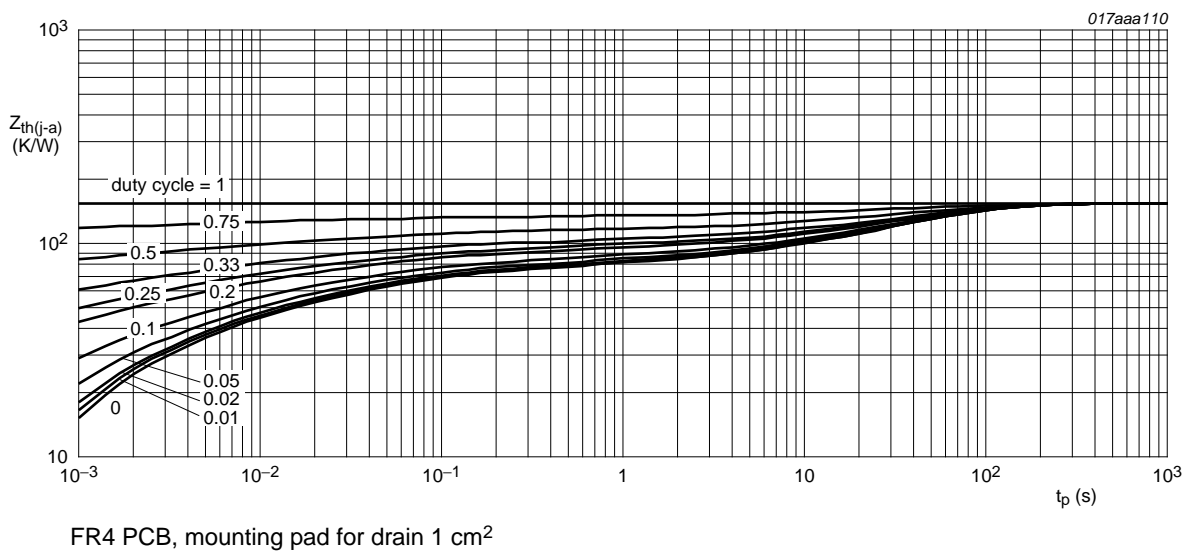
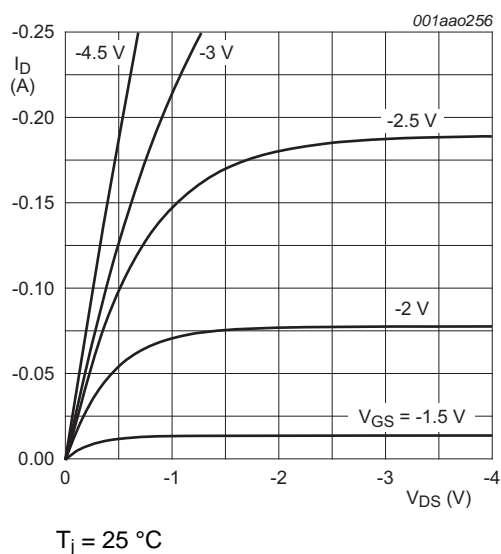


Fig 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

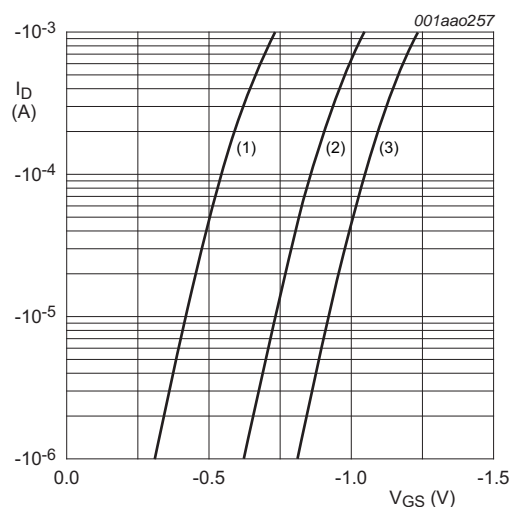
## 7. Characteristics

Table 7. Characteristics

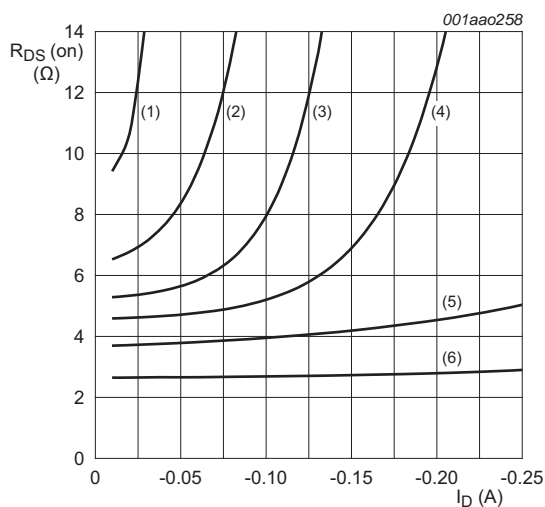
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = -250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-30	-	-	V
V <sub>GSth</sub>	gate-source threshold voltage	I <sub>D</sub> = -250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C	-0.6	-0.9	-1.1	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = -30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 150 °C	-	-	-10	μA
		V <sub>DS</sub> = -30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	-1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-0.2	-1	μA
		V <sub>GS</sub> = -8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-0.2	-1	μA
		V <sub>GS</sub> = 4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-10	-	nA
		V <sub>GS</sub> = -4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-10	-	nA
		V <sub>GS</sub> = 2.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-1	-	nA
		V <sub>GS</sub> = -2.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-1	-	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = -4.5 V; I <sub>D</sub> = -200 mA; T <sub>j</sub> = 25 °C	-	2.8	4.1	Ω
		V <sub>GS</sub> = -4.5 V; I <sub>D</sub> = -200 mA; T <sub>j</sub> = 150 °C	-	5.3	7.8	Ω
		V <sub>GS</sub> = -2.5 V; I <sub>D</sub> = -10 mA; T <sub>j</sub> = 25 °C	-	5.3	6.5	Ω
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = -10 V; I <sub>D</sub> = -200 mA; T <sub>j</sub> = 25 °C	-	160	-	mS
Dynamic characteristics						
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = -15 V; I <sub>D</sub> = -200 mA;	-	0.55	0.72	nC
Q <sub>GS</sub>	gate-source charge	V <sub>GS</sub> = -4.5 V; T <sub>j</sub> = 25 °C	-	0.23	-	nC
Q <sub>GD</sub>	gate-drain charge		-	0.09	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = -15 V; f = 1 MHz; V <sub>GS</sub> = 0 V;	-	31	46	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C	-	6.5	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	2.3	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = -20 V; R <sub>L</sub> = 250 Ω; V <sub>GS</sub> = -4.5 V;	-	19	38	ns
t <sub>r</sub>	rise time	R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C	-	30	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	65	130	ns
t <sub>f</sub>	fall time		-	38	-	ns
Source-drain diode						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = -200 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-0.47	-0.88	-1.2	V



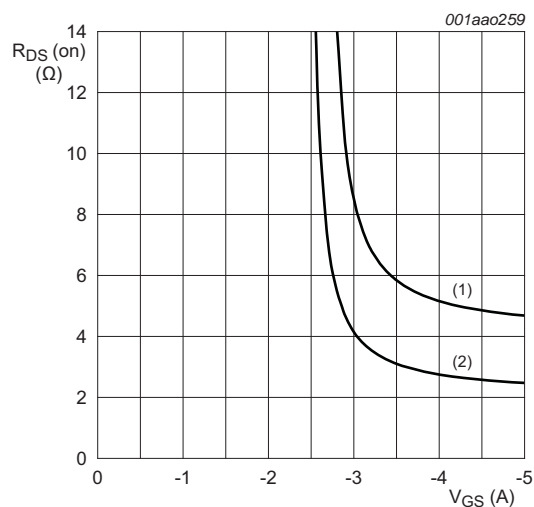
**Fig 7. Output characteristics: drain current as a function of drain-source voltage; typical values**



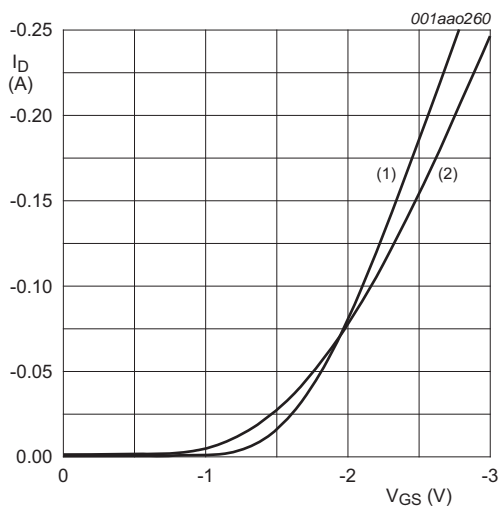
**Fig 8. Subthreshold drain current as a function of gate-source voltage**



**Fig 9. Drain-source on-state resistance as a function of drain current; typical values**

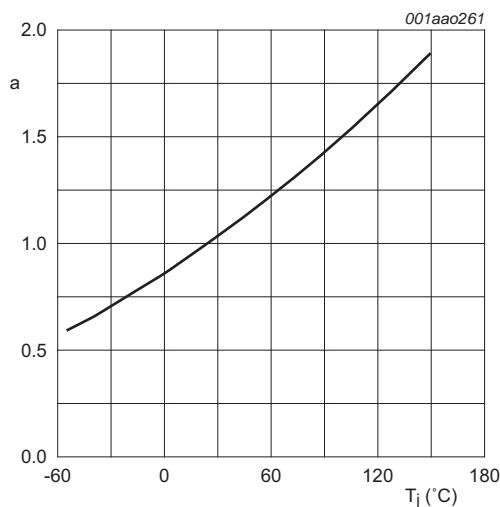


**Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values**



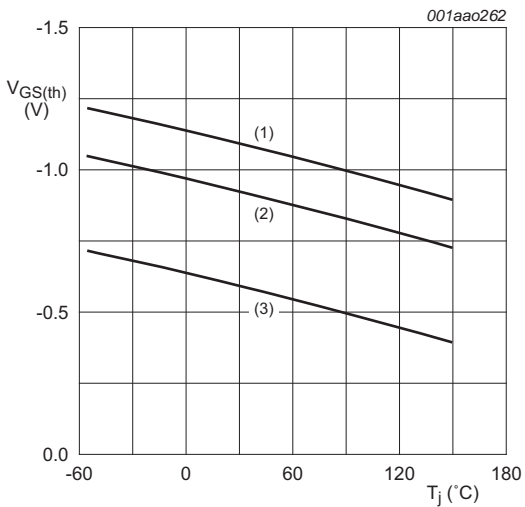
$V_{DS} > I_D \times R_{DS(on)}$   
(1)  $T_j = 25\text{ }^{\circ}\text{C}$   
(2)  $T_j = 150\text{ }^{\circ}\text{C}$

Fig 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values



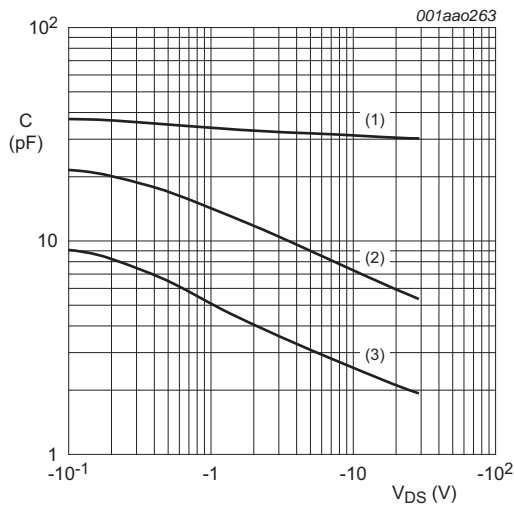
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^{\circ}\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values



$I_D = -0.25\text{ mA}$ ;  $V_{DS} = V_{GS}$   
(1) maximum values  
(2) typical values  
(3) minimum values

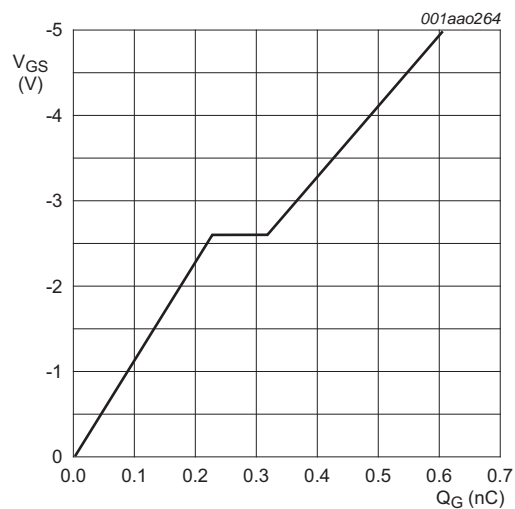
Fig 13. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}$ ;  $V_{GS} = 0\text{ V}$   
(1)  $C_{iss}$   
(2)  $C_{oss}$   
(3)  $C_{rss}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





$I_D = -200$  mA;  $V_{DS} = -15$  V;  $T_{amb} = 25$  °C

Fig 15. Gate-source voltage as a function of gate charge; typical values

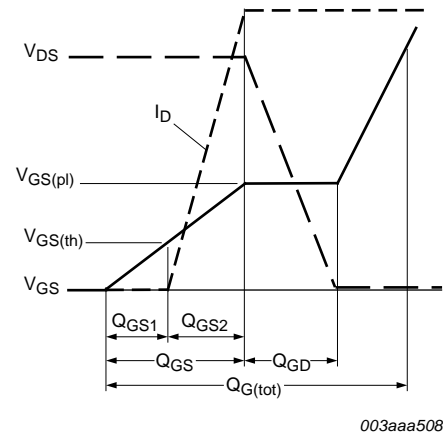
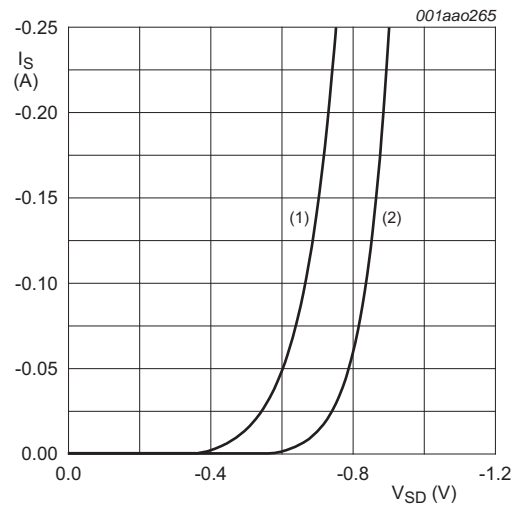


Fig 16. Gate charge waveform definitions



$V_{GS} = 0$  V  
(1)  $T_j = 150$  °C  
(2)  $T_j = 25$  °C

Fig 17. Source current as a function of source-drain voltage; typical values

8. Test information

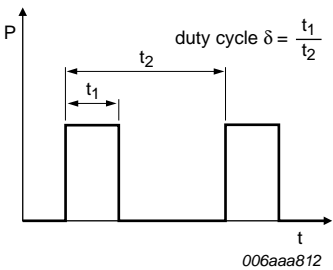


Fig 18. Duty cycle definition

9. Package outline

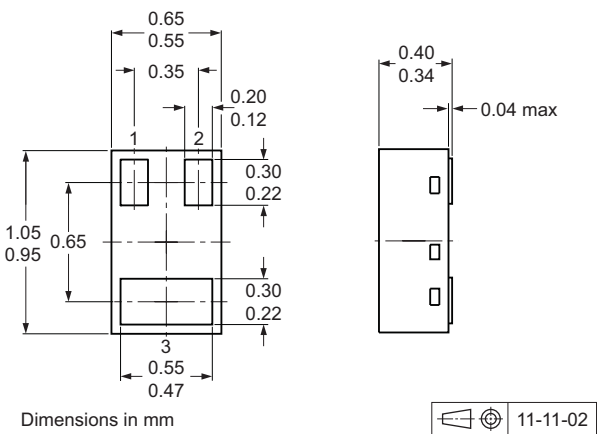


Fig 19. Package outline SOT883B (DFN1006B-3)



## 11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3008PBKMB v.1	20120511	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1] [2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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