

NXL0840

SCR logic level

Rev. 01 — 26 February 2008

Product data sheet

1. Product profile

1.1 General description

Passivated sensitive gate Silicon-Controlled Rectifier (SCR) in a SOT54 plastic package

1.2 Features

- Direct interfacing to logic level ICs
- Direct interfacing to low-power gate drive circuits
- For operation on DC and rectified AC supplies

1.3 Applications

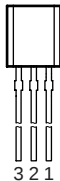
- Christmas lights control
- Protection and safety shutdown circuits e.g. lighting ballasts

1.4 Quick reference data

- $V_{\text{DRM}} \leq 400 \text{ V}$
- $I_{\text{T(RMS)}} \leq 0.8 \text{ A}$
- $I_{\text{TSM}} \leq 8 \text{ A (t = 10 ms)}$
- $I_{\text{T(AV)}} \leq 0.5 \text{ A}$

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	anode (A)		
2	gate (G)		
3	cathode (K)		
		SOT54 (TO-92)	

3. Ordering information

Table 2. Ordering information

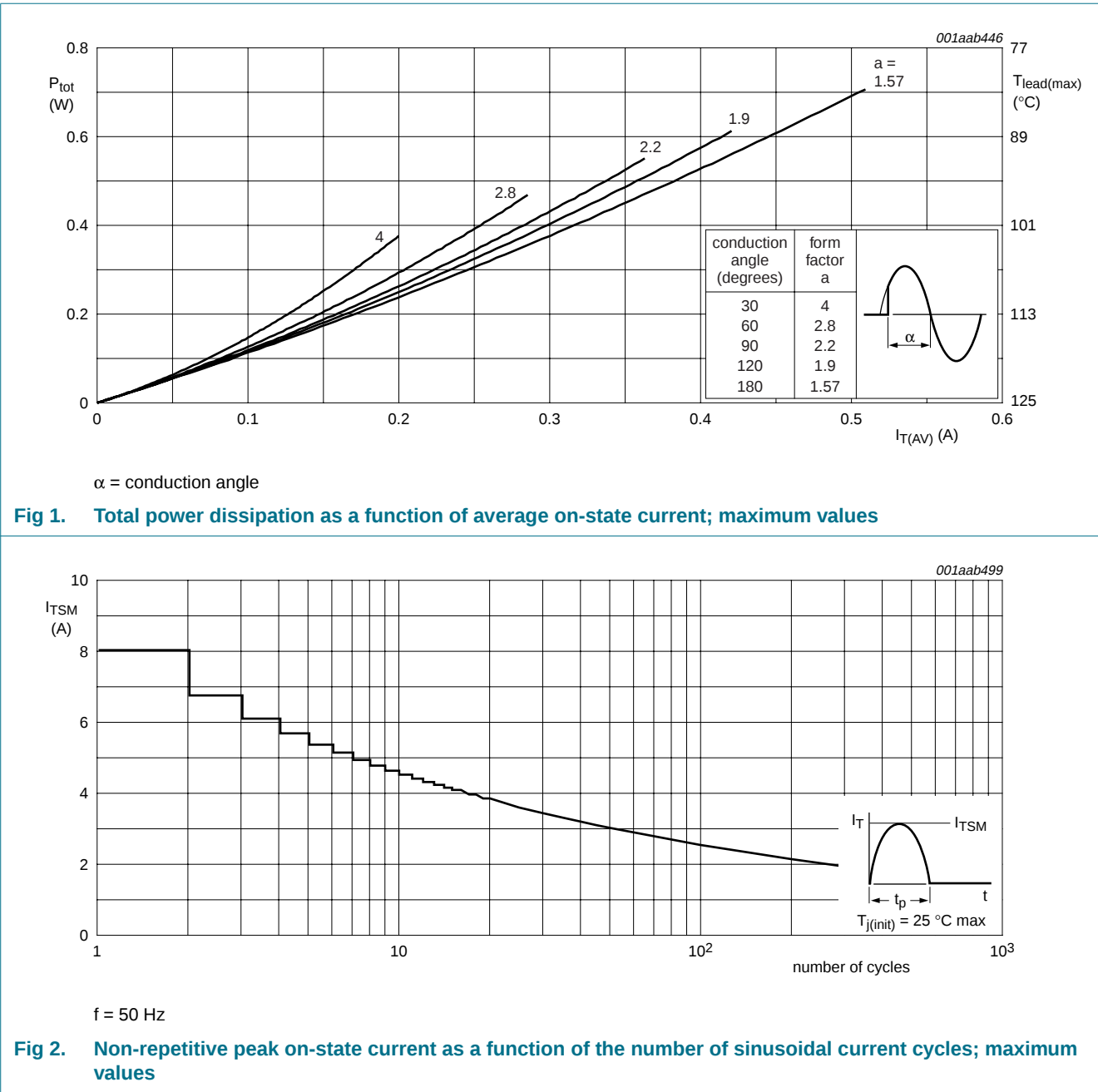
Type number	Package		Version
	Name	Description	
NXL0840	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	400	V
$I_{\text{T(AV)}}$	average on-state current	half sine wave; $T_{\text{lead}} \leq 83\text{ }^{\circ}\text{C}$; see Figure 1	-	0.5	A
$I_{\text{T(RMS)}}$	RMS on-state current	all conduction angles; see Figure 4 and 5	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ }^{\circ}\text{C}$ prior to surge; see Figure 2 and 3			
		$t = 10\text{ ms}$	-	8	A
		$t = 8.3\text{ ms}$	-	9	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$	-	0.32	A^2s
dI_{T}/dt	rate of rise of on-state current	$I_{\text{TM}} = 2\text{ A}$; $I_{\text{G}} = 10\text{ mA}$; $dI_{\text{G}}/dt = 100\text{ mA}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	1	A
V_{GM}	peak gate voltage		-	5	V
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	2	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	+150	$^{\circ}\text{C}$
T_j	junction temperature		-	125	$^{\circ}\text{C}$



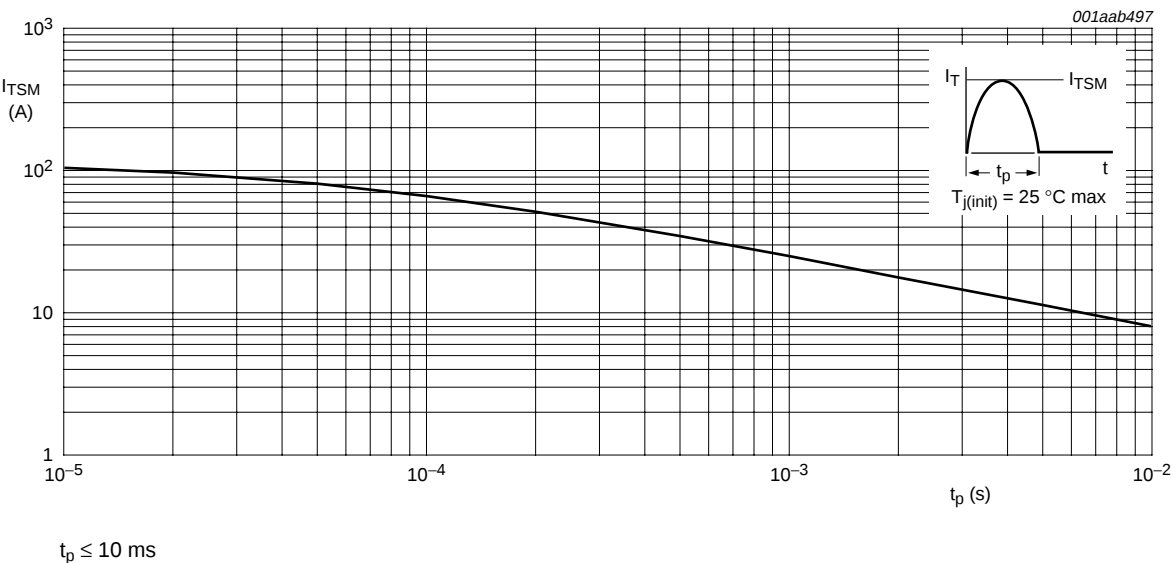


Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values

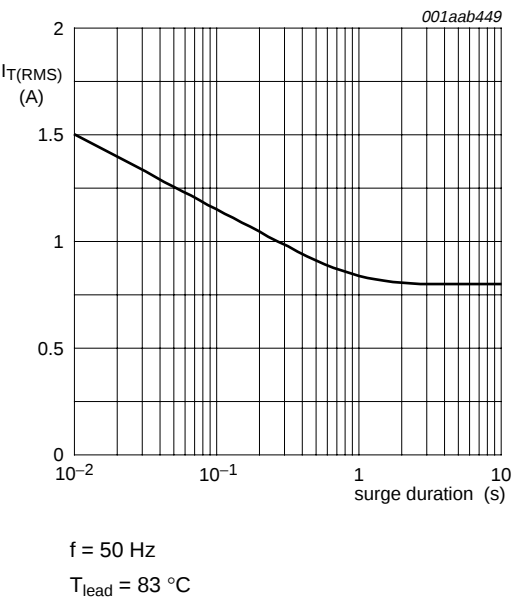


Fig 4. RMS on-state current as a function of surge duration; maximum values

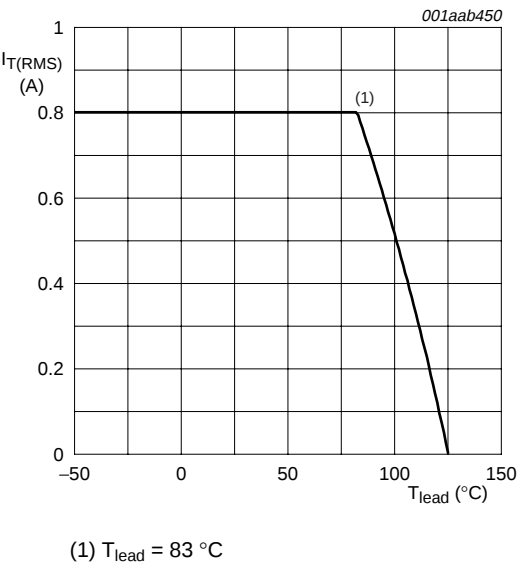


Fig 5. RMS on-state current as a function of lead temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	see Figure 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board mounted; lead length 4 mm	-	150	-	K/W

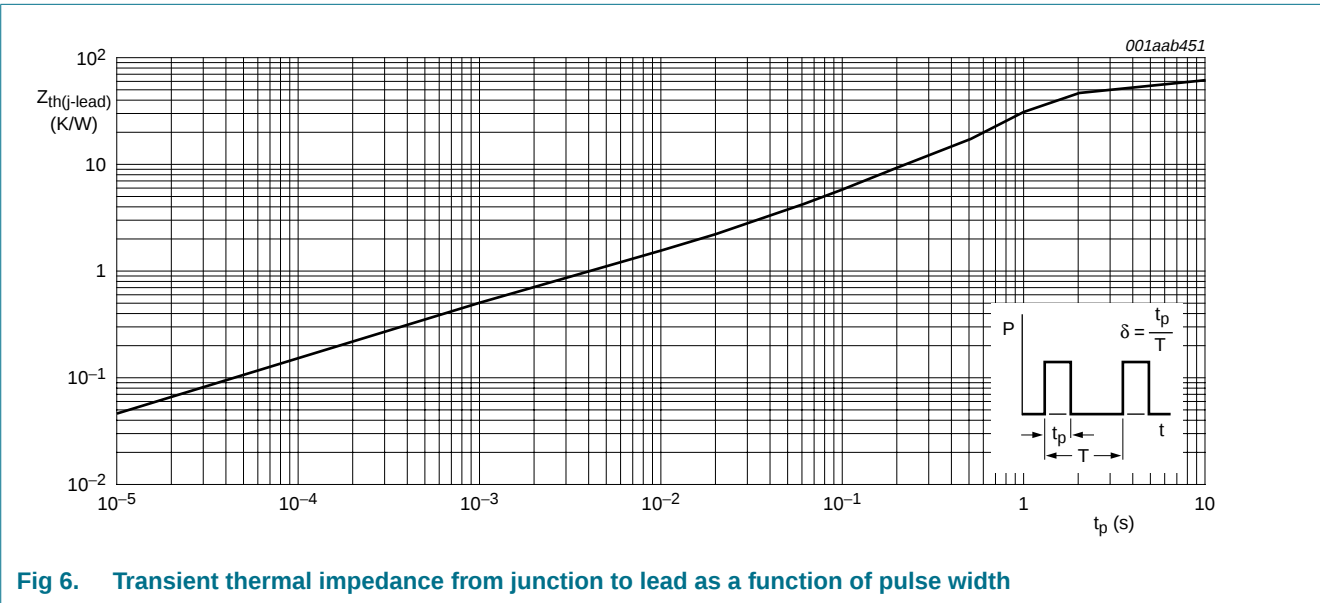
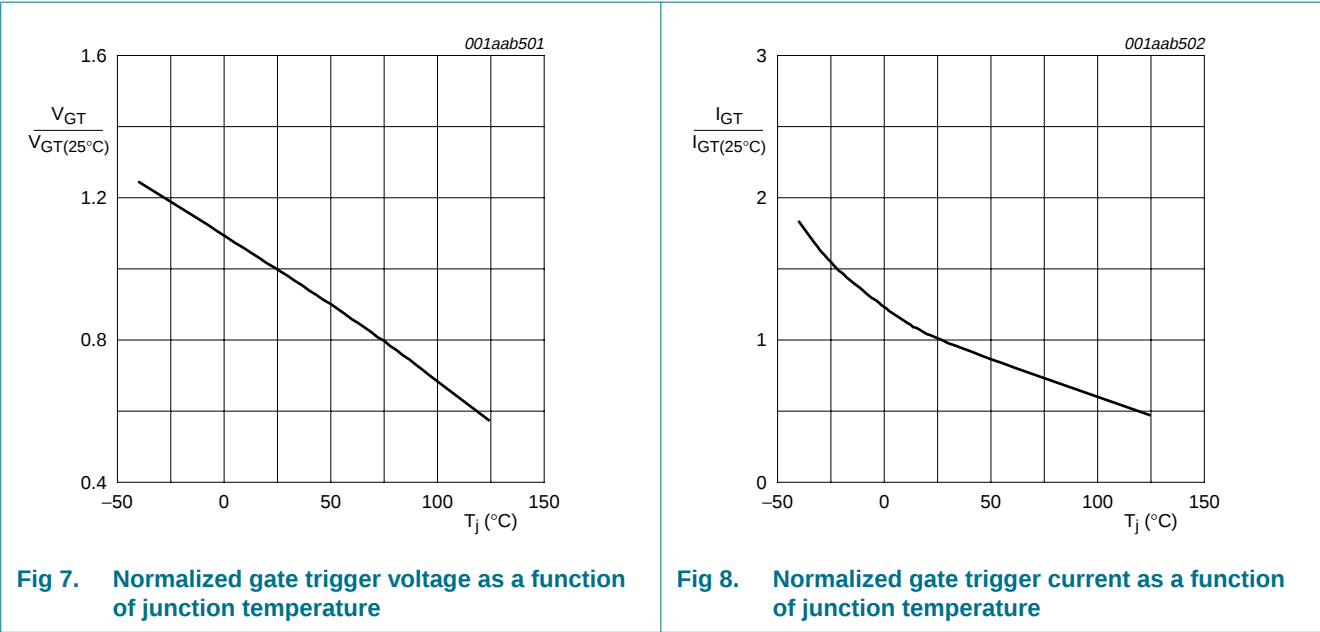


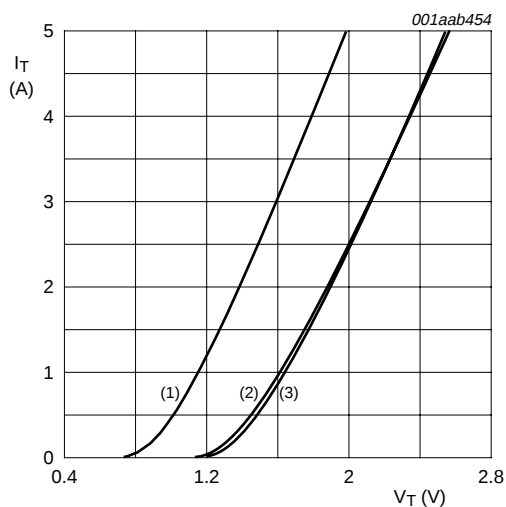
Fig 6. Transient thermal impedance from junction to lead as a function of pulse width

6. Characteristics

Table 5. Characteristics
T_j = 25 °C unless otherwise specified.

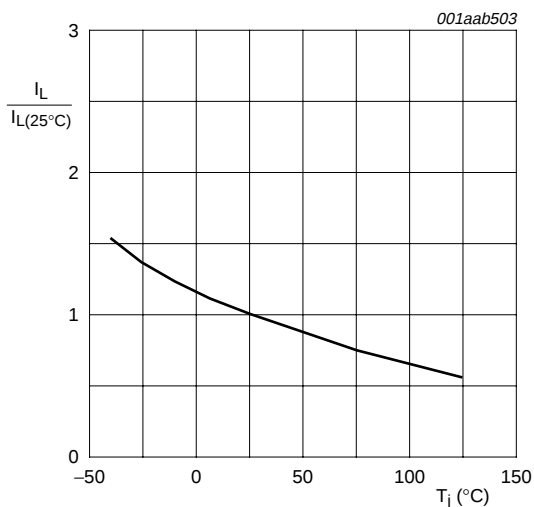
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 10 mA; see Figure 8	-	50	200	μA
I _L	latching current	V _D = 12 V; I _G = 0.5 mA; R _{GK} = 1 kΩ; see Figure 10	-	2	6	mA
I _H	holding current	V _D = 12 V; I _G = 0.5 mA; R _{GK} = 1 kΩ; see Figure 11	-	2	5	mA
V _T	on-state voltage	I _T = 1.2 A; see Figure 9	-	1.25	1.7	V
V _{GT}	gate trigger voltage	I _T = 10 mA; see Figure 7				
		V _D = 12 V	-	0.5	0.8	V
		V _D = V _{DRM(max)} ; T _j = 125 °C	0.2	0.3	-	V
I _D	off-state current	V _D = V _{DRM(max)} ; T _j = 125 °C; R _{GK} = 1 kΩ	-	0.05	0.1	mA
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 0.67 × V _{DRM(max)} ; T _j = 125 °C; exponential waveform; see Figure 12				
		R _{GK} = 1 kΩ	200	600	-	V/μs
		gate open circuit	-	25		V/μs





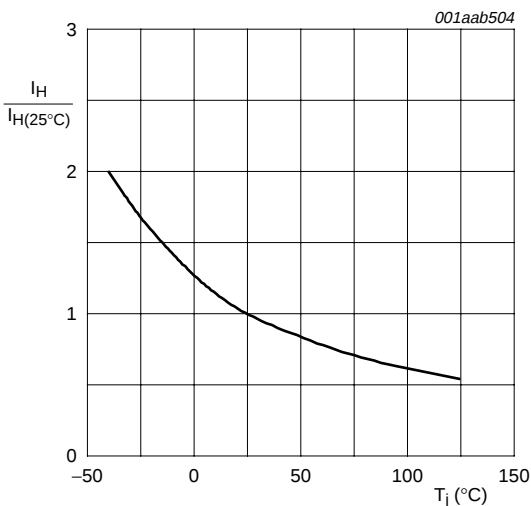
$V_o = 1.067\text{ V}$
 $R_s = 0.187\text{ }\Omega$
 (1) $T_j = 125\text{ }^\circ\text{C}$; typical values
 (2) $T_j = 125\text{ }^\circ\text{C}$; maximum values
 (3) $T_j = 25\text{ }^\circ\text{C}$; maximum values

Fig 9. On-state current as a function of on-state voltage



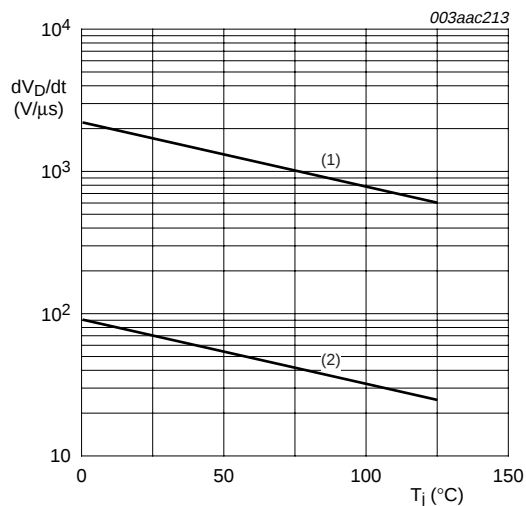
$R_{GK} = 1\text{ k}\Omega$

Fig 10. Normalized latching current as a function of junction temperature



$R_{GK} = 1\text{ k}\Omega$

Fig 11. Normalized holding current as a function of junction temperature



(1) $R_{GK} = 1\text{ k}\Omega$
 (2) Gate open-circuit

Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

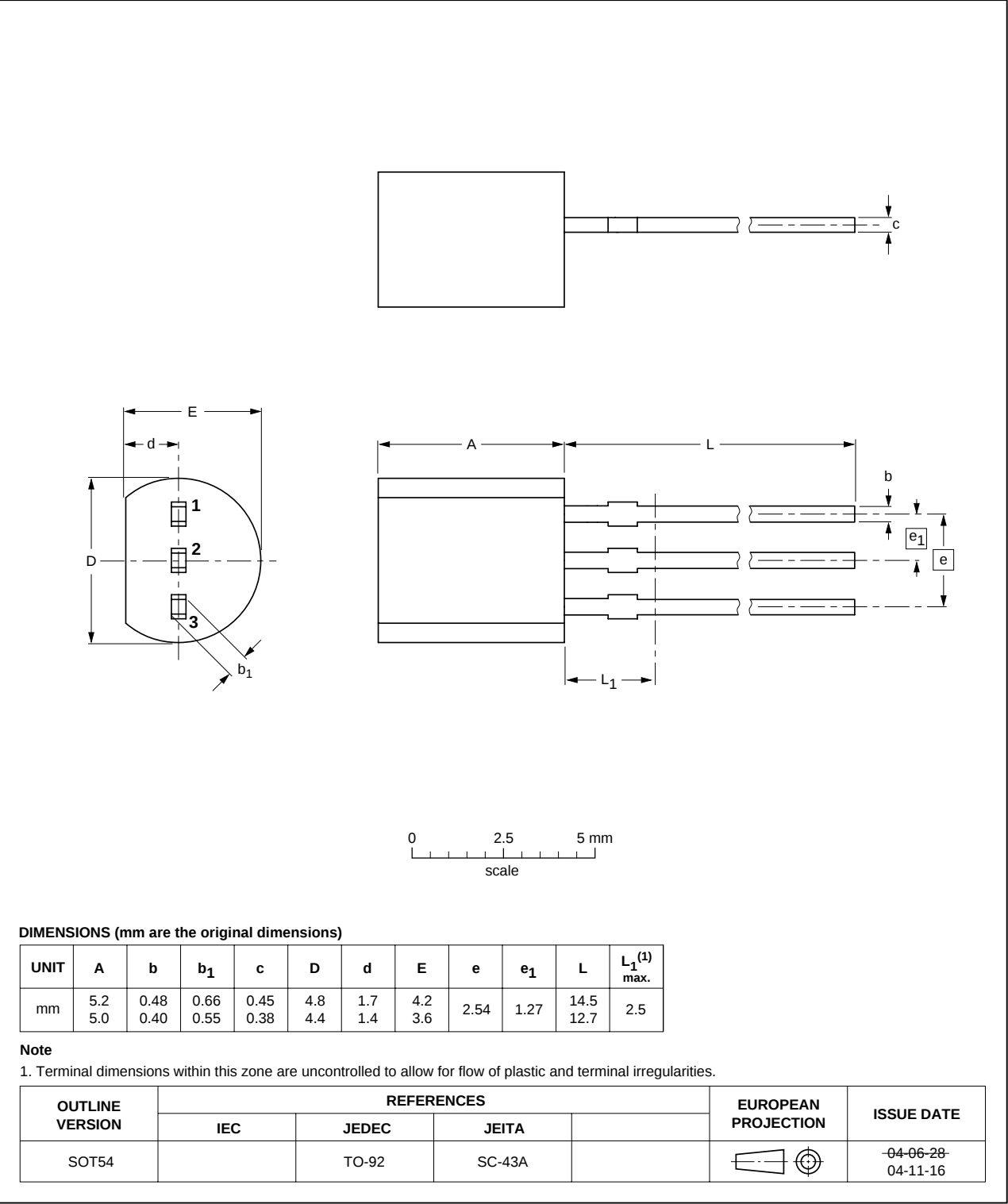


Fig 13. Package outline SOT54 (TO-92)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXL0840_1	20080226	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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