NXQ1TXH5

One-chip 5 V Qi wireless transmitter

Rev. 1.1 — 4 March 2016 Product short data sheet

1. General description

The NXQ1TXH5 is a controller and driver IC for a 5 V Qi-certified/compliant low-power wireless charger. It offers a fully integrated solution that includes a 5 V full-bridge power stage, as defined in Wireless Power Consortium (WPC) 5 V Qi standards A5, A11, A12 and A16.

The NXQ1TXH5 uses a dedicated analog ping circuitry to detect devices. With the analog pin circuitry, an extremely low standby (wait state) power consumption is achieved. When a Qi-compliant receiver is placed, the NXQ1TXH5 starts to communicate with it. After the receiver is recognized, it safely initiates wireless power transfer from the transmitter to the receiver, while monitoring for fault conditions such as overheating or interference from metal objects. The device is optimized to operate from a 5 V USB power supply and uses Smart Power Limiting (SPL) to adjust the output power automatically to compensate for power-limited supplies. The device supports Foreign Object Detection (FOD).

LED outputs and a buzzer output are available for the user interface. The LED outputs feature a number of blinking modes. Static Power Reduction (SPR) allows multiple NXQ1TXH5-based transmitters to operate from a single USB power supply by limiting power consumption per device.

The NXQ1TXH5 is available in a 5 mm × 5 mm, 32-pin HVQFN package.

2. Features and benefits

- Single-chip WPC 1.2 transmitter
- Operates from 5 V supply
- Low EMI radiation meeting EN55022 radiated and conducted emission limits
- Very few external components needed, minimizing cost and board space
- Extremely low-power receiver detection circuitry by integrating an analog ping circuit; standby (wait state) power 10 mW (typical)
- Power stage protected against overcurrents and overtemperature
- Dual-channel Amplitude Shift Keying (ASK) demodulation
- Demodulates communication packets from Qi-compliant receivers
- PID regulation for power drive and control
- Internal 1.8 V digital supply generation
- LED (×2) and buzzer outputs
- NTC input for external temperature check and protection
- On-chip thermal protection
- Small HVQFN 32-pin package (5 mm × 5 mm) with 0.5 mm pitch

- FOD with WPC receiver versions 1.2 and 1.1 and for legacy receiver support (Qi version 1.0)
- Peak efficiency > 75 %
- Excellent low power (< 2 W) transfer efficiency. Ideal for charging wearables

3. Applications

- Wireless Power Consortium (WPC) Qi certified/compliant wireless power transmitters
- Wireless charger for (smart)phones, toys, shavers, pads, and other handheld devices
- High-efficiency low-power wireless charger for smartwatches and other wearables

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDP}	power supply voltage	on pins VDDP1 and VDDP2	3.4	-	5.25	V
I_{DDP}	power supply current	on pins VDDP1 and VDDP2				
		wait state (average current)	-	2	-	mA
		power transfer state (no load)	-	15	-	mA
		power transfer state (with load)	-	1.5	5[1]	A

[1] The maximum average current is 2 A. However, when removing the receiver, the power stage current protection limits the peak current at 5 A.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
NXQ1TXH5	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

5.1 Ordering options

Table 3. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum ordering quantity	Temperature
NXQ1TXH5	NXQ1TXH5/101J	HVQFN32	reel 13" Q1/T1, *standard mark SMD non-dry-pack	6000	T_{amb} = −20 °C to +85 °C

6. Block diagram

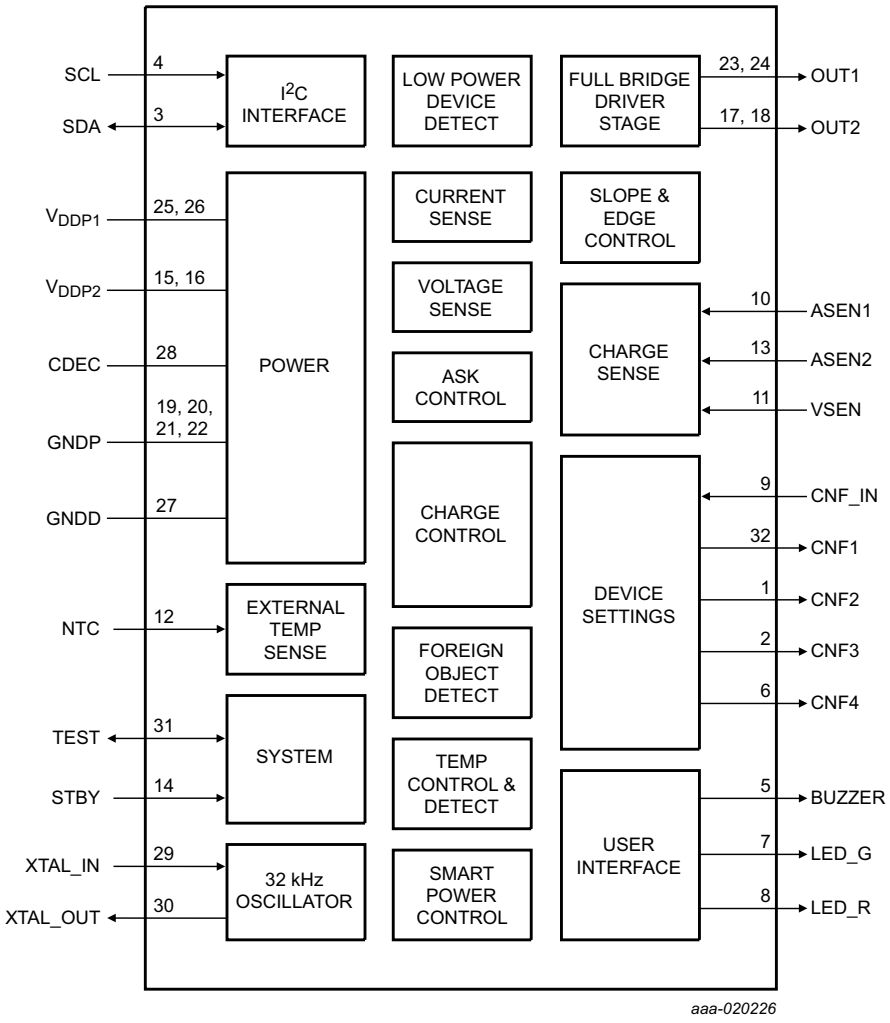
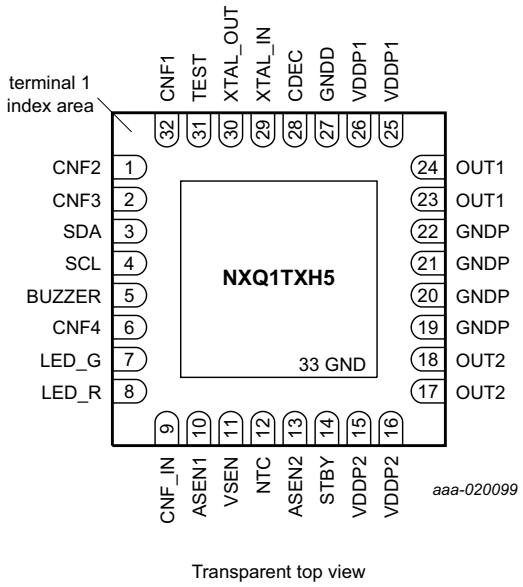


Fig 1. NXQ1TXH5 functional block diagram

7. Pinning information

7.1 Pinning



Transparent top view

For enhanced thermal and electrical performance the exposed die-pad (33), the GNDP and GNDD pins must be directly connected to the top layer board ground (GNDD). The exposed die-pad must also be connected to bottom layer board ground with plated-through vias (see Section 12.4).

Fig 2. Pin configuration

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type	Description
CNF2	1	I	configuration output 2 for FOD_E
CNF3	2	I	configuration output 3 for FOD_threshold
SDA	3	I/O	I^2C-bus data input/output; connect to test pad (see Figure 4)
SCL	4	I	I^2C-bus clock input; connect to test pad (see Figure 4)
BUZZER	5	O	buzzer output
CNF4	6	I	configuration output 4 for LED_mode
LED_G	7	O	green LED output
LED_R	8	O	red LED output
CNF_IN	9	I	configuration input
ASEN1	10	I	analog sense input 1
VSEN	11	I	coil voltage sense
NTC	12	I	temperature measurement using NTC
ASEN2	13	I	analog sense input 2
STBY	14	I	standby function; connect to ground when not used
VDDP2	15, 16	P	power supply pin 2

Table 4. Pin description *...continued*

Symbol	Pin	Type	Description
OUT2	17, 18	O	transmitter output 2
GNDP	19, 20, 21, 22	P	power ground
OUT1	23, 24	O	transmitter output 1
VDDP1	25, 26	P	power supply pin 1
GNDD	27	P	digital ground
CDEC	28	P	decoupling connection for internal LDO
XTAL_IN	29	I	crystal input
XTAL_OUT	30	O	crystal output
TEST	31	I/O	test pin; connect to ground
CNF1	32	O	configuration output 1 for SPR

8. Functional description

The NXQ1TXH5 is a fully integrated 5 V wireless charger with an internal full-bridge power stage. It efficiently integrates all the functions required to control the power transfer with a Qi-compliant receiver. It can deliver up to 8 W continuous power into the Qi-compliant type A5, A11, A12 or A16 transmitter coil.

Figure 1 shows a block diagram of the NXQ1TXH5. It is operational when a 5 V supply is connected and pin STBY is LOW. The NXQ1TXH5 starts checking for a device on the transmitter base station. When a receiver is detected, power transfer is initiated for the detected receiver.

The power transfer can be monitored via the LEDs and BUZZER outputs.

Additional inputs are provided for configuring the NXQ1TXH5:

- LED mode selection
- Configuring FOD according to the application design and coil/capacitor selection
- Setting the SPR level
- Enabling/disabling SPL

8.1 NXQ1TXH5 operating states

The NXQ1TXH5 supports a number of operating states:

- **Power-on state:**
  The NXQ1TXH5 generates a power-on LED blinking sequence after which it is operational (standby = low).
- **Standby state**:
  The device is inactive in standby state. The NXQ1TXH5 is in standby state when pin STBY is HIGH. STBY must be connected to ground in standalone applications.
- **Wait state (analog and digital ping)**:
  The NXQ1TXH5 performs extremely low-power device detection using analog circuitry in analog ping mode. The NXQ1TXH5 performs standard device detection using the DSP in digital ping mode.
- **ID and config state**:
  The NXQ1TXH5 communicates with and begins to supply power to a Qi-compliant receiver.
- **Power transfer state**:
  The NXQ1TXH5 charges the Qi-compliant receiver in power transfer state.
- **Charged state**:
  The NXQ1TXH5 switches to charged state when it receives a ‘charge complete’ message from the receiver.
- **Fault state**:
  The NXQ1TXH5 switches to a fault state when:
  - A receiver error is reported
  - A foreign object is detected between receiver and the transmitter
  - A receiver/transmitter overtemperature condition occurs

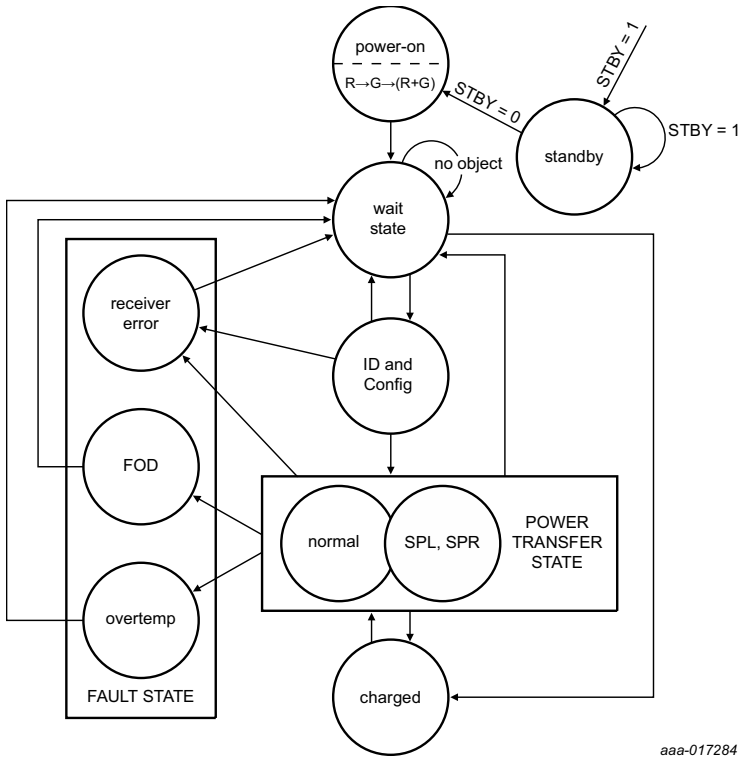


Fig 3. NXQ1TXH5 state diagram

8.2 Protections

The NXQ1TXH5 incorporates three built-in protections.

- Temperature reduction and temperature protection mechanism
- OverCurrent Protection (OCP)
- NTC, which monitors the voltage level on an external NTC network

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to ground. See Limiting Values disclaimer in Section 15.3.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDP}	power supply voltage	on pin VDDP1 and VDDP2	–0.3	+6.0	V
T_j	junction temperature		-	+150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–20	+85	°C
V_{ESD}	electrostatic discharge voltage	according to the Human Body Model (HBM)	–2	+2	kV
		according to the Charge Device Model (CDM)	–500	+500	V

10. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	2-layer application board positioned horizontally in free air; dimensions 45 mm × 45 mm × 0.8 mm; natural convection; copper coverage on each layer > 95 %; copper thickness each layer 70 μm	30	K/W

11. Characteristics

Table 7. DC characteristics

T_{amb} = 25 °C, default settings unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDP}	power supply voltage	on pin VDDP1 and VDDP2 [1]	3.5	-	5.25	V
I_{DDP}	power supply current	on pins VDDP1 and VDDP2:				
		wait state (peak current) [2]	-	1	-	A
		wait state (average current) [2]	-	2	-	mA
		standby state (STBY HIGH)	-	15	50	μA
		power transfer state (no-load)	-	15	-	mA
		power transfer state (average current with load) [2]	-	-	2	A
		power transfer state (absolute peak current with load)	-	-	5	A

[1] The maximum DC V_{DDP} input voltage is 5.25 V. However, at the maximum load, spikes can occur due to high dI/dt. With the proper decoupling circuitry and snubbers at the outputs, these spikes must never exceed 7 V (see Section 12.2 and Section 12.3).

[2] The current consumption depends on the load impedance of the LC tank connected to the output stage at 175 kHz. Assumed typical value: L = 6.3 μF, 60 mΩ and C = 384 nF.

Table 8. AC characteristics

T_{amb} = 25 °C, default settings unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Full-bridge power stage						
f_{sw}	switching frequency	start-up and power transfer states	110	-	205	kHz
$f_{sw(step)}$	switching frequency step size	start-up and power transfer states	-	500	-	Hz
δ	duty cycle	start-up and power transfer states	10	-	50	%
δ_{step}	duty cycle step size	start-up and power transfer states	-	0.1	-	%
pin STBY						
V_{IH}	HIGH-level input voltage	standby state	1.2	-	V_{DDP}	V
V_{IL}	LOW-level input voltage	operating state	-	-	0.6	V
pins CNF_IN, ASEN1, ASEN2, VSEN, and NTC						
V_I	input voltage	operating range [1]	0	-	1.5	V
LED_G, LED_R and CNF1, CNF2, CNF3, and CNF4 outputs						
V_O	output voltage	set externally	400	-	V_{DDP}	mV
I_{load}	load current	open-drain output [2]	-	-	20	mA
BUZZER output						
V_O	output voltage	set externally	400	-	V_{DDP}	mV
I_{load}	load current	open-drain output [2]	-	-	20	mA
I^2C pins: SCL and SDA						
V_{IH}	HIGH-level input voltage		1	-	3.6	V
V_{IL}	LOW-level input voltage		-	-	0.6	V
oscillator: pins XTAL_IN and XTAL_OUT						
V_I	input voltage		-	-	1.8	V
external crystal requirements						
f_{nom}	nominal frequency		32	32.768	33.5	kHz
D_L	drive level		-	-	1	µW
C_L	load capacitance	[3]	8	12	14	pF

[1] The nominal operating range is from 0 V to 1.5 V. However, any level between 1.5 V and V_{DDP} has the same effect (as 1.5 V).

[2] The output voltage at maximum load current is guaranteed not to exceed 400 mV.

[3] The load capacitors are embedded in the NXQ1TXH5.

12. Application information

12.1 Crystal oscillator

The NXQ1TXH5 uses an external low-cost 32.768 kHz crystal, with a 1 % accuracy. The crystal should support a load capacitance of ≈12 pF (the load capacitance is embedded in the NXQ1TXH5). Do not connect the crystal to the NXQ1TXH5 using vias, but directly on the top layer of the PCB. If possible, shield the crystal by connecting the casing to ground. The crystal is connected to the oscillator input pin (XTAL_IN) via a 2.2 pF series capacitor.

12.2 Supply decoupling

Effective supply decoupling is required. The decoupling capacitors must to be chosen such that the effective capacitance is at least 10 μF at a DC bias voltage of 5.5 V. The frequency must be 205 kHz for each supply pin. X5R capacitors of 22 μF normally fulfill this requirement. To prevent spikes that are too high on the VDDP pins and to improve HF behavior and reduce EMI, use smaller (10 nF) high-quality capacitors. These capacitors must be mounted as close as possible to the VDDP pins of the NXQ1TXH5 in parallel with the 22 μF capacitors (see Figure 4).

12.3 Snubber network

Snubber RC networks are connected to outputs OUT1 and OUT2. Each snubber network consists of a 6.8 nF capacitor in series with a 1 Ω resistor to ground (see Figure 4). The snubber network must be connected as close as possible to the NXQ1TXH5 OUT1 and OUT2 pins.

12.4 Exposed die-pad ground and thermal connection

For optimal thermal and electrical performance, the device bottom exposed VSS pin (pin 33) MUST be soldered to a PCB solder land under the exposed die-pad. To have good electrical contact and thermal flow from the device to the bottom copper layer, the PCB solder pad under the device MUST be connected with plated-through vias to the copper bottom layer of the PCB. In this way, the PCB bottom copper layer can provide heat sinking for the device dissipation.

In the NXQ1TXH5 application note examples are provided for recommended layouts with good thermal and electrical performance.

12.5 Support interface

For NXP Semiconductors support purposes, connecting interface wires must be made possible to tune the FOD resistors and to check DSP operation. To connect the interface wires, the NXQ1TXH5 I^2C interface pins (pins 3 and 4) must be made available on the PCB layout as exposed test-pads with minimum 2 mm^2 solder area. A test pad for ground connection must also be placed close to the I^2C test-pad connections. Do not connect pull-up resistors to VDDP for the I^2C interface pins. For more advanced debug options for NXP Semiconductors, pins 1, 2, and 32 require the same test options.

12.6 Application diagram

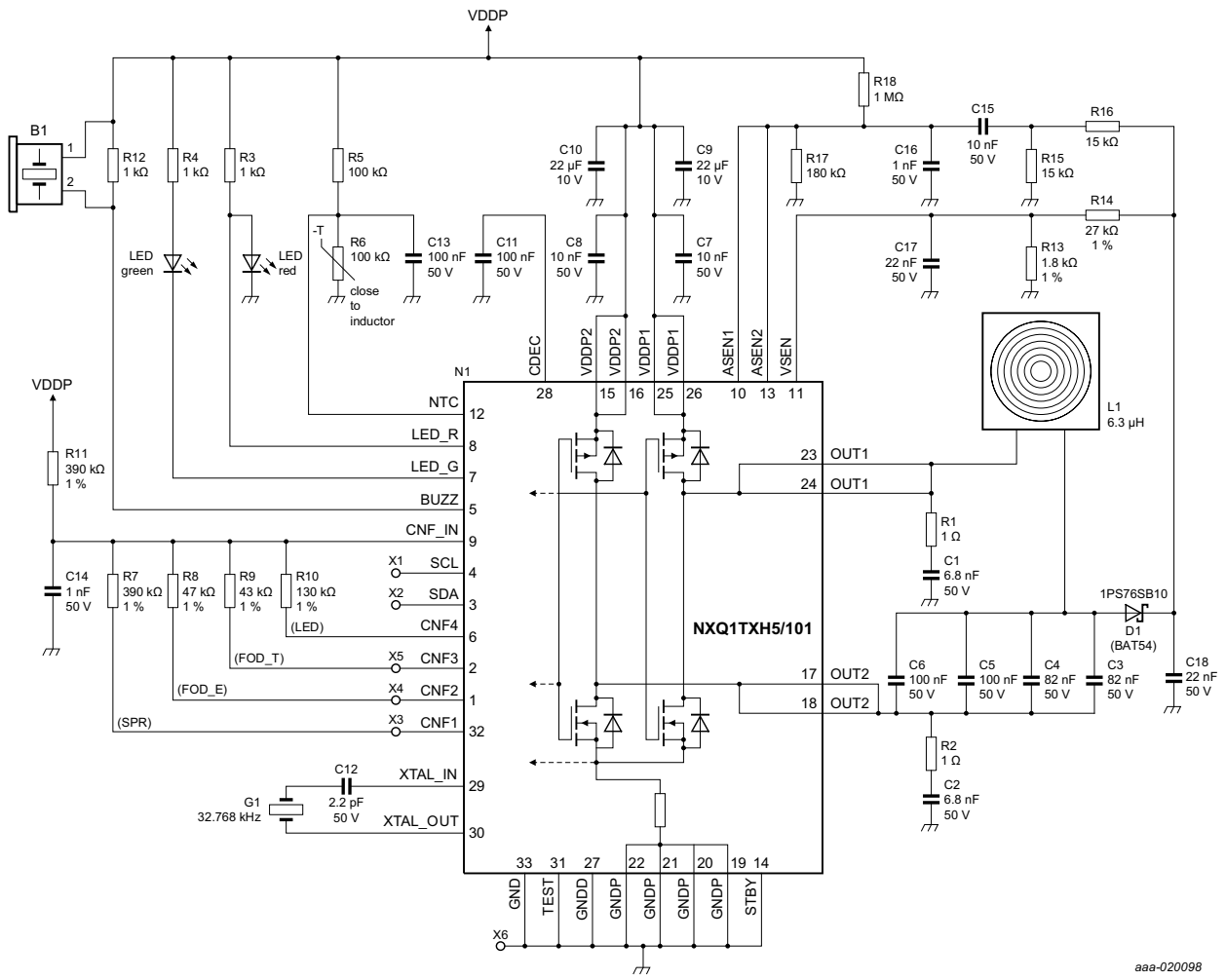


Fig 4. Application diagram

12.7 Efficiency

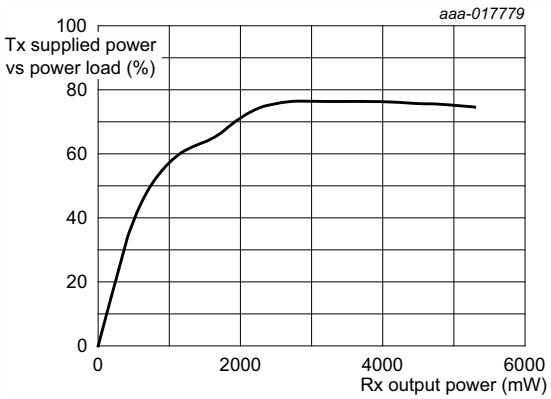


Fig 5. Graph of system efficiency as a function of output power at V_{DDP} = 5 V

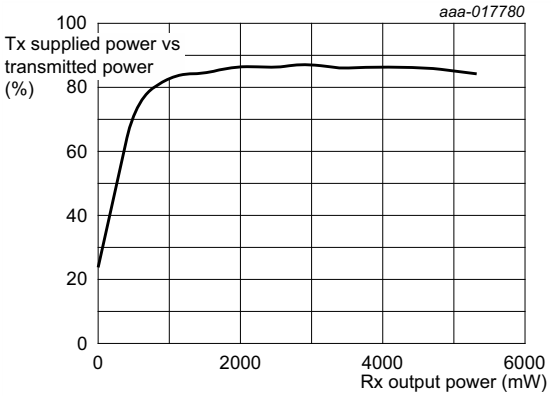


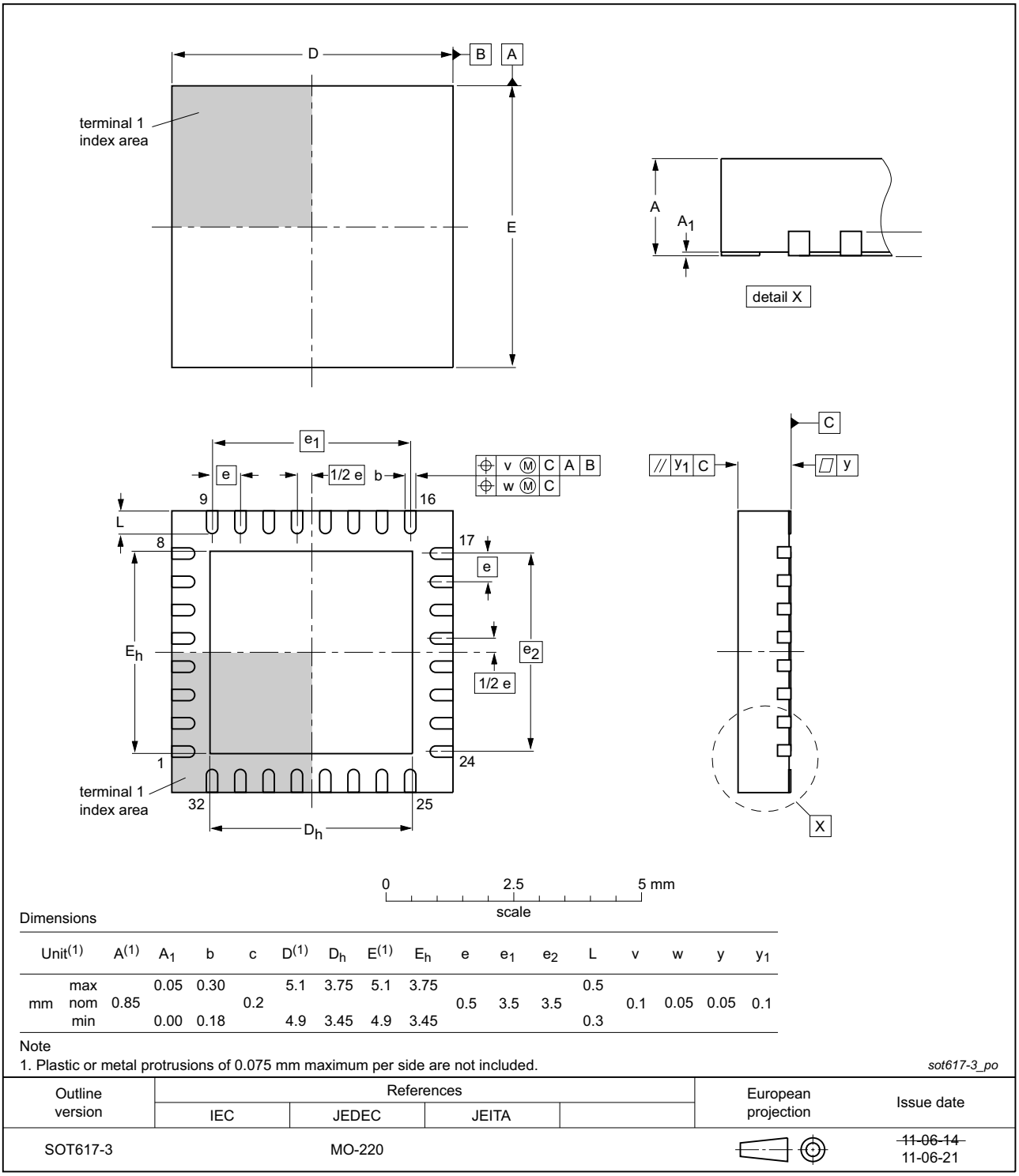
Fig 6. Graph of power transfer efficiency as a function of output power at V_{DDP} = 5 V

Remark: The curves in Figure 5 and Figure 6 are measured on the NXP Semiconductors DB1340 boards with:

- Coil: Elec&Eltek (E&E); Y31-60055F
- Capacitors:
  - 82 nF; 5 %; 50 V; C0G; 1206; Murata; GRM31C5C1H823JA01L
  - 100 nF; 5 %; 50 V; C0G; 1206; TDK; CGA5L2C0G1H104J160AA

13. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-3**



Dimensions

Unit(1)		A(1)	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot617-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-3		MO-220				~~11-06-14~~ 11-06-21

Fig 7. Package outline SOT617-3 (HVQFN32)

14. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXQ1TXH5 v.1.1	20160304	Product short data sheet	-	NXQ1TXH5 v.1
Modifications:	• Table 7 “DC characteristics” has been updated.			
NXQ1TXH5 v.1	20160211	Product short data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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17. Contents

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