

PHKD6N02LT

Dual N-channel TrenchMOS logic level FET

Rev. 04 — 27 April 2010

Product data sheet

1. Product profile

1.1 General description

Dual logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources

1.3 Applications

- Battery chargers
- DC-to-DC converters
- Notebook computers
- Portable equipment

1.4 Quick reference data

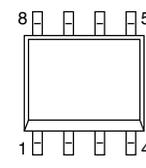
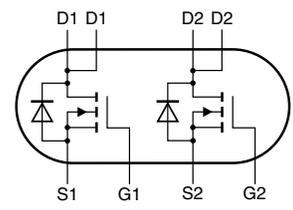
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	20	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; Single device conducting; see Figure 1 ; see Figure 3	-	-	10.9	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 2	-	-	4.17	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 2.5\text{ V}$; $I_D = 3\text{ A}$; $T_j = 25\text{ °C}$	-	25	35	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 6\text{ A}$; $V_{DS} = 16\text{ V}$; $T_j = 25\text{ °C}$; see Figure 11	-	6	-	nC



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>SOT96-1 (SO8)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

3. Ordering information

Table 3. Ordering information

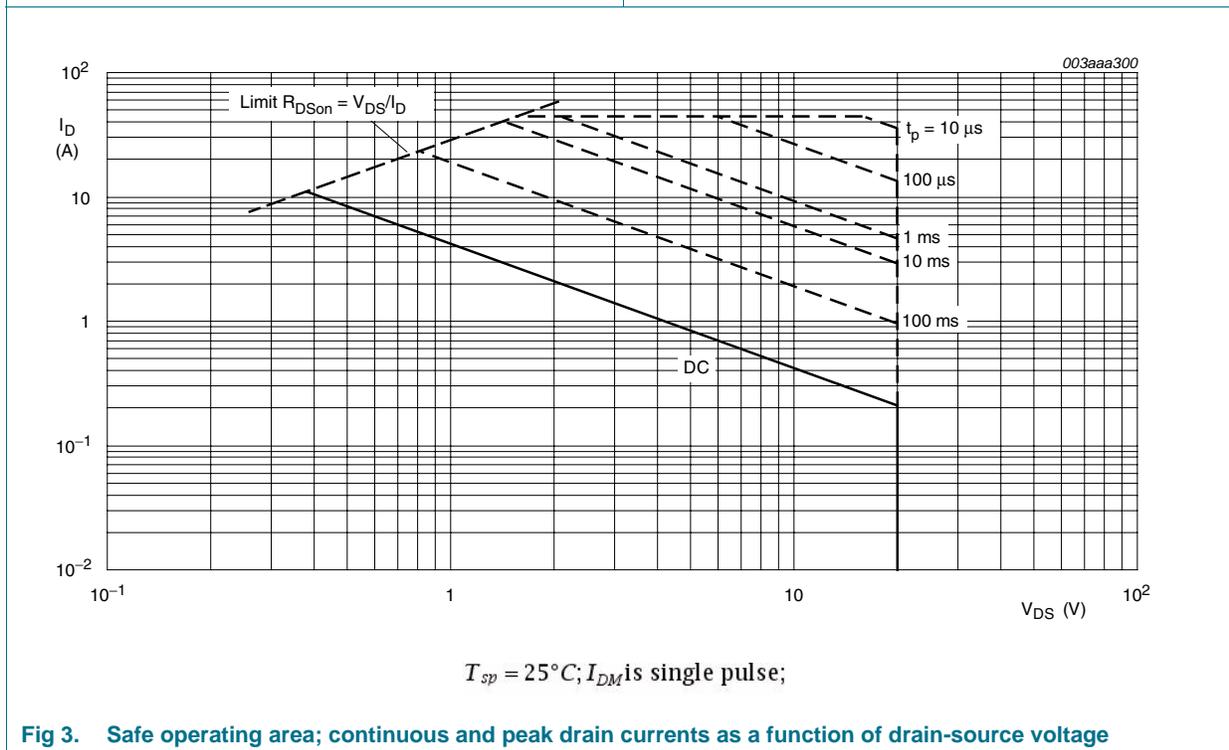
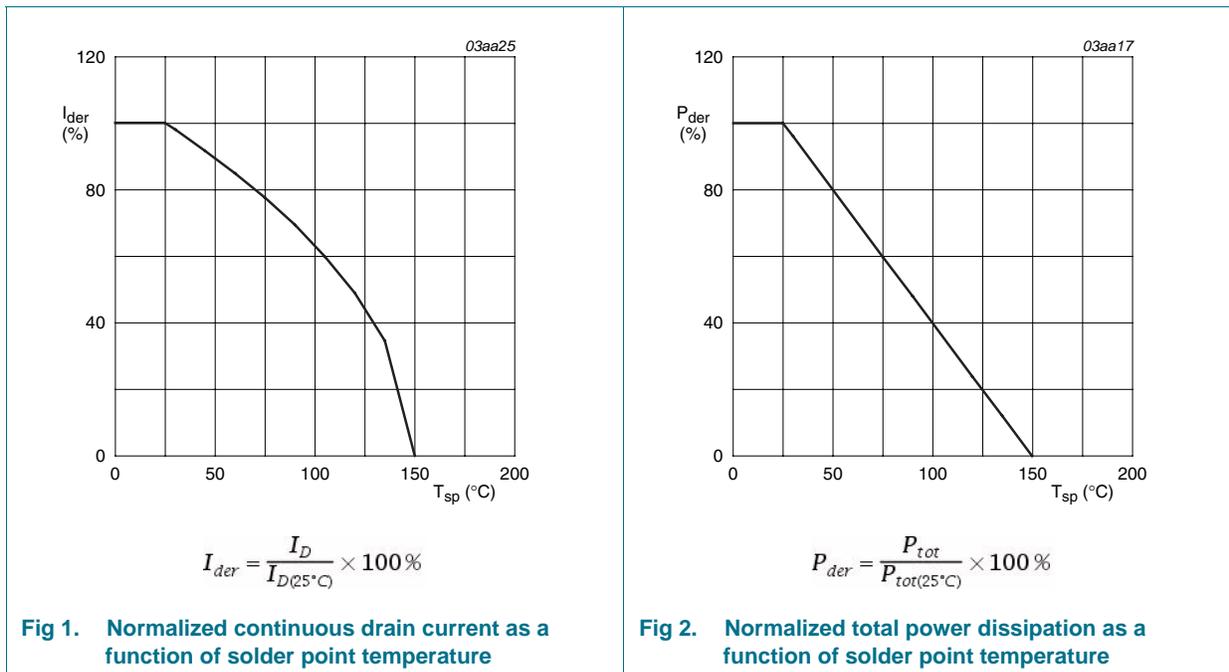
Type number	Package		Version
	Name	Description	
PHKD6N02LT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	20	V
V_{DGR}	drain-gate voltage	$T_j \leq 150\text{ °C}$; $T_j \geq 25\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	-	20	V
V_{GS}	gate-source voltage		-12	-	12	V
I_D	drain current	$T_{sp} = 100\text{ °C}$; Single device conducting; see Figure 1	-	-	6.8	A
		$T_{sp} = 25\text{ °C}$; Single device conducting; see Figure 1 ; see Figure 3	-	-	10.9	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; $t_p \leq 100\text{ }\mu\text{s}$; pulsed; Single device conducting; see Figure 3	-	-	44	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 2	-	-	4.17	W
T_{stg}	storage temperature		-55	-	150	°C
T_j	junction temperature		-55	-	150	°C
Source-drain diode						
I_S	source current	$T_{sp} = 25\text{ °C}$	-	-	3.5	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed	-	-	44	A



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	30	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on printed-circuit board	-	70	-	K/W

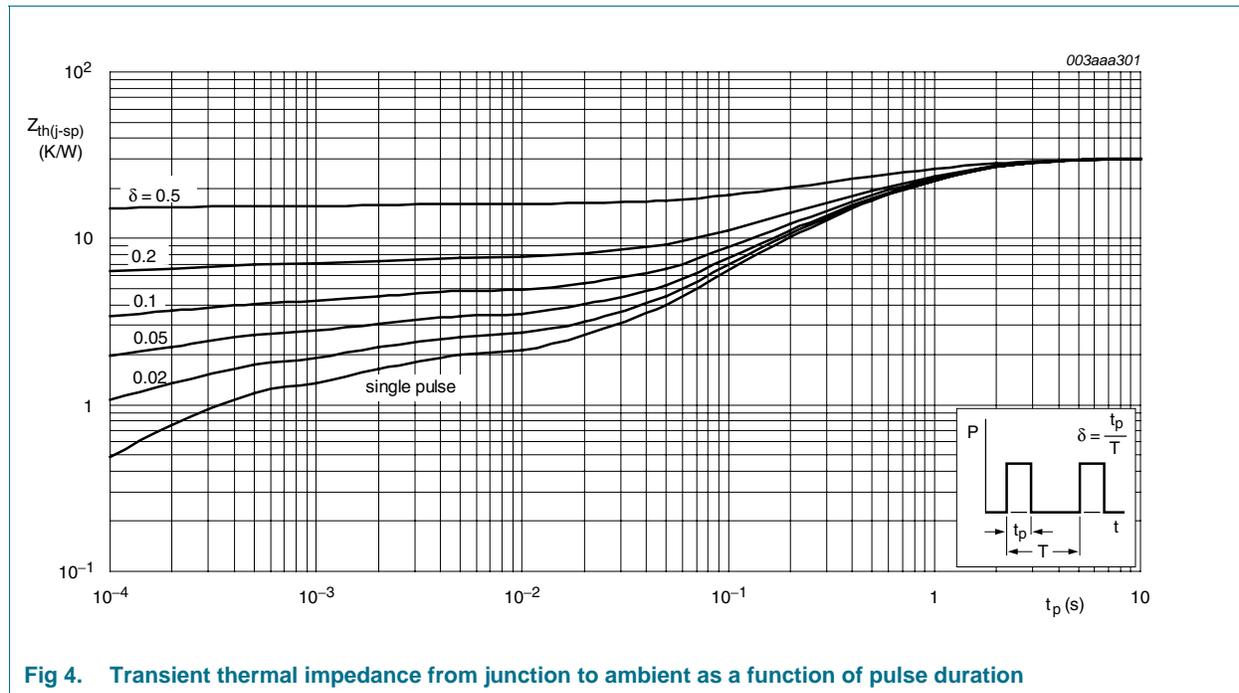


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	20	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250 \mu\text{A}$; $V_{DS} = 10 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 8	0.5	-	1.5	V
I_{DSS}	drain leakage current	$V_{DS} = 20 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	μA
		$V_{DS} = 20 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 150 \text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 12 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -12 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 2.5 \text{ V}$; $I_D = 3 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	25	35	m Ω
		$V_{GS} = 5 \text{ V}$; $I_D = 3 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$; see Figure 9 ; see Figure 10	-	-	35	m Ω
		$V_{GS} = 5 \text{ V}$; $I_D = 3 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 9 ; see Figure 10	-	16	20	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 6 \text{ A}$; $V_{DS} = 16 \text{ V}$; $V_{GS} = 5 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 11	-	15.3	-	nC
Q_{GS}	gate-source charge		-	2.2	-	nC
Q_{GD}	gate-drain charge		-	6	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 12	-	950	-	pF
C_{oss}	output capacitance		-	355	-	pF
C_{rSS}	reverse transfer capacitance		-	256	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 \text{ V}$; $R_L = 3.3 \Omega$; $V_{GS} = 5 \text{ V}$;	-	15	-	ns
t_r	rise time	$R_{G(ext)} = 4.7 \Omega$; $T_j = 25 \text{ }^\circ\text{C}$	-	49	-	ns
$t_{d(off)}$	turn-off delay time		-	50	-	ns
t_f	fall time		-	23	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 6 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 13	-	-	1.2	V
t_{rr}	reverse recovery time	$I_S = 6 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	40	-	ns
Q_r	recovered charge	$V_{DS} = 20 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	7	-	nC

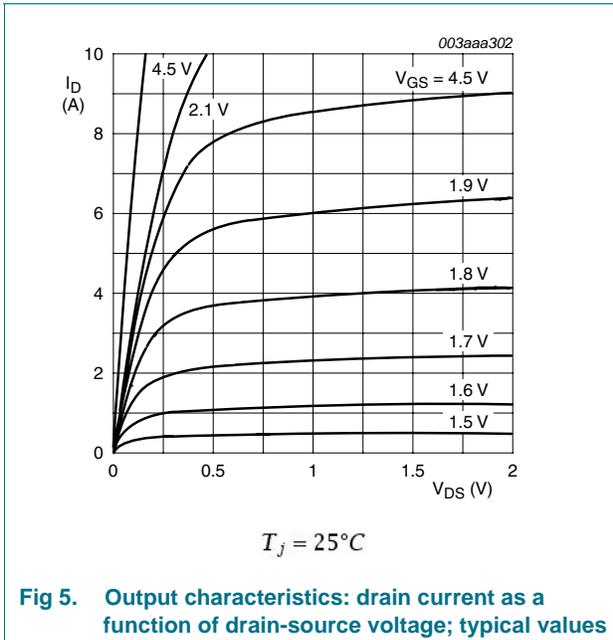


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

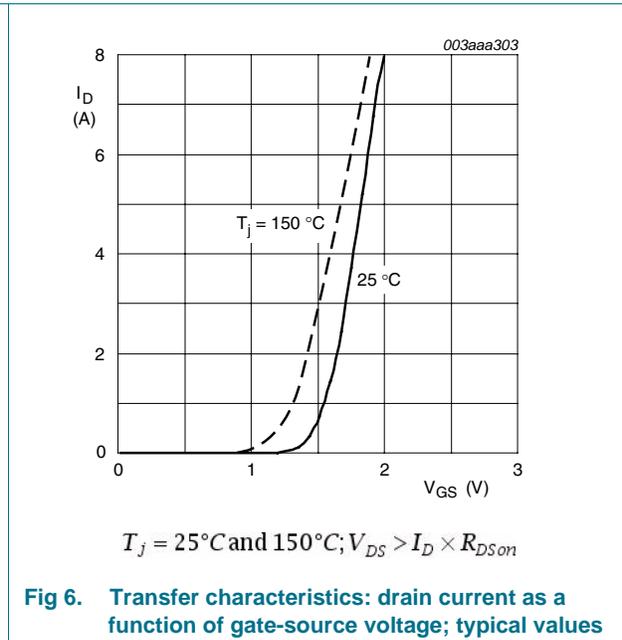


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

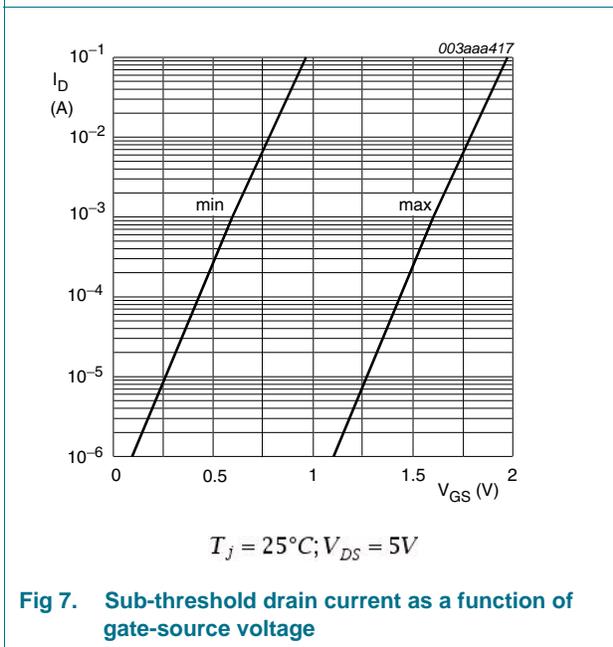


Fig 7. Sub-threshold drain current as a function of gate-source voltage

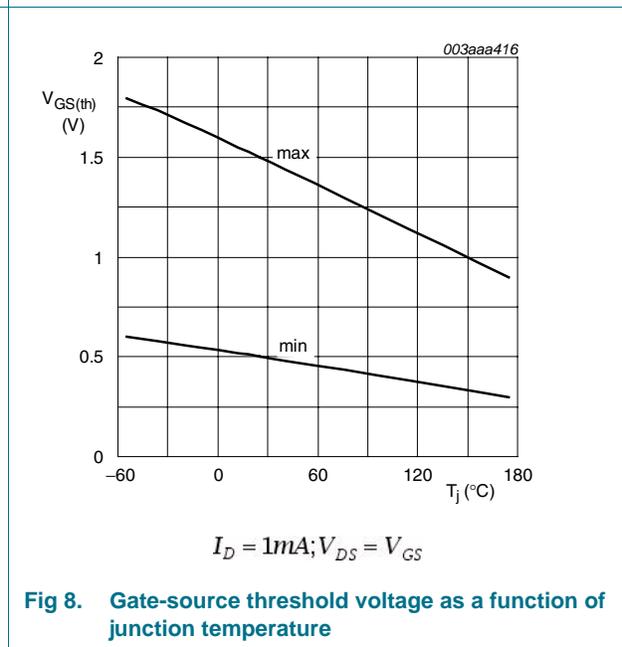
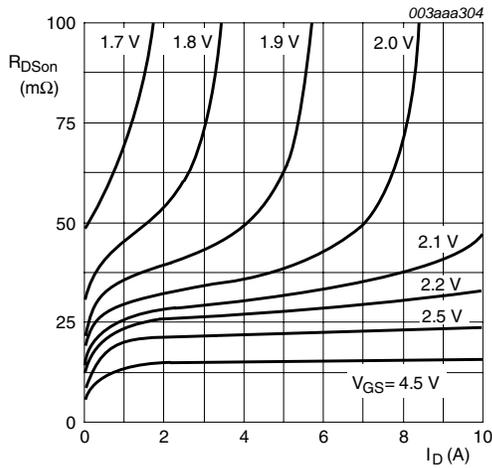
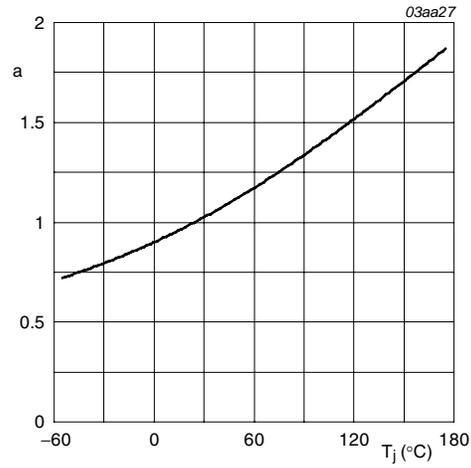


Fig 8. Gate-source threshold voltage as a function of junction temperature



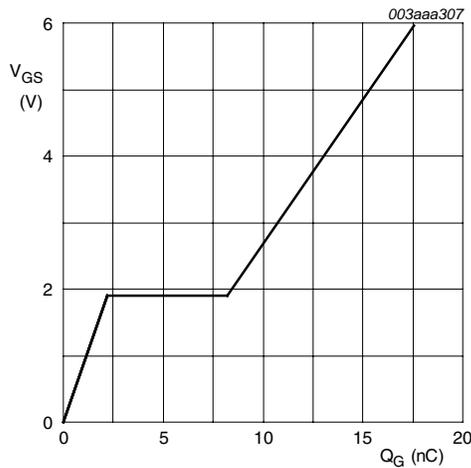
$T_j = 25^\circ\text{C}$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



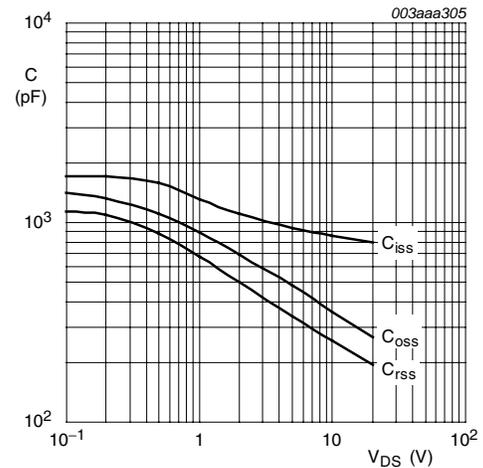
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



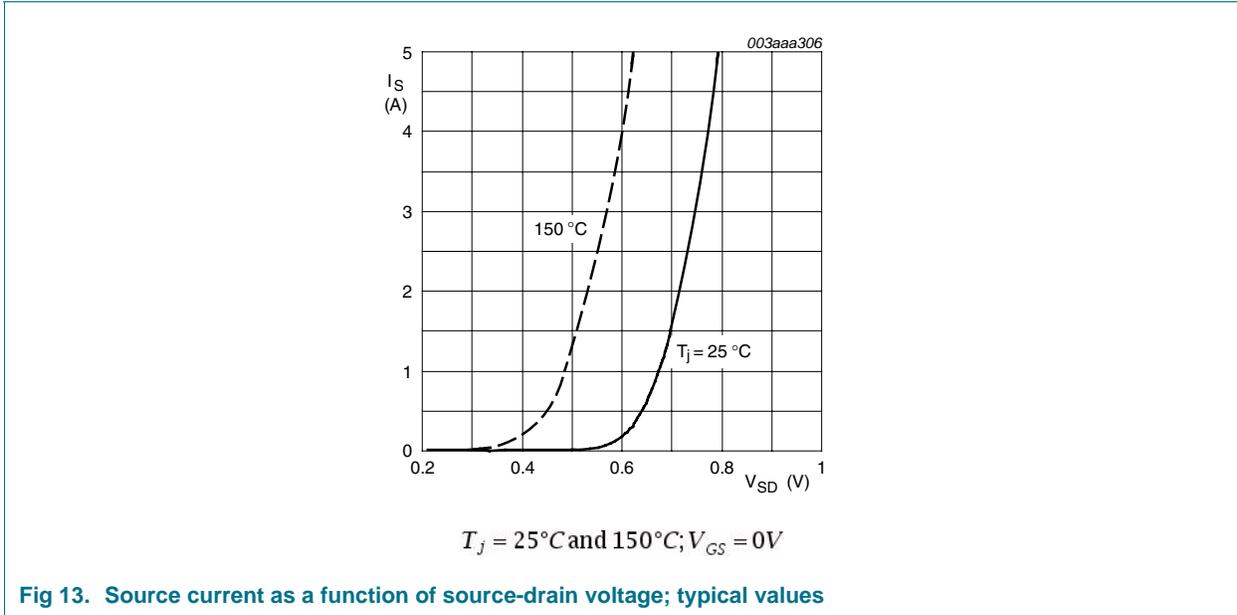
$I_D = 6\text{A}; V_{DS} = 16\text{V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

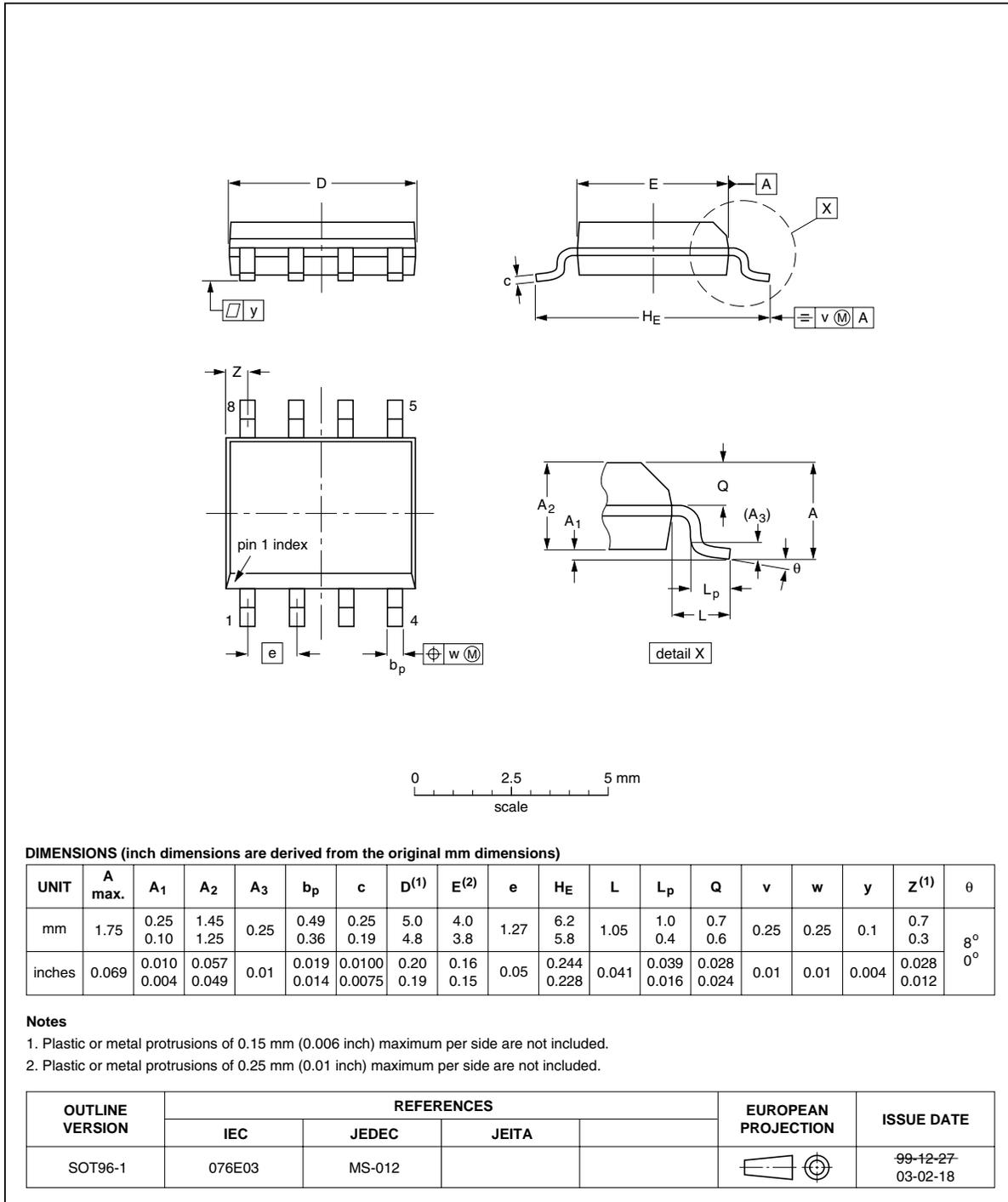


Fig 14. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHKD6N02LT_4	20100427	Product data sheet	-	PHKD6N02LT_3
Modifications:	• Various changes to content.			
PHKD6N02LT_3	20091119	Product data sheet	-	PHKD6N02LT-02
PHKD6N02LT-02	20030812	Product data	-	PHKD6N02LT-01
PHKD6N02LT-01	20010907	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
6	Characteristics	5
7	Package outline	9
8	Revision history	10
9	Legal information	11
9.1	Data sheet status	11
9.2	Definitions	11
9.3	Disclaimers	11
9.4	Trademarks	12
10	Contact information	12

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