

2.5V-3.3V Low-Skew 1-4 Differential PECL Fanout Buffer

FEATURES

- Four differential 2.5V/3.3V LVPECL output pairs.
- Output Frequency: $\leq 1\text{GHz}$.
- Two selectable differential input pairs.
- Translates any standard single-ended or differential input format to LVPECL output. It can accept the following standard input formats and more:
 - LVPECL, LVCMOS, LVDS, HCSL, SSTL, LVHSTL, CML.
- Output Skew: 25ps (typ.).
- Part-to-part skew: 140ps (typ.).
- Propagation delay: 1.5ns (typ.).
- Additive Jitter: $<100\text{fs}$ (typ.).
- Operating Supply Voltage: 2.375V ~ 3.63V.
- Operating temperature range from -40°C to 85°C .
- Package availability: 20-pin TSSOP.

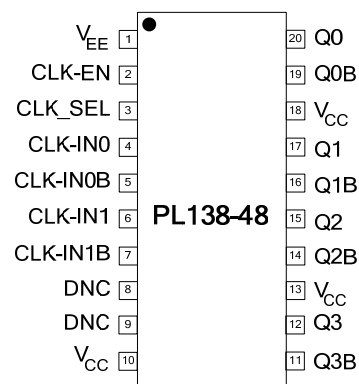
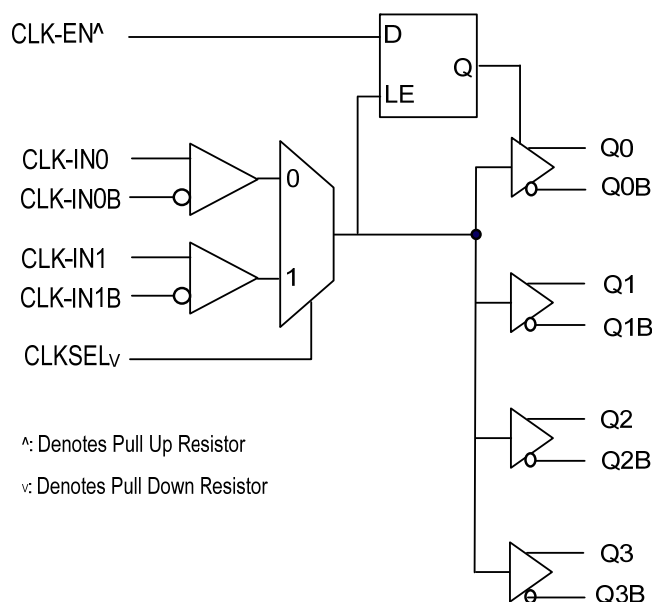
DESCRIPTION

The PL138-48 is a high performance low-cost 1: 4 outputs Differential LVPECL fanout buffer.

PhaseLink's family of Differential LVPECL buffers are designed to operate from a single power supply of $2.5\text{V} \pm 5\%$ or $3.3\text{V} \pm 10\%$. The differential input pairs are designed to accept most standard input signal levels, using an appropriate resistor bias network, and produce a high quality set of outputs with the lowest possible skew on the outputs, which is guaranteed for part-to-part or lot-to lot skew.

Designed to fit in a small form-factor package, PL138 family offers up to 1GHz of output operation with very low-power consumption, and lowest additive jitter of any comparable device.

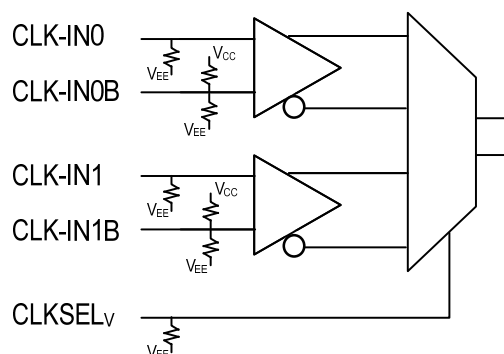
BLOCK DIAGRAM



20-Pin TSSOP Package

2.5V-3.3V Low-Skew 1-4 Differential PECL Fanout Buffer
PIN DESCRIPTIONS

Name	Package Pin #	Type (Mode)	Description
	LQFP-20		
V _{EE}	1	Power	Power Supply pin connection
CLK-EN	2	Input (Pullup)	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When 'Low', Q outputs are forced low, QB outputs are forced high. LVTTTL / LVCMOS interface levels.
CLK-SEL	3	Input (Pulldown)	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVTTTL / LVCMOS interface levels.
CLK-IN0	4	Input (Pulldown)	True part of differential clock input signal.
CLK-IN0B	5	Input (Pullup/Pulldown)	Complementary part of differential clock input signal.
CLK-IN1	6	Input (Pulldown)	True part of differential clock input signal.
CLK-IN1B	7	Input (Pullup/Pulldown)	Complementary part of differential clock input signal.
DNC	8, 9	-	Do Not Connect.
V _{CC}	10, 13, 18	Power	Power Supply pin connection
QB0 ~ QB3	11, 14, 16, 19	Output	LVPECL Complementary output
Q0 ~ Q3	12, 15, 17, 20	Output	LVPECL True output

INPUT LOGIC BLOCK DIAGRAM

INPUT PIN CHARACTERISTICS

Parameter	Min.	Typ.	Max.	Units
Input Pulldown Resistor		75		kΩ
Pullup/Pulldown Resistors		100		kΩ

INPUT CLOCK CONTROL SELECTION

CLK_SEL	Selected Source
0	CLK-IN0
1	CLK-IN1

INPUT CLOCK FUNCTION

Inputs			Outputs	
CLK-EN	CLKSEL	Source	Q0:Q3	Q0B:Q3B
0	0	CLK-IN0	Disabled Low	Disabled High
0	1	CLK-IN1	Disabled Low	Disabled High
1	0	CLK-IN0	Enabled	Enabled
1	1	CLK-IN1	Enabled	Enabled

2.5V-3.3V Low-Skew 1-4 Differential PECL Fanout Buffer
ELECTRICAL SPECIFICATIONS
Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	-0.5	$V_{DD}+0.5$	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		110	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model	2			kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

DC CHARACTERISTICS, $V_{CC} = 3.3V$; $V_{EE} = 0V$

Parameter	Symbol	-40°C			25°C			80°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output High Voltage*	V_{OH}	2.215	2.320	2.420	2.275	2.350	2.420	2.275	2.35	2.420	V
Output Low Voltage*	V_{OL}	1.470	1.610	1.745	1.490	1.585	1.680	1.490	1.585	1.680	V
Input High Voltage	V_{IH}	2.075		2.420	2.135		2.420	2.135		2.420	V
Input Low Voltage	V_{IL}	1.470		1.890	1.490		1.825	1.490		1.825	V
Output Voltage Reference**	V_{BB}	1.86		1.98	1.92		2.04	1.92		2.04	V
Input High Voltage Common Mode Range† ††	V_{CMR}	1.2		3.3	1.2		3.3	1.2		3.3	V
Input High Current	CLK-IN0, CLK-IN1	I_{IH}		75			75			75	μA
Input Low Current	CLK-IN0B, CLK-IN1B	I_{IL}	-75		-75			-75			μA

Input and output parameters vary 1:1 with V_{CC} when V_{CC} varies $\pm 10\%$.

* Outputs terminated with 50Ω to $V_{CCO} - 2V$.

** Single-ended input operation is limited to $V_{CC} \geq 3V$ in LVPECL mode.

† Common mode voltage is defined as V_{IH}

†† For single-ended applications, the maximum input voltage for CLK-INx, CLK-INxB is $V_{CC} + 0.3V$

2.5V-3.3V Low-Skew 1-4 Differential PECL Fanout Buffer
DC CHARACTERISTICS, V_{CC} = 2.5V; V_{EE} = 0V

Parameter	Symbol	-40°C			25°C			80°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output High Voltage*	V _{OH}	1.415	1.520	1.620	1.475	1.550	1.620	1.475	1.55	1.620	V
Output Low Voltage*	V _{OL}	0.670	0.810	0.945	0.690	0.785	0.880	0.690	0.785	0.880	V
Input High Voltage	V _{IH}	1.275		1.620	1.335		1.620	1.335		1.620	V
Input Low Voltage	V _{IL}	0.670		1.090	0.690		1.025	0.690		1.025	V
Input High Voltage Common Mode Range†	V _{CMR}	1.2		2.5	1.2		2.5	1.2		2.5	V
Input High Current	CLK-IN0, CLK-IN1 CLK-IN0B, CLK-IN1B	I _{IH}		60			60			60	μA
Input Low Current		I _{IL}	-60		-60			-60			μA

Input and output parameters vary 1:1 with V_{CC} when V_{CC} varies ±5%.

* Outputs terminated with 50Ω to V_{CCO} – 2V.

** Common mode voltage is defined as V_{IH}

† For single-ended applications, the maximum input voltage for CLK-IN_x, CLK-IN_xB is V_{CC} + 0.3V

AC Electrical Characteristics

V_{CC} = -3.8V to -2.375V or, V_{CC} = 2.375V to 3.8V; V_{EE} = 0V, T_A = -40°C to 85°C

Parameter		Symbol	-40°C			25°C			80°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Frequency		f _{MAX}			700			700			700	MHz
Propagation Delay*		t _{PD}	600	680	750	650	725	790	690	790	890	ps
Output Skew ** †		tsk(o)		25	37		25	37		25	37	ps
Part-to-Part Skew *** †		tsk(pp)		85	225		85	225		85	225	ps
Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		t _{APJ}		0.10			0.10			0.10		ps
Peak-to-Peak Input Voltage (Differential Configuration)		V _{PP}	150	800	1200	150	800	1200	150	800	1200	mV
Output Rise/Fall Time	20%to80%	t _R / t _F	200		700	200		700	200		700	ps

All parameters are measured at f ≤ 700MHz, unless otherwise noted.

* Measured from the differential input crossing point to the differential output crossing point.

** Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

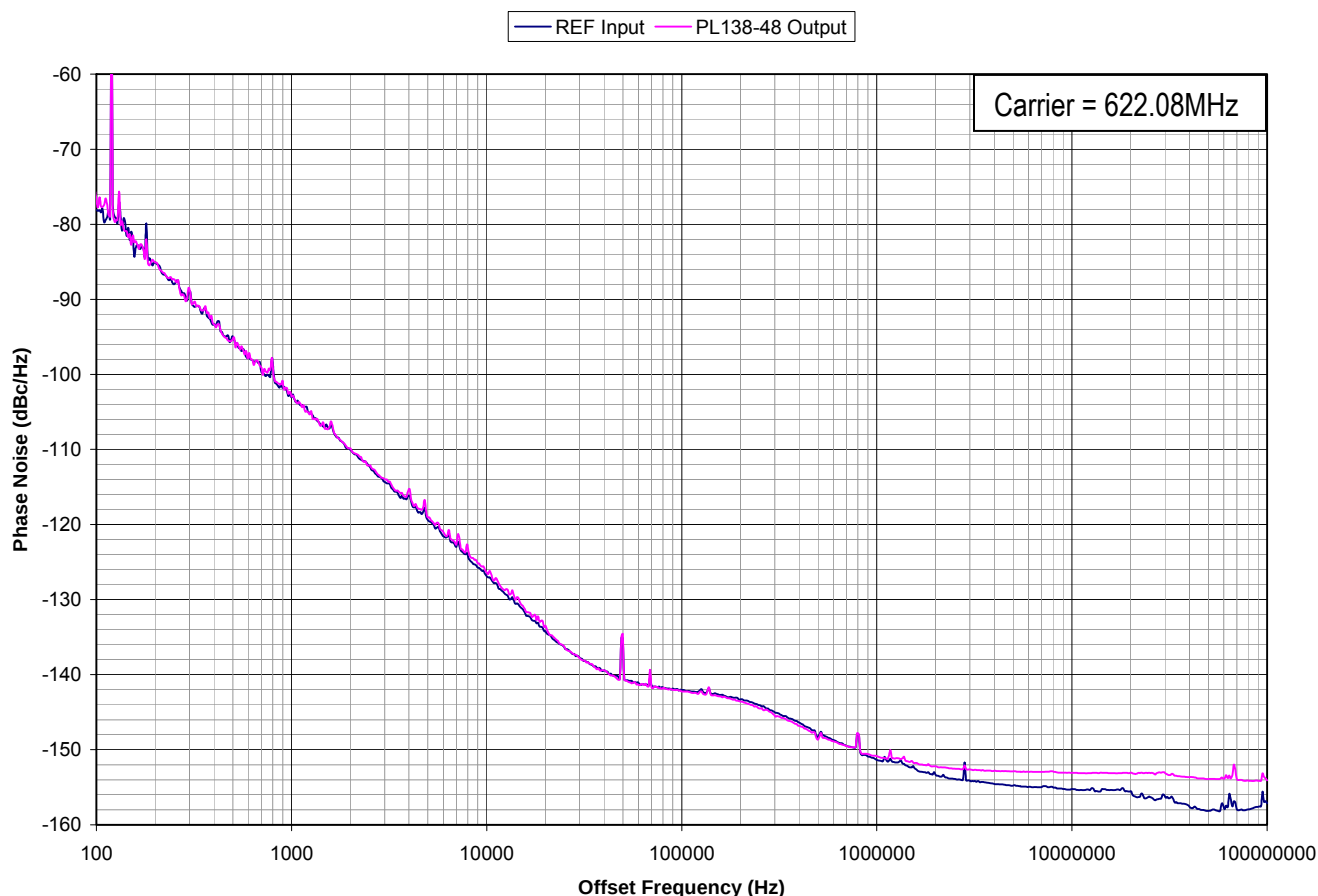
*** Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

† This parameter is defined in accordance with JEDEC Standard 65.

2.5V-3.3V Low-Skew 1-4 Differential PECL Fanout Buffer

NOISE CHARACTERISTICS (Commercial and Industrial Temperature Devices)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
t _{APJ}	Additive Phase Jitter	V _{DD} = 3.3V, Frequency = 622.08MHz Offset = 12KHz ~ 20MHz		20	40	fs
		V _{DD} = 3.3V, Frequency = 156.25MHz Offset = 12KHz ~ 20MHz		50	100	fs
		V _{DD} = 3.3V, Frequency = 50MHz Offset = 1KHz ~ 1MHz		50	100	fs
		V _{DD} = 3.3V, Frequency = 25MHz Offset = 1KHz ~ 1MHz		50	100	fs



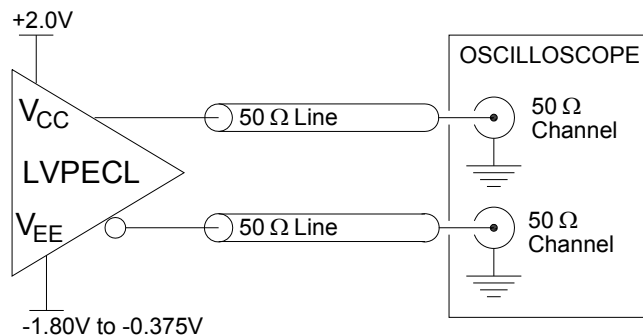
When a buffer is used to pass a signal then the buffer will add a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. To quantify the noise addition in the buffer we compare the Phase Jitter numbers from the input and the output. The difference is called "Additive Phase Jitter". The formula for the Additive Phase Jitter is as follows:

$$\text{Additive Phase Jitter} = \sqrt{(\text{Output Phase Jitter})^2 - (\text{Input Phase Jitter})^2}$$

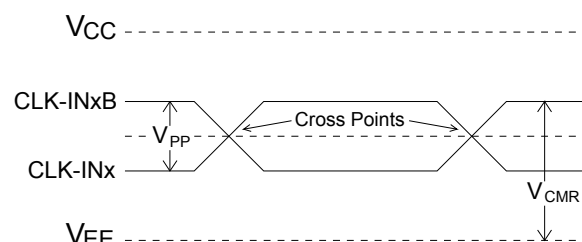
2.5V-3.3V Low-Skew 1-4 Differential PECL Fanout Buffer

PARAMETER MEASUREMENT INFORMATION

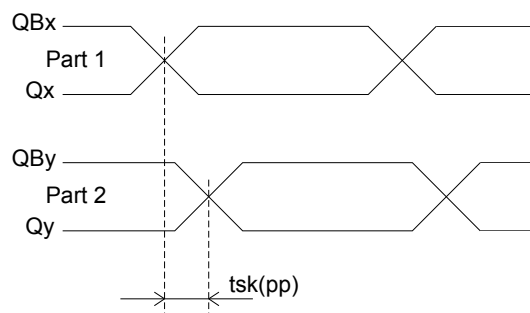
Output Waveform Test Circuit:



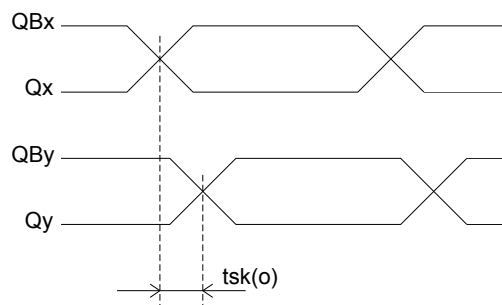
Differential Input Level:



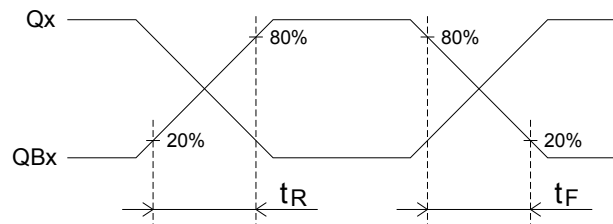
Part-to-Part Skew:



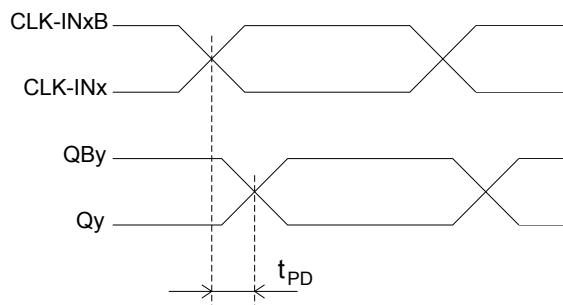
Output Skew:



Output Rise/Fall Time:



Propagation Delay:

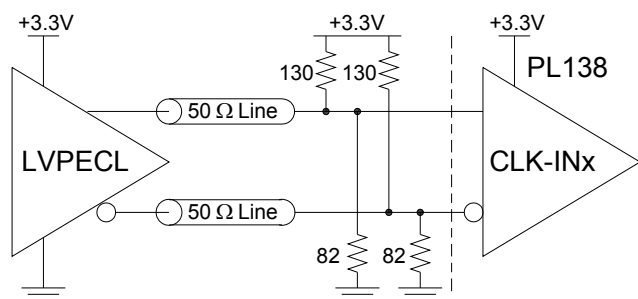


2.5V-3.3V Low-Skew 1-4 Differential PECL Fanout Buffer

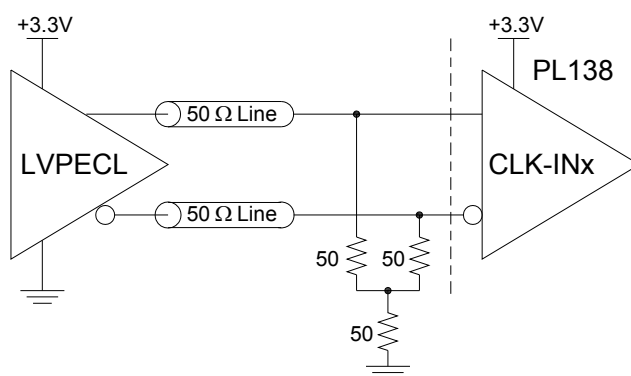
APPLICATION INFORMATION

The following circuits show different configurations for different input logic type signals. For good signal integrity at the PL138 input, the signals need to be properly terminated according to the logic type requirements. The signals need to be presented at the PL138 input according to V_{CMR} , V_{PP} and other input requirements.

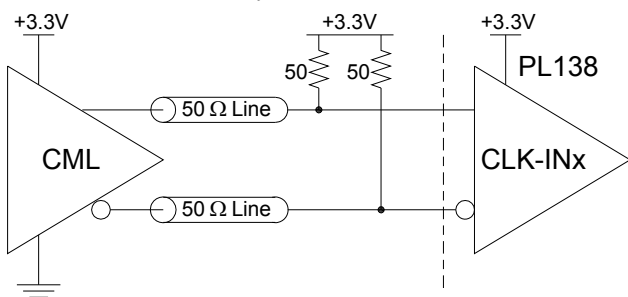
CLK-IN Input Driven by a 3.3V LVPECL Driver:



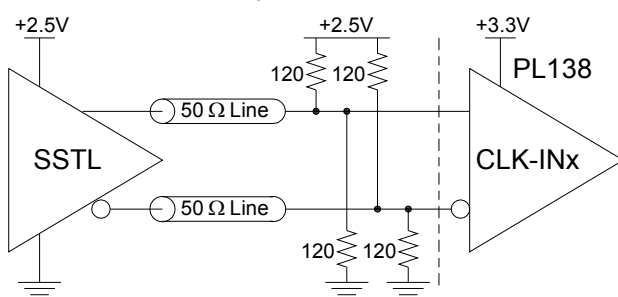
3.3V LVPECL Driver, Alternative Termination:



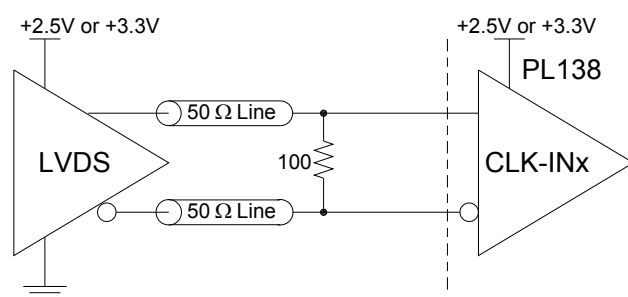
CLK-IN Input Driven by a CML Driver:



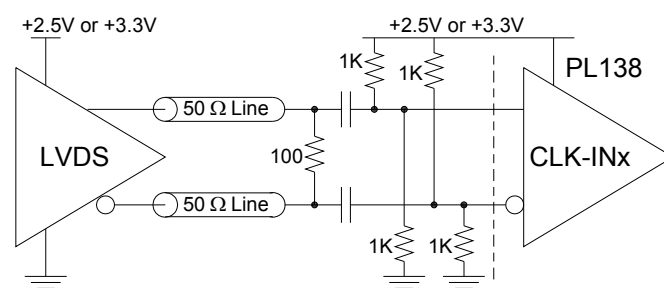
CLK-IN Input Driven by an SSTL Driver:



CLK-IN Input Driven by an LVDS Driver:



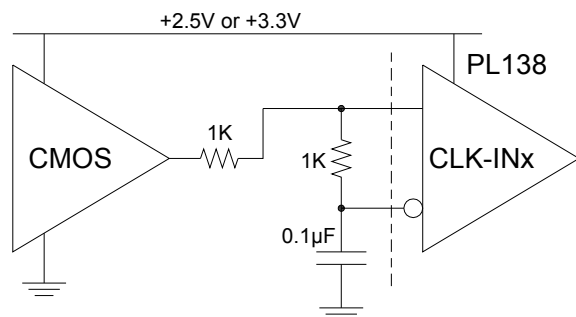
LVDS Driver, Alternative AC Coupling:



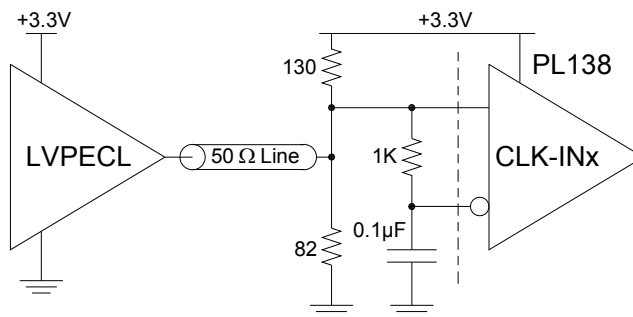
This circuit is for compatibility only. AC coupling is not really required for LVDS. The V_{CMR} range of the PL138 reaches low enough that LVDS signals can be connected directly to the PL138 input like in the circuit to the left.

2.5V-3.3V Low-Skew 1-4 Differential PECL Fanout Buffer

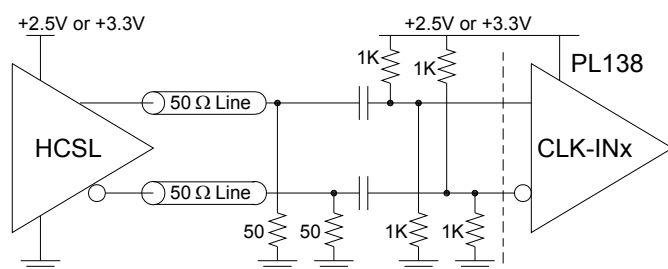
CLK-IN Input Driven by a CMOS Driver:



CLK-IN Input Driven by Single Ended LVPECL:



CLK-IN Input Driven by an HCSL Driver:

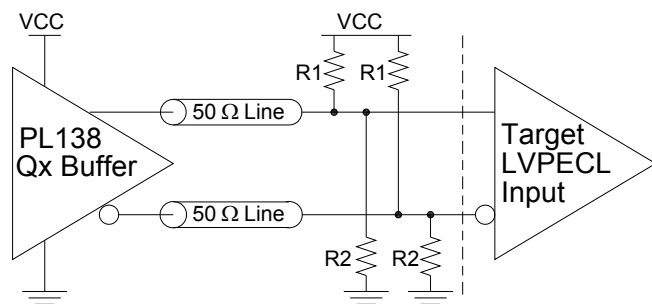


HCSL presents its signals very close to the ground rail, below the V_{CMR} range, so the HCSL signals can not be connected to the PL138 input directly. AC coupling is required for HCSL signals on the PL138 input.

TERMINATION FOR LVPECL OUTPUTS

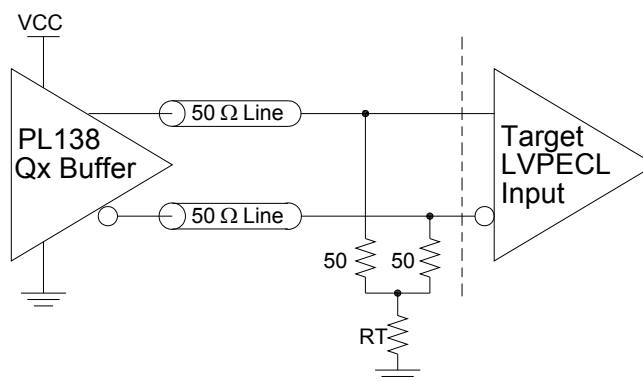
The required termination for LVPECL is 50Ω to a $V_{CC}-2V$ DC voltage level. Below are two schematics to implement this termination.

LVPECL Termination Schematic #1:



VCC=3.3V, Ideal values: $R1=127\Omega$, $R2=82.5\Omega$
 Commercial values (E24): $R1=130\Omega$, $R2=82\Omega$
 VCC=2.5V, Ideal values: $R1=250\Omega$, $R2=62.5\Omega$
 Commercial values (E24): $R1=240\Omega$, $R2=62\Omega$

LVPECL Termination Schematic #2:



Schematic #2 is an alternative simplified termination.
 VCC=3.3V, Ideal value: $RT=48.7\Omega$
 Commercial value: $RT=50\Omega$ (E24: 51Ω)
 VCC=2.5V, Ideal value: $RT=18.7\Omega$
 Commercial value: $RT=18\Omega$

2.5V-3.3V Low-Skew 1-4 Differential PECL Fanout Buffer

POWER CONSIDERATIONS

Driving LVPECL outputs requires an amount of power that can warm up the chip significantly.

The general requirement for the chip is that the junction temperature should not exceed +110°C.

The power consumption can be divided into two parts:

- 1) Core power dissipation
- 2) Output buffers power dissipation

CORE POWER DISSIPATION

The chip core power is equal to $VCC \times IEE$. With a worst case VCC and IEE the power dissipation in the core is $3.63V \times 45mA = 163mW$.

OUTPUT BUFFER POWER DISSIPATION

The output buffers are not exposed to the full VCC-VEE voltage. On the differential output, one line is at logic 1 with a small voltage across the buffer and a large output current. The other line is at logic 0 with a larger voltage across the buffer and a smaller output current. The power dissipation per output buffer is 32mW. Only buffers that are loaded will have power dissipation. With all 4 buffers loaded the worst case output buffer power dissipation will be 128mW.

Total Chip Power Dissipation, worst case, is $163mW + 128mW = 291mW$.

JUNCTION TEMPERATURE

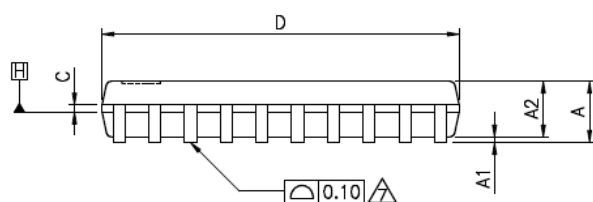
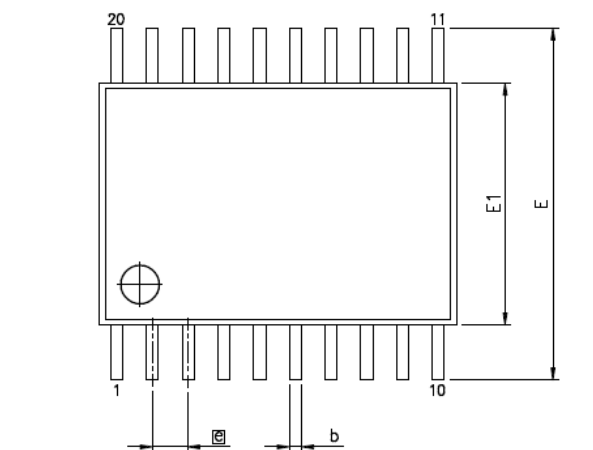
How much the chip is warmed up from the power dissipation depends upon the thermal resistance from the chip to the environment, also known as "junction to ambient". The thermal resistance depends upon the type of package, how the package is assembled to the PCB and if there is additional air flow for improved cooling. For the TSSOP package the thermal resistance is as follows:

TSSOP 20-pin Package	Air Flow Velocity in Linear Feet per Minute		
	0	200	500
JEDEC Standard Multi Layer PCB	$\theta_{JA} = 73^{\circ}C/W$	$\theta_{JA} = 67^{\circ}C/W$	$\theta_{JA} = 64^{\circ}C/W$

The temperature of the chip (junction) will be higher than the environment (ambient) with an amount equal to $\theta_{JA} \times \text{Power}$. For an ambient temperature of +85°C, all outputs loaded and no air flow, the junction temperature $T_J = 85^{\circ}C + 73 \times 0.291 = 106^{\circ}C$.

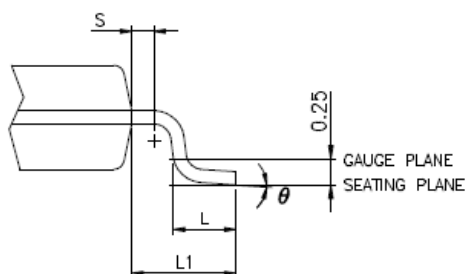
PACKAGE DRAWING (GREEN PACKAGE COMPLIANT)

TSSOP173 20L



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	0.90	1.05
b	0.19	—	0.30
C	0.09	—	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	—	—
θ	0°	—	8°



NOTES:

- JEDEC OUTLINE :
STANDARD : MO-153 AC REV.F
THERMALLY ENHANCED : MO-153 ACT REV.F
- DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
- DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
- DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
- DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE .

2.5V-3.3V Low-Skew 1-4 Differential PECL Fanout Buffer**ORDERING INFORMATION (GREEN PACKAGE)**

For part ordering, please contact our Sales Department:

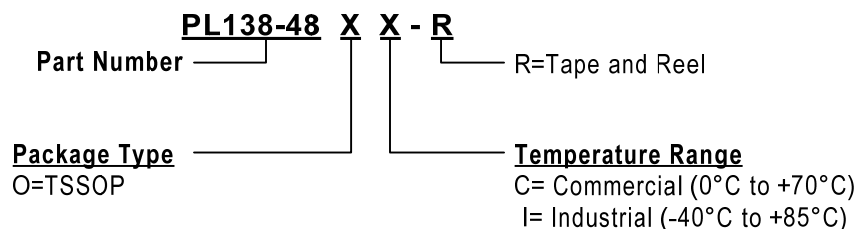
2880 Zanker Road, San Jose, CA 95134 USA

Tel (408) 571-1668 Fax (408) 571-1688

PART NUMBER

The order number for this device is a combination of the following:

Part number, Package type and Operating temperature range



Part/Order Number	Marking	Package Option
PL138-48OC	P138-48 OC LLLLL	20-Pin TSSOP (Tube)

*Note: LLLLL designates lot number

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Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf

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