

PM50CLB060

FLAT-BASE TYPE
INSULATED PACKAGE

PM50CLB060



FEATURE

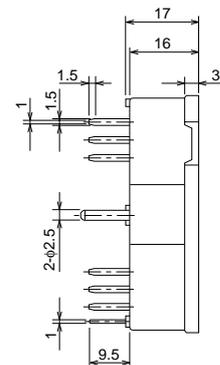
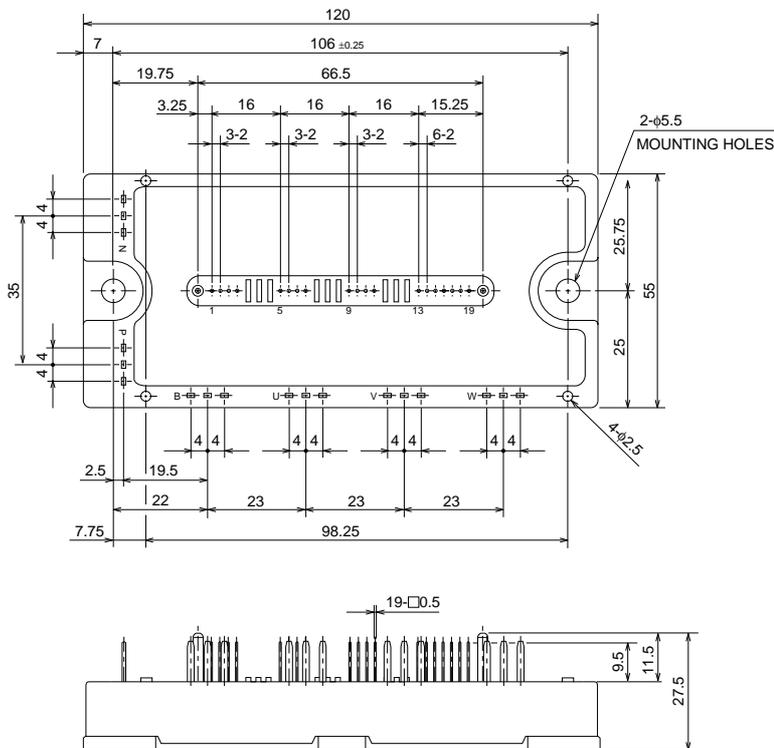
- a) Adopting new 5th generation IGBT (CSTBT) chip, which performance is improved by 1 μ m fine rule process.
For example, typical $V_{ce(sat)}=1.5V$ @ $T_J=125^\circ C$
- b) I adopt the over-temperature conservation by T_J detection of CSTBT chip, and error output is possible from all each conservation upper and lower arm of IPM.
- c) New small package
Reduce the package size by 32%, thickness by 22% from S-DASH series.
 - 3 ϕ 50A, 600V Current-sense IGBT type inverter
 - Monolithic gate drive & protection logic
 - Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage (P-Fo available from upper arm devices)
 - Acoustic noise-less 3.7kW class inverter application

APPLICATION

General purpose inverter, servo drives and other motor controls

PACKAGE OUTLINES

Dimensions in mm

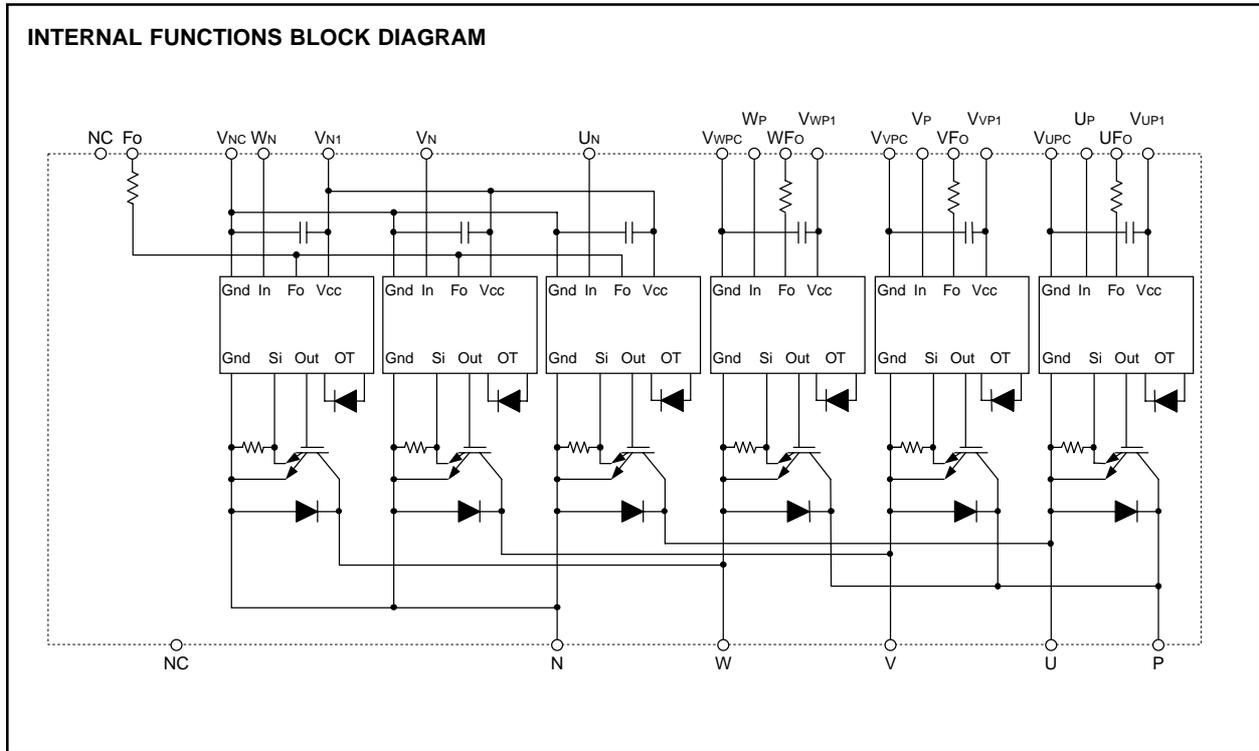


Terminal code

- | | |
|---------|----------|
| 1. VUPC | 11. WP |
| 2. UFO | 12. VWP1 |
| 3. UP | 13. VNC |
| 4. VUP1 | 14. VN1 |
| 5. VVPC | 15. NC |
| 6. VFO | 16. UN |
| 7. VP | 17. VN |
| 8. VVP1 | 18. WN |
| 9. VWPC | 19. Fo |
| 10. WFO | |

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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

| Symbol | Parameter | Condition | Ratings | Unit |
|--------------|---------------------------|---|------------|------------------|
| V_{CES} | Collector-Emitter Voltage | $V_D = 15\text{V}$, $V_{CIN} = 15\text{V}$ | 600 | V |
| $\pm I_C$ | Collector Current | $T_C = 25^\circ\text{C}$ | 50 | A |
| $\pm I_{CP}$ | Collector Current (Peak) | $T_C = 25^\circ\text{C}$ | 100 | A |
| P_C | Collector Dissipation | $T_C = 25^\circ\text{C}$ (Note-1) | 101 | W |
| T_j | Junction Temperature | | -20 ~ +150 | $^\circ\text{C}$ |

CONTROL PART

| Symbol | Parameter | Condition | Ratings | Unit |
|-----------|-----------------------------|---|---------|------|
| V_D | Supply Voltage | Applied between : $V_{UP1}-V_{UPC}$ $V_{VP1}-V_{VPC}$, $V_{WP1}-V_{WPC}$, $V_{N1}-V_{NC}$ | 20 | V |
| V_{CIN} | Input Voltage | Applied between : U_P-V_{UPC} , V_P-V_{VPC} W_P-V_{WPC} , $U_N \cdot V_N \cdot W_N-V_{NC}$ | 20 | V |
| V_{FO} | Fault Output Supply Voltage | Applied between : $U_{FO}-V_{UPC}$, $V_{FO}-V_{VPC}$, $W_{FO}-V_{WPC}$ F_O-V_{NC} | 20 | V |
| I_{FO} | Fault Output Current | Sink current at U_{FO} , V_{FO} , W_{FO} , F_O terminals | 20 | mA |

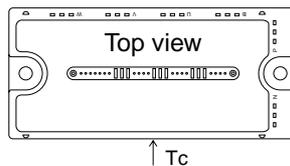
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TOTAL SYSTEM

| Symbol | Parameter | Condition | Ratings | Unit |
|------------------|-----------------------------------|--|------------|------------------|
| VCC(PROT) | Supply Voltage Protected by SC | V _D = 13.5 ~ 16.5V, Inverter Part, T _j = +125°C Start | 400 | V |
| VCC(surge) | Supply Voltage (Surge) | Applied between : P-N, Surge value | 500 | V |
| T _c | Module Case Operating Temperature | (Note-1) | -20 ~ +100 | °C |
| T _{stg} | Storage Temperature | | -40 ~ +125 | °C |
| V _{iso} | Isolation Voltage | 60Hz, Sinusoidal, Charged part to Base, AC 1 min. | 2500 | V _{rms} |

(Note-1) T_c (base plate) measurement point is below.



THERMAL RESISTANCES

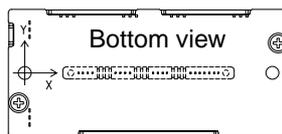
| Symbol | Parameter | Condition | Limits | | | Unit |
|-----------------------|--------------------------------------|--|--------|------|-------|------|
| | | | Min. | Typ. | Max. | |
| R _{th(j-c)Q} | Junction to case Thermal Resistances | Inverter IGBT part (per 1/6) (Note-2) | — | — | 0.95* | °C/W |
| R _{th(j-c)F} | | Inverter FWDi part (per 1/6) (Note-2) | — | — | 1.61* | |
| R _{th(j-c)Q} | | Inverter IGBT part (per 1/6) (Note-1) | — | — | 1.24 | |
| R _{th(j-c)F} | | Inverter FWDi part (per 1/6) (Note-1) | — | — | 2.09 | |
| R _{th(c-f)} | Contact Thermal Resistance | Case to fin, (per 1 module) Thermal grease applied (Note-1) | — | — | 0.038 | |

* If you use this value, R_{th(f-a)} should be measured just under the chips.

(Note-2) T_c (under the chip) measurement point is below.

(unit : mm)

| axis | arm | | VP | | WP | | UN | | VN | | WN | |
|------|------|------|------|------|------|------|------|------|------|------|------|------|
| | IGBT | FWDi |
| X | 29.0 | 29.5 | 64.6 | 65.1 | 85.9 | 86.4 | 38.1 | 37.6 | 54.8 | 55.3 | 76.1 | 75.6 |
| Y | -7.3 | 1.6 | -7.3 | 2.1 | -7.3 | 2.1 | 5.3 | -4.6 | 5.3 | -4.6 | 5.3 | -4.6 |



ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

| Symbol | Parameter | Condition | Limits | | | Unit | |
|----------------------|--------------------------------------|--|------------------------|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| V _{CE(sat)} | Collector-Emitter Saturation Voltage | V _D = 15V, I _C = 50A V _{CIN} = 0V, Pulsed (Fig. 1) | T _j = 25°C | — | 1.6 | 2.1 | V |
| | | | T _j = 125°C | — | 1.5 | 2.0 | |
| V _{EC} | FWDi Forward Voltage | -I _C = 50A, V _D = 15V, V _{CIN} = 15V (Fig. 2) | — | 2.2 | 3.3 | V | |
| t _{on} | Switching Time | V _D = 15V, V _{CIN} = 0V ↔ 15V V _{CC} = 300V, I _C = 50A T _j = 125°C Inductive Load (Fig. 3,4) | 0.5 | 1.0 | 2.4 | μs | |
| t _{rr} | | | — | 0.2 | 0.4 | | |
| t _{c(on)} | | | — | 0.4 | 1.0 | | |
| t _{off} | | | — | 1.2 | 2.5 | | |
| t _{c(off)} | | | — | 0.5 | 1.0 | | |
| I _{CES} | Collector-Emitter Cutoff Current | V _{CE} = V _{CE(s)} , V _{CIN} = 15V (Fig. 5) | T _j = 25°C | — | — | 1 | mA |
| | | | T _j = 125°C | — | — | 10 | |

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CONTROL PART

| Symbol | Parameter | Condition | Limits | | | Unit | |
|----------------------|---|---|-------------|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| Id | Circuit Current | V _D = 15V, V _{CIN} = 15V | VN1-VNC | — | 15 | 25 | mA |
| | | | VXP1-VXPC | — | 5 | 10 | |
| V _{th(ON)} | Input ON Threshold Voltage | Applied between : UP-VU _{PC} , VP-VV _{PC} , WP-VW _{PC} UN • VN • WN-VNC | 1.2 | 1.5 | 1.8 | V | |
| V _{th(OFF)} | Input OFF Threshold Voltage | | 1.7 | 2.0 | 2.3 | | |
| SC | Short Circuit Trip Level | -20 ≤ T _j ≤ 125°C, V _D = 15V (Fig. 3,6) | 100 | — | — | A | |
| t _{off(SC)} | Short Circuit Current Delay Time | V _D = 15V (Fig. 3,6) | — | 0.2 | — | μs | |
| OT | Over Temperature Protection | V _D = 15V Detect T _j of IGBT chip | Trip level | 135 | 145 | — | °C |
| | | | Reset level | — | 125 | — | |
| UV | Supply Circuit Under-Voltage Protection | -20 ≤ T _j ≤ 125°C | Trip level | 11.5 | 12.0 | 12.5 | V |
| | | | Reset level | — | 12.5 | — | |
| I _{FO(H)} | Fault Output Current | V _D = 15V, V _{FO} = 15V (Note-3) | — | — | 0.01 | mA | |
| I _{FO(L)} | | | — | 10 | 15 | | |
| t _{FO} | Minimum Fault Output Pulse Width | V _D = 15V (Note-3) | 1.0 | 1.8 | — | ms | |

(Note-3) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

MECHANICAL RATINGS AND CHARACTERISTICS

| Symbol | Parameter | Condition | Limits | | | Unit |
|--------|-----------------|--------------------------|--------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| — | Mounting torque | Mounting part screw : M5 | 2.5 | 3.0 | 3.5 | N • m |
| — | Weight | — | — | 340 | — | g |

RECOMMENDED CONDITIONS FOR USE

| Symbol | Parameter | Condition | Recommended value | Unit |
|-----------------------|---------------------------------|---|-------------------|------|
| V _{CC} | Supply Voltage | Applied across P-N terminals | ≤ 400 | V |
| V _D | Control Supply Voltage | Applied between : VUP1-VU _{PC} , VVP1-VV _{PC} VWP1-VW _{PC} , VN1-VNC (Note-4) | 15 ± 1.5 | V |
| V _{CIN(ON)} | Input ON Voltage | Applied between : UP-VU _{PC} , VP-VV _{PC} , WP-VW _{PC} UN • VN • WN-VNC | ≤ 0.8 | V |
| V _{CIN(OFF)} | Input OFF Voltage | | ≥ 9.0 | |
| f _{PWM} | PWM Input Frequency | Using Application Circuit of Fig. 8 | ≤ 20 | kHz |
| t _{dead} | Arm Shoot-through Blocking Time | For IPM's each input signals (Fig. 7) | ≥ 2.0 | μs |

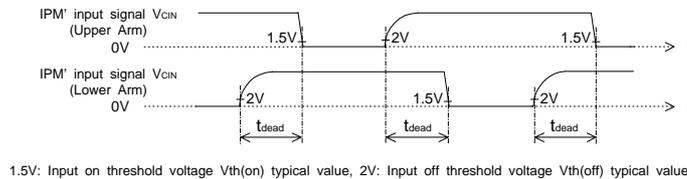
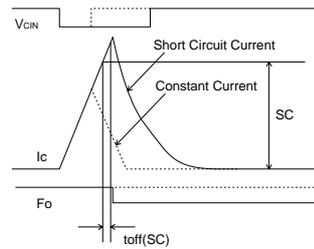
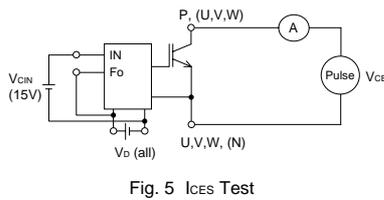
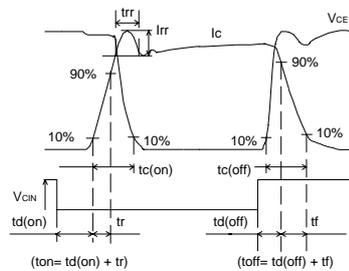
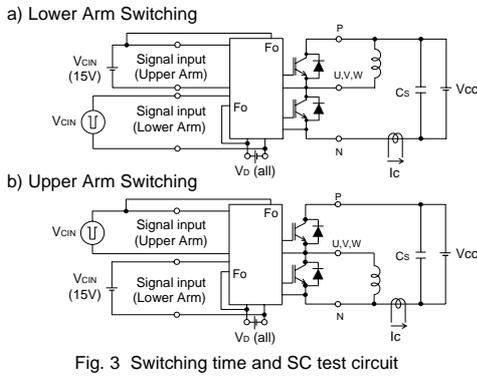
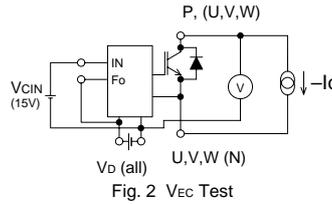
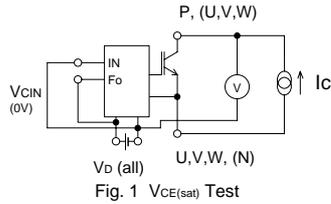
(Note-4) With ripple satisfying the following conditions dv/dt swing ≤ ±5V/μs, Variation ≤ 2V peak to peak

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PRECAUTIONS FOR TESTING

1. Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
After this, the specified ON and OFF level setting for each input signal should be done.
2. When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)



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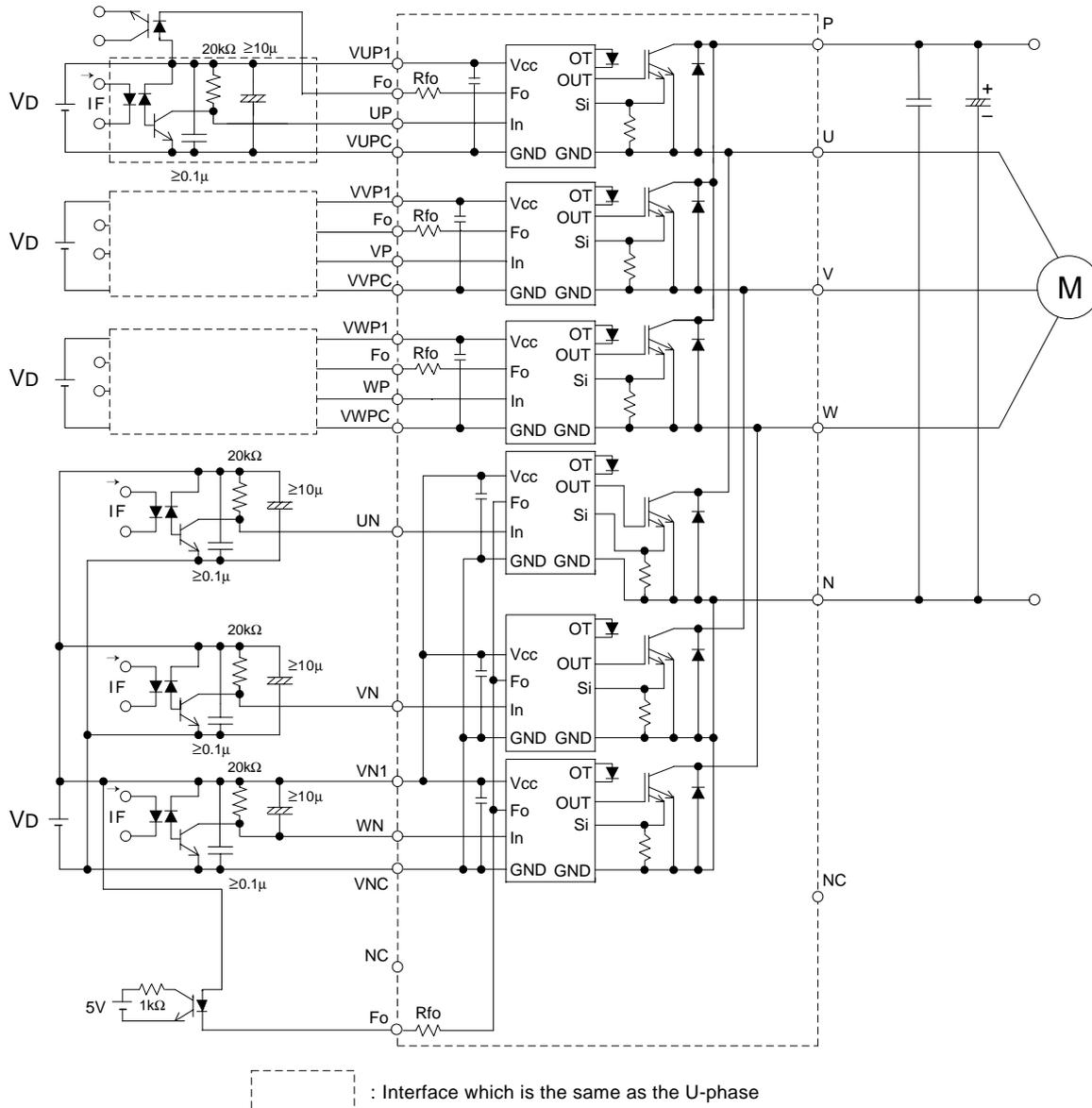


Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: $t_{PLH}, t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 4 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.