

PMGD8000LN

Dual μ TrenchMOS™ logic level FET

Rev. 01 — 27 February 2003

Product data

1. Description

Dual N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PMGD8000LN in SOT363 (SC-88).

2. Features

- TrenchMOS™ technology
- Very fast switching
- Logic level compatible
- Subminiature surface mount package.

3. Applications

- Battery management
- High-speed switch
- Low power DC-to-DC converter.

4. Pinning information

Table 1: Pinning - SOT363 (SC-88), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	source (s1)	<p>Top view MSA370</p>	<p style="text-align: right;">MSD901</p>
2	gate (g1)		
3	drain (d2)		
4	source (s2)		
5	gate (g2)		
6	drain (d1)		

SOT363 (SC-88)



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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
I_D	drain current (DC)	$T_{amb} = 25\text{ °C}; V_{GS} = 4\text{ V}$	-	125	mA
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	-	0.2	W
T_j	junction temperature		-	150	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4\text{ V}; I_D = 10\text{ mA}$	1.8	8	Ω
		$V_{GS} = 2.5\text{ V}; I_D = 1\text{ mA}$	2.9	13	Ω

6. Limiting values

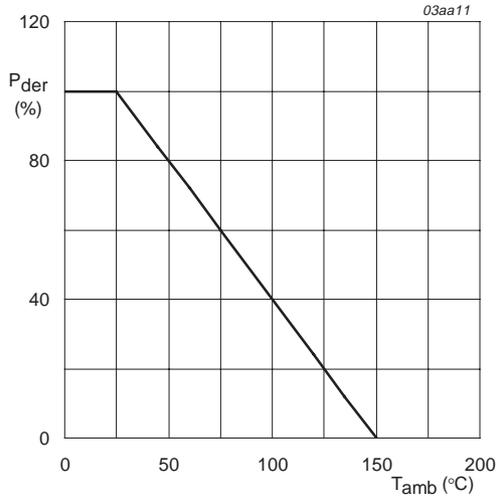
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage (DC)		-	± 15	V
I_D	drain current (DC)	$T_{amb} = 25\text{ °C}; V_{GS} = 4\text{ V};$ Figure 2 and 3	-	125	mA
		$T_{amb} = 70\text{ °C}; V_{GS} = 4\text{ V};$ Figure 2	-	100	mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	250	mA
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C};$ Figure 1	-	0.2	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C

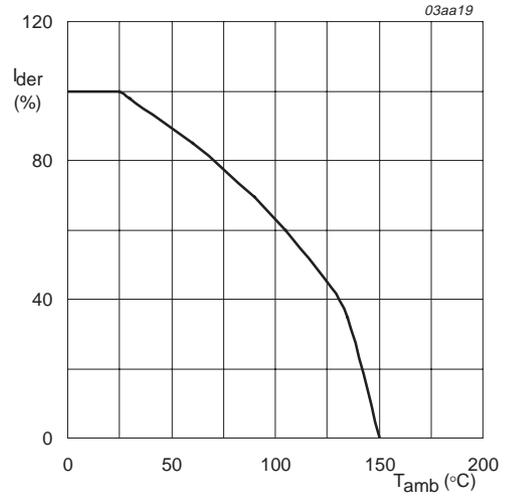
Source-drain diode

I_S	source (diode forward) current (DC)	$T_{amb} = 25\text{ °C}$	-	125	mA
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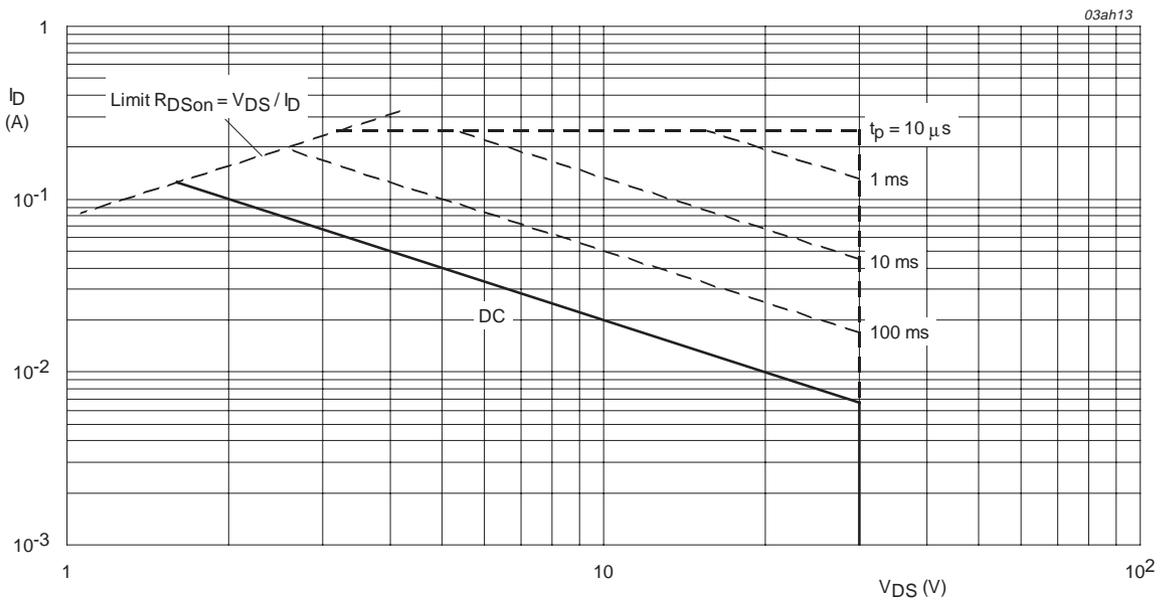
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of ambient temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature.



$T_{amb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 4 V$.

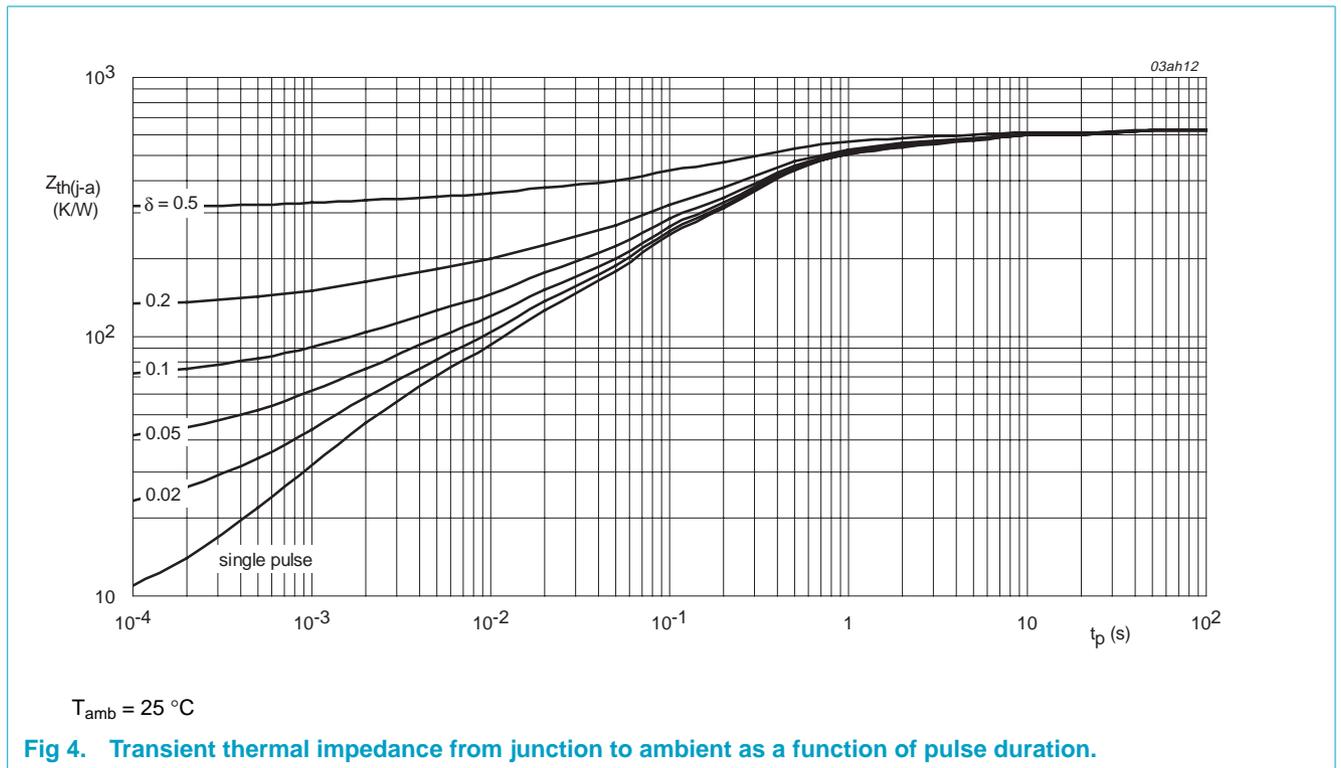
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a PCB; vertical in still air	-	-	625	K/W

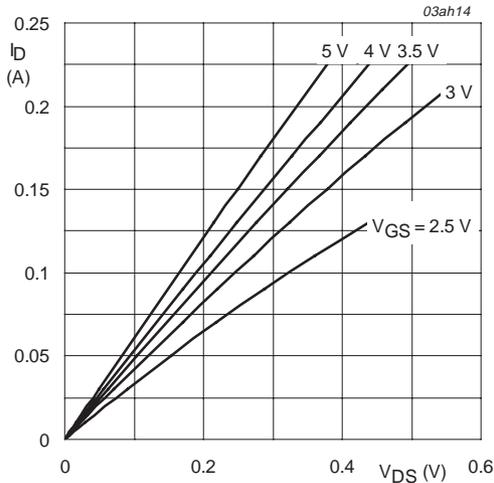
7.1 Transient thermal impedance



8. Characteristics

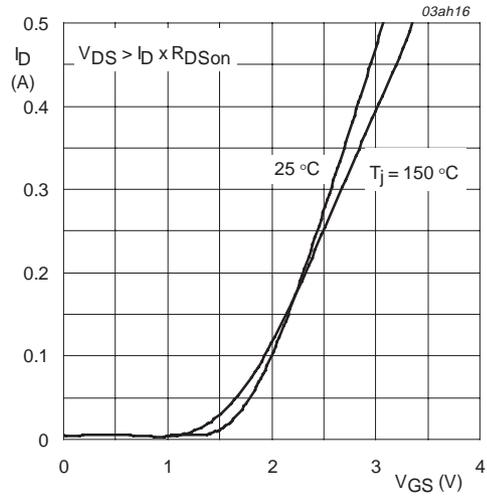
Table 5: Characteristics
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$	30	-	-	V	
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 100\text{ }\mu\text{A}$; $V_{DS} = V_{GS}$; Figure 9	0.8	-	1.5	V	
I_{DSS}	drain-source leakage current	$V_{DS} = 30\text{ V}$; $V_{GS} = 0\text{ V}$	$T_j = 25\text{ }^\circ\text{C}$	-	0.01	1.0	μA
			$T_j = 55\text{ }^\circ\text{C}$	-	-	10	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}$; $V_{DS} = 0\text{ V}$	-	10	100	nA	
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4\text{ V}$; $I_D = 10\text{ mA}$; Figure 7 and 8	$T_j = 25\text{ }^\circ\text{C}$	-	1.8	8	Ω
			$T_j = 150\text{ }^\circ\text{C}$	-	2.9	12.8	Ω
		$V_{GS} = 2.5\text{ V}$; $I_D = 1\text{ mA}$; Figure 7 and 8	$T_j = 25\text{ }^\circ\text{C}$	-	2.9	13	Ω
			$T_j = 150\text{ }^\circ\text{C}$	-	4.6	21	Ω
Dynamic characteristics							
$Q_{g(tot)}$	total gate charge	$V_{DD} = 10\text{ V}$; $V_{GS} = 4.5\text{ V}$; $I_D = 0.1\text{ A}$; Figure 13	-	350	-	pC	
Q_{gs}	gate-source charge		-	60	-	pC	
Q_{gd}	gate-drain (Miller) charge		-	120	-	pC	
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 5\text{ V}$; $f = 1\text{ MHz}$; Figure 11	-	18.5	-	pF	
C_{oss}	output capacitance		-	12.5	-	pF	
C_{rss}	reverse transfer capacitance		-	9	-	pF	
$t_{d(on)}$	turn-on delay time	$V_{DD} = 3\text{ V}$; $R_L = 100\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_G = 6\text{ }\Omega$	-	10	-	ns	
t_r	rise time		-	7	-	ns	
$t_{d(off)}$	turn-off delay time		-	15	-	ns	
t_f	fall time		-	7	-	ns	
Source-drain diode							
V_{SD}	source-drain (diode forward) voltage	$I_S = 0.1\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	-	0.77	1.35	V	



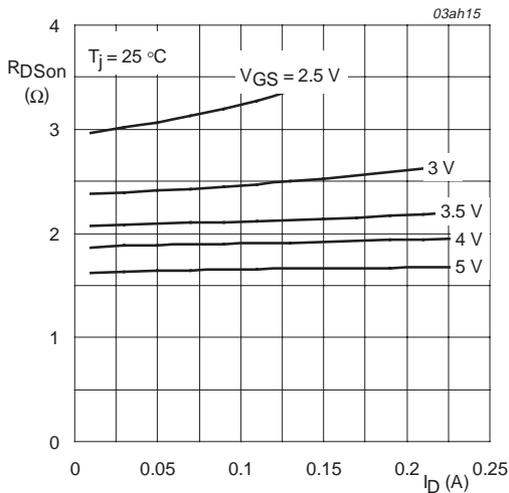
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



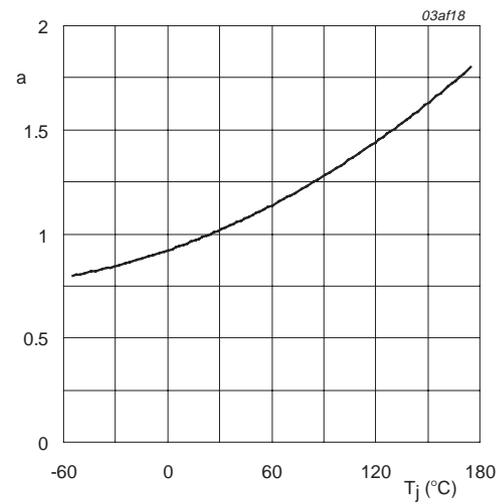
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



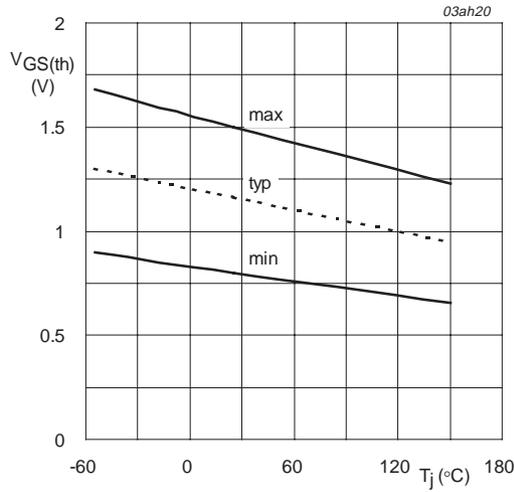
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



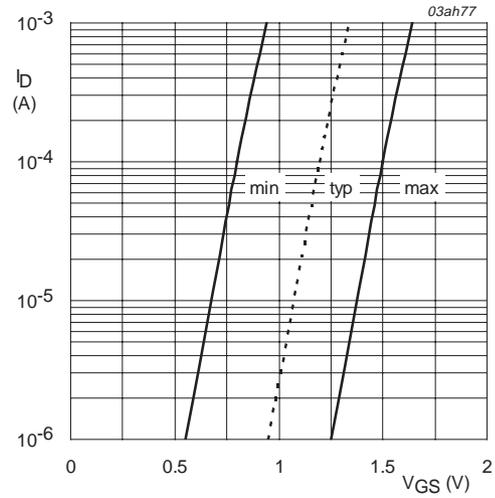
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



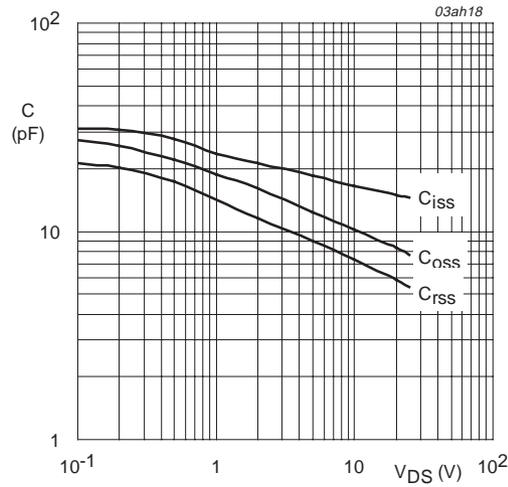
$I_D = 100 \mu A$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



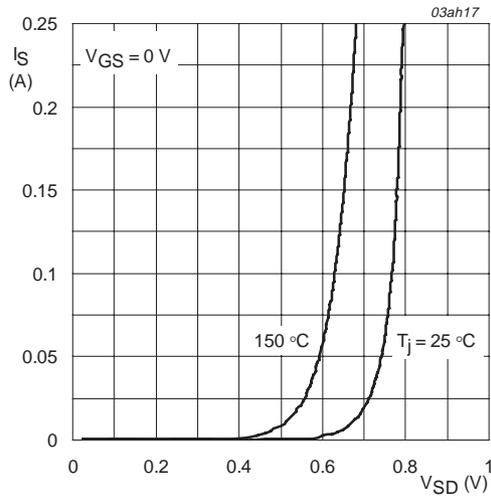
$T_j = 25 \text{ }^{\circ}C$; $V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



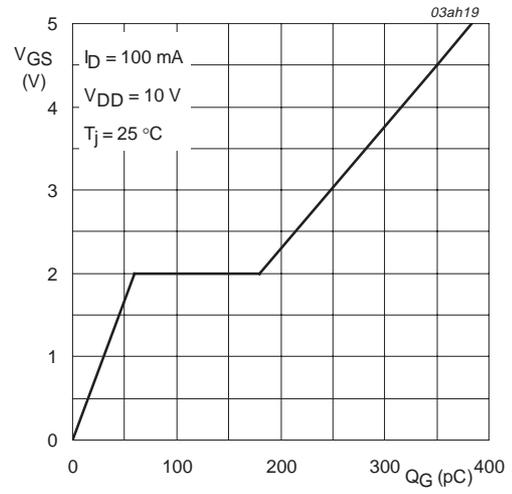
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 100\text{ mA}$; $V_{DD} = 10\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic surface mounted package; 6 leads

SOT363

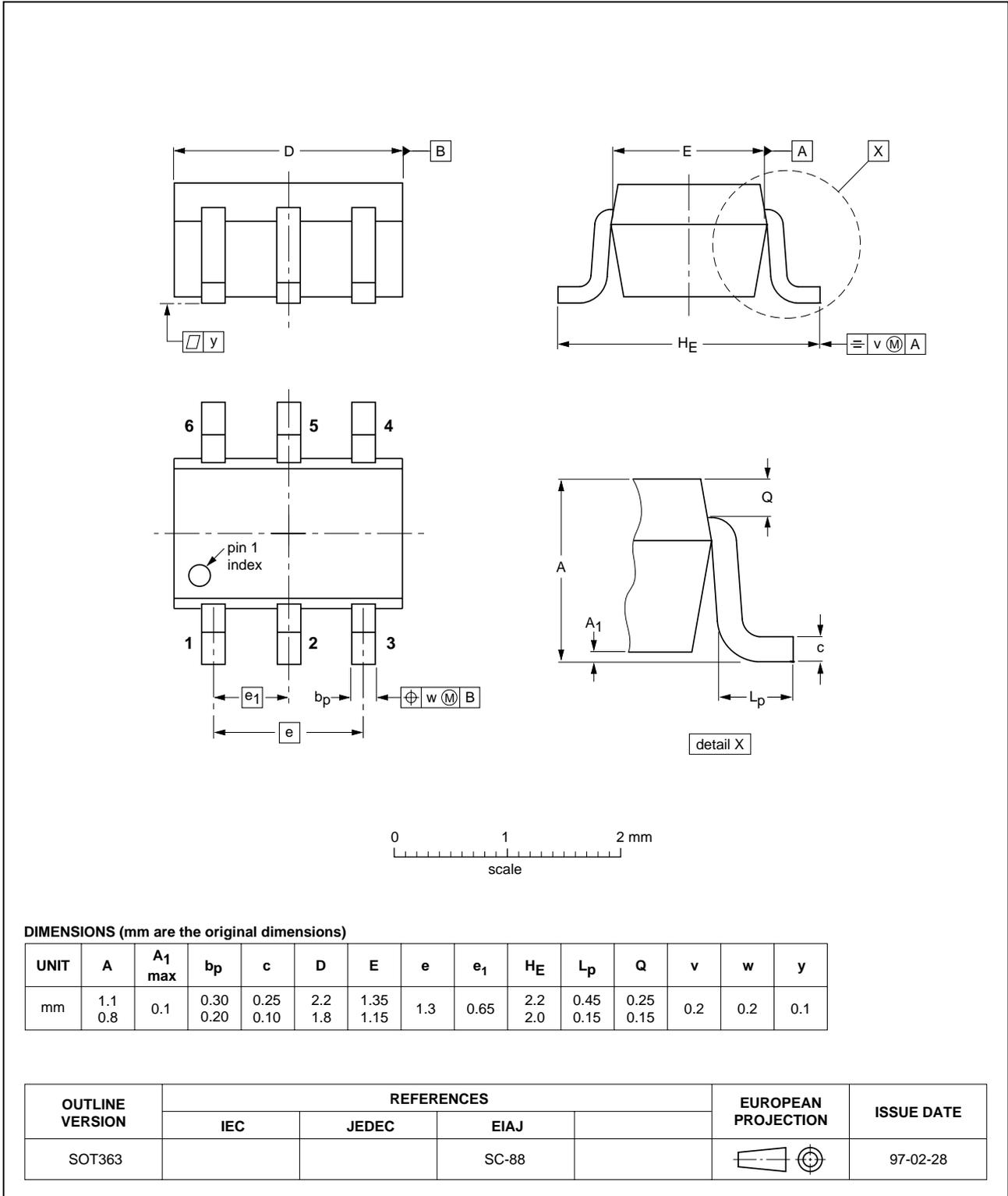


Fig 14. SOT363 (SC-88).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20030227	-	Product data (9397 750 10939)

11. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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