

Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.nxp.com, http://www.nexperia.com/, http://www.nexperia.com/, use http://www.nexperia.com/

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use salesaddresses@nexperia.com (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © Nexperia B.V. (year). All rights reserved.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

PMK35EP

P-channel TrenchMOS extremely low level FET

Rev. 02 — 29 April 2010

Product data sheet

1. Product profile

1.1 General description

Extremely low level P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

 Low conduction losses due to low on-state resistance

1.3 Applications

Battery management

Load switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 150 °C	-	-	-30	V
I _D	drain current	$T_{sp} = 25 ^{\circ}\text{C}; V_{GS} = -10 \text{V}; \text{see}$ Figure 1; see Figure 3	-	-	-14. 9	Α
P _{tot}	total power dissipation	T _{sp} = 25 °C; see <u>Figure 2</u>	-	-	6.9	W
Static char	racteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = -10 \text{ V}; I_D = -9.2 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 9}}{\text{ of } 100 \text{ m}}$	-	16	19	mΩ
Dynamic c	haracteristics					
Q _{GD}	gate-drain charge	$V_{GS} = -10 \text{ V}; I_D = -9.2 \text{ A};$ $V_{DS} = -15 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 11</u> ; see <u>Figure 12</u>	-	6	-	nC



P-channel TrenchMOS extremely low level FET

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source	8月月月5	D
3	S	source		
4	G	gate		G $+$ $+$ $+$ $+$ $+$ $+$ $+$ $+$ $+$ $+$
5	D	drain	1	
6	D	drain	SOT96-1 (SO8)	S 001aaa025
7	D	drain		
8	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMK35EP	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

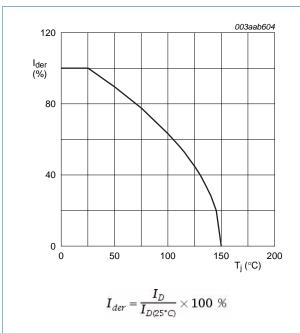
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 150 °C	-	-	-30	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	-	-30	V
V_{GS}	gate-source voltage		-25	-	25	V
I _D	drain current	$T_{sp} = 25 ^{\circ}\text{C}$; $V_{GS} = -10 \text{V}$; see <u>Figure 1</u> ; see <u>Figure 3</u>	-	-	-14.9	Α
		T_{sp} = 100 °C; V_{GS} = -10 V; see <u>Figure 1</u>	-	-	-7	Α
I _{DM}	peak drain current	T_{sp} = 25 °C; $t_p \le 10 \mu s$; pulsed; see Figure 3	-	-	-28.8	Α
P _{tot}	total power dissipation	T _{sp} = 25 °C; see <u>Figure 2</u>	-	-	6.9	W
T _{stg}	storage temperature		-55	-	150	°C
Tj	junction temperature		-55	-	150	°C
Source-dra	in diode					
Is	source current	$T_{sp} = 25 ^{\circ}C$	-	-	-5.8	Α
I _{SM}	peak source current	T_{sp} = 25 °C; $t_p \le 10 \mu s$; pulsed	-	-	-23	Α

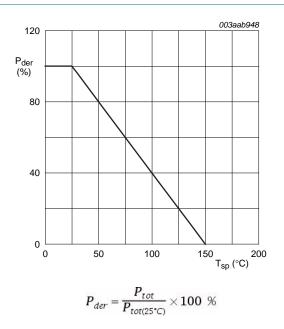
Product data sheet

PMK35EP **NXP Semiconductors**

P-channel TrenchMOS extremely low level FET



Normalized continuous drain current as a function of solder point temperature



Normalized total power dissipation as a function of solder point temperature

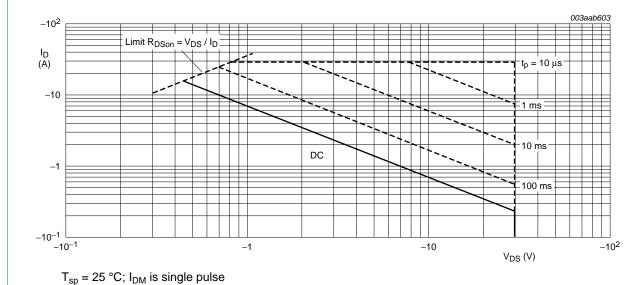


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

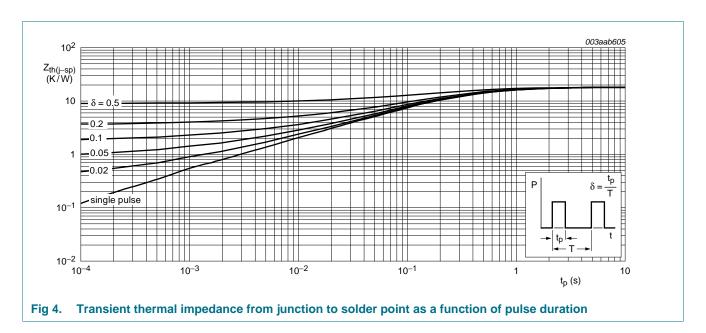
Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see <u>Figure 4</u>	-	-	18	K/W

PMK35EP **NXP Semiconductors**

P-channel TrenchMOS extremely low level FET



Characteristics 6.

Characteristics Table 6.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics					
V _{(BR)DSS}	drain-source	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 ^{\circ}C$	-30	-	-	V
	breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	-27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = -250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ °C}$; see <u>Figure 7</u> ; see <u>Figure 8</u>	-1	-	-3	V
		$I_D = -250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 150 ^{\circ}\text{C}$; see <u>Figure 8</u>	-0.7	-	-	V
		$I_D = -250 \mu A$; $V_{DS} = V_{GS}$; $T_j = -55 ^{\circ}C$; see <u>Figure 7</u> ; see <u>Figure 8</u>	-	-	-3.3	V
I _{DSS} drain leakage current	$V_{DS} = -30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-1	μΑ	
	$V_{DS} = -30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 70 \text{ °C}$	-	-	-10	μΑ	
I _{GSS} gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-100	nΑ	
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-100	nΑ
R_{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_{D} = -9.2 A; T_{j} = 25 °C; see <u>Figure 9</u>	-	16	19	mΩ
		V_{GS} = -10 V; I_{D} = -9.2 A; T_{j} = 150 °C; see <u>Figure 9</u>	-	25	31	mΩ
		V_{GS} = -4.5 V; I_D = -6.8 A; T_j = 25 °C; see <u>Figure 10</u> ; see <u>Figure 9</u>	-	26	35	mΩ
Dynamic ch	aracteristics					
Q _{G(tot)}	total gate charge	$I_D = -9.2 \text{ A}; V_{DS} = -15 \text{ V}; V_{GS} = -10 \text{ V};$	-	42	-	nC
Q_{GS}	gate-source charge	T _j = 25 °C; see <u>Figure 11</u> ; see <u>Figure 12</u>	-	8	-	nC
Q_{GD}	gate-drain charge		-	6	-	nC

P-channel TrenchMOS extremely low level FET

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{GS(pl)}$	gate-source plateau voltage	I_D = -9.2 A; V_{DS} = -15 V; T_j = 25 °C; see <u>Figure 11</u> ; see <u>Figure 12</u>	-	-2.5	-	V
C _{iss}	input capacitance	$V_{DS} = -25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	2100	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 13</u>	-	365	-	pF
C _{rss}	reverse transfer capacitance		-	275	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = -25 V; R_L = 6 Ω ; V_{GS} = -10 V;	-	9	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	9	-	ns
t _{d(off)}	turn-off delay time		-	50	-	ns
t _f	fall time		-	24	-	ns
Source-drain	n diode					
V_{SD}	source-drain voltage	$I_S = -3.45 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see Figure 14	-	-0.8	-1.2	V

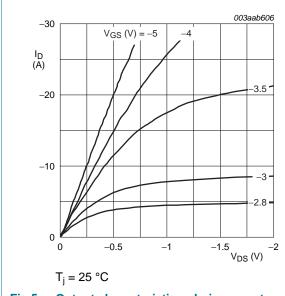


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

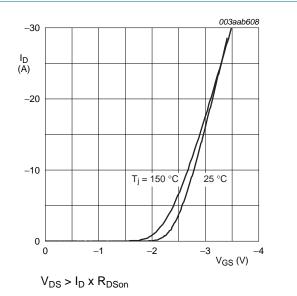


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

P-channel TrenchMOS extremely low level FET

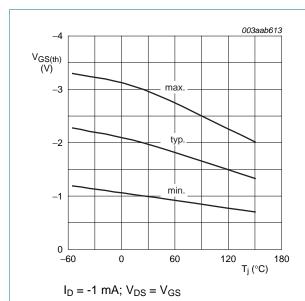
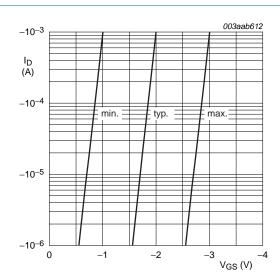


Fig 7. Gate-source threshold voltage as a function of junction temperature



 $T_j = 25$ °C; $V_{DS} = -5$ V

Fig 8. Sub-threshold drain current as a function of gate-source voltage

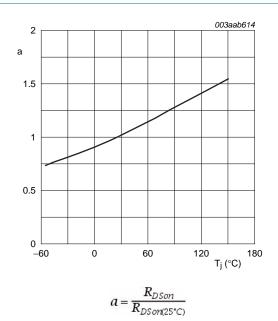


Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature

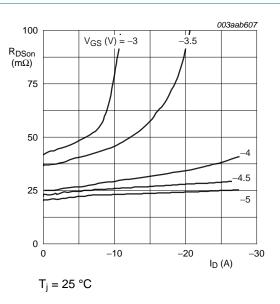


Fig 10. Drain-source on-state resistance as a function of drain current; typical values

P-channel TrenchMOS extremely low level FET

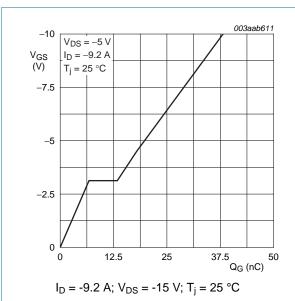


Fig 11. Gate-source voltage as a function of gate charge; typical values

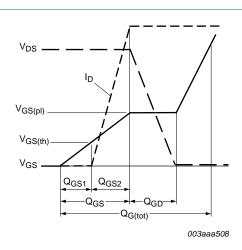


Fig 12. Gate charge waveform definitions

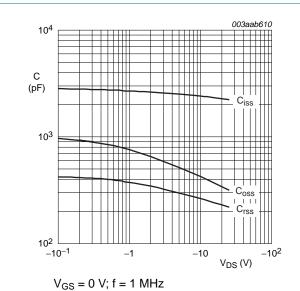


Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

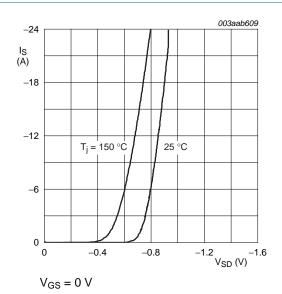


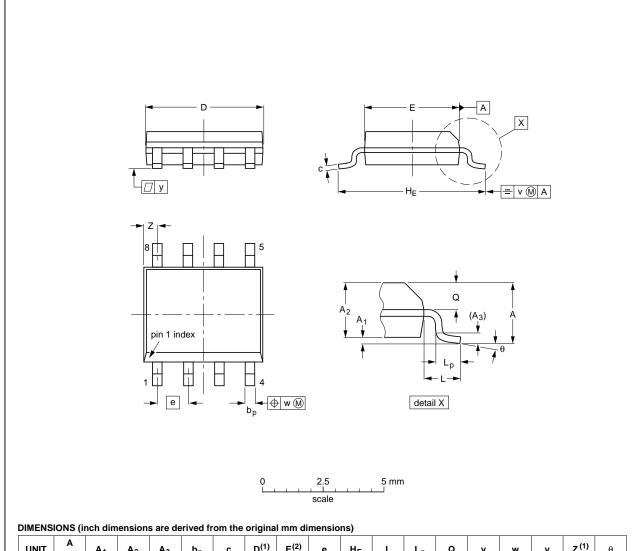
Fig 14. Source current as a function of source-drain voltage; typical values

P-channel TrenchMOS extremely low level FET

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	e	HE	٦	Lp	σ	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
- 2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT96-1	076E03	MS-012				99-12-27 03-02-18

Fig 15. Package outline SOT96-1 (SO8)

PMK35EP

P-channel TrenchMOS extremely low level FET

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMK35EP_2	20100429	Product data sheet	-	PMK35EP_1
Modifications:	 Various cha 	inges to content.		
PMK35EP_1	20070917	Product data sheet	-	-

P-channel TrenchMOS extremely low level FET

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

9.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

9.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on a weakness or default in the customer application/use or the application/use of customer's third party customer(s) (hereinafter both referred to as "Application"). It is customer's sole responsibility to check whether the NXP Semiconductors product is suitable and fit for the Application planned. Customer has to do all necessary testing for the Application in order to avoid a default of the Application and the product. NXP Semiconductors does not accept any liability in this respect.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding. Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

PMK35EP

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

P-channel TrenchMOS extremely low level FET

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Adelante, Bitport, Bitsound, CoolFlux, CoReUse, DESFire, EZ-HV, FabKey, GreenChip, HiPerSmart, HITAG, I²C-bus logo, ICODE, I-CODE, ITEC, Labelution, MIFARE, MIFARE Plus, MIFARE Ultralight, MoReUse, QLPAK, Silicon Tuner, SiliconMAX, SmartXA, STARplug, TOPFET, TrenchMOS, TriMedia and UCODE — are trademarks of NXP B.V.

HD Radio and **HD Radio** logo — are trademarks of iBiquity Digital Corporation.

10. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

PMK35EP **NXP Semiconductors**

P-channel TrenchMOS extremely low level FET

11. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	3
6	Characteristics	4
7	Package outline	3
8	Revision history)
9	Legal information10)
9.1	Data sheet status)
9.2	Definitions10)
9.3	Disclaimers)
9.4	Trademarks1	1
10	Contact information1	1

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

PMK35EP,518