PMV45EN

N-channel TrenchMOS logic level FET

Rev. 2 — 7 November 2011 **Product data sheet**

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications.

1.2 Features and benefits

- Logic-level compatible
- Trench MOSFET technology
- Very fast switching

1.3 Applications

- Battery management
- High-speed switching

1.4 Quick reference data

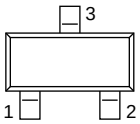
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-	30	V
I_D	drain current	T_{sp} = 25 °C; V_{GS} = 10 V; see Figure 1; see Figure 3	-	-	5.4	A
V_{GS}	gate-source voltage		-20	-	20	V
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 2 A; T_j = 25 °C; see Figure 9; see Figure 10	-	35	42	mΩ

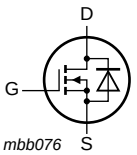
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	D	drain		



SOT23 (TO-236AB)



3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV45EN	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

4. Marking

Table 4. Marking codes

Type number	Marking code[1]
PMV45EN	%4N

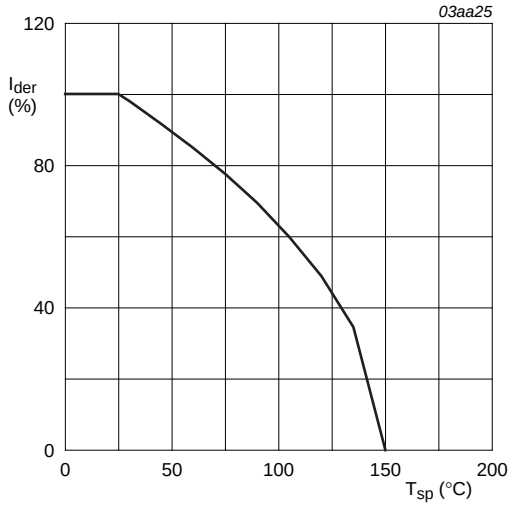
[1] % = placeholder for manufacturing site code

5. Limiting values

Table 5. Limiting values

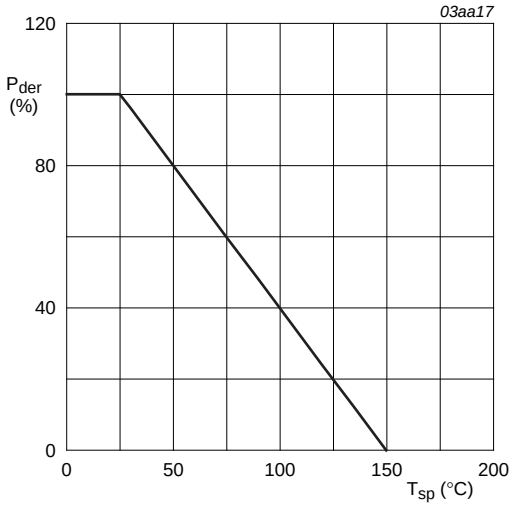
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C; $R_{GS} = 20$ kΩ	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{sp} = 100$ °C; $V_{GS} = 10$ V; see Figure 1	-	3.4	A
		$T_{sp} = 25$ °C; $V_{GS} = 10$ V; see Figure 1; see Figure 3	-	5.4	A
I_{DM}	peak drain current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ µs; see Figure 3	-	21.6	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; see Figure 2	-	2	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25$ °C	-	1.7	A
I_{SM}	peak source current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ µs	-	6.9	A



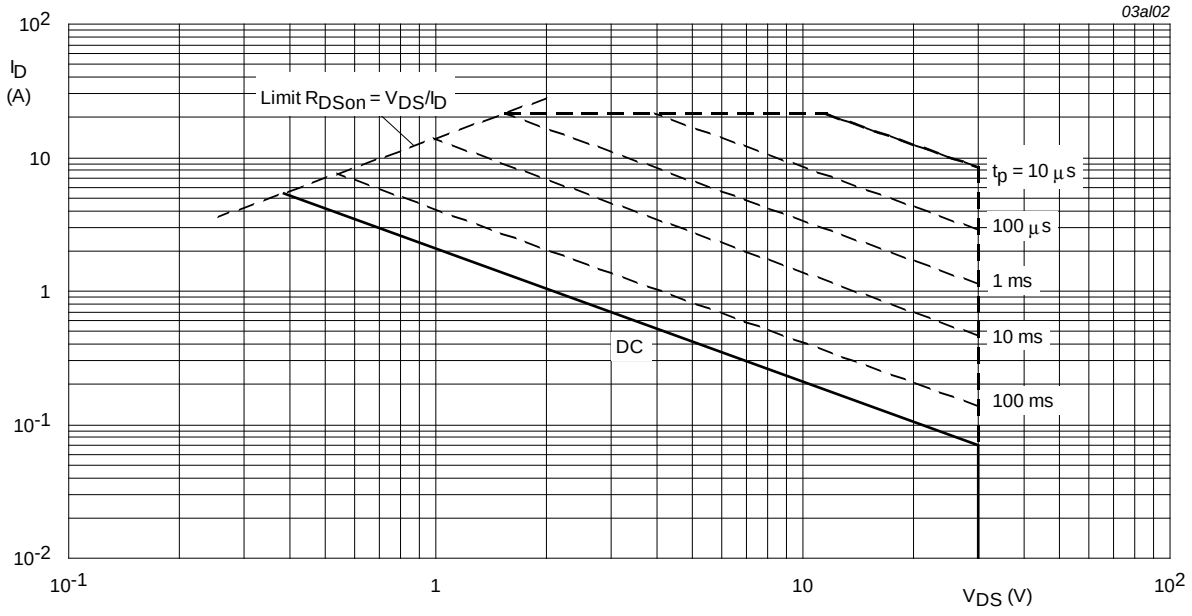
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$$T_{sp} = 25°C; I_{DM} \text{ is single pulse}; V_{GS} = 10V$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	60	K/W

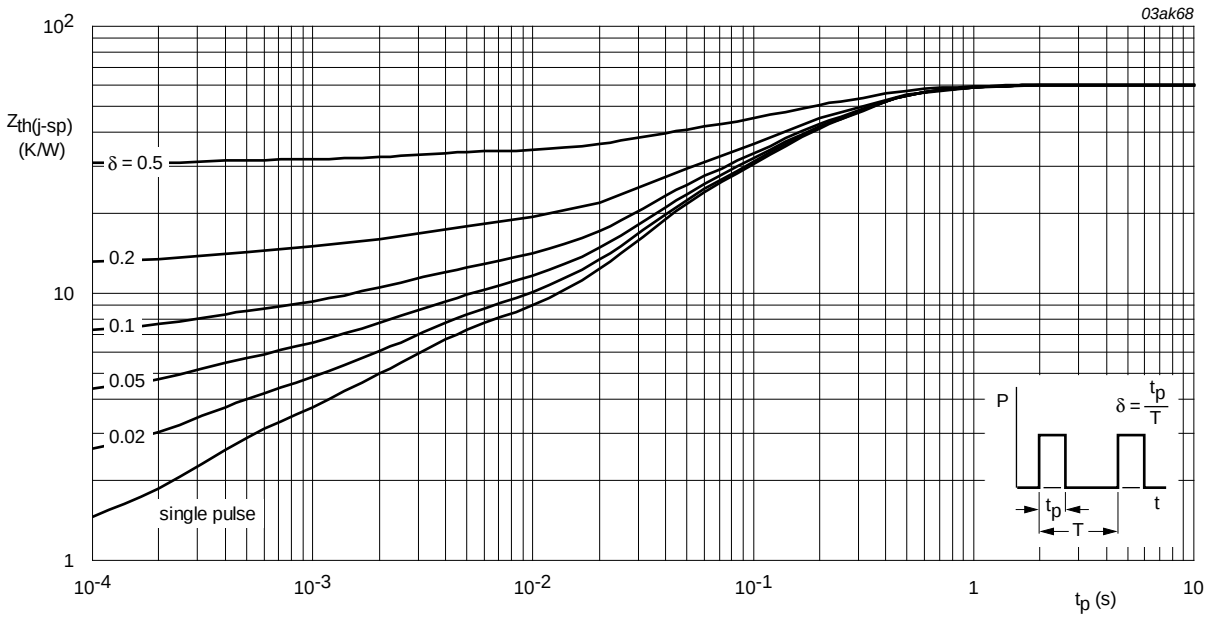
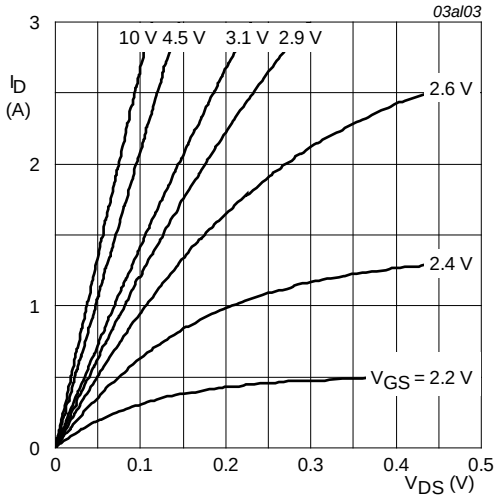


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	30	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 8	1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 8	0.6	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 8	-	-	2.2	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C	-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 2 A; T_j = 25 °C; see Figure 9; see Figure 10	-	35	42	mΩ
		V_{GS} = 10 V; I_D = 2 A; T_j = 150 °C; see Figure 9; see Figure 10	-	59.5	71.4	mΩ
		V_{GS} = 4.5 V; I_D = 1.5 A; T_j = 25 °C; see Figure 9; see Figure 10	-	45	54	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 3 A; V_{DS} = 15 V; V_{GS} = 10 V; T_j = 25 °C; see Figure 11	-	9.4	-	nC
Q_{GS}	gate-source charge		-	1.2	-	nC
Q_{GD}	gate-drain charge		-	1.9	-	nC
C_{iss}	input capacitance	V_{DS} = 30 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C	-	350	-	pF
C_{oss}	output capacitance		-	70	-	pF
C_{rss}	reverse transfer capacitance		-	50	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 15 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C	-	5	-	ns
t_r	rise time		-	7	-	ns
$t_{d(off)}$	turn-off delay time		-	16	-	ns
t_f	fall time		-	5.5	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 1.5 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 12	-	0.79	1.2	V



$T_j = 25°C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

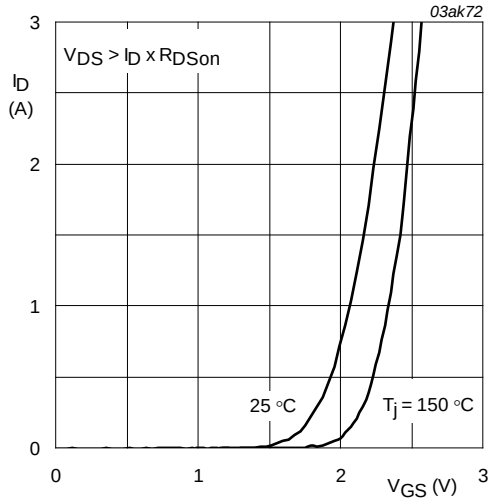
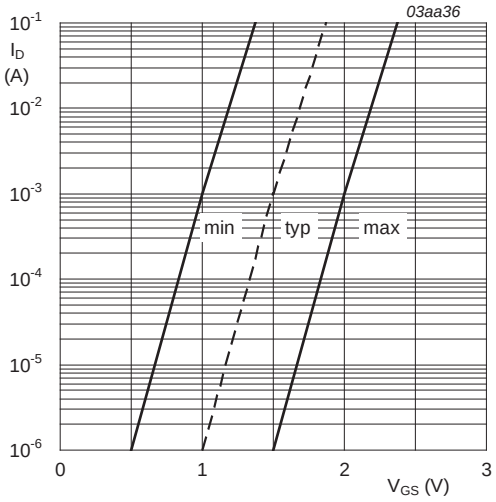
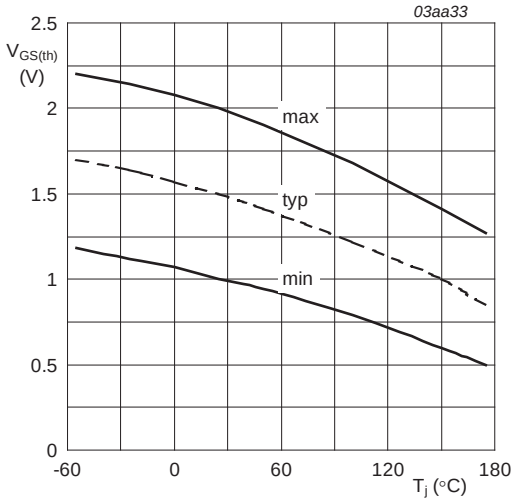


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



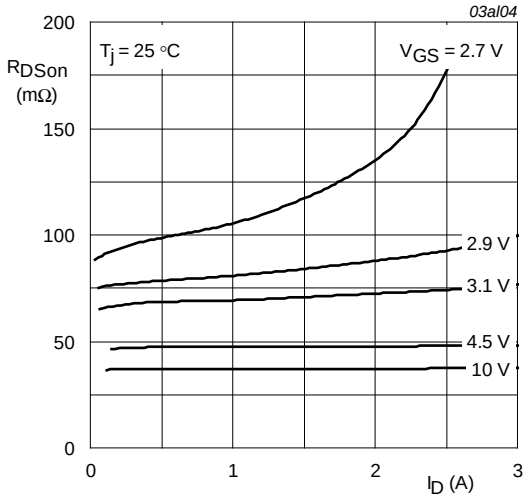
$T_j = 25\ °C;\ V_{DS} = 5\ V$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



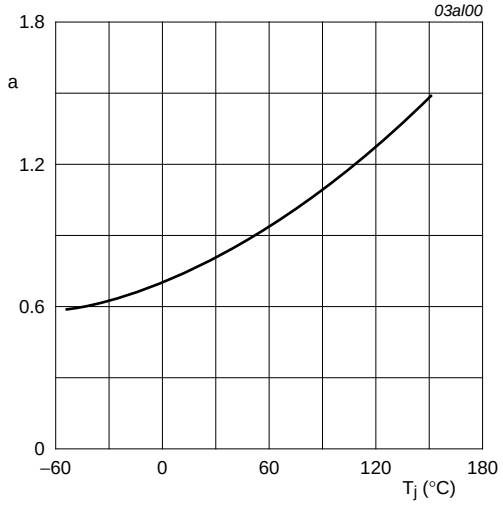
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



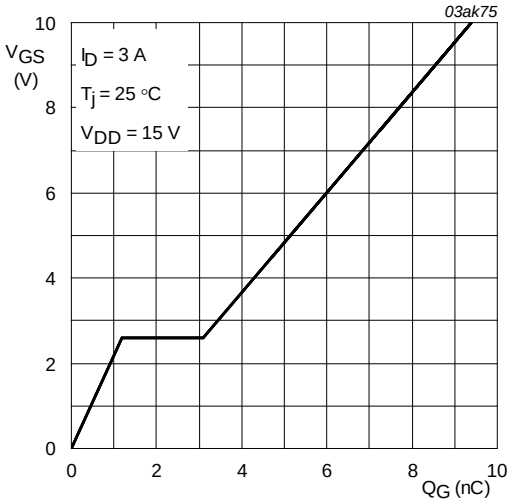
$T_j = 25°C$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



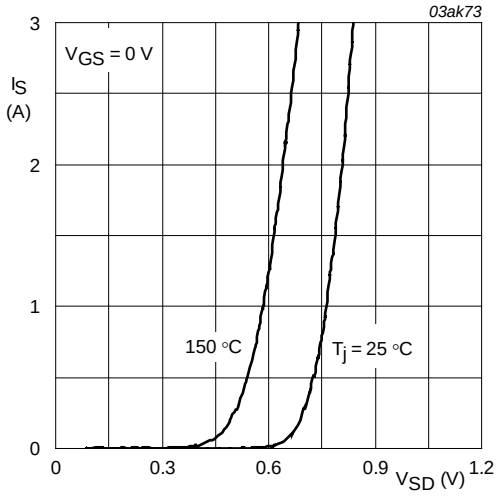
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



$I_D = 3A; V_{DS} = 15V$

Fig 11. Gate-source voltage as a function of gate charge; typical values

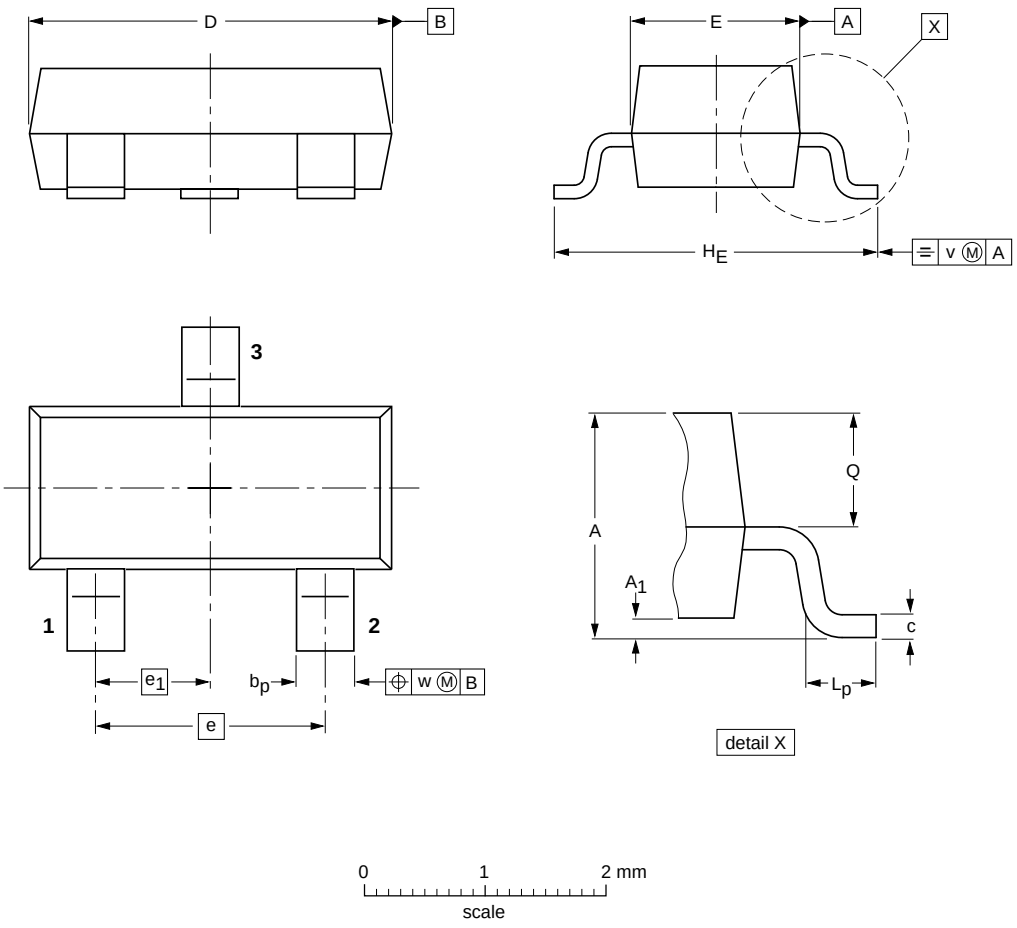


$T_j = 25°C$ and $150°C; V_{GS} = 0V$

Fig 12. Source current as a function of source-drain voltage; typical value

8. Package outline

Plastic surface-mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				~~04-11-04~~ 06-03-16

Fig 13. Package outline SOT23 (TO-236AB)

9. Soldering

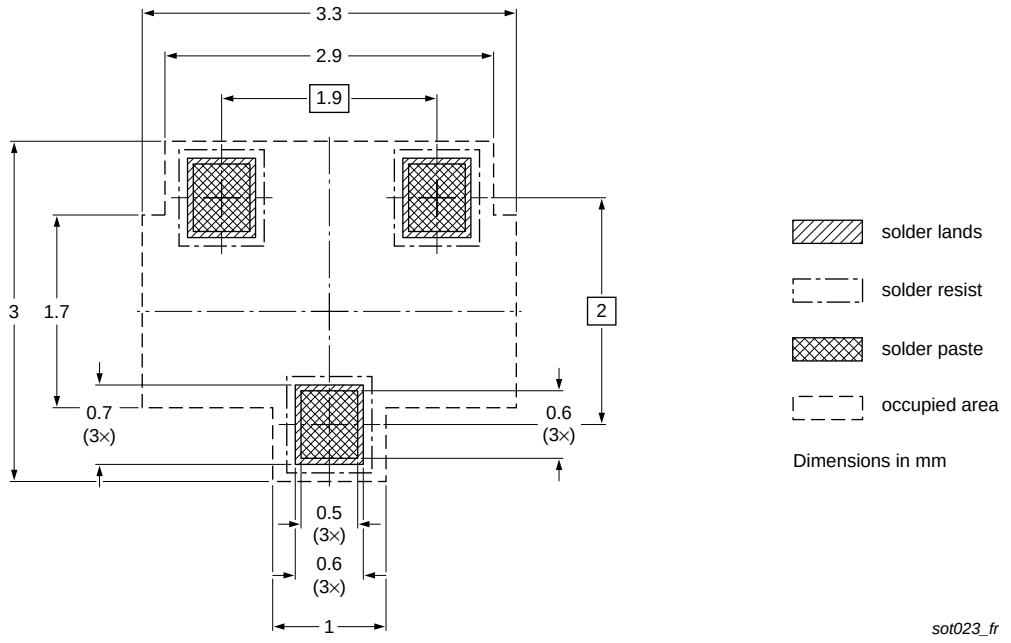


Fig 14. Reflow soldering footprint for SOT23 (TO-236AB)

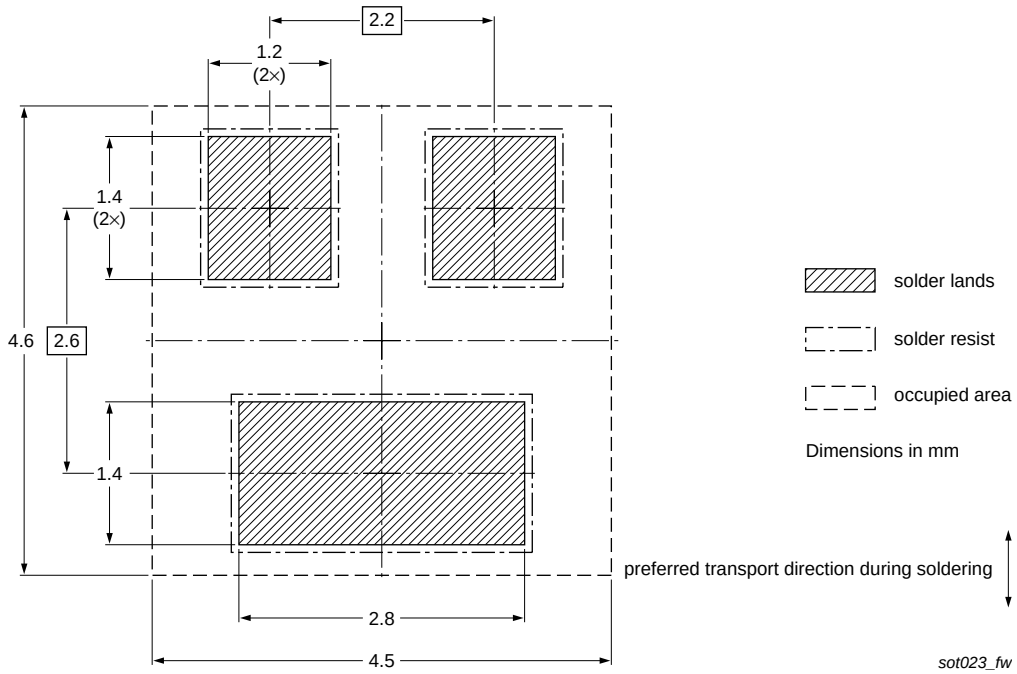


Fig 15. Wave soldering footprint for SOT23 (TO-236AB)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMV45EN v.2	20111107	Product data sheet	-	PMV45EN v.1
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • 1 “Product profile”: updated • 3 “Ordering information”: added • 4 “Marking”: added • Fig 13.: updated • 9 “Soldering”: added • 11 “Legal information”: updated			
PMV45EN v.1	20030115	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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13. Contents

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